

The RF Sub-Micron MOSFET Line
RF Power Field Effect Transistors
N-Channel Enhancement-Mode Lateral MOSFETs

MRF282S
MRF282Z

Designed for class A and class AB PCN and PCS base station applications at frequencies up to 2600 MHz. Suitable for FM, TDMA, CDMA, and multicarrier amplifier applications.

- Specified Two-Tone Performance @ 2000 MHz, 26 Volts
Output Power = 10 Watts (PEP)
Power Gain = 11 dB
Efficiency = 30%
Intermodulation Distortion = -30 dBc
- Specified Single-Tone Performance @ 2000 MHz, 26 Volts
Output Power = 10 Watts (CW)
Power Gain = 11 dB
Efficiency = 40%
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- S-Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 2000 MHz, 10 Watts (CW) Output Power
- Gold Metallization for Improved Reliability

10 W, 2000 MHz, 26 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 458-03, STYLE 1
(MRF282S)



CASE 458A-01, STYLE 1
(MRF282Z)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	65	Vdc
Gate-Source Voltage	V _{GS}	±20	Vdc
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	60 0.34	Watts W/°C
Storage Temperature Range	T _{stg}	-65 to +150	°C
Operating Junction Temperature	T _J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	2.9	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

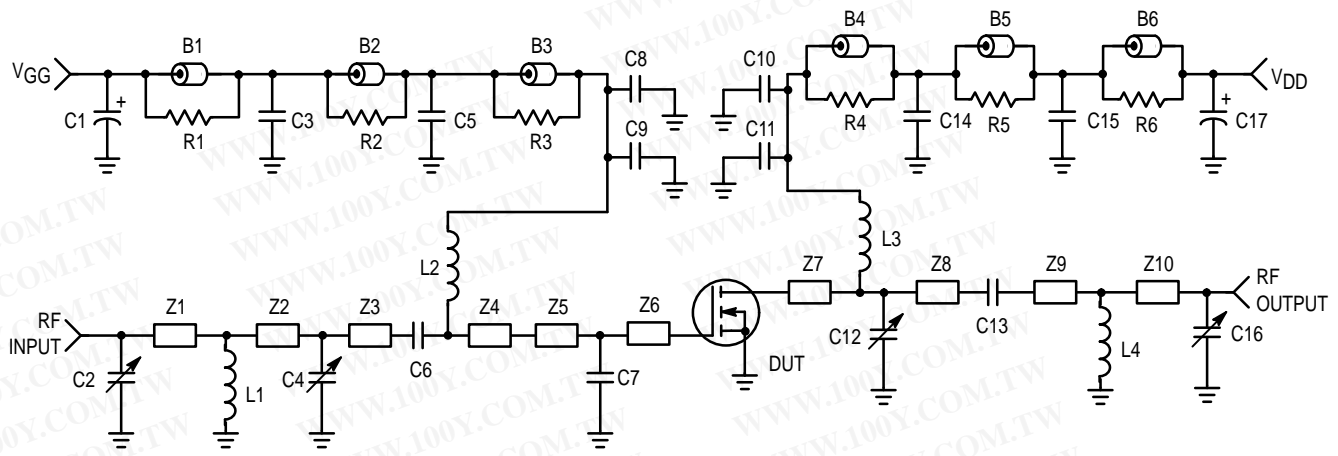
Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 10 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 28 Vdc, V _{GS} = 0)	I _{DSS}	—	—	1.0	μAdc
Gate-Source Leakage Current (V _{GS} = 20 Vdc, V _{DS} = 0)	I _{GSS}	—	—	1.0	μAdc

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.



ELECTRICAL CHARACTERISTICS continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

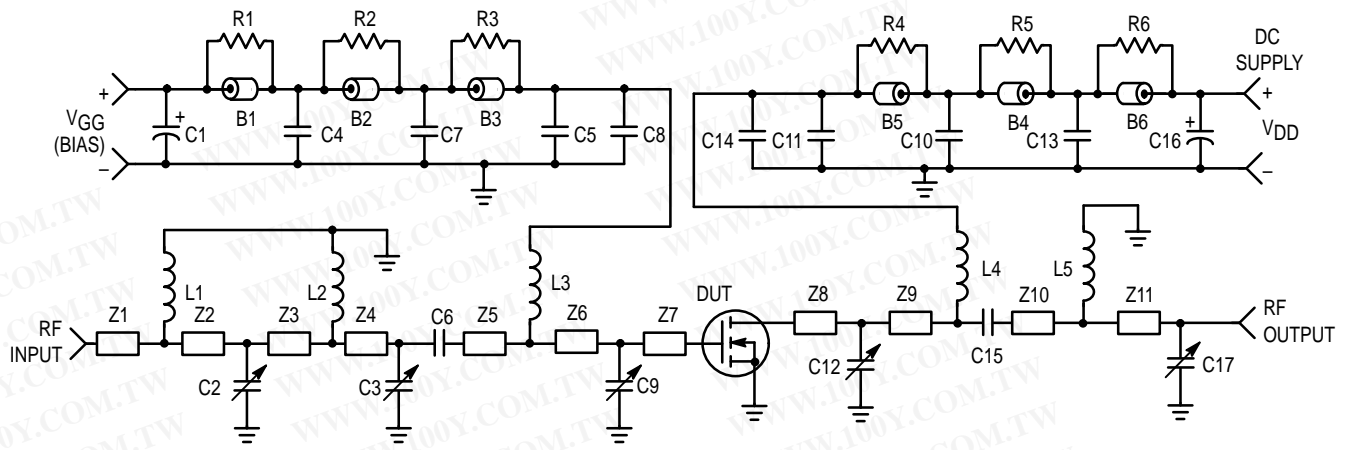
Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 50\ \mu\text{Adc}$)	$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Drain–Source On–Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 0.5\text{ Adc}$)	$V_{DS(on)}$	—	0.4	0.6	Vdc
Forward Transconductance ($V_{DS} = 10\text{ Vdc}$, $I_D = 0.5\text{ Adc}$)	g_{fs}	0.5	0.7	—	S
Gate Quiescent Voltage ($V_{DS} = 26\text{ Vdc}$, $I_D = 75\text{ mAdc}$)	$V_{GS(q)}$	3.0	4.0	5.0	Vdc
DYNAMIC CHARACTERISTICS					
Input Capacitance ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0$, $f = 1.0\text{ MHz}$)	C_{iss}	—	15	—	pF
Output Capacitance ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0$, $f = 1.0\text{ MHz}$)	C_{oss}	—	8.0	—	pF
Reverse Transfer Capacitance ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0$, $f = 1.0\text{ MHz}$)	C_{rss}	—	0.45	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 10\text{ W (PEP)}$, $I_{DQ} = 75\text{ mA}$, $f_1 = 2000.0\text{ MHz}$, $f_2 = 2000.1\text{ MHz}$)	G_{ps}	11	12.6	—	dB
Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 10\text{ W (PEP)}$, $I_{DQ} = 75\text{ mA}$, $f_1 = 2000.0\text{ MHz}$, $f_2 = 2000.1\text{ MHz}$)	η	30	34	—	%
Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 10\text{ W (PEP)}$, $I_{DQ} = 75\text{ mA}$, $f_1 = 2000.0\text{ MHz}$, $f_2 = 2000.1\text{ MHz}$)	I_{MD}	—	–32.5	–30	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 10\text{ W (PEP)}$, $I_{DQ} = 75\text{ mA}$, $f_1 = 2000.0\text{ MHz}$, $f_2 = 2000.1\text{ MHz}$)	I_{RL}	10	14	—	dB
Common–Source Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 10\text{ W (PEP)}$, $I_{DQ} = 75\text{ mA}$, $f_1 = 1930.0\text{ MHz}$, $f_2 = 1930.1\text{ MHz}$)	G_{ps}	11	12.6	—	dB
Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 10\text{ W (PEP)}$, $I_{DQ} = 75\text{ mA}$, $f_1 = 1930.0\text{ MHz}$, $f_2 = 1930.1\text{ MHz}$)	η	—	30	—	%
Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 10\text{ W (PEP)}$, $I_{DQ} = 75\text{ mA}$, $f_1 = 1930.0\text{ MHz}$, $f_2 = 1930.1\text{ MHz}$)	I_{MD}	—	–32.5	—	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 10\text{ W (PEP)}$, $I_{DQ} = 75\text{ mA}$, $f_1 = 1930.0\text{ MHz}$, $f_2 = 1930.1\text{ MHz}$)	I_{RL}	10	14	—	dB
Common–Source Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 10\text{ W CW}$, $I_{DQ} = 75\text{ mA}$, $f = 2000.0\text{ MHz}$)	G_{ps}	11	12.3	—	dB
Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 10\text{ W CW}$, $I_{DQ} = 75\text{ mA}$, $f = 2000.0\text{ MHz}$)	η	40	45	—	%
Output Mismatch Stress ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 10\text{ W CW}$, $I_{DQ} = 75\text{ mA}$, $f_1 = 2000.0\text{ MHz}$, $f_2 = 2000.1\text{ MHz}$, Load VSWR = 10:1, All Phase Angles at Frequency of Test)	Ψ	No Degradation In Output Power			



B1, B2, B3,	Ferrite Bead, Ferroxcube, 56–590–65–3B	R1, R2, R3,	12 Ω, 0.2 W Chip Resistor, Rohm
B4, B5, B6		R4, R5, R6	
C1, C17	470 μF, Electrolytic Capacitor, Mallory	Z1	0.155" x 0.08" Microstrip
C2, C4, C12	0.6–4.5 pF, Variable Capacitor, Johanson	Z2	0.280" x 0.08" Microstrip
C3, C15	0.1 μF, Chip Capacitor, Kemet	Z3	0.855" x 0.08" Microstrip
C5, C14	1000 pF, B Case Chip Capacitor, ATC	Z4	0.483" x 0.08" Microstrip
C6, C8, C10, C13	12 pF, B Case Chip Capacitor, ATC	Z5	0.200" x 0.330" Microstrip
C7	1.8 pF, B Case Chip Capacitor, ATC	Z6	0.220" x 0.330" Microstrip
C9, C11	100 pF, B Case Chip Capacitor, ATC	Z7	0.490" x 0.330" Microstrip
C16	0.4–2.5 pF, Variable Capacitor, Johanson	Z8	0.510" x 0.08" Microstrip
L1	Straight Wire, 21 AWG, 0.3"	Z9	0.990" x 0.08" Microstrip
L2	8 Turns, 0.042" ID, 24 AWG, Enamel	Z10	0.295" x 0.08" Microstrip
L3	9 Turns, 0.046" ID, 26 AWG, Enamel	Board	35 Mils Glass Teflon®, Arlon GX–300, ε _r = 2.55
L4	3 Turns, 0.048" ID, 25 AWG, Enamel		

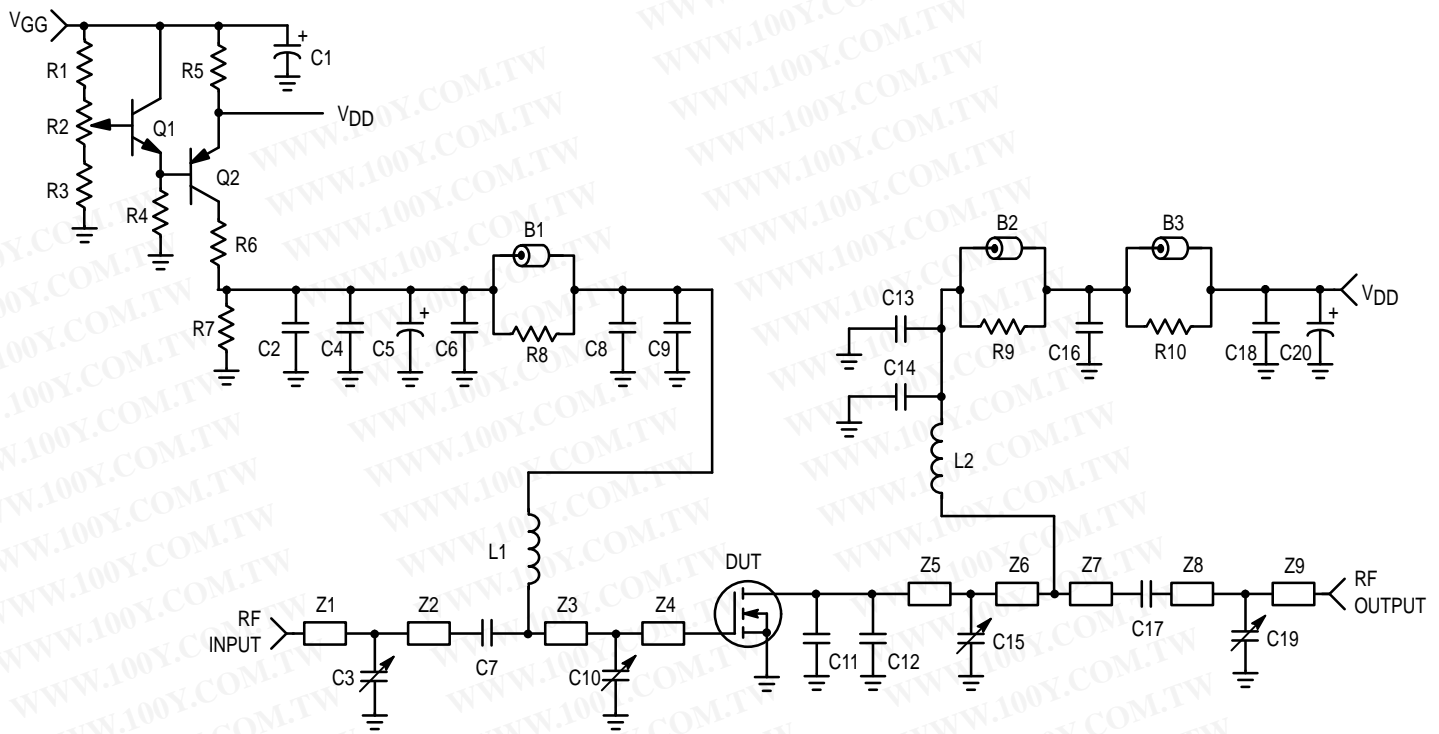
Input/Output Connectors Type N Flange Mount

Figure 1. Schematic of 1.93 – 2.0 GHz Broadband Test Circuit



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|------------------|--|-------------|---|
| B1, B2, B3, | Ferrite Bead, Fair Rite, (2743021446) | R1, R2, R3, | 12 Ω , 1/8 W Fixed Film Chip Resistor, |
| B4, B5, B6 | | R4, R5, R6 | 0.08" x 0.13" |
| C1, C16 | 470 μ F, 63 V, Electrolytic Capacitor, Mallory | W1, W2 | Beryllium Copper, 0.010" x 0.110" x 0.210" |
| C2, C9, C12 | 0.6–4.5 pF, Variable Capacitor, Johanson Gigatrim | Z1 | 0.122" x 0.08" Microstrip |
| C3 | 0.8–4.5 pF, Variable Capacitor, Johanson Gigatrim | Z2 | 0.650" x 0.08" Microstrip |
| C4, C13 | 0.1 μ F, Chip Capacitor | Z3 | 0.160" x 0.08" Microstrip |
| C5, C14 | 100 pF, B Case Chip Capacitor, ATC | Z4 | 0.030" x 0.08" Microstrip |
| C6, C8, C11, C15 | 12 pF, B Case Chip Capacitor, ATC | Z5 | 0.045" x 0.08" Microstrip |
| C7, C10 | 1000 pF, B Case Chip Capacitor, ATC | Z6 | 0.291" x 0.08" Microstrip |
| C17 | 0.1 pF, B Case Chip Capacitor, ATC | Z7 | 0.483" x 0.330" Microstrip |
| L1 | 3 Turns, 27 AWG, 0.087" OD, 0.050" ID,
0.053" Long, 6.0 nH | Z8 | 0.414" x 0.330" Microstrip |
| L2 | 5 Turns, 27 AWG, 0.087" OD, 0.050" ID,
0.091" Long, 15 nH | Z9 | 0.392" x 0.08" Microstrip |
| L3, L4 | 9 Turns, 26 AWG, 0.080" OD, 0.046" ID,
0.170" Long, 30.8 nH | Z10 | 0.070" x 0.08" Microstrip |
| L5 | 4 Turns, 27 AWG, 0.087" OD, 0.050" ID,
0.078" Long, 10 nH | Z11 | 1.110" x 0.08" Microstrip |
| | | Board | 1 = 0.03 Glass Teflon [®] , Arlon GX-0300-55-22,
2 oz Copper, 3 x 5" Dimension, 0.030", $\epsilon_r = 2.55$ |

Figure 2. Schematic of 1.81 – 1.88 GHz Broadband Test Circuit



B1, B2, B3,	Ferrite Bead, Ferroxcube, 56-590-65-3B	R2	1.0 k Ω , 1/2 W Potentiometer
C1, C20	470 μ F, 63 V, Electrolytic Capacitor, Mallory	R3	13 k Ω , Axial, 1/4 W Resistor
C2	0.01 μ F, B Case Chip Capacitor, ATC	R4, R6, R7	390 Ω , 1/8 W Chip Resistor, Rohm
C3, C10, C15	0.6-4.5 pF, Variable Capacitor, Johanson	R5	1.0 Ω , 10 W 1% Resistor, DALE
C4, C16	0.02 μ F, B Case Chip Capacitor, ATC	R8, R9, R10	12 Ω , 1/8 W Chip Resistor, Rohm
C5	100 μ F, 50 V, Electrolytic Capacitor, Sprague	Z1	0.624" x 0.08" Microstrip
C6, C7, C9,	12 pF, B Case Chip Capacitor, ATC	Z2	0.725" x 0.08" Microstrip
C14, C17		Z3	0.455" x 0.08" Microstrip
C8, C13	51 pF, B Case Chip Capacitor, ATC	Z4	0.530" x 0.330" Microstrip
C11, C12	0.3 pF, B Case Chip Capacitor, ATC	Z5	0.280" x 0.330" Microstrip
C18	0.1 μ F, Chip Capacitor, Kemet	Z6	0.212" x 0.330" Microstrip
C19	0.4-2.5 pF, Variable Capacitor, Johanson	Z7	0.408" x 0.08" Microstrip
L1	8 Turns, 0.042" ID, 24 AWG, Enamel	Z8	0.990" x 0.08" Microstrip
L2	9 Turns, 0.046" ID, 26 AWG, Enamel	Z9	0.295" x 0.08" Microstrip
Q1	NPN, 15 W, Bipolar Transistor, MJD310	Board	35 Mils Glass Teflon [®] , Arlon GX-0300, $\epsilon_r = 2.55$
Q2	PNP, 15 W, Bipolar Transistor, MJD320	Input/Output	Type N Flange Mount RF55-22, Connectors, Omni Spectra
R1	200 Ω , Axial, 1/4 W Resistor		

Figure 3. Schematic of Class A Test Circuit

TYPICAL CHARACTERISTICS

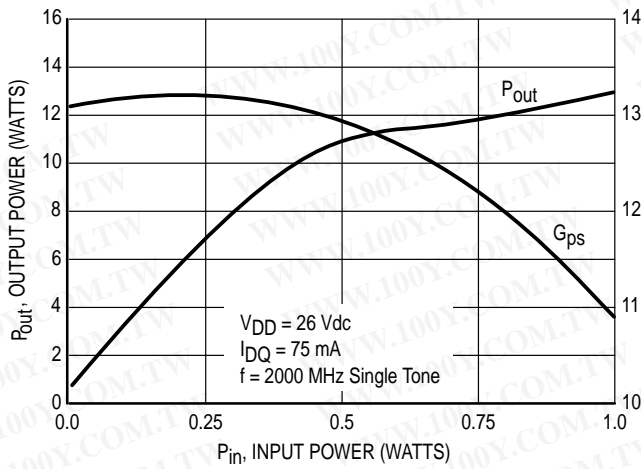


Figure 4. Output Power & Power Gain versus Input Power

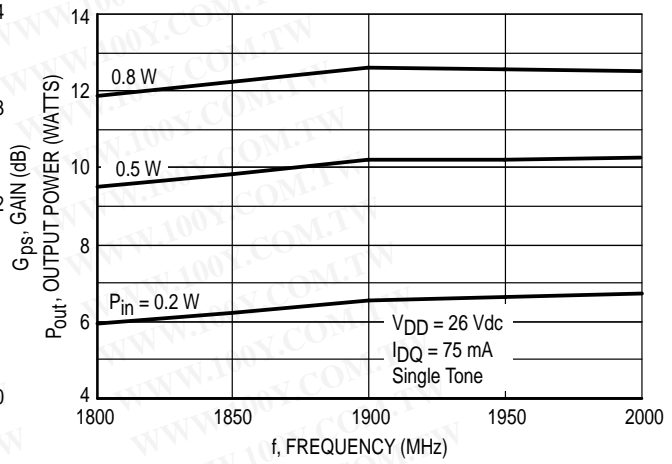


Figure 5. Output Power versus Frequency

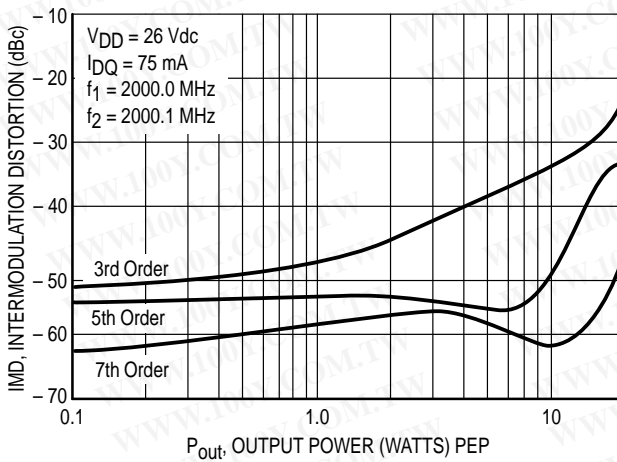


Figure 6. Intermodulation Distortion versus Output Power

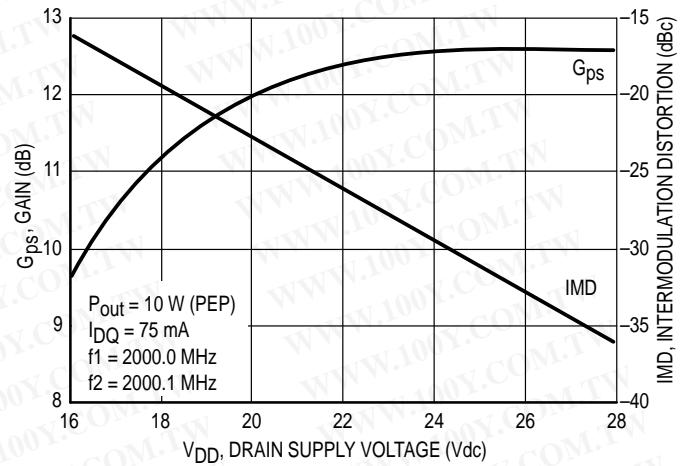


Figure 7. Power Gain and Intermodulation Distortion versus Supply Voltage

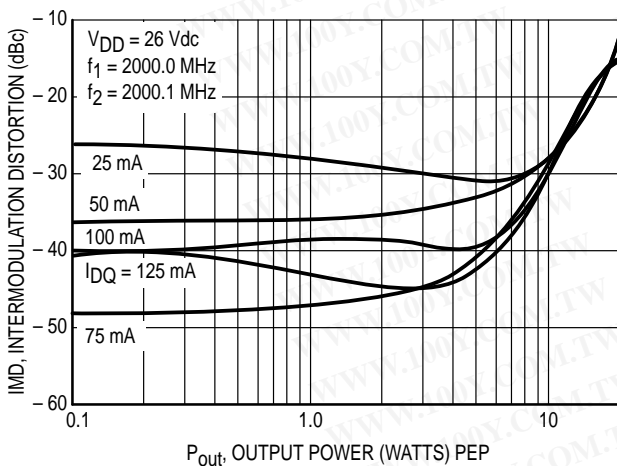


Figure 8. Intermodulation Distortion versus Output Power

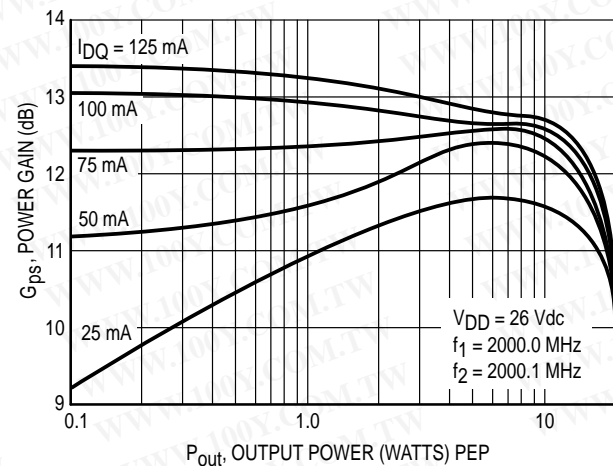


Figure 9. Power Gain versus Output Power

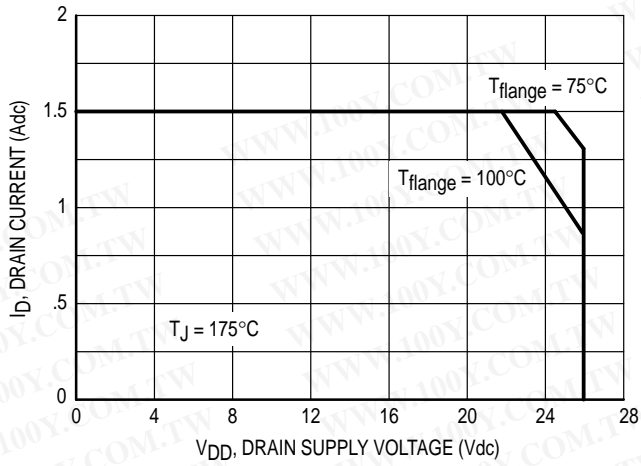


Figure 10. Class A DC Safe Operating Area

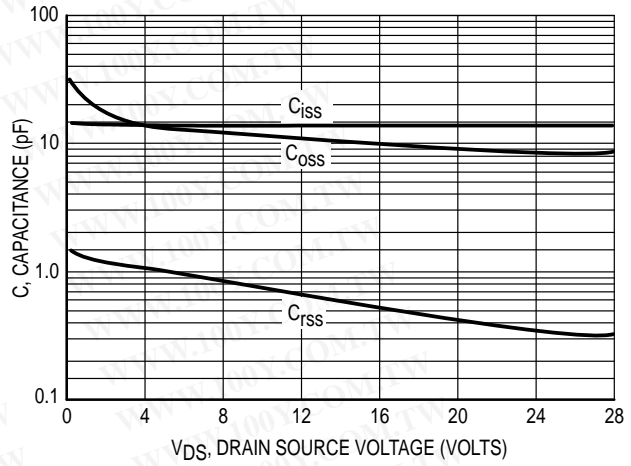


Figure 11. Capacitance versus Drain Source Voltage

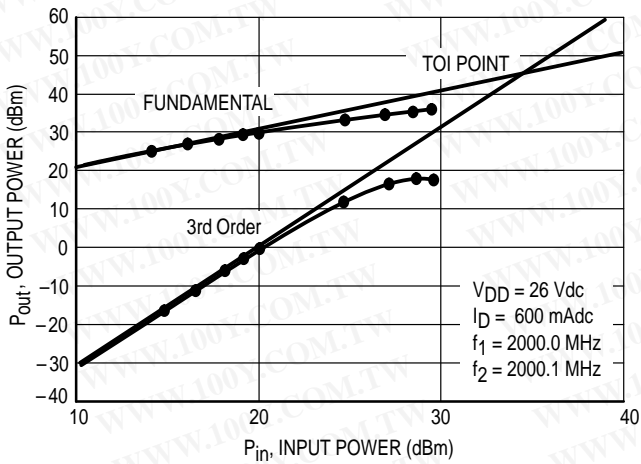


Figure 12. Class A Third Order Intercept Point

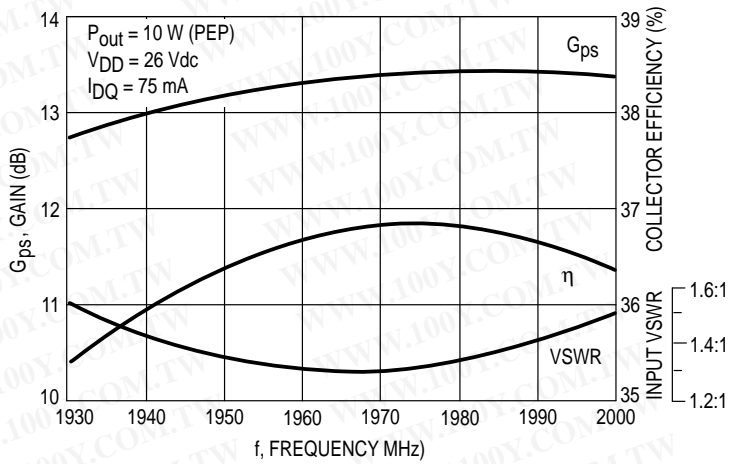
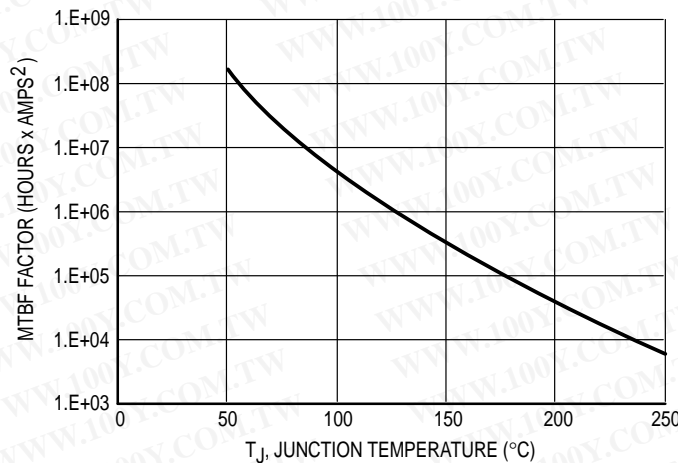
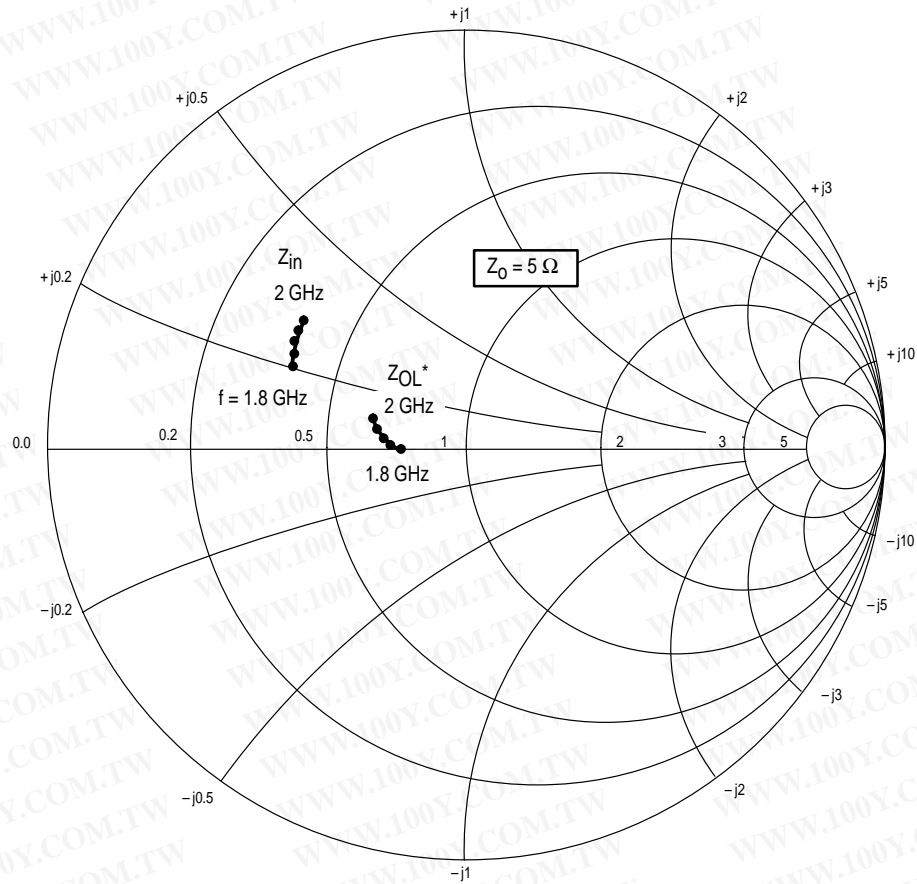


Figure 13. Performance in Broadband Circuit



This graph displays calculated MTBF in hours x ampere² drain current. Life tests at elevated temperature have correlated to better than $\pm 10\%$ of the theoretical prediction for metal failure. Divide MTBF factor by I_D^2 for MTBF in a particular application.

Figure 14. MTBF Factor versus Junction Temperature



$V_{CC} = 26 \text{ V}$, $I_{CQ} = 75 \text{ mA}$, $P_{out} = 10 \text{ W (PEP)}$

f MHz	$Z_{in(1)}$ Ω	Z_{OL}^* Ω
1800	$2.1 + j1.0$	$3.8 - j0.15$
1860	$2.05 + j1.15$	$3.77 - j0.13$
1900	$2.0 + j1.2$	$3.75 - j0.1$
1960	$1.9 + j1.4$	$3.65 + j0.1$
2000	$1.85 + j1.6$	$3.55 + j0.2$

$Z_{in(1)}$ = Conjugate of fixture gate terminal impedance.

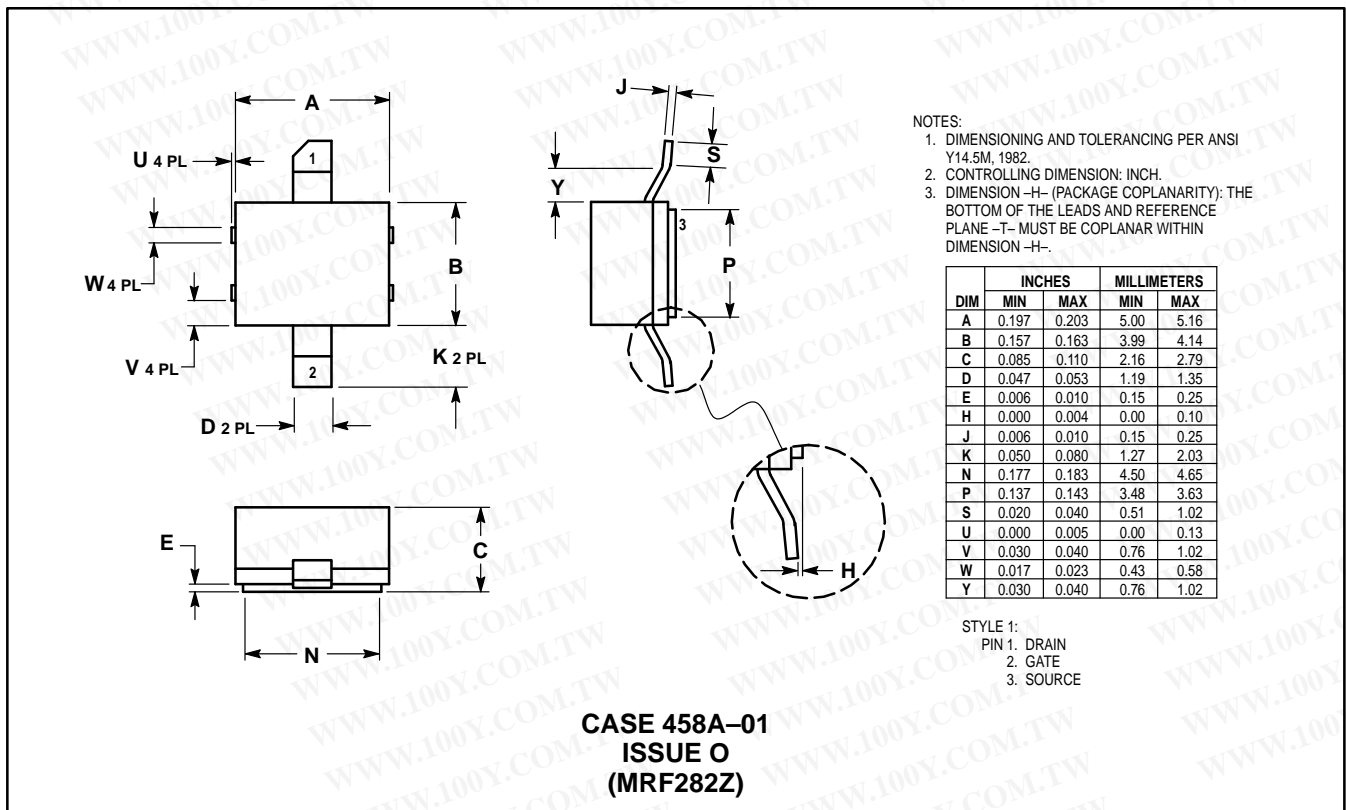
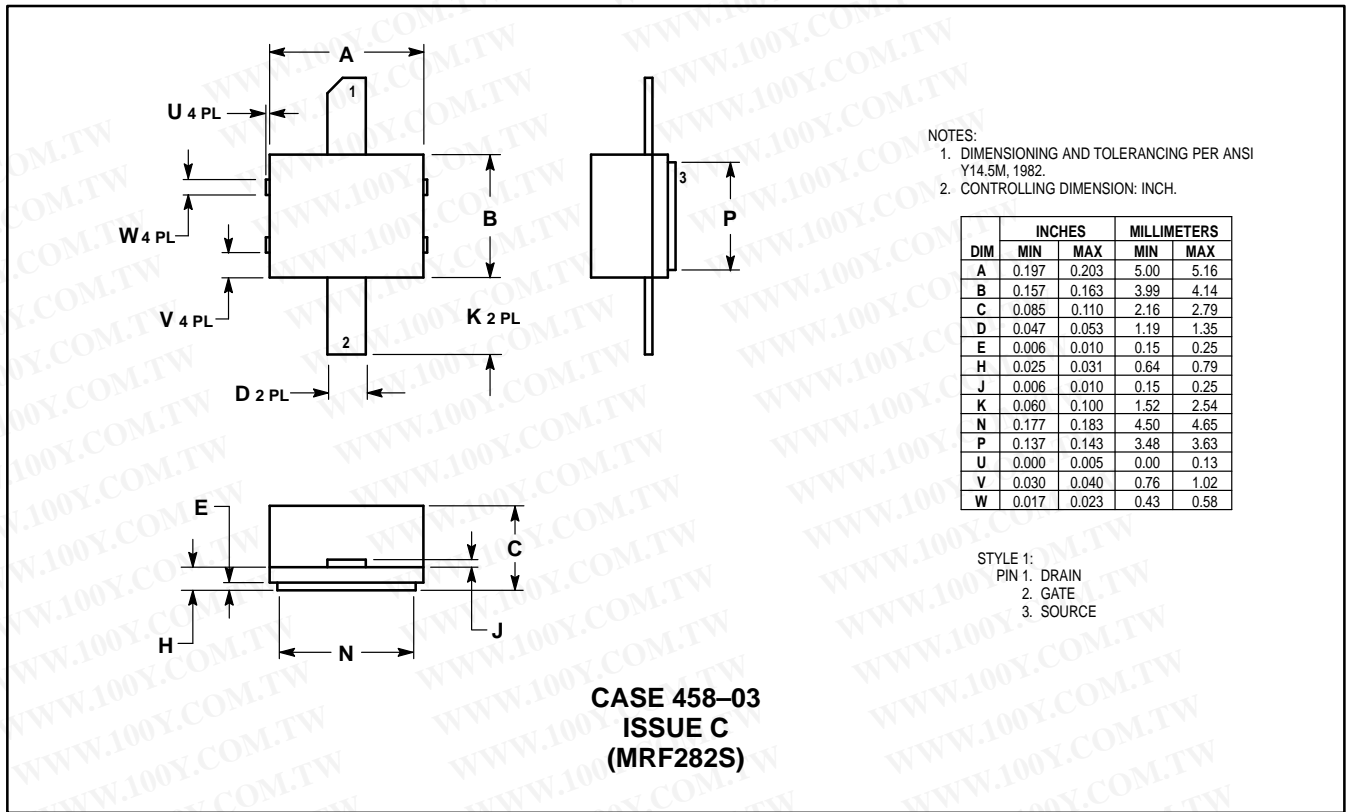
Z_{OL}^* = Conjugate of the optimum load impedance at given output power, voltage, IMD, bias current and frequency.

Figure 15. Series Equivalent Input and Output Impedence

Table 1. Common Source S-Parameters at $V_{DS} = 24$ Vdc, $I_D = 600$ mAdc

f GHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
0.1	0.916	-81	33.41	128	0.016	41	0.498	-60
0.2	0.850	-118	20.81	101	0.020	16	0.499	-88
0.3	0.843	-135	14.45	84	0.020	2	0.532	-106
0.4	0.848	-144	10.61	73	0.019	-7	0.552	-117
0.5	0.861	-151	8.34	63	0.017	-15	0.609	-125
0.6	0.872	-154	6.61	55	0.015	-19	0.647	-132
0.7	0.882	-158	5.43	47	0.013	-23	0.675	-139
0.8	0.895	-160	4.54	41	0.011	-24	0.728	-145
0.9	0.901	-163	3.82	34	0.009	-24	0.740	-150
1.0	0.902	-164	3.27	29	0.008	-18	0.773	-160
1.1	0.909	-166	2.83	24	0.006	-6	0.794	-164
1.2	0.917	-168	2.48	19	0.006	10	0.813	-168
1.3	0.923	-169	2.18	14	0.006	14	0.826	-172
1.4	0.931	-171	1.94	10	0.006	15	0.842	-176
1.5	0.933	-172	1.73	6	0.005	43	0.853	-179
1.6	0.934	-174	1.55	2	0.007	60	0.859	177
1.7	0.937	-175	1.40	-1	0.009	60	0.869	174
1.8	0.938	-176	1.27	-4	0.010	63	0.869	171
1.9	0.942	-177	1.16	-7	0.011	71	0.874	169
2.0	0.943	-178	1.06	-10	0.014	73	0.876	166
2.1	0.946	-178	0.98	-12	0.016	71	0.884	163
2.2	0.950	-179	0.92	-15	0.019	67	0.897	160
2.3	0.953	-180	0.86	-18	0.019	63	0.903	157
2.4	0.954	179	0.80	-21	0.020	62	0.907	154
2.5	0.955	178	0.76	-24	0.020	65	0.907	151
2.6	0.961	177	0.71	-26	0.024	69	0.912	149

PACKAGE DIMENSIONS



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 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)