



2N7002KQB

60 V N-channel Trench MOSFET

22 September 2021

Product data sheet

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1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in an ultra small DFN1110D-3 (SOT8015) leadless Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic-level compatible
- Side wettable flanks for optical solder inspection
- Ultra small and leadless SMD plastic package: 1.1 x 1 x 0.48 mm
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 1 kV HBM (Class H1C)
- AEC-Q101 qualified

3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

4. Quick reference data

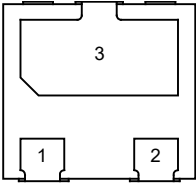
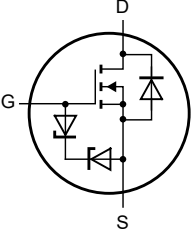
Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|----------------------------------|---|-----|-----|-----|------|
| V_{DS} | drain-source voltage | $T_j = 25\text{ }^{\circ}\text{C}$ | - | - | 60 | V |
| V_{GS} | gate-source voltage | | -16 | - | 16 | V |
| I_D | drain current | $V_{GS} = 10\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ | [1] | - | 720 | mA |
| Static characteristics | | | | | | |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10\text{ V}; I_D = 720\text{ mA}; T_j = 25\text{ }^{\circ}\text{C}$ | - | 635 | 850 | mΩ |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------|---|--|
| 1 | G | gate |  <p>Transparent top view DFN1110D-3 (SOT8015)</p> |  <p>017aaa255</p> |
| 2 | S | source | | |
| 3 | D | drain | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|-------------|------------|--|---------|
| | Name | Description | Version |
| 2N7002KQB | DFN1110D-3 | plastic, leadless extremely thin small outline package with side-wettable flanks (SWF); 3 terminals; 0.65 mm pitch; 1.1 mm x 1 mm x 0.48 mm body | SOT8015 |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|-------------|--------------|
| 2N7002KQB | C7 |

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|-----------------------------|--|---|-----|-----|------|------|
| V _{DS} | drain-source voltage | T _j = 25 °C | | - | 60 | V |
| V _{GS} | gate-source voltage | | | -16 | 16 | V |
| V _{GSMlim} | peak gate-source voltage | δ _{factor} = 0.1; t _p = 50 μs; T _j = 25 °C | | -20 | 20 | V |
| I _D | drain current | V _{GS} = 10 V; T _{amb} = 25 °C | [1] | - | 720 | mA |
| | | V _{GS} = 10 V; T _{amb} = 100 °C | [1] | - | 460 | mA |
| I _{DM} | peak drain current | T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs | | - | 2.9 | A |
| P _{tot} | total power dissipation | T _{amb} = 25 °C | [2] | - | 420 | mW |
| | | | [1] | - | 960 | mW |
| | | T _{sp} = 25 °C | | - | 4.2 | W |
| T _j | junction temperature | | | -55 | 150 | °C |
| T _{amb} | ambient temperature | | | -55 | 150 | °C |
| T _{stg} | storage temperature | | | -65 | 150 | °C |
| Source-drain diode | | | | | | |
| I _S | source current | T _{amb} = 25 °C | [1] | - | 700 | mA |
| ESD maximum rating | | | | | | |
| V _{ESD} | electrostatic discharge voltage | HBM | | - | 1000 | V |
| Avalanche ruggedness | | | | | | |
| E _{DS(AL)S} | non-repetitive drain-source avalanche energy | T _{j(initial)} = 25 °C; I _D = 0.05 A | | - | 1.5 | mJ |

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².
 [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

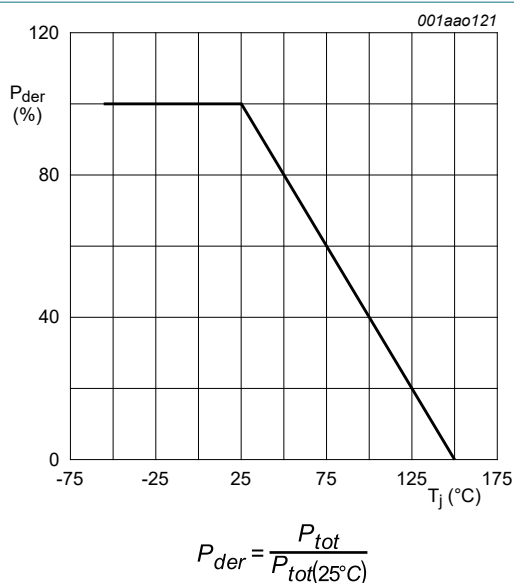


Fig. 1. Normalized total power dissipation as a function of junction temperature

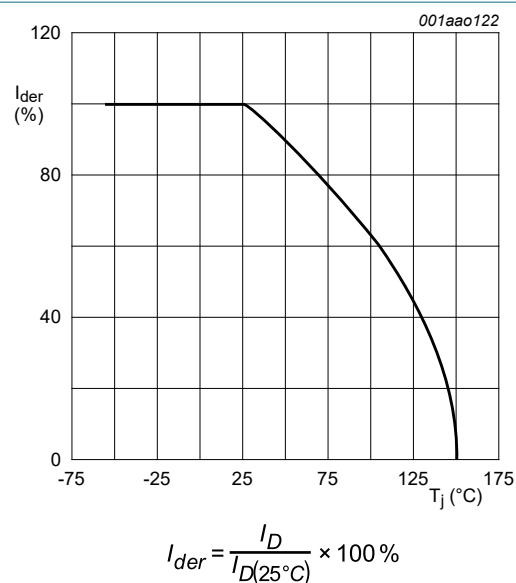
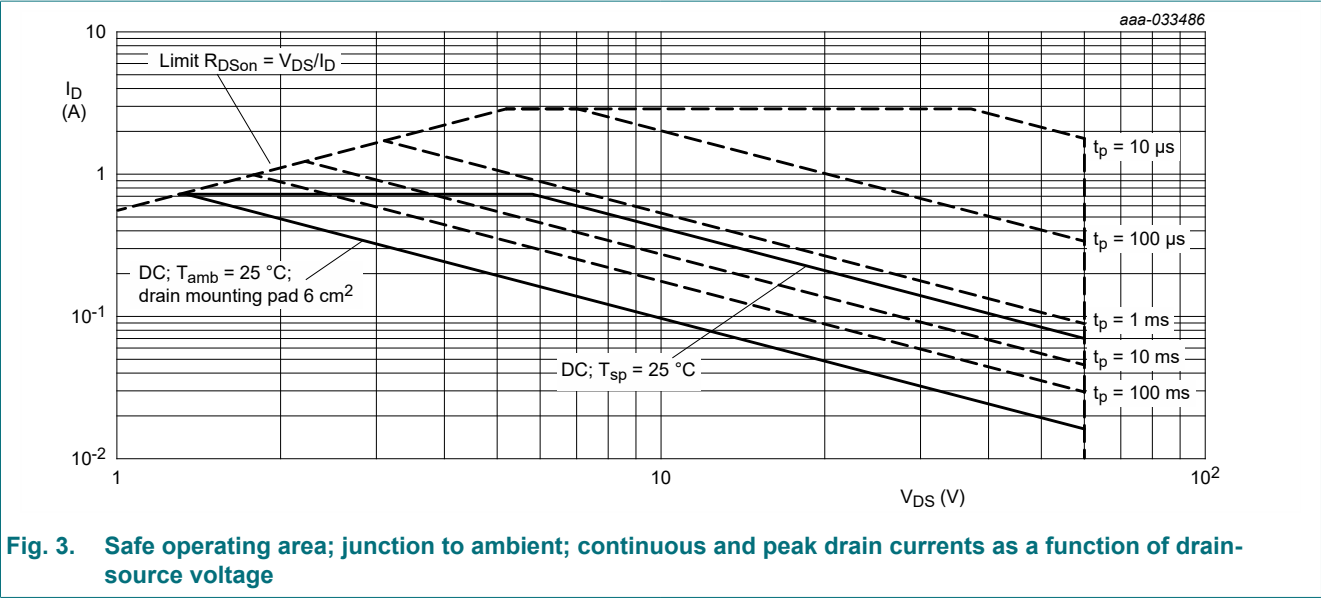


Fig. 2. Normalized continuous drain current as a function of junction temperature



9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|----------------|--|-------------|-----|-----|-----|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | 245 | 300 | K/W |
| | | | [2] | - | 110 | 130 | K/W |
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | | | - | 25 | 30 | K/W |

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².

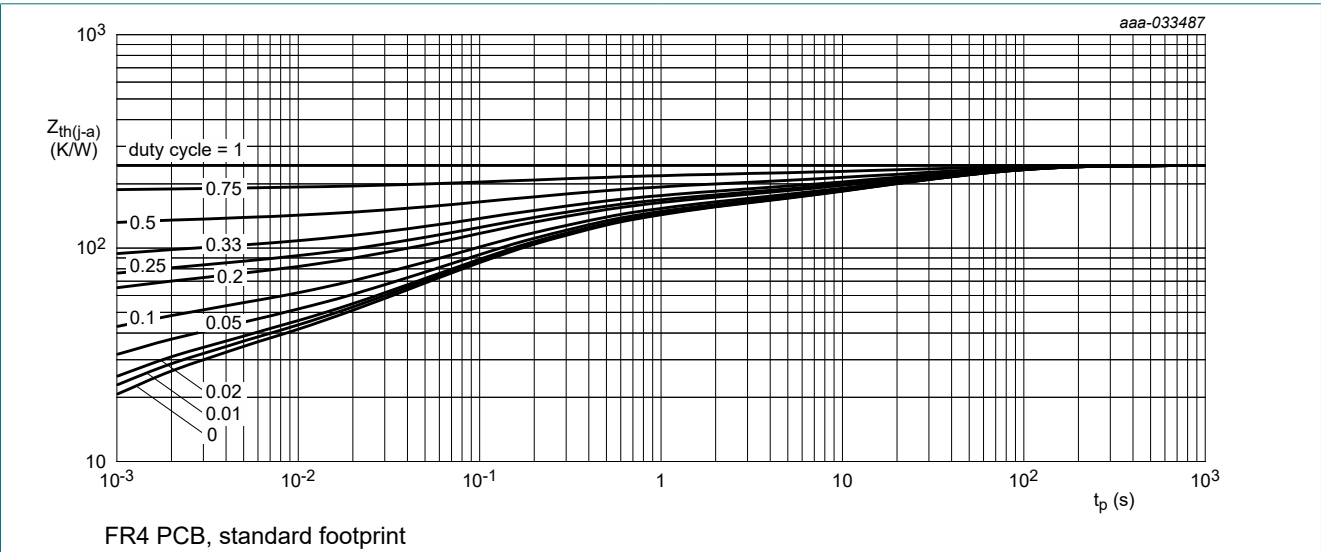


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

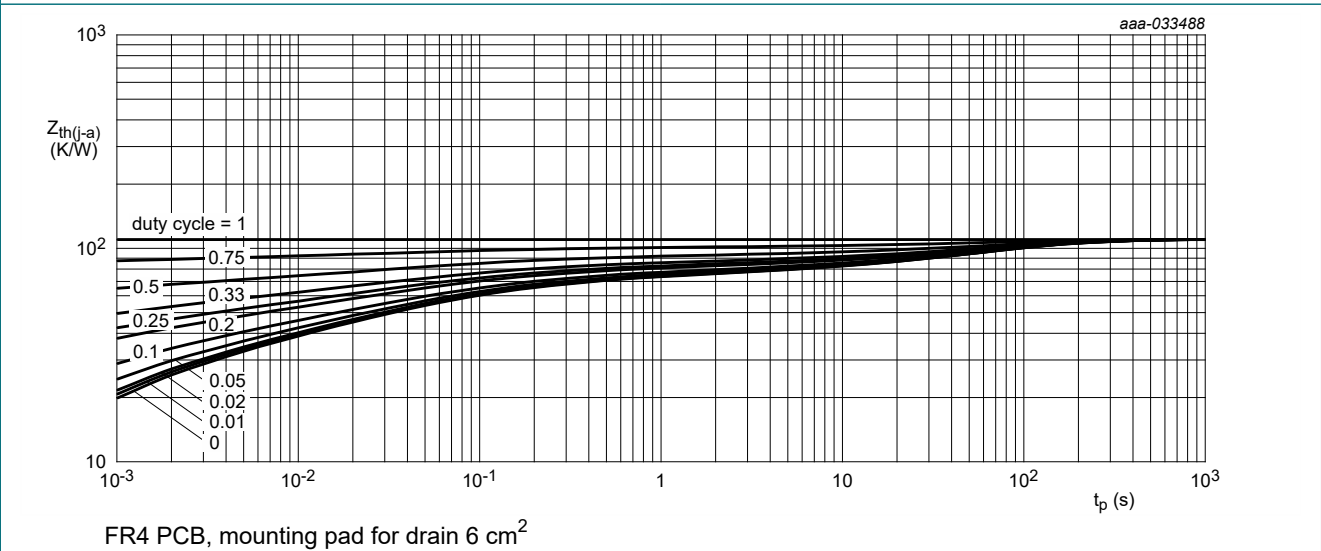


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|-------------------------|----------------------------------|---|--|-----|------|------|------|
| Static characteristics | | | | | | | |
| V _{(BR)DSS} | drain-source breakdown voltage | I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C | | 60 | - | - | V |
| V _{GSth} | gate-source threshold voltage | I _D = 250 μA; V _{DS} = V _{GS} ; T _j = 25 °C | | 1.3 | 1.7 | 2.6 | V |
| I _{DSS} | drain leakage current | V _{DS} = 60 V; V _{GS} = 0 V; T _j = 25 °C | | - | - | 1 | μA |
| I _{GSS} | gate leakage current | V _{GS} = 16 V; V _{DS} = 0 V; T _j = 25 °C | | - | - | 10 | μA |
| | | V _{GS} = -16 V; V _{DS} = 0 V; T _j = 25 °C | | - | - | -10 | μA |
| R _{DSon} | drain-source on-state resistance | V _{GS} = 10 V; I _D = 720 mA; T _j = 25 °C | | - | 635 | 850 | mΩ |
| | | V _{GS} = 10 V; I _D = 720 mA; T _j = 150 °C | | - | 1400 | 1800 | mΩ |
| | | V _{GS} = 4.5 V; I _D = 630 mA; T _j = 25 °C | | - | 765 | 1100 | mΩ |
| g _{fs} | forward transconductance | V _{DS} = 5 V; I _D = 720 mA; T _j = 25 °C | | - | 1.1 | - | S |
| Dynamic characteristics | | | | | | | |
| Q _{G(tot)} | total gate charge | V _{DS} = 30 V; I _D = 0.7 A; V _{GS} = 10 V; T _j = 25 °C | | - | 0.61 | 0.92 | nC |
| Q _{GS} | gate-source charge | | | - | 0.07 | - | nC |
| Q _{GD} | gate-drain charge | | | - | 0.15 | - | nC |
| C _{iss} | input capacitance | V _{DS} = 30 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C | | - | 28 | - | pF |
| C _{oss} | output capacitance | | | - | 5 | - | pF |
| C _{rss} | reverse transfer capacitance | | | - | 3 | - | pF |
| t _{d(on)} | turn-on delay time | V _{DS} = 30 V; I _D = 0.7 A; V _{GS} = 10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C | | - | 1 | - | ns |
| t _r | rise time | | | - | 1 | - | ns |
| t _{d(off)} | turn-off delay time | | | - | 6 | - | ns |
| t _f | fall time | | | - | 3 | - | ns |
| Source-drain diode | | | | | | | |
| V _{SD} | source-drain voltage | I _S = 0.7 A; V _{GS} = 0 V; T _j = 25 °C | | - | 0.7 | 1.2 | V |
| t _{rr} | reverse recovery time | I _S = 0.7 A; dI _S /dt = -100 A/s; V _{GS} = 10 V; V _{DS} = 30 V; T _j = 25 °C | | - | 8 | - | ns |
| Q _r | recovered charge | I _S = 0.7 A; dI _S /dt = -100 A/μs; V _{GS} = 10 V; V _{DS} = 30 V; T _j = 25 °C | | - | 2 | - | nC |

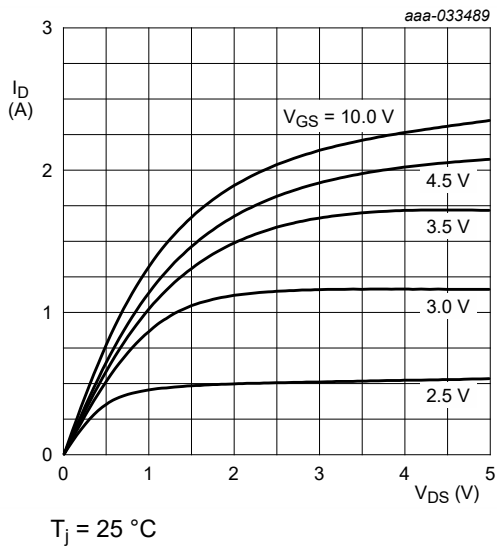


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

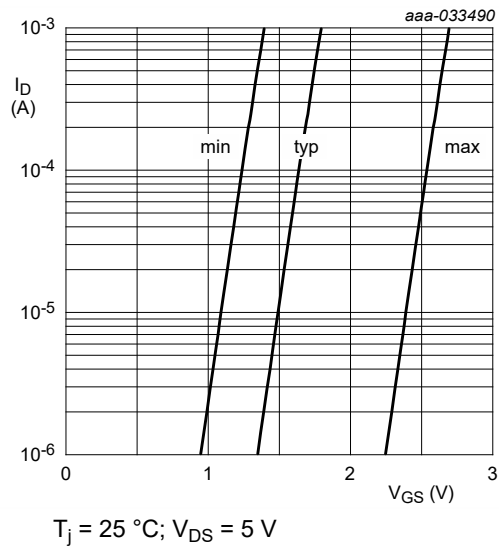


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

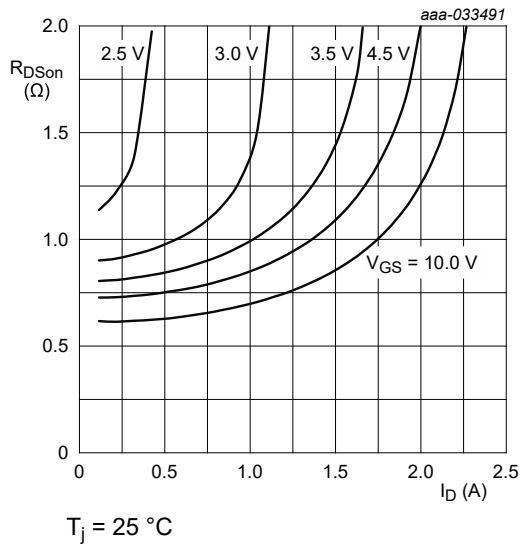


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

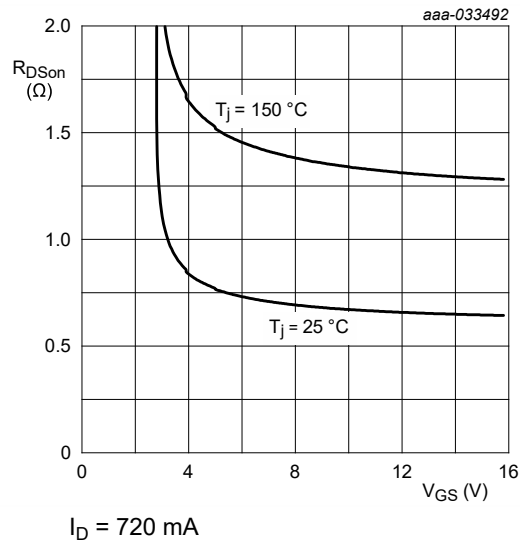


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

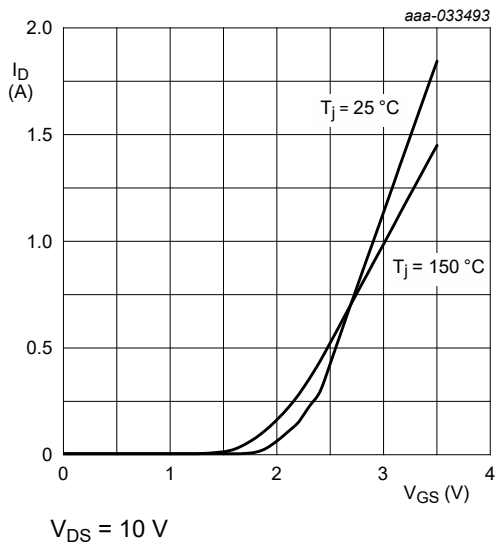


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

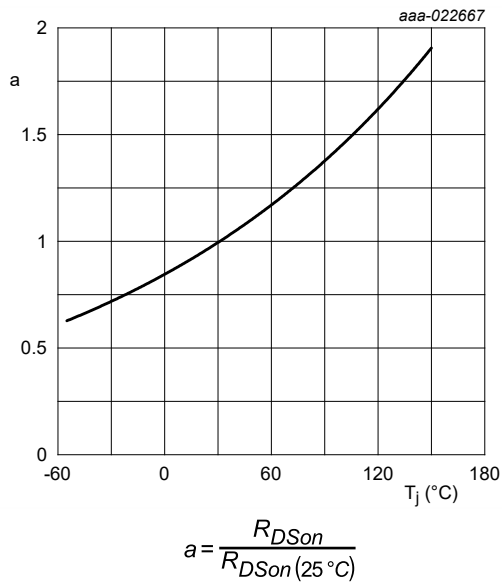


Fig. 11. Normalized drain-source on-state resistance as a function of ambient temperature; typical values

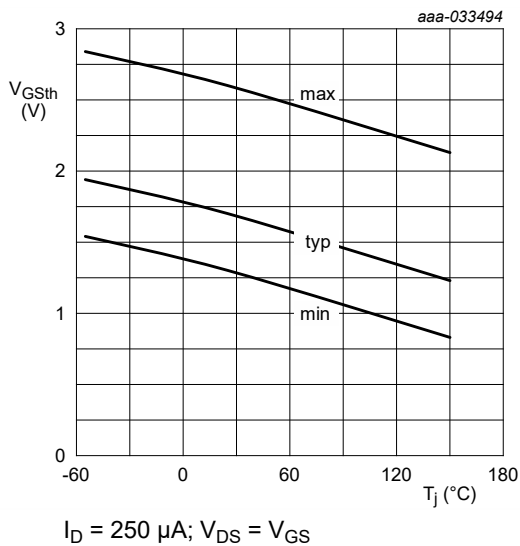


Fig. 12. Gate-source threshold voltage as a function of junction temperature

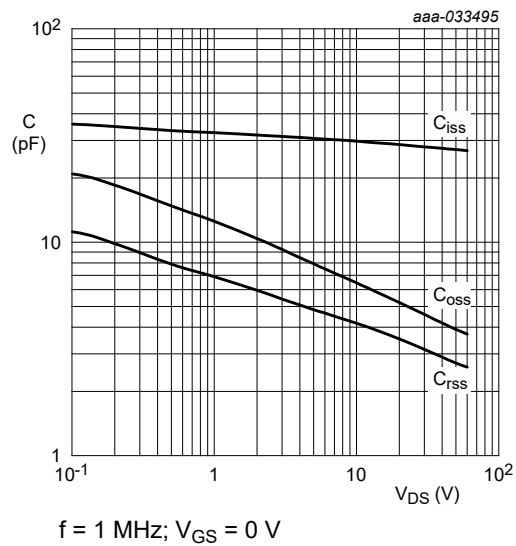


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

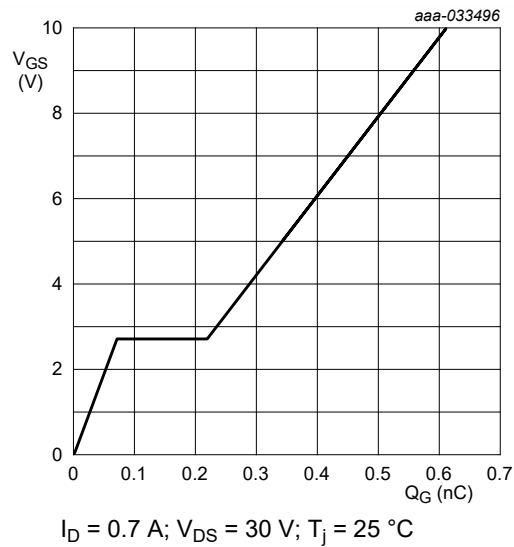


Fig. 14. Gate-source voltage as a function of gate charge; typical values

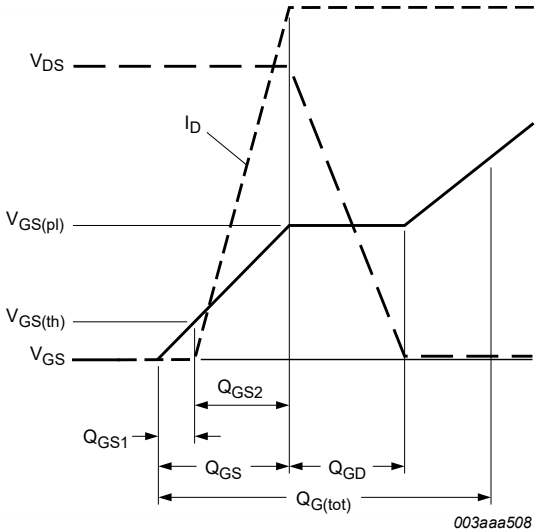


Fig. 15. Gate charge waveform definitions

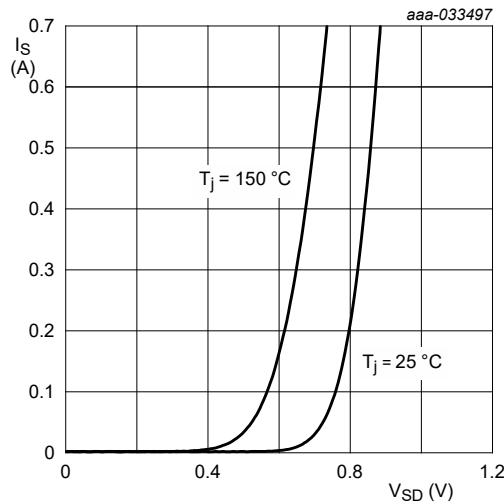


Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

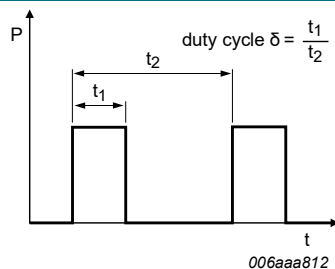


Fig. 17. Duty cycle definition

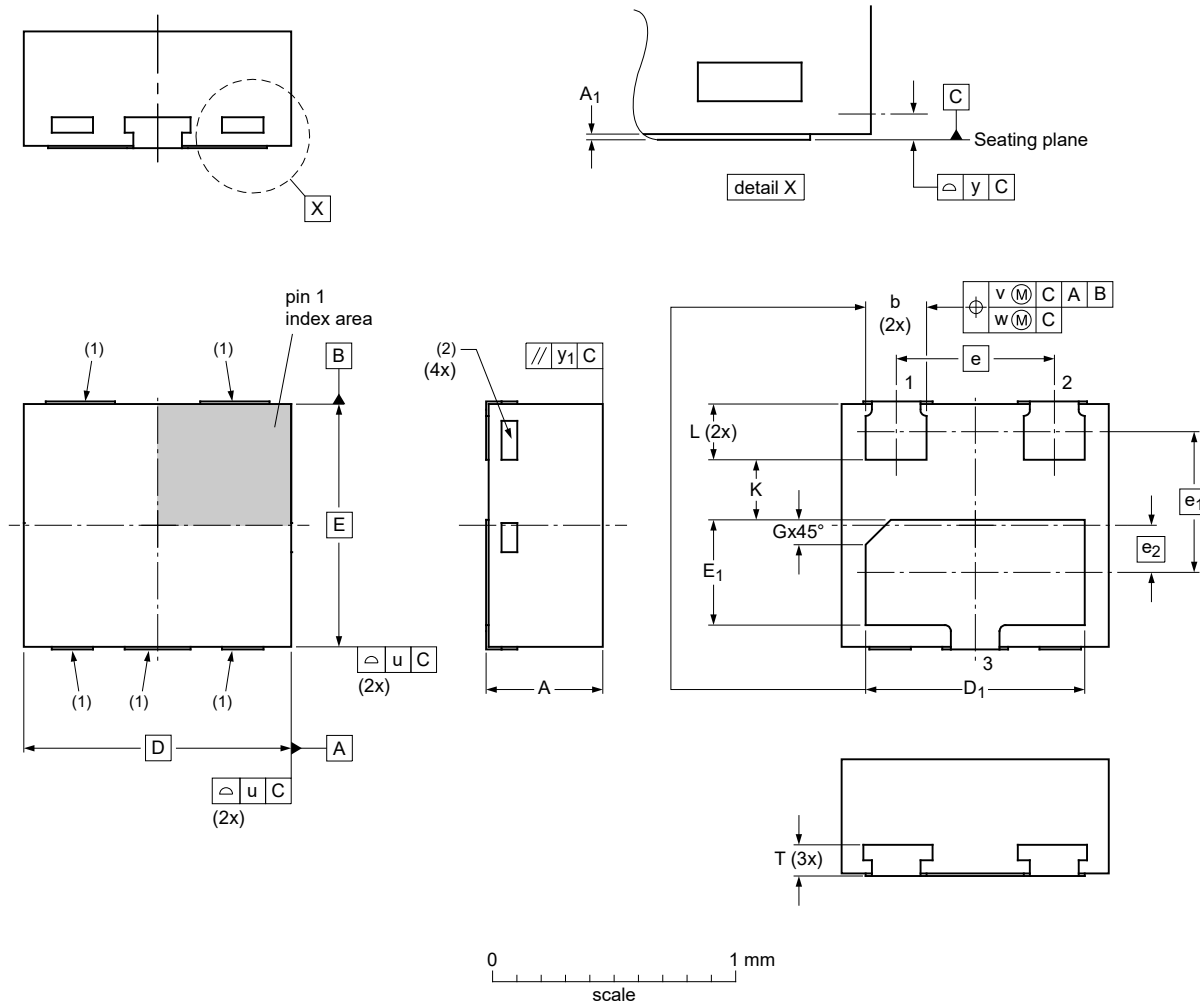
Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

DFN1110D-3: plastic, leadless extremely thin small outline package with side-wettable flanks (SWF); 3 terminals; 0.65 mm pitch; 1.1 mm x 1 mm x 0.48 mm body

SOT8015



Dimensions (mm are the original dimensions)

| Unit | A | A ₁ | b | D | D ₁ | E | E ₁ | e | e ₁ | e ₂ | G | K | L | T | u | v | w | y | y ₁ |
|------|------|----------------|------|-----|----------------|---|----------------|------|----------------|----------------|-------|-----|------|------|------|-----|------|------|----------------|
| max | 0.50 | 0.040 | 0.30 | | 0.95 | | 0.48 | | | | | | 0.27 | 0.22 | | | | | |
| nom | 0.47 | 0.020 | 0.25 | 1.1 | 0.90 | 1 | 0.43 | 0.65 | 0.58 | 0.19 | 0.09 | | 0.23 | 0.16 | 0.05 | 0.1 | 0.05 | 0.05 | 0.05 |
| min | 0.44 | 0.005 | 0.22 | | 0.87 | | 0.40 | | | | (ref) | 0.2 | 0.20 | 0.10 | | | | | |

Note

1. Side Wettable Flank, protrusion max. 0.02 mm.

2. Visible depend upon used manufacturing technology.

Dimension A and T are including plating thickness.

sot8015_po

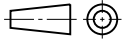
| Outline version | References | | | | European projection | Issue date |
|-----------------|------------|----------|-------|--|---|----------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT8015 | | MO-340BA | | |  | 19-12-02 19-12-04 |

Fig. 18. Package outline DFN1110D-3 (SOT8015)

13. Soldering

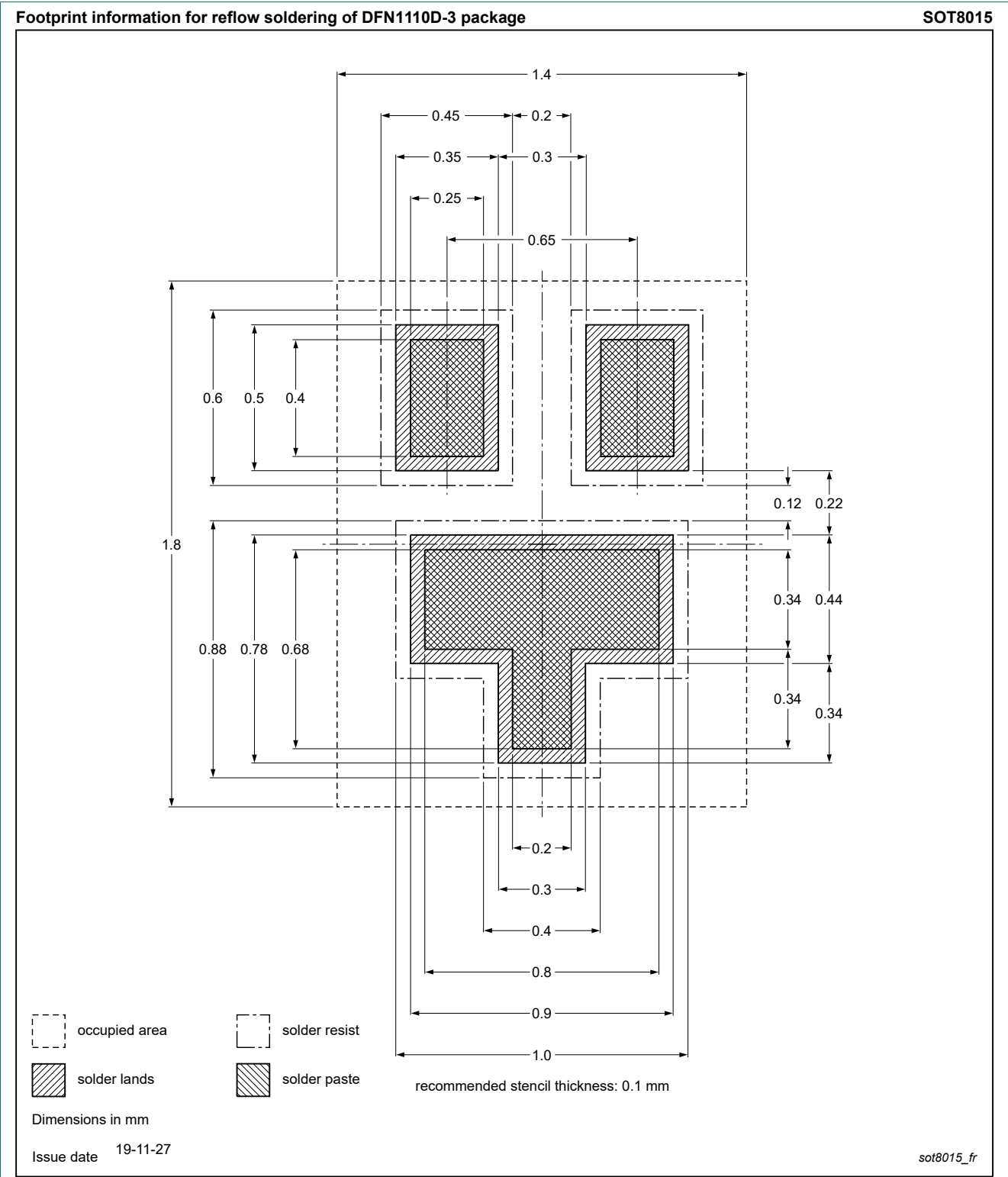


Fig. 19. Reflow soldering footprint for DFN1110D-3 (SOT8015)

14. Revision history

Table 8. Revision history

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------|--------------|--------------------|---------------|------------|
| 2N7002KQB v.1 | 20210922 | Product data sheet | - | - |

15. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

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