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STFI34NM60N

N-channel 600 V, 0.092 Ω , 29 A MDmesh™ II Power MOSFET in I²PAKFP package

Datasheet — production data

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STFI34NM60N	600 V	0.105 Ω	29 A	40 W

- Fully insulated and low profile package with increased creepage path from pin to heatsink plate
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

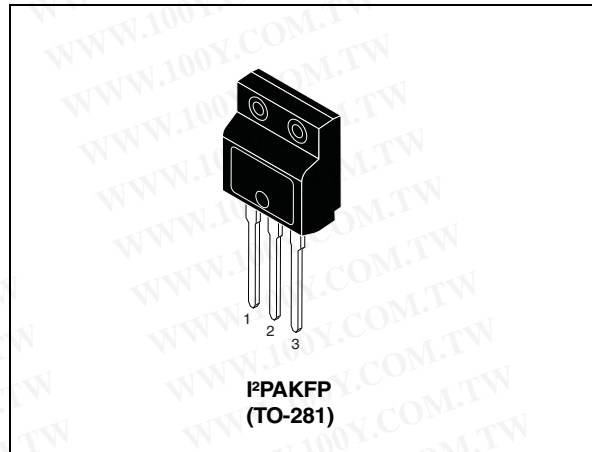


Figure 1. Internal schematic diagram

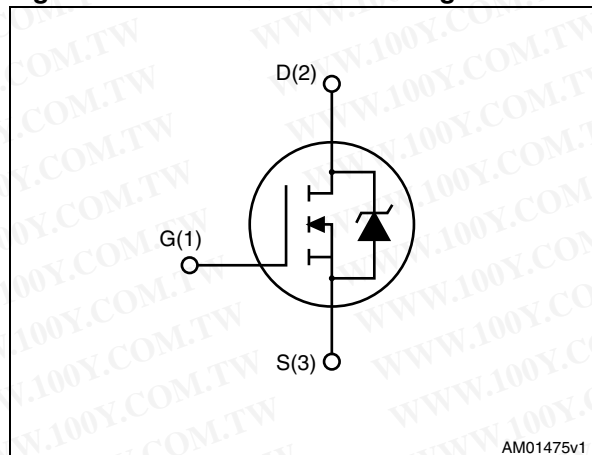


Table 1. Device summary

Order code	Marking	Package	Packaging
STFI34NM60N	34NM60N	I ² PAKFP (TO-281)	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate- source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	29 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	18 ⁽¹⁾	A
$I_{DM}^{(2)}$	Drain current (pulsed)	116	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	40	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	10.5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	345	mJ
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ }^\circ\text{C}$)	2500	V
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_J	Max. operating junction temperature	150	

1. Limited by maximum junction temperature.

2. Pulse width limited by safe operating area.

3. $I_{SD} \leq 29\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS\text{ peak}} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	3.1	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 600\text{ V}$ $V_{DS} = 600\text{ V}, T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 14.5\text{ A}$		0.092	0.105	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$		2722		pF	
C_{oss}	Output capacitance		-	173	-	pF	
C_{rss}	Reverse transfer capacitance				1.75	pF	
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0\text{ to }480\text{ V}$	-	458	-	pF	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}, I_D = 14.5\text{ A}$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 19), (see Figure 14)		17		ns	
t_r	Rise time			34		ns	
$t_{d(off)}$	Turn-off delay time				106		ns
t_f	Fall time				70		ns
Q_g	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 29\text{ A},$ $V_{GS} = 10\text{ V},$ (see Figure 15)		84		nC	
Q_{gs}	Gate-source charge			14		nC	
Q_{gd}	Gate-drain charge			45		nC	
R_g	Gate input resistance	f=1MHz Gate DC Bias=0 Test signal level=20 mV Open drain	-	2.9	-	Ω	

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		29	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		116	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 29\text{ A}, V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 29\text{ A}, V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ (see Figure 16)	-	408		ns
Q_{rr}	Reverse recovery charge		-	8		μC
I_{RRM}	Reverse recovery current		-	39		A
t_{rr}	Reverse recovery time	$I_{SD} = 29\text{ A}, V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 16)	-	480		ns
Q_{rr}	Reverse recovery charge		-	10		μC
I_{RRM}	Reverse recovery current		-	42		A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

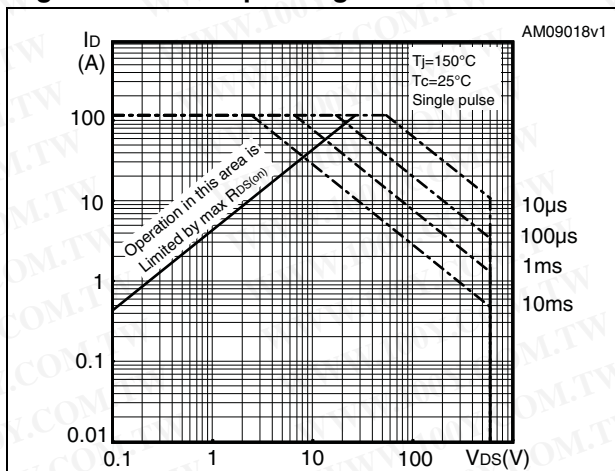


Figure 3. Thermal impedance

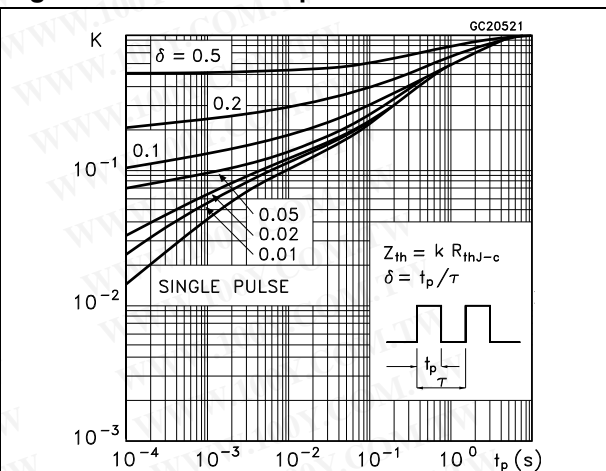


Figure 4. Output characteristics

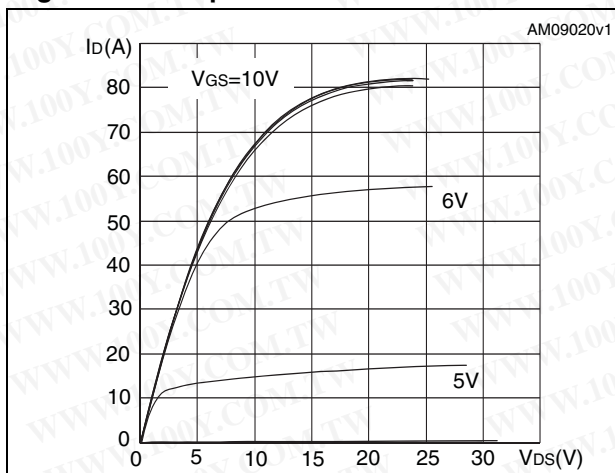


Figure 5. Transfer characteristics

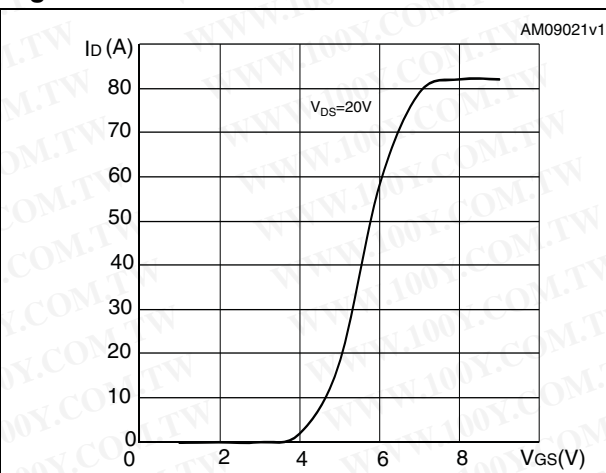


Figure 6. Gate charge vs. gate-source voltage

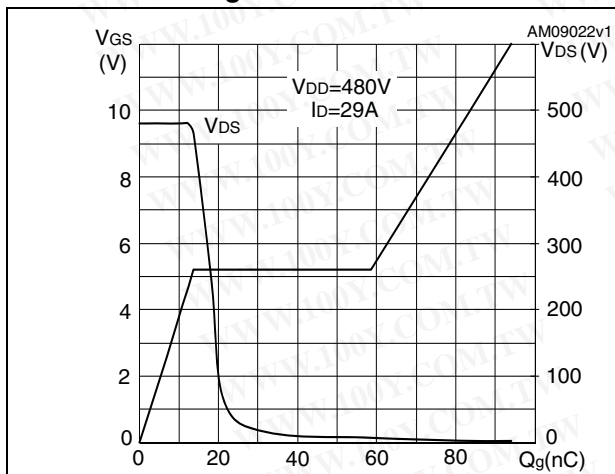


Figure 7. Static drain-source on-resistance

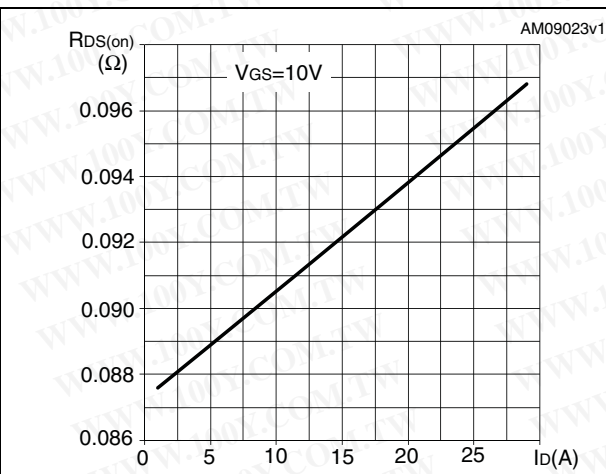


Figure 8. Capacitance variations

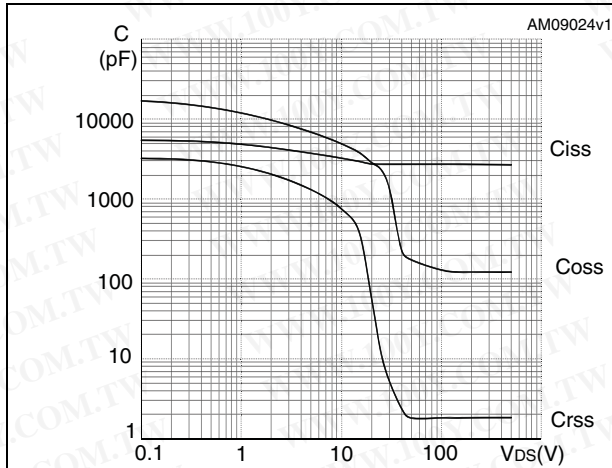


Figure 9. Output capacitance stored energy

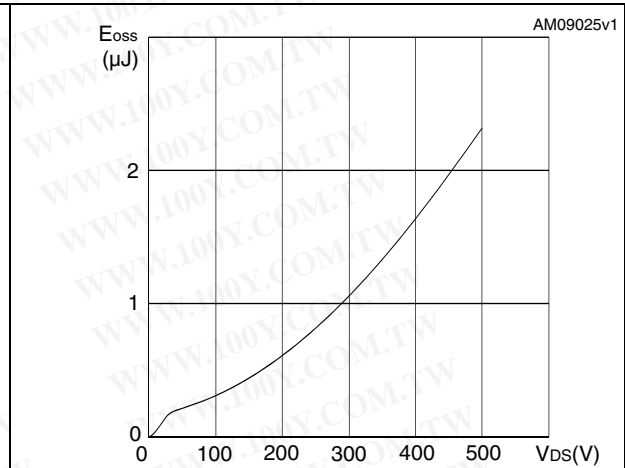


Figure 10. Normalized gate threshold voltage vs. temperature

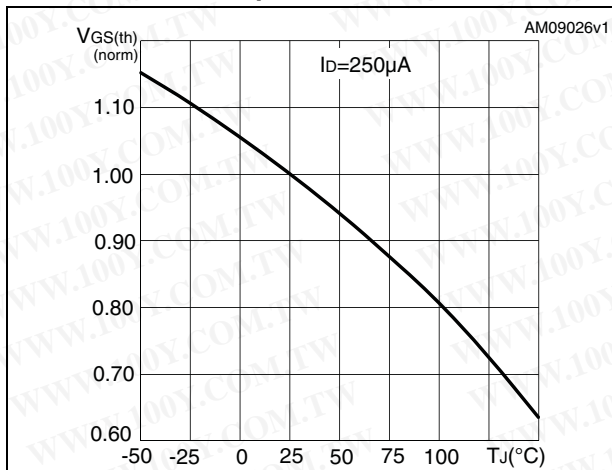


Figure 11. Normalized on-resistance vs. temperature

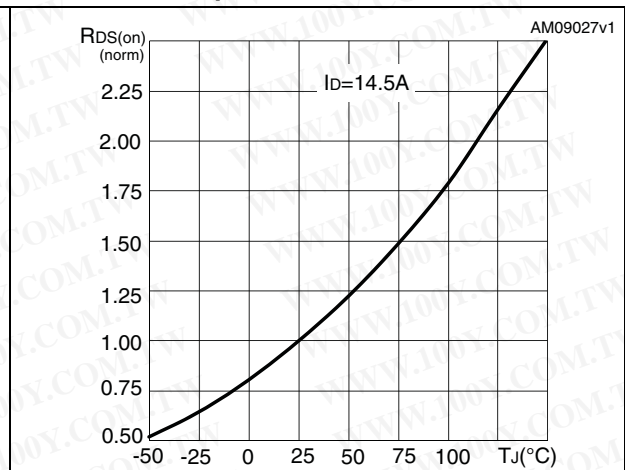


Figure 12. Normalized V_{DS} vs. temperature

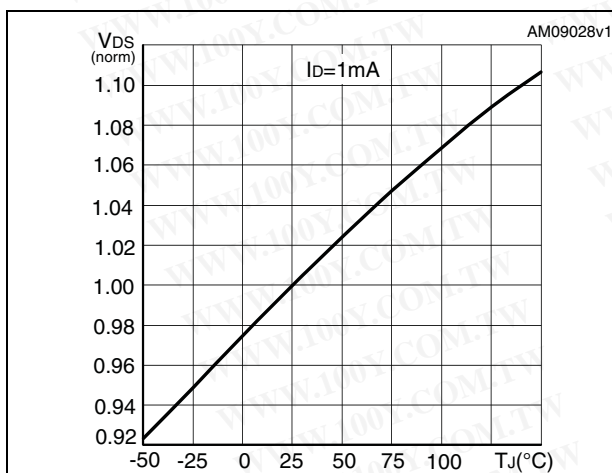
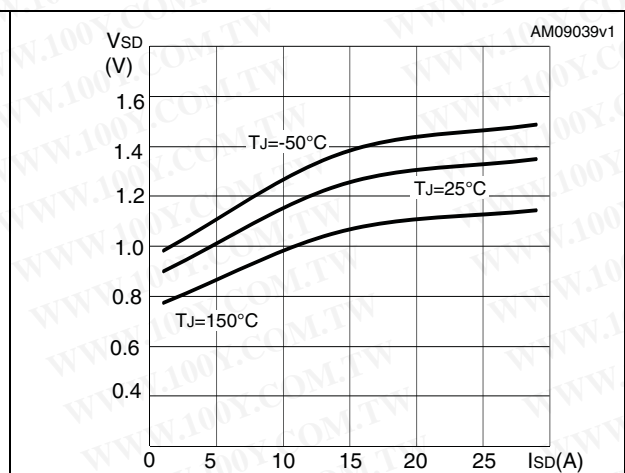


Figure 13. Source-drain diode forward characteristics



3 Test circuits

Figure 14. Switching times test circuit for resistive load

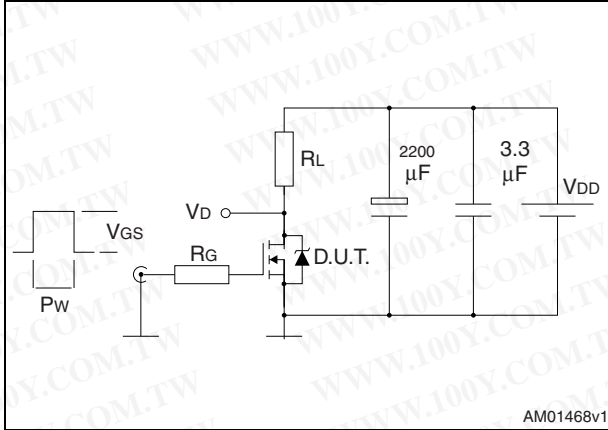


Figure 15. Gate charge test circuit

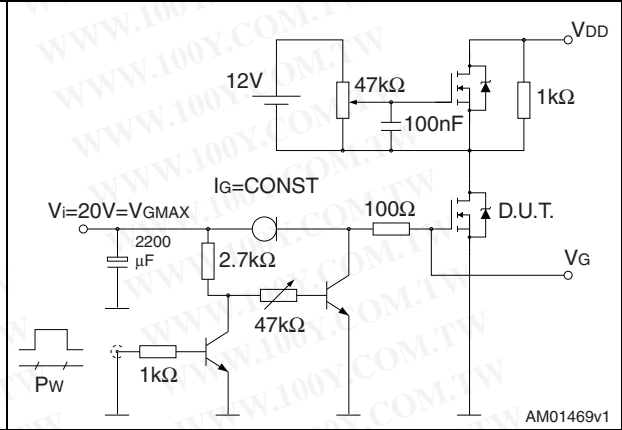


Figure 16. Test circuit for inductive load switching and diode recovery times

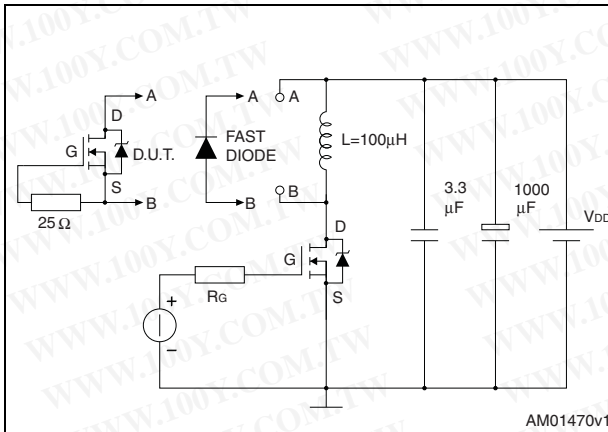


Figure 17. Unclamped inductive load test circuit

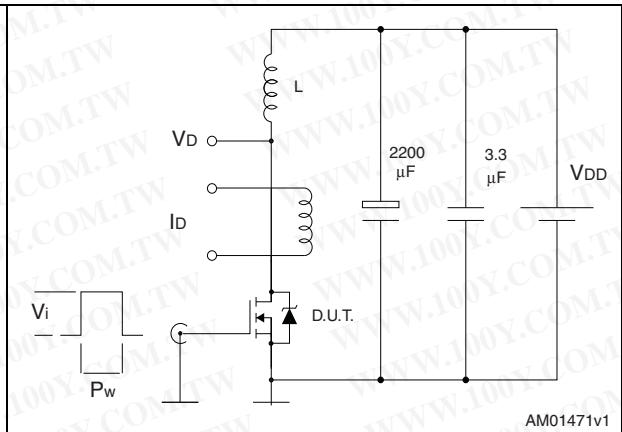


Figure 18. Unclamped inductive waveform

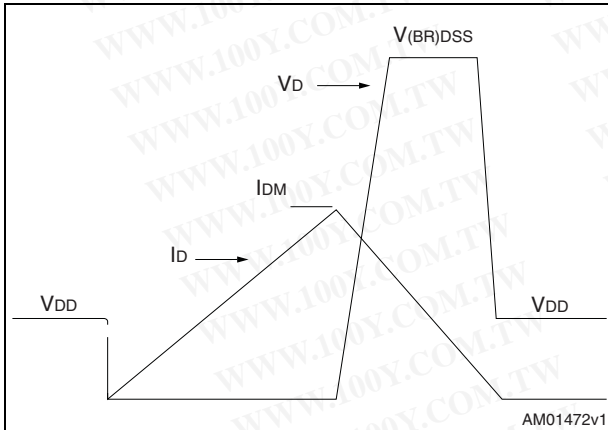
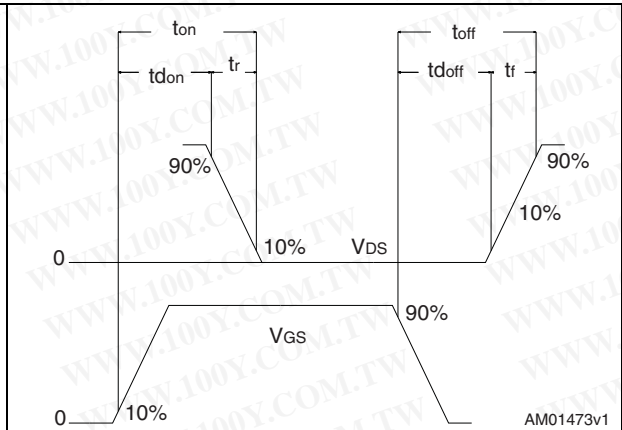


Figure 19. Switching time waveform



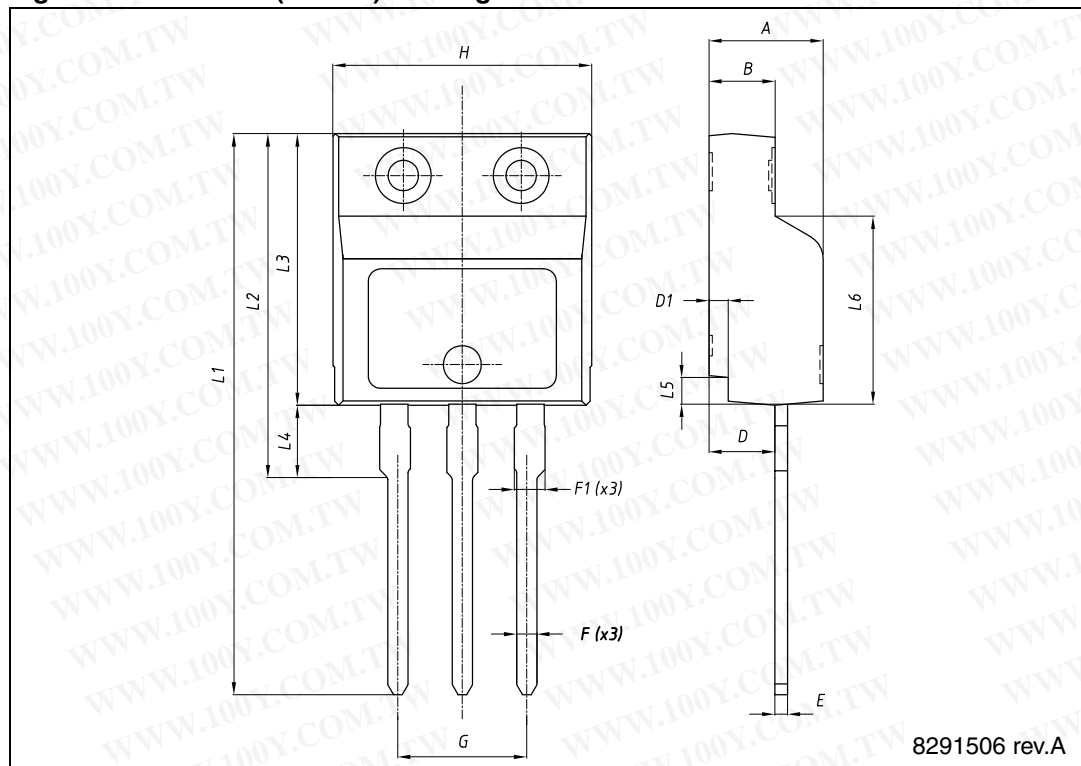
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 7. I²PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95	-	5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

Figure 20. I²PAKFP (TO-281) drawing



5 Revision history

Table 8. Document revision history

Date	Revision	Changes
07-Nov-2011	1	Initial release.
19-Apr-2012	2	Units in Table 6: Source drain diode have been corrected. Figure 6: Gate charge vs. gate-source voltage has been updated. Minor text changes.

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