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# STF8N80K5, STFI8N80K5

N-channel 800 V, 0.8 Ω typ., 6 A Zener-protected SuperMESH™ 5 Power MOSFET in TO-220FP and I<sup>2</sup>PAKFP packages

Datasheet – preliminary data

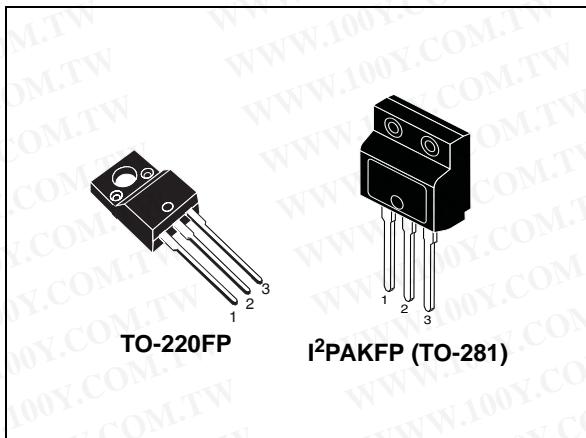


Figure 1. Internal schematic diagram

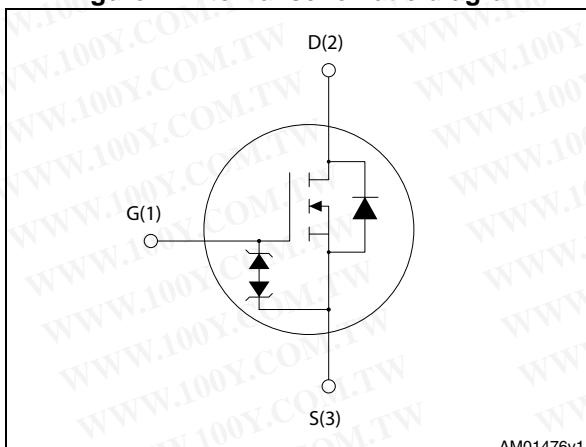


Table 1. Device summary

Order codes	Marking	Package	Packaging
STF8N80K5	8N80K5	TO-220FP	Tube
STFI8N80K5		I <sup>2</sup> PAKFP (TO-281)	

## Features

Order codes	V <sub>DS</sub>	R <sub>DS(on)max.</sub>	I <sub>D</sub>	P <sub>TOT</sub>
STF8N80K5	800 V	0.95 Ω	6 A	25 W
STFI8N80K5				

- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

## Applications

- Switching applications

## Description

These N-channel Zener-protected Power MOSFETs are designed using ST's revolutionary avalanche-rugged very high voltage SuperMESH™ 5 technology, based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance, and ultra-low gate charge for applications which require superior power density and high efficiency.

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current $T_C = 25^\circ\text{C}$	6 <sup>(1)</sup>	A
$I_D$	Drain current $T_C = 100^\circ\text{C}$	4 <sup>(1)</sup>	A
$I_{DM}^{(2)}$	Drain current (pulsed)	24 <sup>(1)</sup>	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	25	W
$I_{AR}^{(3)}$	Max current during repetitive or single pulse avalanche	2	A
$E_{AS}^{(4)}$	Single pulse avalanche energy (starting $T_J = 25^\circ\text{C}$ , $I_D=I_{AS}$ , $V_{DD}=50\text{ V}$ )	114	mJ
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t=1\text{ s}; T_C=25^\circ\text{C}$ )	2500	V
$dv/dt^{(5)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(6)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_j$	Operating junction temperature	-55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature		$^\circ\text{C}$

1. Limited by package.
2. Pulse width limited by safe operating area.
3. Pulse width limited by  $T_{Jmax}$ .
4. Starting  $T_J = 25^\circ\text{C}$ ,  $I_D=I_{AS}$ ,  $V_{DD}=50\text{ V}$
5.  $I_{SD} \leq 6\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ ,  $V_{DS(\text{peak})} \leq V_{(\text{BR})DSS}$
6.  $V_{DS} \leq 640\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	5	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb max.	62.5	$^\circ\text{C}/\text{W}$

## 2 Electrical characteristics

( $T_{CASE} = 25^\circ\text{C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	800			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 800 \text{ V}$ ,			1	$\mu\text{A}$
		$V_{DS} = 800 \text{ V}, T_c = 125^\circ\text{C}$			50	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 \text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100 \mu\text{A}$	3	4	5	V
$R_{DS(\text{on})}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}, I_D = 3 \text{ A}$		0.8	0.95	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0$	-	450	-	pF
$C_{oss}$	Output capacitance		-	50	-	pF
$C_{rss}$	Reverse transfer capacitance		-	1	-	pF
$C_{o(\text{tr})}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0, V_{DS} = 0 \text{ to } 640 \text{ V}$	-	57	-	pF
$C_{o(\text{er})}^{(2)}$	Equivalent capacitance energy related		-	24	-	pF
$R_G$	Intrinsic gate resistance	$f = 1 \text{ MHz open drain}$	-	6	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 640 \text{ V}, I_D = 6 \text{ A}$ $V_{GS} = 10 \text{ V}$ (see <a href="#">Figure 16</a> )	-	16.5	-	nC
$Q_{gs}$	Gate-source charge		-	3.2	-	nC
$Q_{gd}$	Gate-drain charge		-	11	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400 \text{ V}$ , $I_D = 3 \text{ A}$ , $R_G = 4.7 \Omega$ , $V_{GS} = 10 \text{ V}$ (see <i>Figure 18</i> )	-	12	-	ns
$t_r$	Rise time			14	-	ns
$t_{d(off)}$	Turn-off delay time			32	-	ns
$t_f$	Fall time			20	-	ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		6	A
$I_{SDM}$	Source-drain current (pulsed)				24	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 6 \text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 6 \text{ A}$ , $V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$ , (see <i>Figure 17</i> )	-	300		ns
$Q_{rr}$	Reverse recovery charge			3		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			20		A
$t_{rr}$	Reverse recovery time		-	415		ns
$Q_{rr}$	Reverse recovery charge	$I_{SD} = 6 \text{ A}$ , $V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$ , $T_j = 150^\circ\text{C}$ (see <i>Figure 17</i> )	-	3.8		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	18		A

1. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

**Table 8. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$ , $I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

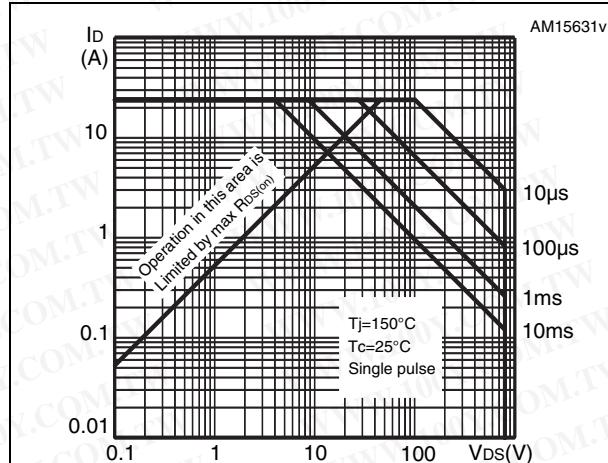


Figure 3. Thermal impedance

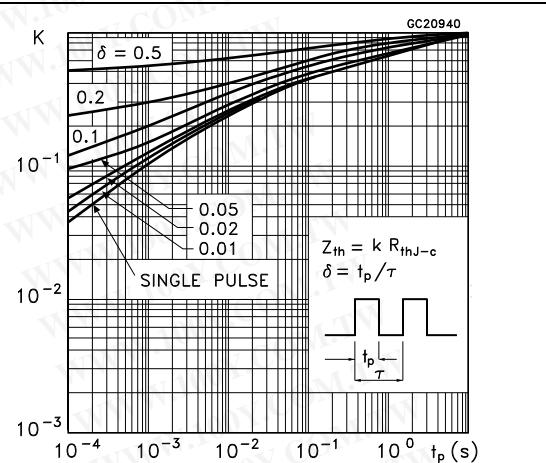


Figure 4. Output characteristics

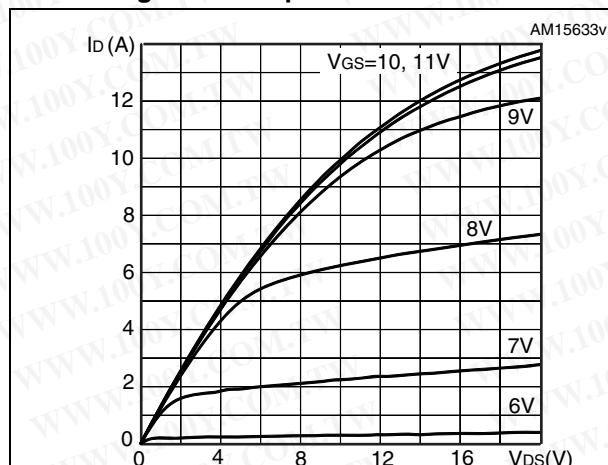


Figure 5. Transfer characteristics

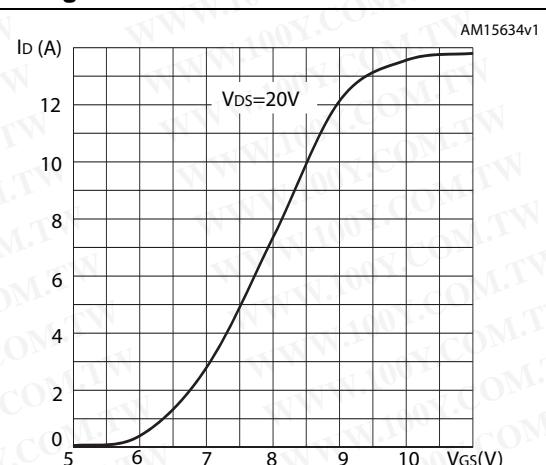


Figure 6. Gate charge vs gate-source voltage

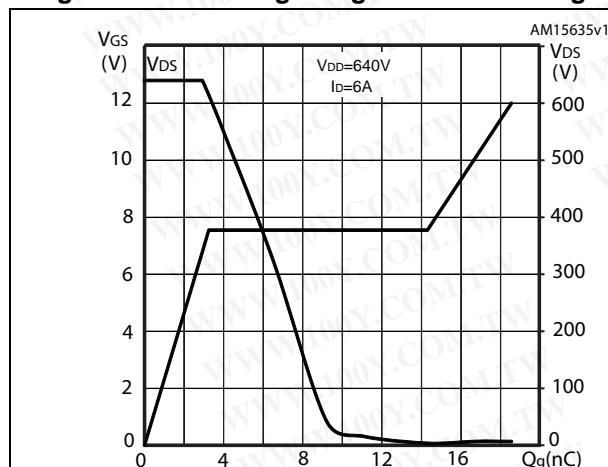
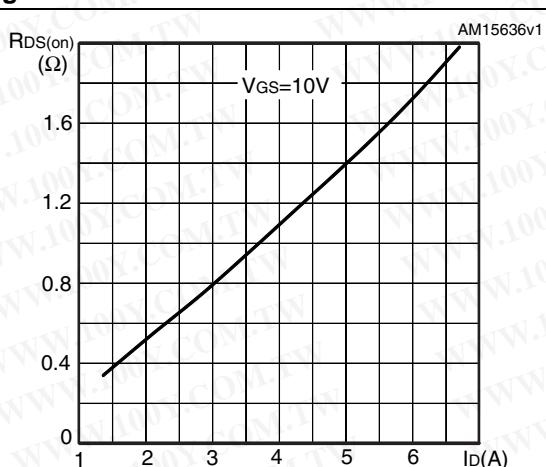
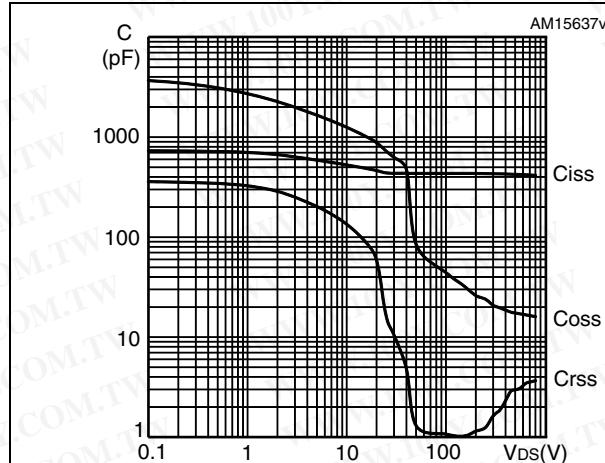
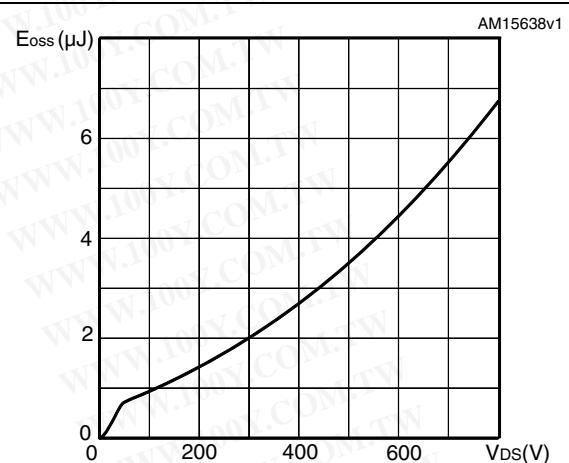
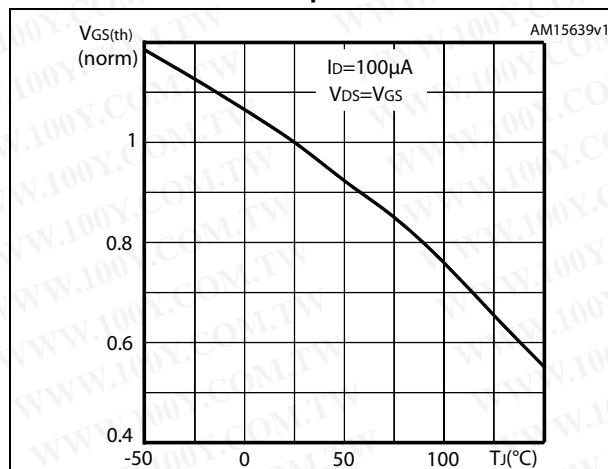
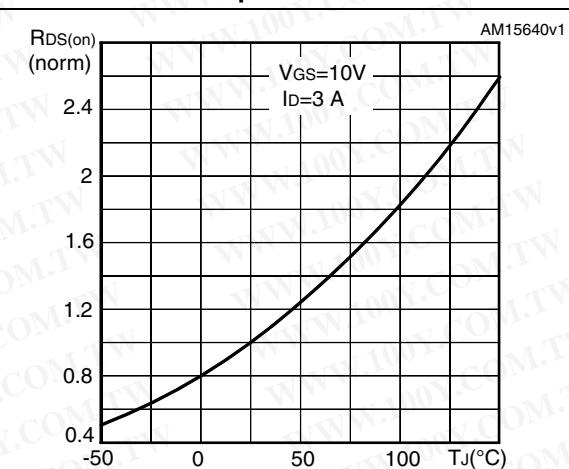
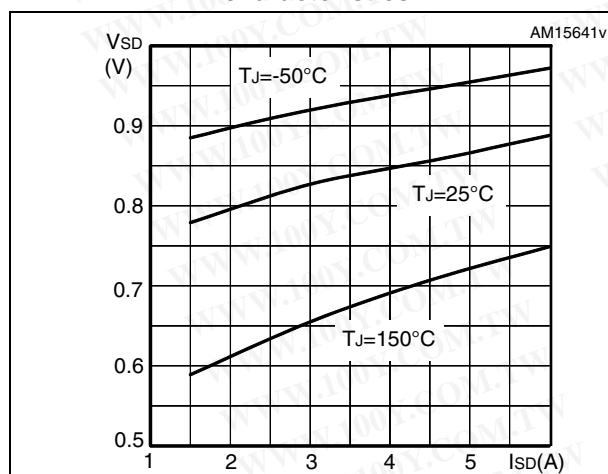
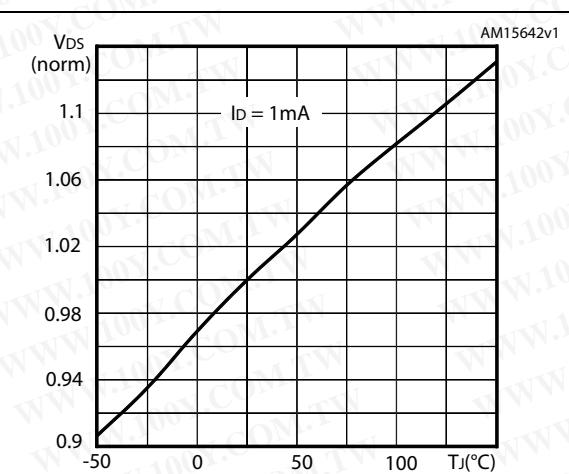
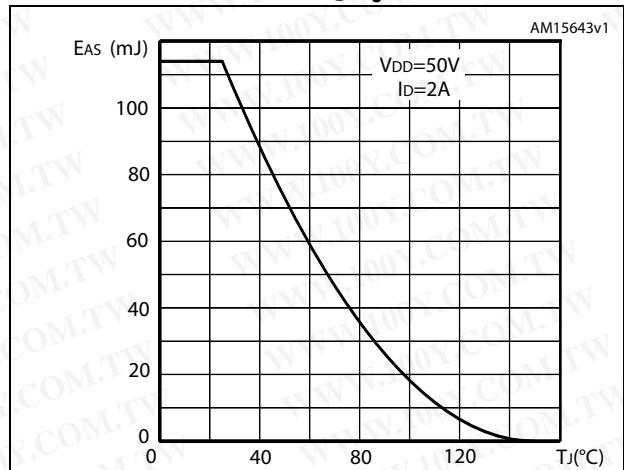


Figure 7. Static drain-source on-resistance



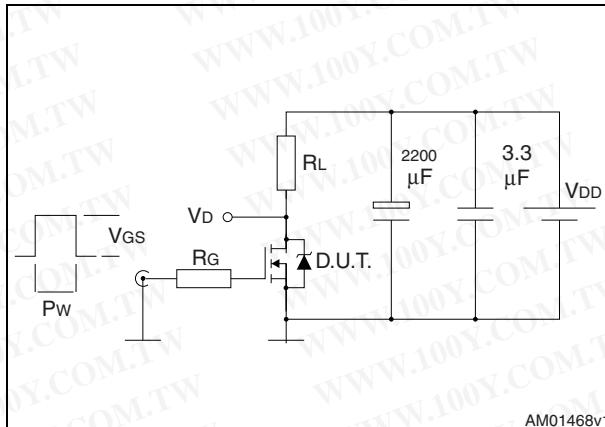
**Figure 8. Capacitance variations****Figure 9. Output capacitance stored energy****Figure 10. Normalized gate threshold voltage vs. temperature****Figure 11. Normalized on-resistance vs. temperature****Figure 12. Drain-source diode forward characteristics****Figure 13. Normalized  $V_{DS}$  vs. temperature**

**Figure 14. Maximum avalanche energy vs.  
starting  $T_J$**

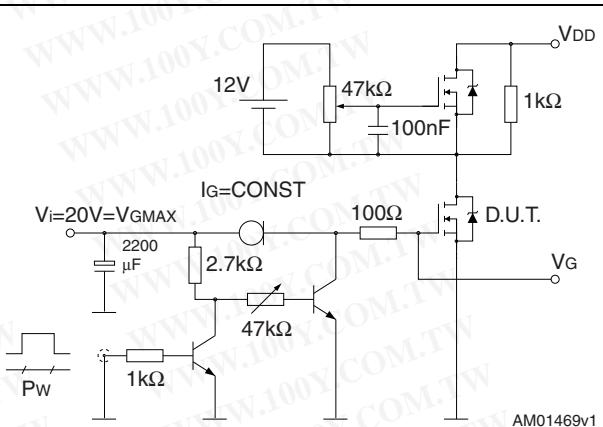


### 3 Test circuits

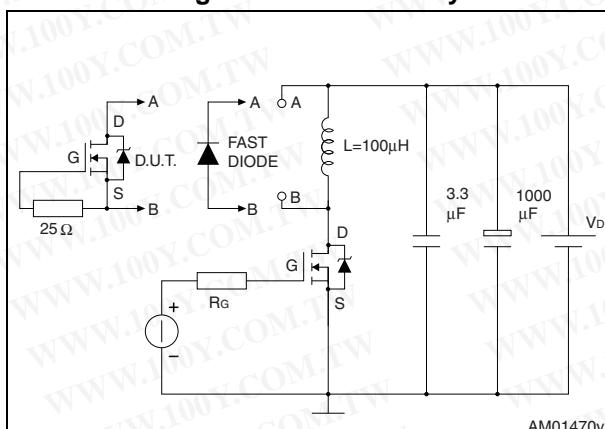
**Figure 15. Switching times test circuit for resistive load**



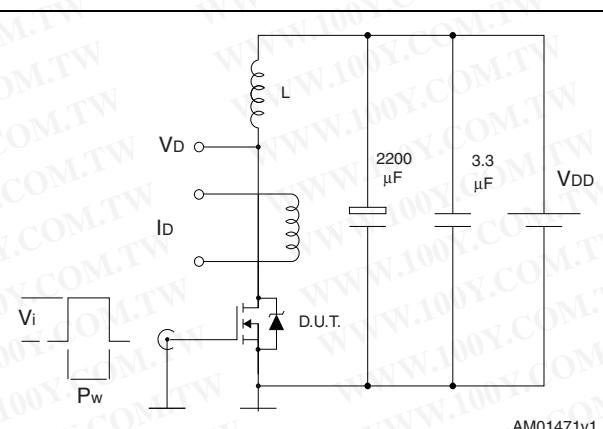
**Figure 16. Gate charge test circuit**



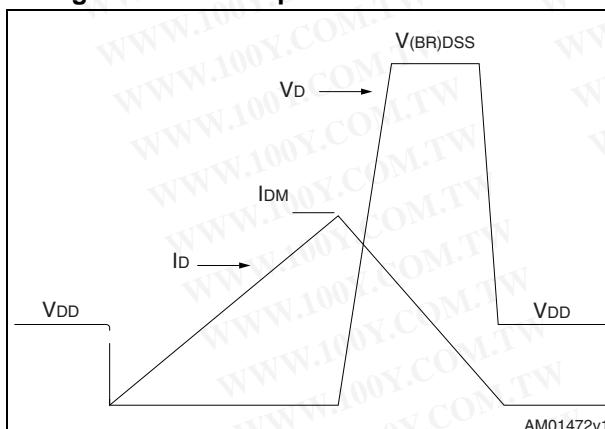
**Figure 17. Test circuit for inductive load switching and diode recovery times**



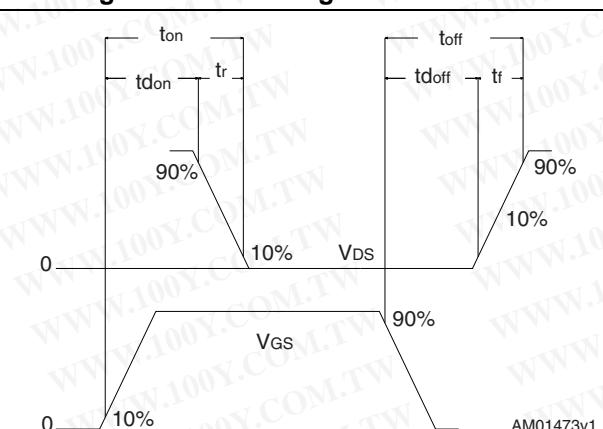
**Figure 18. Unclamped inductive load test circuit**



**Figure 19. Unclamped inductive waveform**



**Figure 20. Switching time waveform**



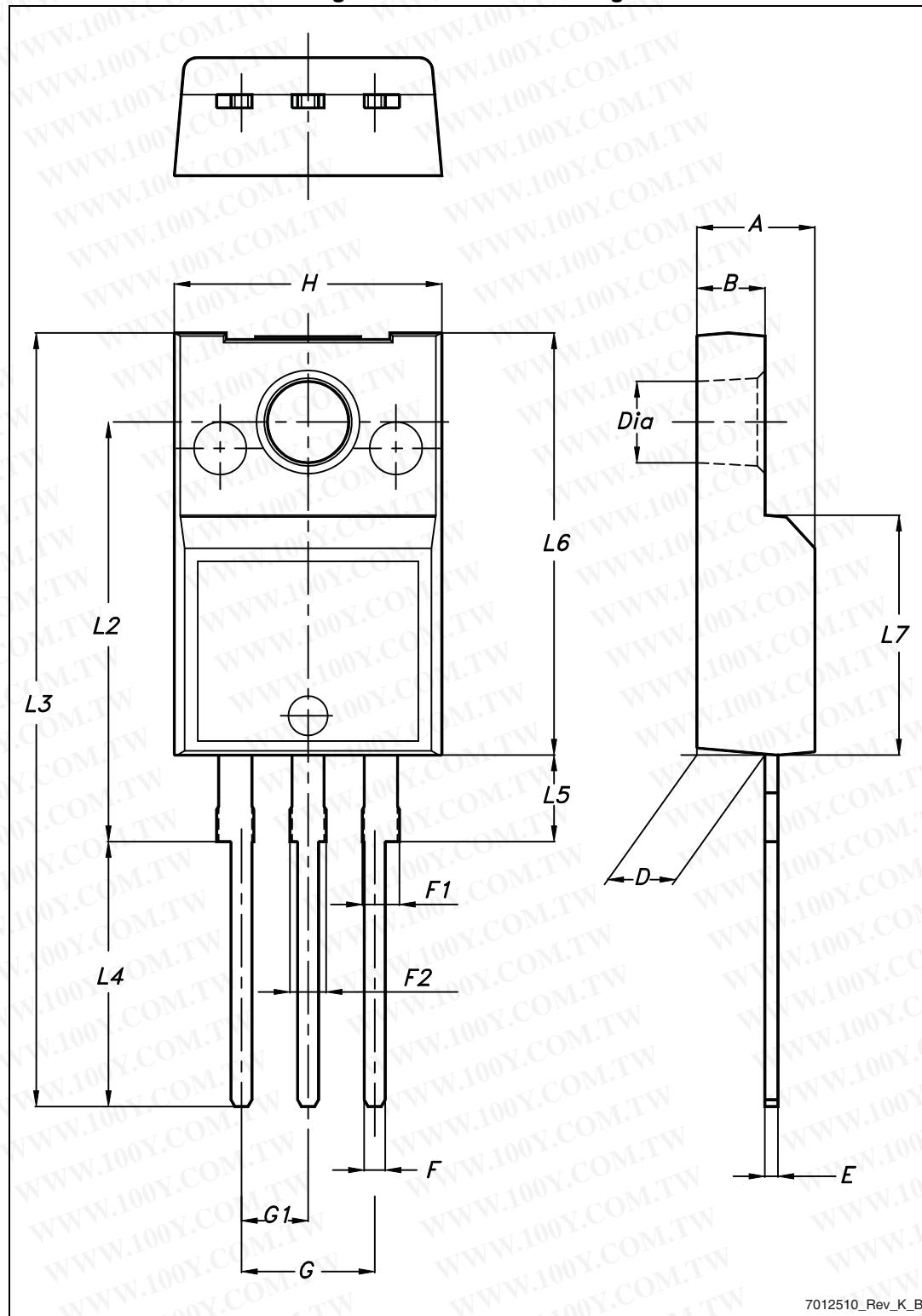
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).  
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**Table 9. TO-220FP mechanical data**

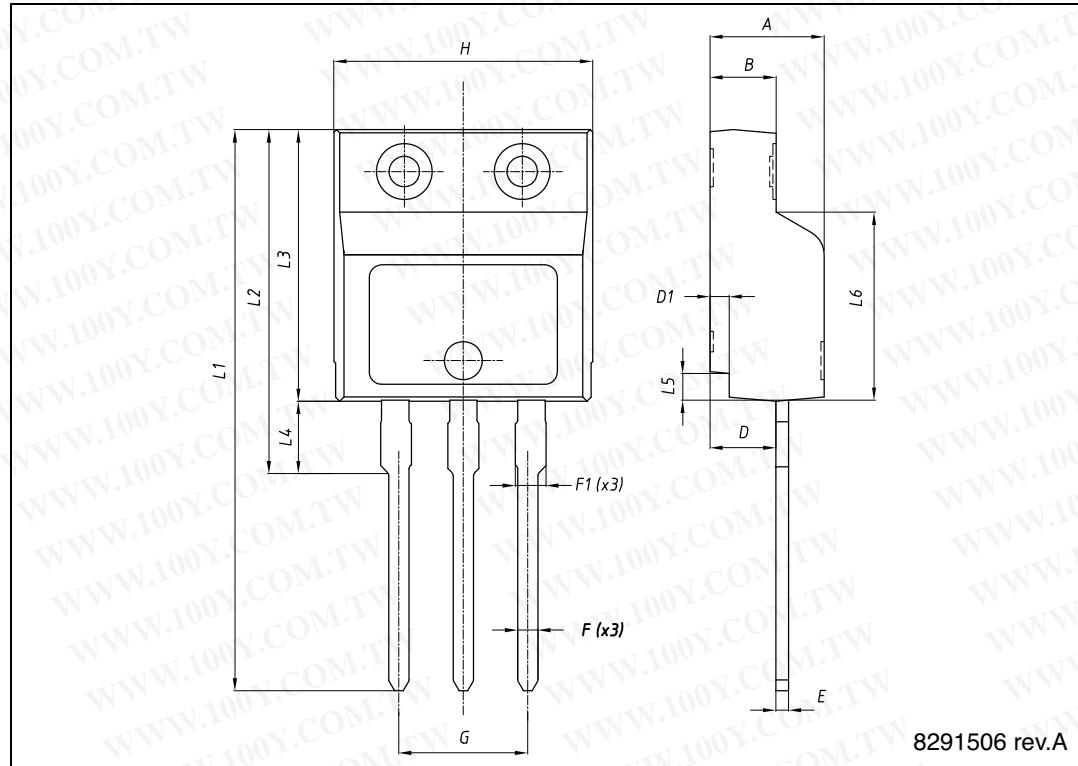
Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 21. TO-220FP drawing



**Table 10. I<sup>2</sup>PAKFP (TO-281) mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95		5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

**Figure 22. I<sup>2</sup>PAKFP (TO-281) drawing**

## 5 Revision history

**Table 11. Document revision history**

Date	Revision	Changes
25-Mar-2012	1	First release. Part numbers previously included in datasheet DM00062075
27-Mar-2013	2	Added: MOSFET dv/dt ruggedness on <a href="#">Table 2</a>

勝特力材料 886-3-5753170  
胜特力电子(上海) 86-21-34970699  
胜特力电子(深圳) 86-755-83298787  
[Http://www.100y.com.tw](http://www.100y.com.tw)

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