



STL6N2VH5

N-channel 20 V, 0.025 Ω typ., 6 A STripFET™ V Power MOSFET in PowerFLAT™ 2x2 package

Datasheet – preliminary data

Features

Order code	V _{DSS}	R _{DS(on)} max.	I _D	P _{TOT}
STL6N2VH5	20 V	0.03 Ω (V _{GS} =4.5 V) 0.04 Ω (V _{GS} =2.5 V)	6 A	2.4 W

- Very low switching gate charge
- Very low thermal resistance
- Conduction losses reduced
- Switching losses reduced
- 2.5 V gate drive
- Very low threshold device

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™V technology. The device has been optimized to achieve very low on-state resistance, contributing to an FOM that is among the best in its class.

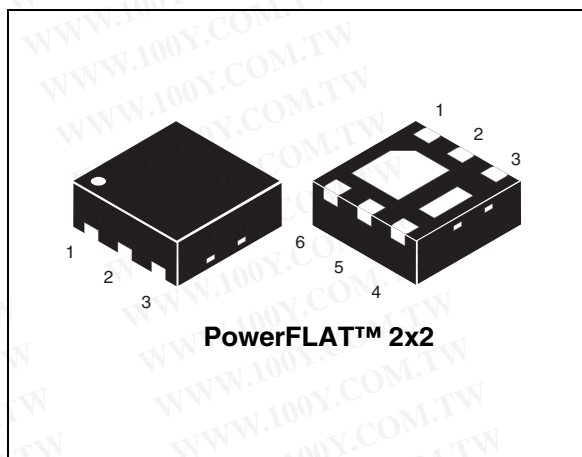


Figure 1. Internal schematic diagram

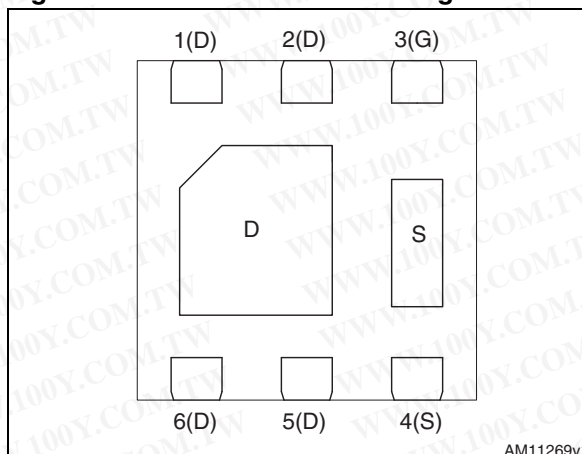


Table 1. Device summary

Order code	Marking	Package	Packaging
STL6N2VH5	STD1	PowerFLAT™ 2x2	Tape and reel

勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-34970699
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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	20	V
V_{GS}	Gate-source voltage	± 8	V
$I_D^{(1)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	6	A
$I_D^{(1)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	3.75	A
$I_{DM}^{(1),(2)}$	Drain current (pulsed)	24	A
$P_{TOT}^{(1)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	2.4	W
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. The value is rated according $R_{thj-pcb}$
2. Pulse width limited by safe operating area.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	52	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{ sec}$

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	20			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 20\ \text{V}$, $V_{DS} = 20\ \text{V}$, $T_J = 125\text{ °C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 8\ \text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	0.7			V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 4.5\ \text{V}$, $I_D = 3\ \text{A}$ $V_{GS} = 2.5\ \text{V}$, $I_D = 3\ \text{A}$		0.025 0.031	0.03 0.04	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 16\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0$		550		pF
C_{oss}	Output capacitance		-	110	-	pF
C_{rss}	Reverse transfer capacitance				16	
Q_g	Total gate charge	$V_{DD} = 10\ \text{V}$, $I_D = 6\ \text{A}$ $V_{GS} = 4.5\ \text{V}$ (see Figure 3)		6		nC
Q_{gs}	Gate-source charge		-	TBD	-	nC
Q_{gd}	Gate-drain charge				TBD	

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 10\ \text{V}$, $I_D = 3\ \text{A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 4.5\ \text{V}$ (see Figure 2)		TBD		ns
t_r	Rise time			TBD		ns
$t_{d(off)}$	Turn-off delay time		-		TBD	ns
t_f	Fall time				TBD	ns

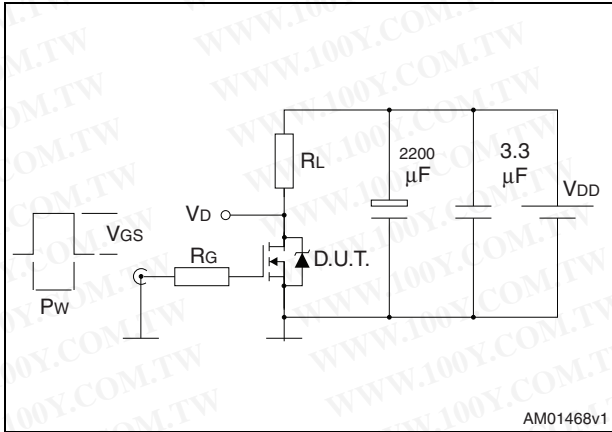
Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		6	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		24	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 6 \text{ A}, V_{GS} = 0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 6 \text{ A},$ $di/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD} = 16 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$	-	TBD		ns
Q_{rr}	Reverse recovery charge			TBD		nC
I_{RRM}	Reverse recovery current			TBD		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

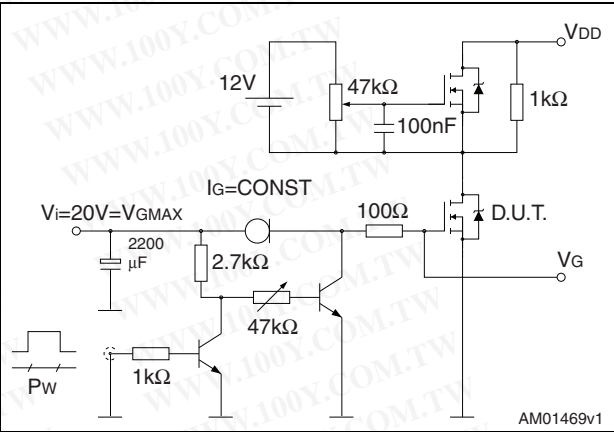
3 Test circuits

Figure 2. Switching times test circuit for resistive load



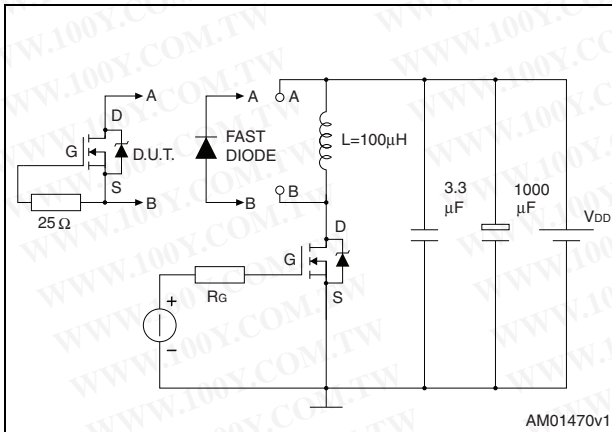
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Figure 3. Gate charge test circuit



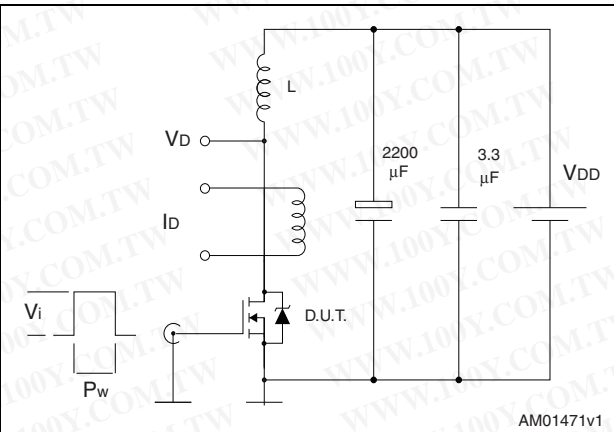
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Figure 4. Test circuit for inductive load switching and diode recovery times



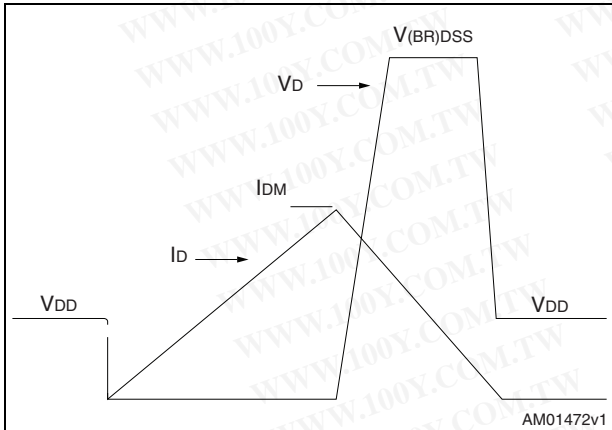
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Figure 5. Unclamped inductive load test circuit



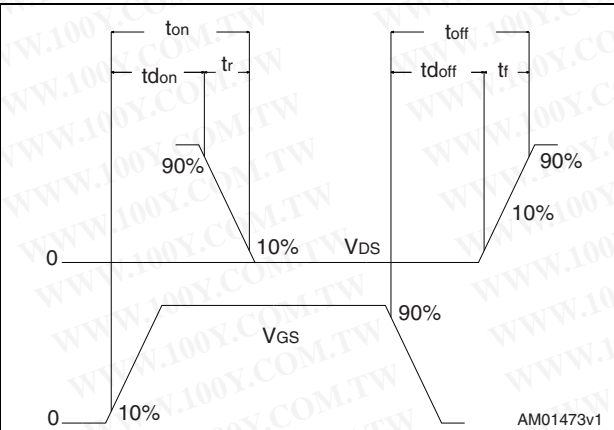
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Figure 6. Unclamped inductive waveform



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Figure 7. Switching time waveform



AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 8. PowerFLAT™ 2x2 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.90	1.00	1.10
E2	0.80	0.90	1.00
e	0.55	0.65	0.75
K	0.15	0.25	0.35
K1	0.20	0.30	0.40
K2	0.25	0.35	0.45
L	0.20	0.25	0.30
L1	0.65	0.75	0.85

Figure 8. PowerFLAT™ 2 x 2 drawing

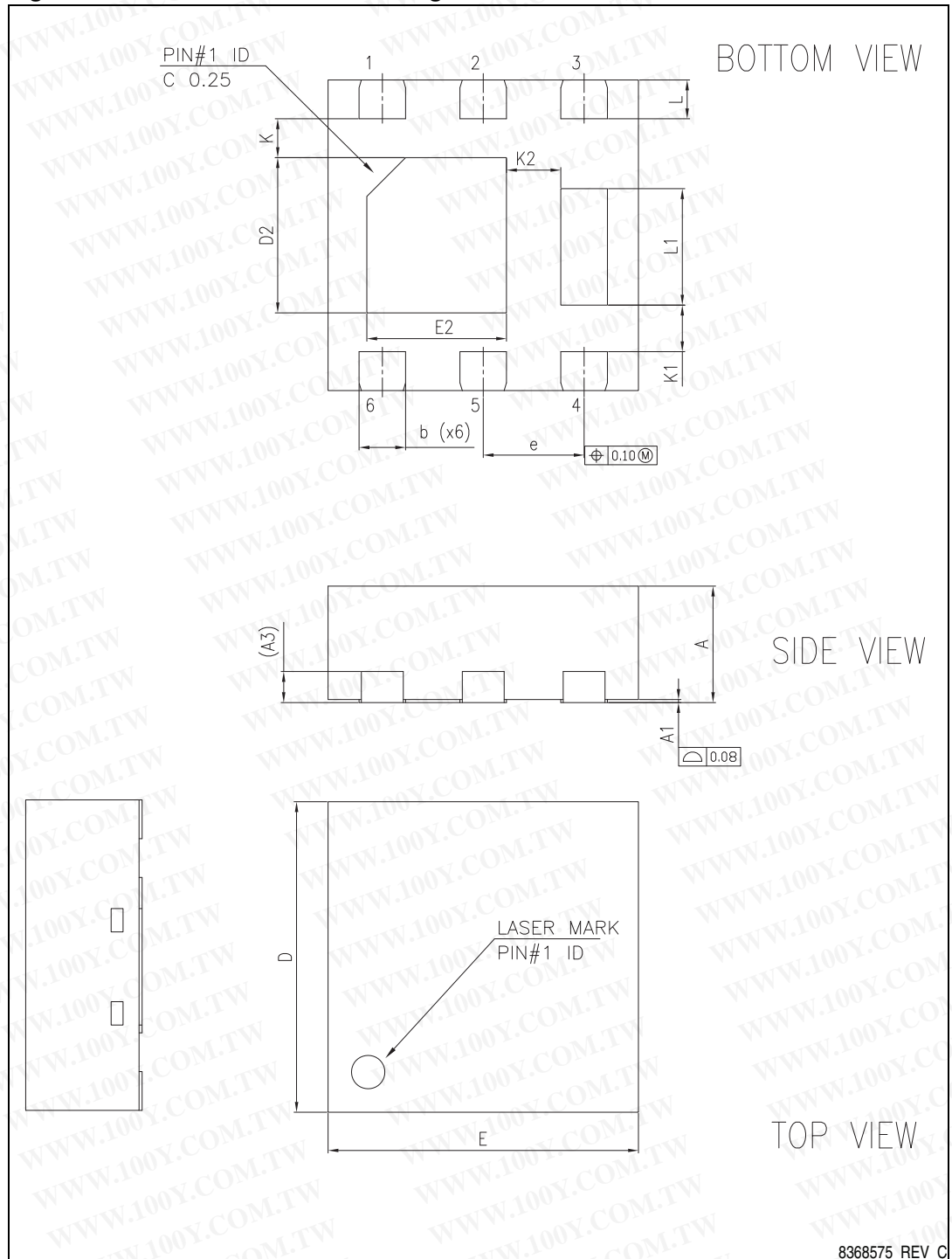
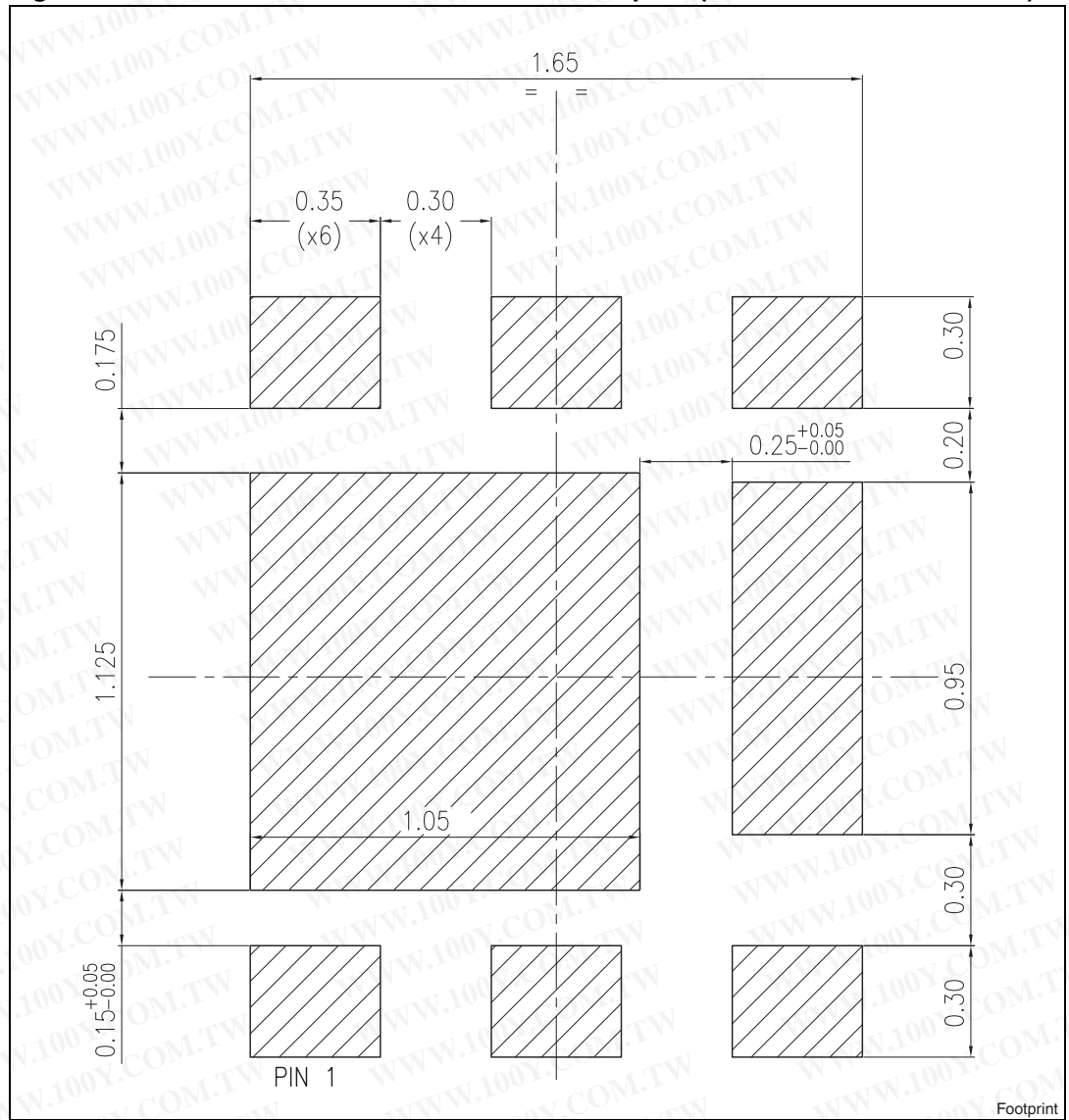


Figure 9. PowerFLAT™ 2 x 2 recommended footprint (dimensions in millimeters)



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
24-Apr-2012	1	First release.
10-Jan-2013	2	– Modified: $R_{DS(on)}$ values – Document status promoted from target data to preliminary data

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