



STB2N62K3, STD2N62K3, STF2N62K3, STP2N62K3, STU2N62K3

N-channel 620 V, 3 Ω, 2.2 A SuperMESH3™ Power MOSFET
 in D²PAK, DPAK, TO-220FP, TO-220 and IPAK packages

Datasheet — production data

Features

Order codes	V _{DSS}	R _{DS(on) max}	I _D	P _{TOT}
STB2N62K3 STD2N62K3	620 V	< 3.6 Ω	2.2 A	45 W
STF2N62K3				20 W
STP2N62K3 STU2N62K3				45 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

These SuperMESH3™ Power MOSFETs are the result of improvements applied to STMicroelectronics' SuperMESH™ technology, combined with a new optimized vertical structure. These devices boast an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering them suitable for the most demanding applications.

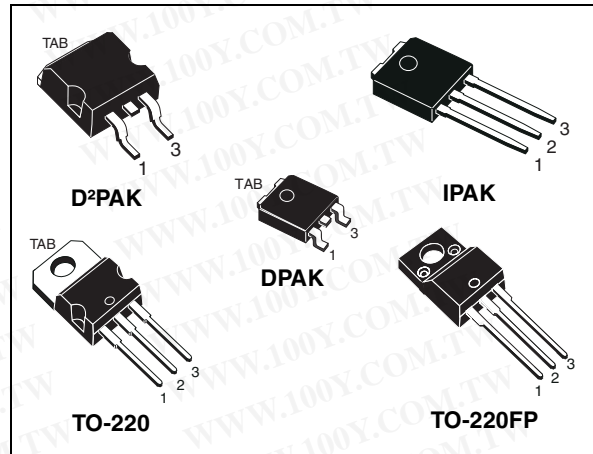


Figure 1. Internal schematic diagram

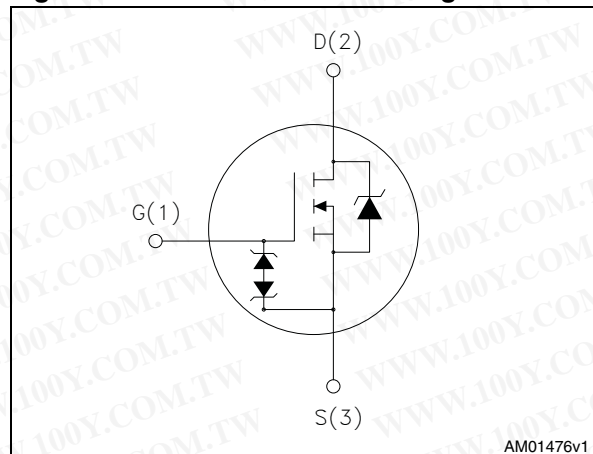


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB2N62K3 STD2N62K3	2N62K3	D ² PAK DPAK	Tape and reel
STF2N62K3 STP2N62K3 STU2N62K3	2N62K3	TO-220FP TO-220 IPAK	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D ² PAK, DPAK, TO-220, IPAK	TO-220FP	
V _{DS}	Drain-source voltage	620		V
V _{GS}	Gate- source voltage	± 30		V
I _D	Drain current (continuous) at T _C = 25 °C	2.2	2.2 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100 °C	1	1 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	8.8	8.8 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25 °C	45	20	W
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _j max)	2.2		A
E _{AS}	Single pulse avalanche energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	85		mJ
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T _C =25 °C)		2500	V
dv/dt ⁽³⁾	Peak diode recovery voltage slope	12		V/ns
T _{stg}	Storage temperature	-55 to 150		°C
T _j	Max. operating junction temperature	150		°C

1. Limited by maximum junction temperature

2. Pulse width limited by safe operating area

3. I_{SD} ≤ 2.2 A, di/dt ≤ 400 A/μs, V_{DS} peak ≤ V_{(BR)DSS}, V_{DD} = 80% V_{(BR)DSS}

Table 3. Thermal data

Symbol	Parameter	Value					Unit
		D ² PAK	DPAK	IPAK	TO-220	TO-220FP	
R _{thj-case}	Thermal resistance junction-case max	2.78			6.25	°C/W	
R _{thj-pcb}	Thermal resistance junction-pcb max	30	50			°C/W	
R _{thj-amb}	Thermal resistance junction-ambient max			100	62.5	°C/W	

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	620			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 620\text{ V}$ $V_{DS} = 620\text{ V}$, $T_C = 125\text{ °C}$			1 50	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 1.1\text{ A}$		3	3.6	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	340	-	pF
C_{oss}	Output capacitance			26		
C_{rss}	Reverse transfer capacitance			4		
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related			17		
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	5	-	Ω
Q_g	Total gate charge	$V_{DD} = 496\text{ V}$, $I_D = 1.1\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 20)	-	15	-	nC
Q_{gs}	Gate-source charge			3		nC
Q_{gd}	Gate-drain charge			9		nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 310\text{ V}$, $I_D = 1.1\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 19)	-	8	-	ns
t_r	Rise time		-	4.4	-	ns
$t_{d(off)}$	Turn-off-delay time		-	21	-	ns
t_f	Fall time		-	22	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2.2	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		8.8	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 2.2\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 2.2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 24)	-	200		ns
Q_{rr}	Reverse recovery charge		-	900		nC
I_{RRM}	Reverse recovery current		-	9		A
t_{rr}	Reverse recovery time	$I_{SD} = 2.2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 24)	-	240		ns
Q_{rr}	Reverse recovery charge		-	1150		nC
I_{RRM}	Reverse recovery current		-	10		A

1. Pulse width limited by safe operating area

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	$I_{gs} = \pm 1\text{ mA}$ (open drain)	30			V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK and IPAК

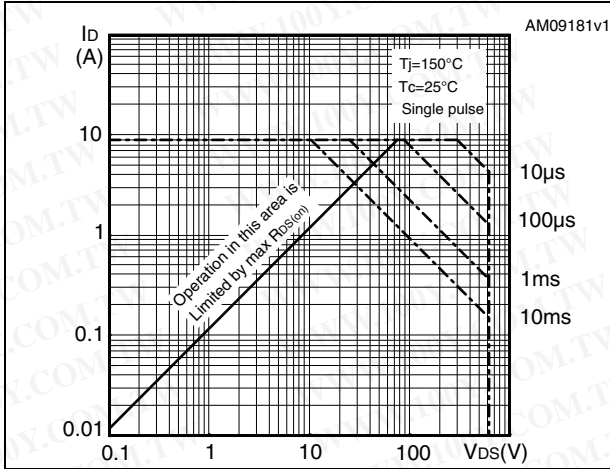


Figure 3. Thermal impedance for DPAK and IPAК

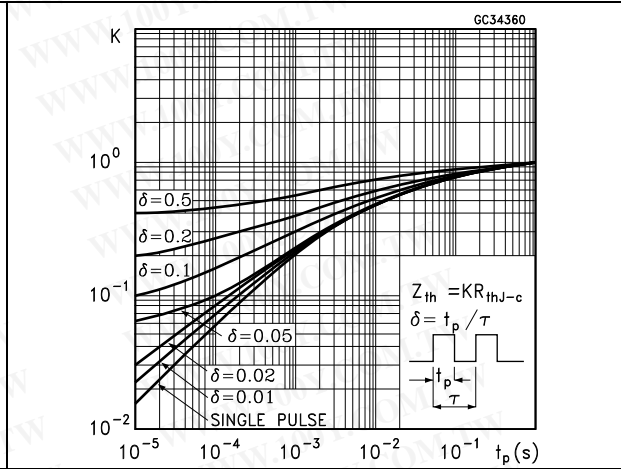


Figure 4. Safe operating area for TO-220FP

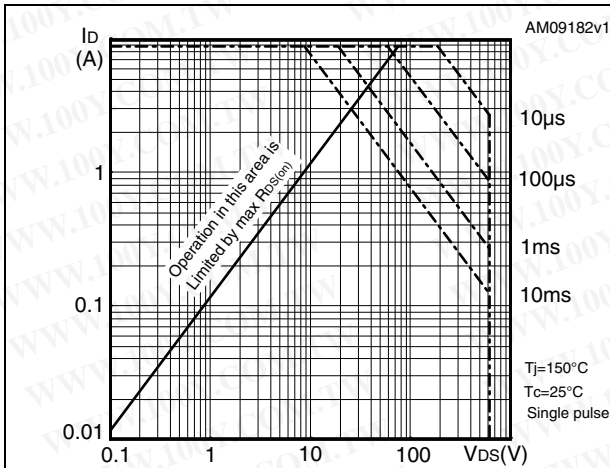


Figure 5. Thermal impedance for TO-220FP

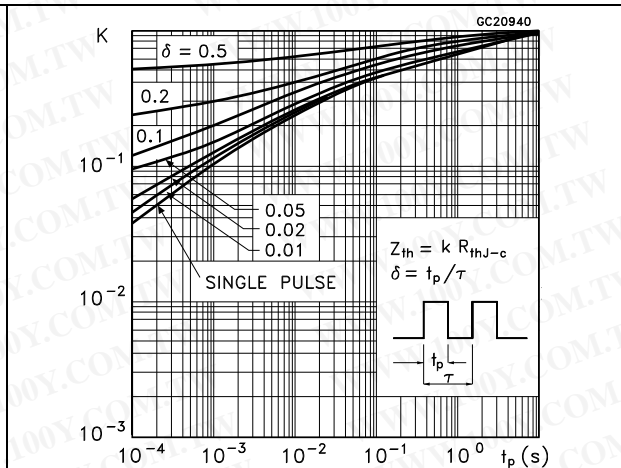


Figure 6. Safe operating area for TO-220 and D²PAK

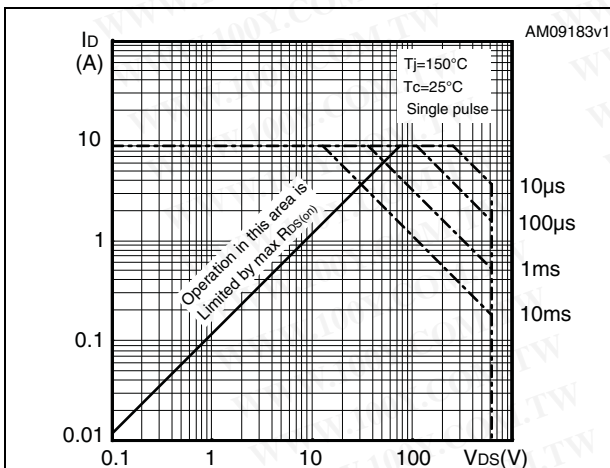


Figure 7. Thermal impedance for TO-220 and D²PAK

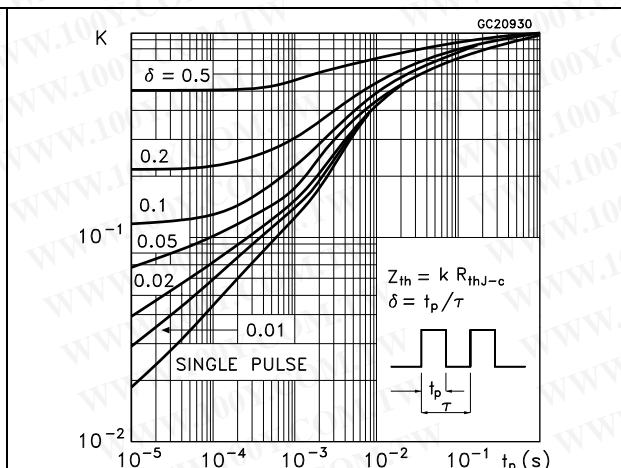


Figure 8. Output characteristics

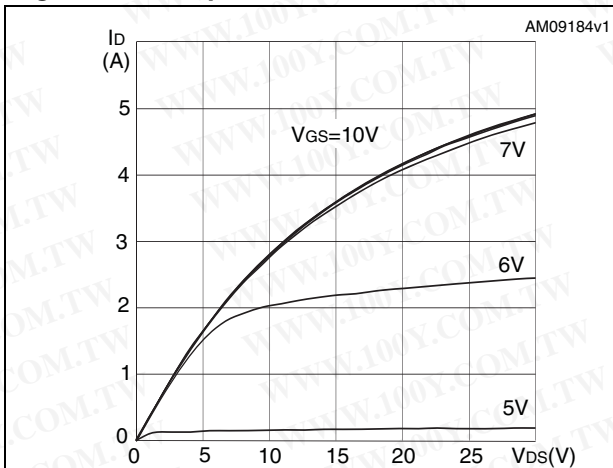


Figure 9. Transfer characteristics

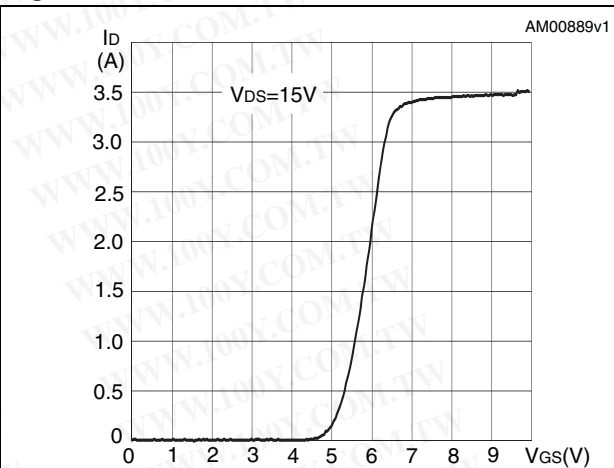


Figure 10. Gate charge vs gate-source voltage

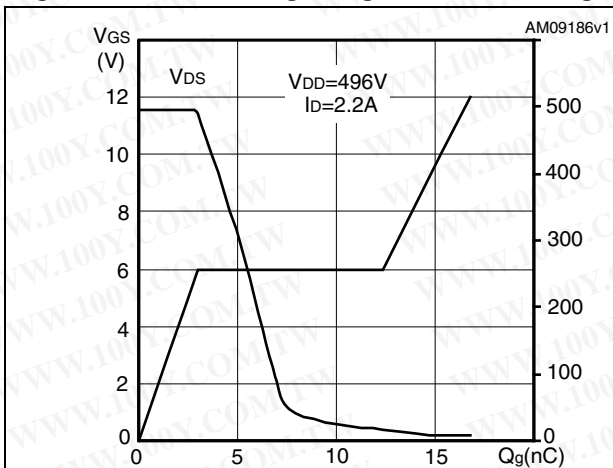


Figure 11. Static drain-source on-resistance

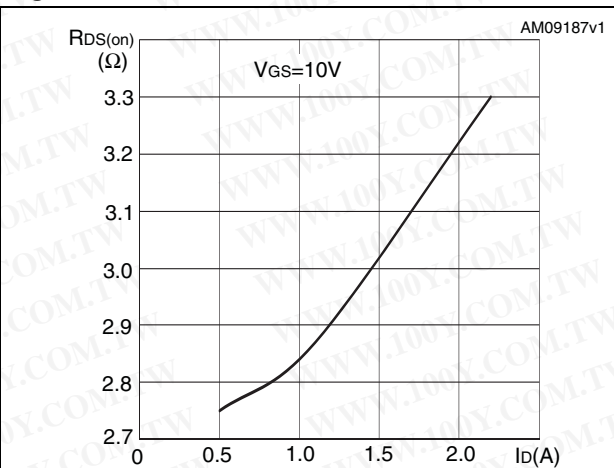


Figure 12. Capacitance variations

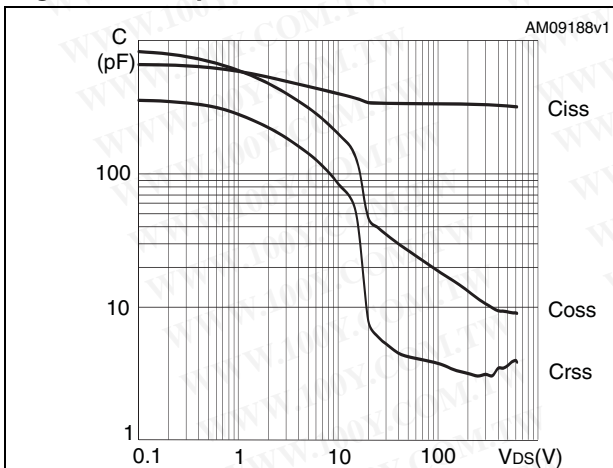


Figure 13. Output capacitance stored energy

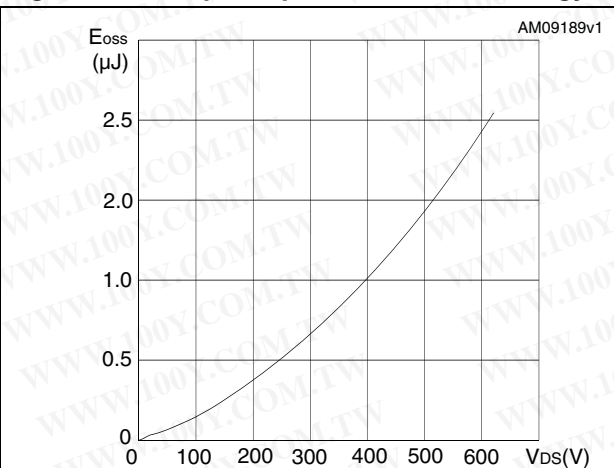


Figure 14. Normalized gate threshold voltage vs temperature

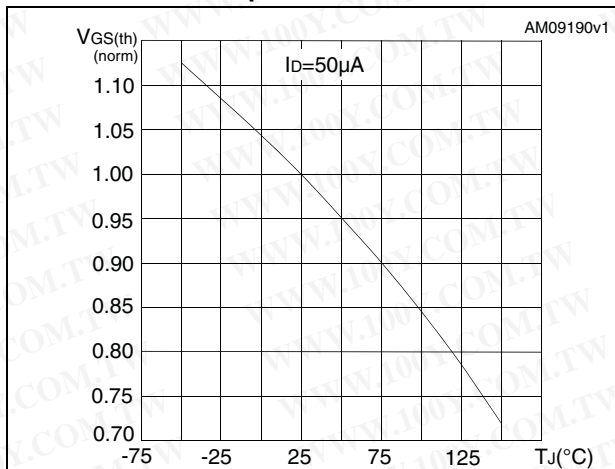


Figure 15. Normalized on-resistance vs temperature

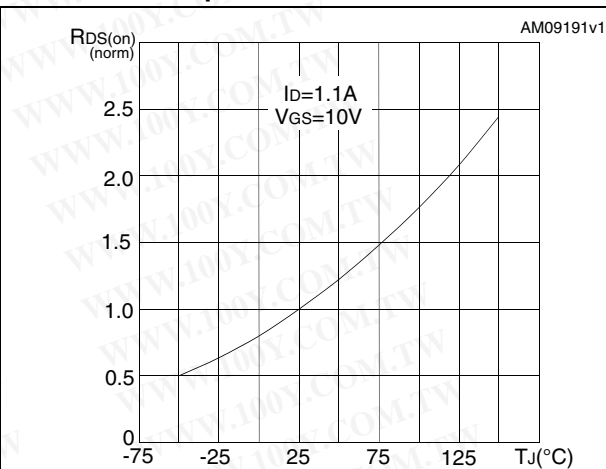


Figure 16. Source-drain diode forward characteristics

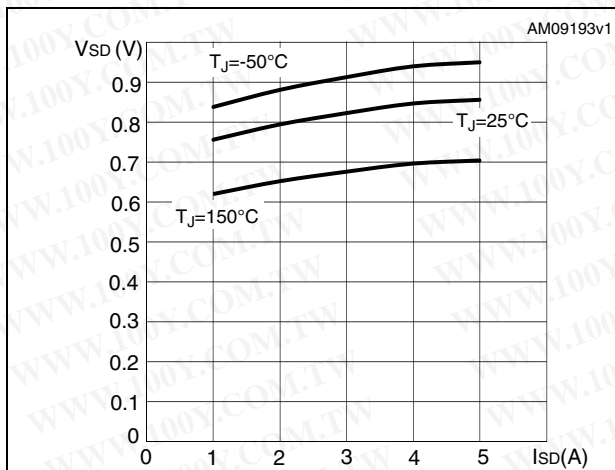


Figure 17. Normalized BV_{DSS} vs temperature

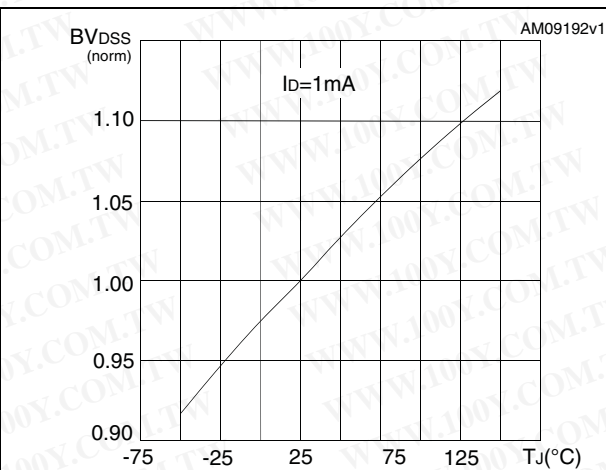
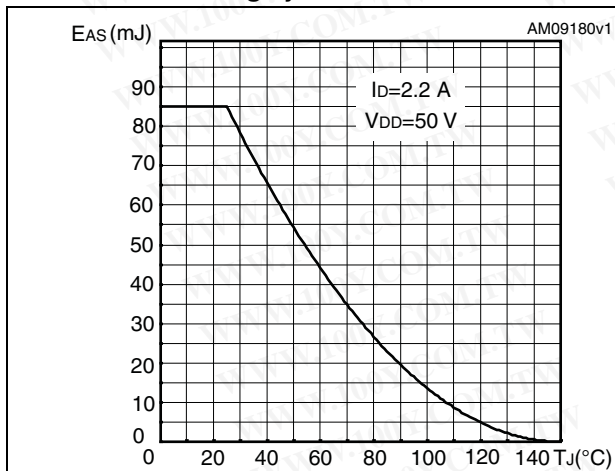


Figure 18. Maximum avalanche energy vs starting Tj



3 Test circuits

Figure 19. Switching times test circuit for resistive load

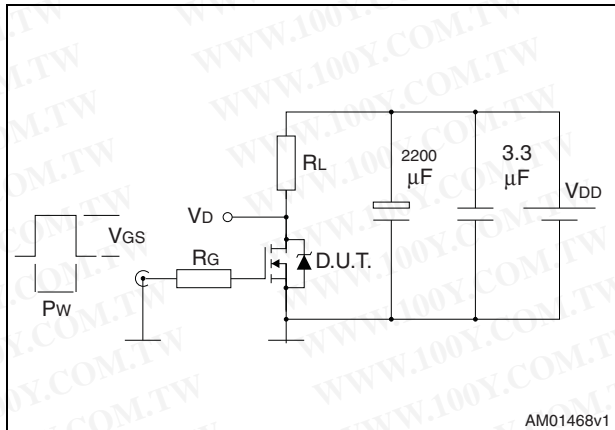


Figure 20. Gate charge test circuit

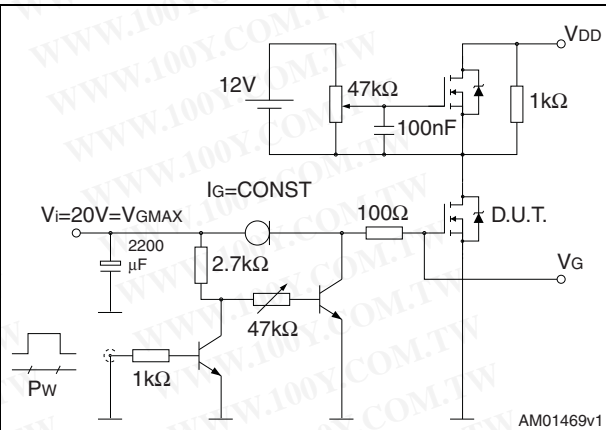


Figure 21. Test circuit for inductive load switching and diode recovery times

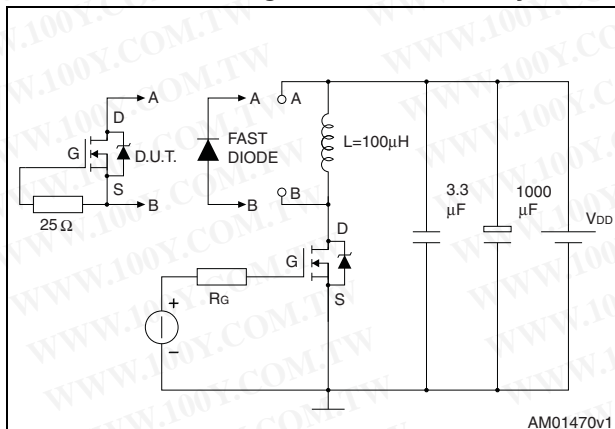


Figure 22. Unclamped inductive load test circuit

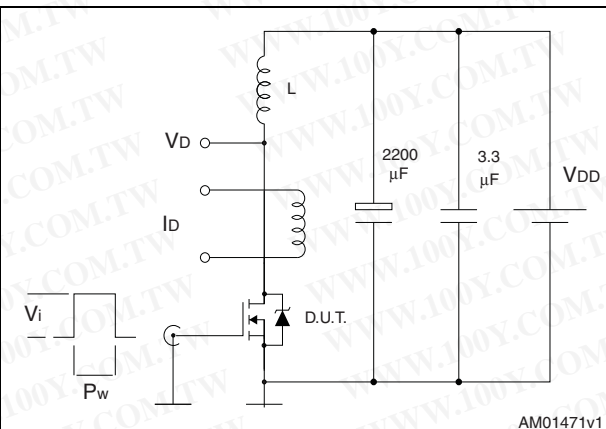


Figure 23. Unclamped inductive waveform

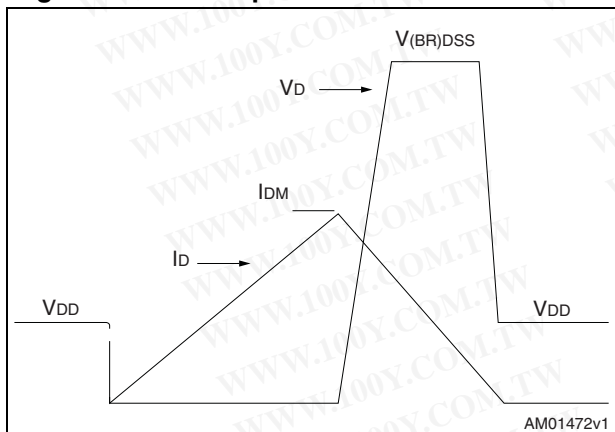
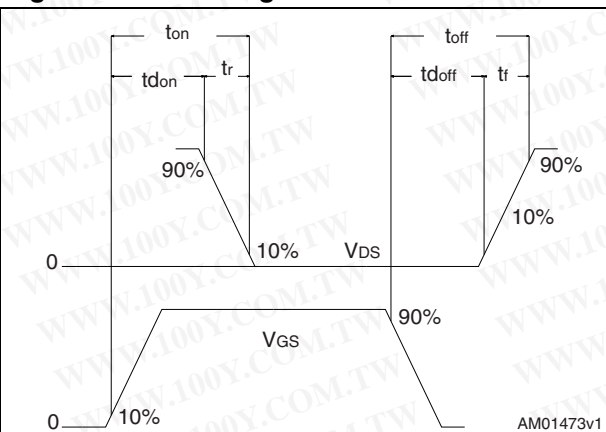


Figure 24. Switching time waveform



4 Package mechanical data

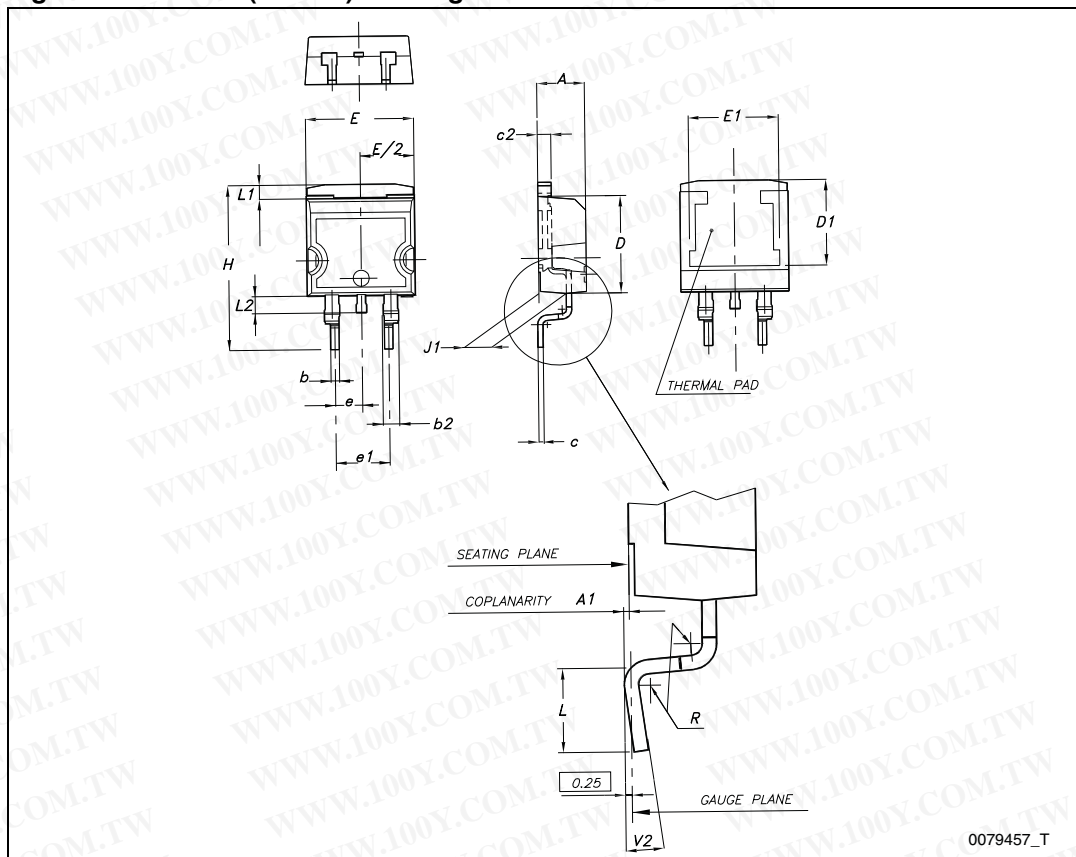
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.



Table 9. D²PAK (TO-263) mechanical data

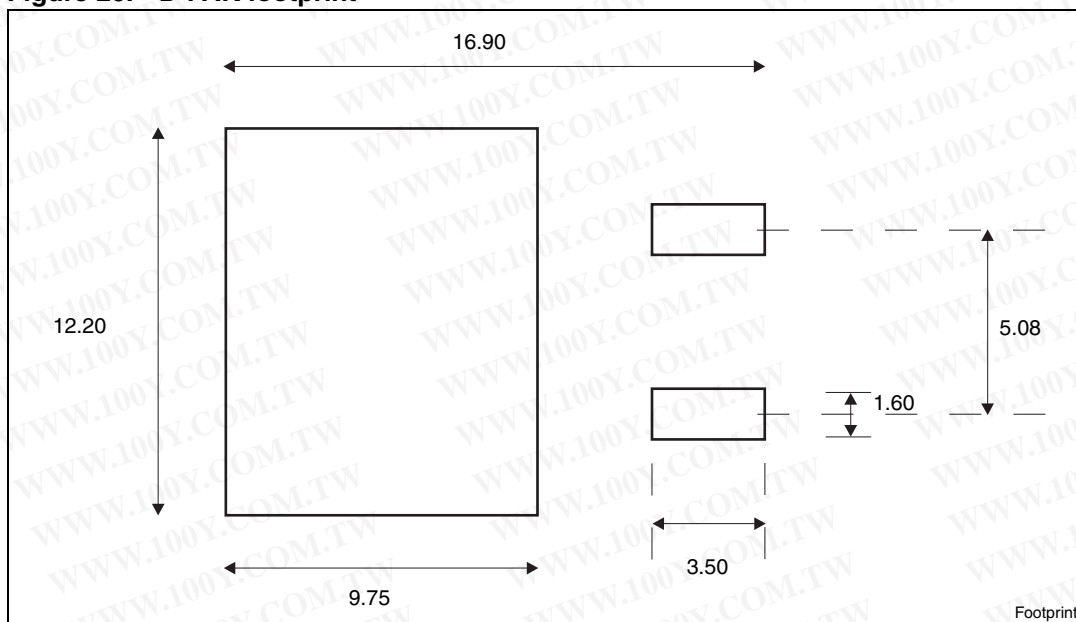
Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 25. D²PAK (TO-263) drawing



0079457_T

Figure 26. D²PAK footprint^(a)



a. All dimensions are in millimeters

Table 10. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		1.50
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 27. DPAK (TO-252) drawing

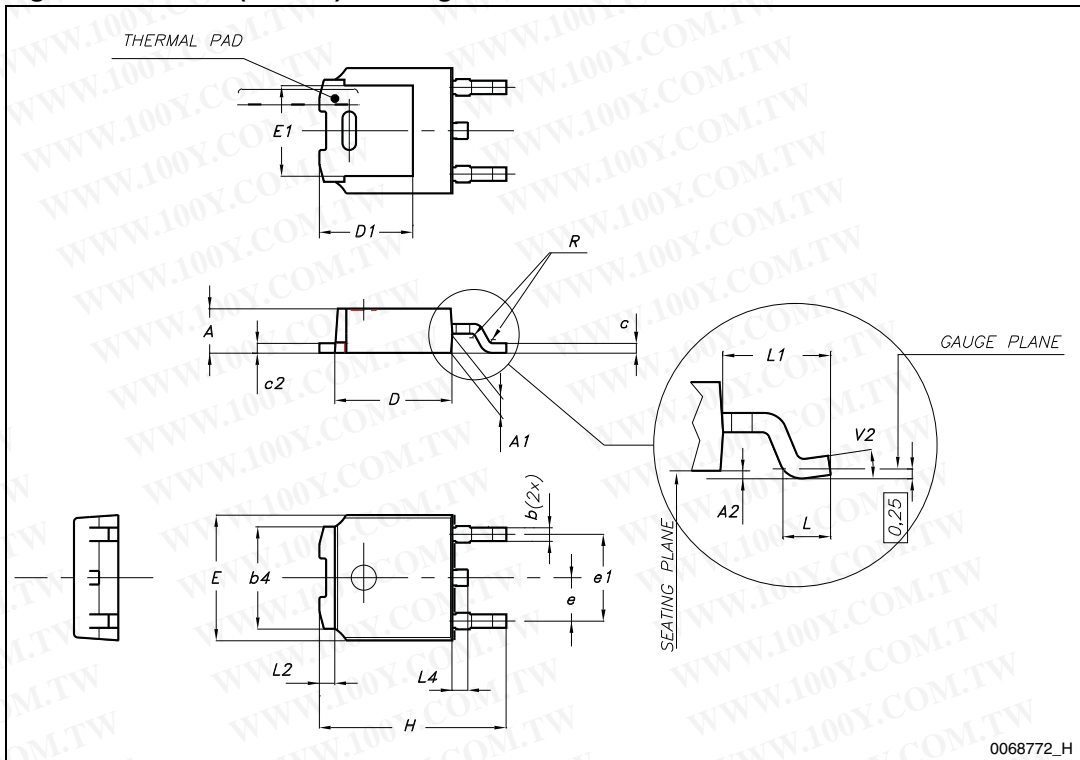
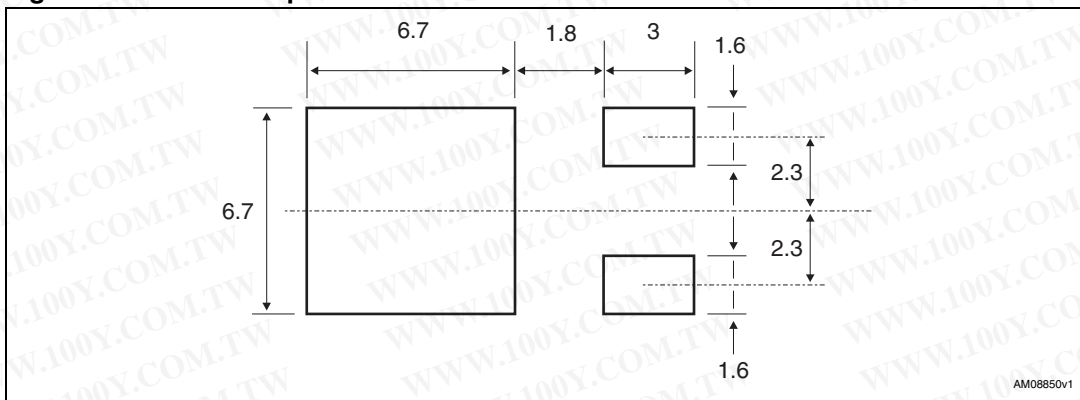


Figure 28. DPAK footprint^(b)



b. All dimensions are in millimeters

Table 11. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 29. TO-220FP drawing

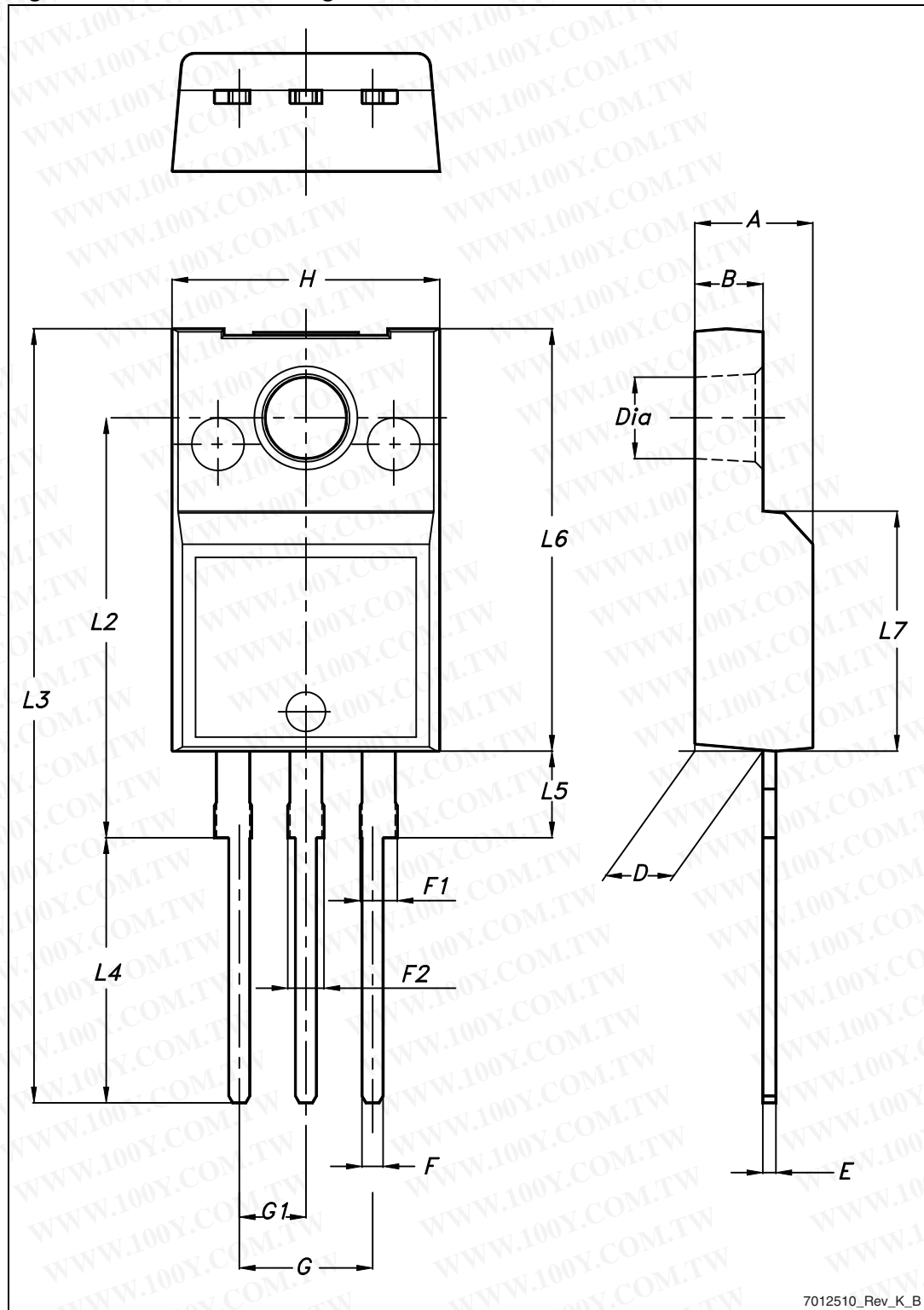


Table 12. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Figure 30. TO-220 type A drawing

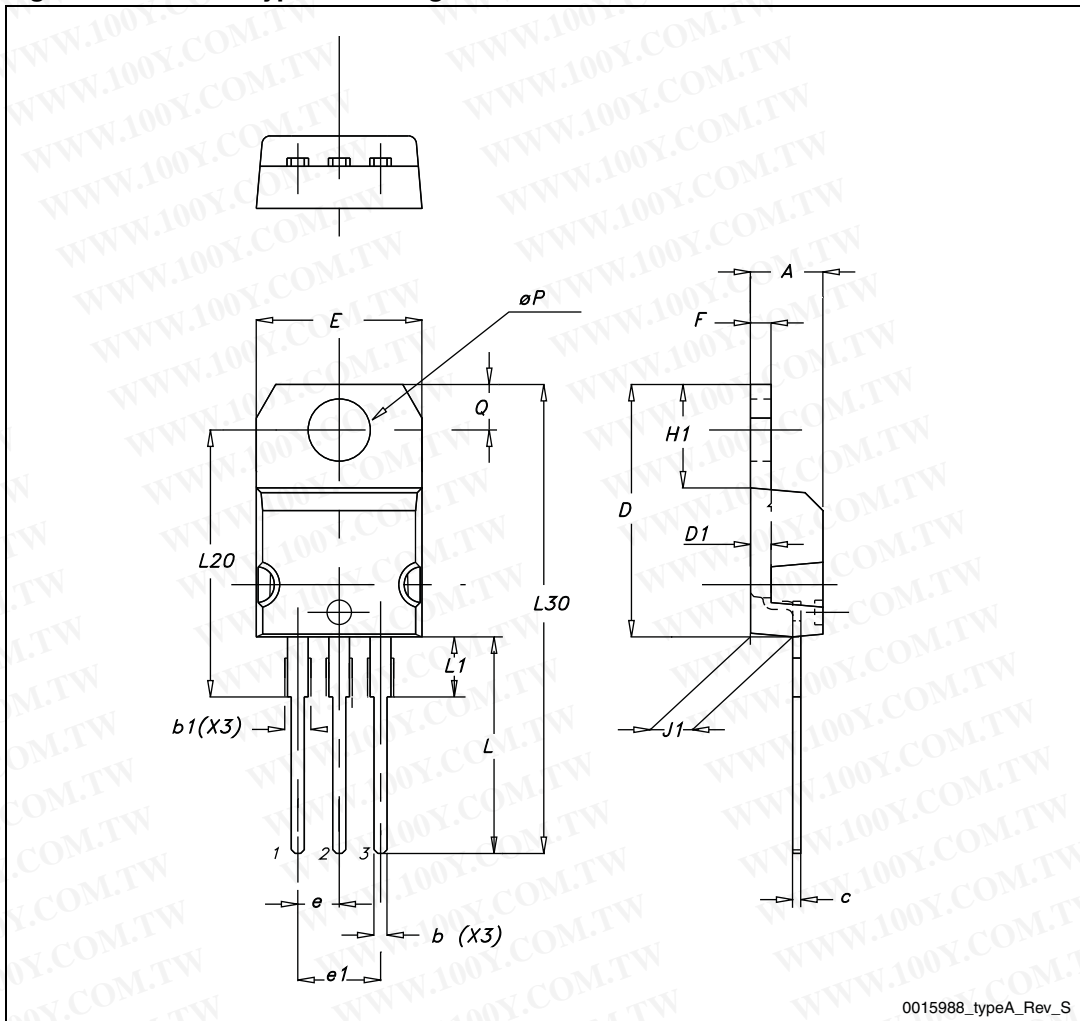
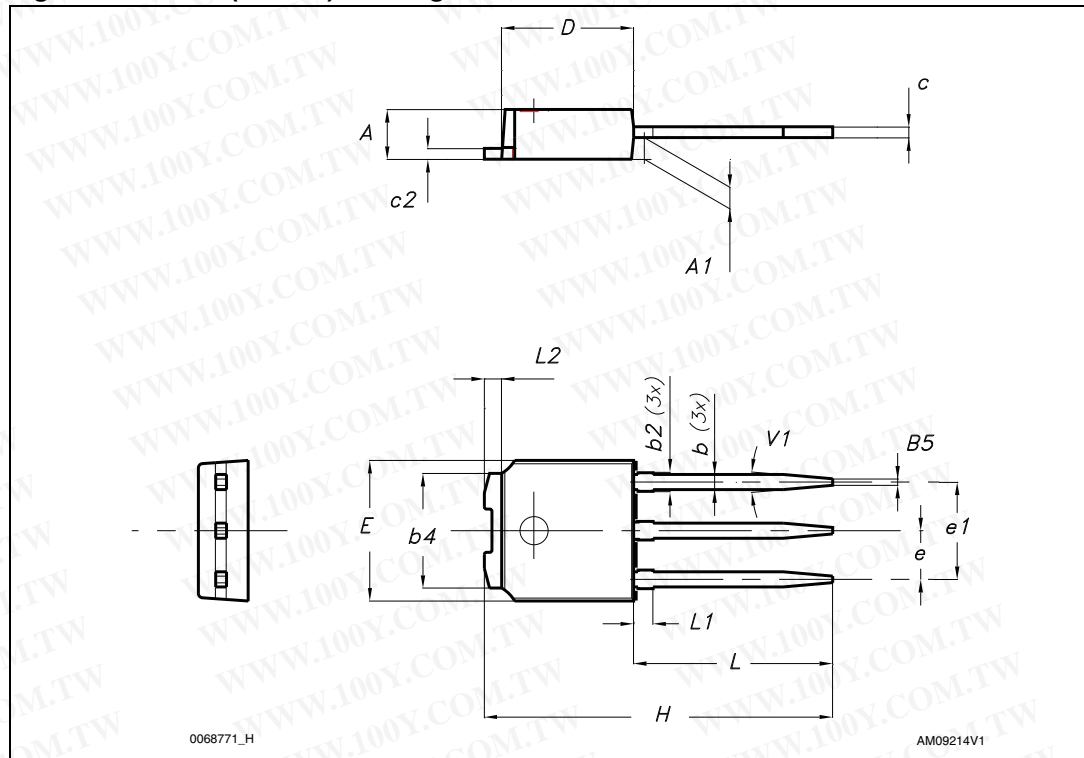


Table 13. IPAK (TO-251) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.3	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10 °	

Figure 31. IPAK (TO-251) drawing



5 Packaging mechanical data

Table 14. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1		Base qty.	2500
P1	7.9	8.1		Bulk qty.	2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Table 15. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1		Base qty	1000
P2	1.9	2.1		Bulk qty	1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 32. Tape for DPAK (TO-252) and D²PAK (TO-263)

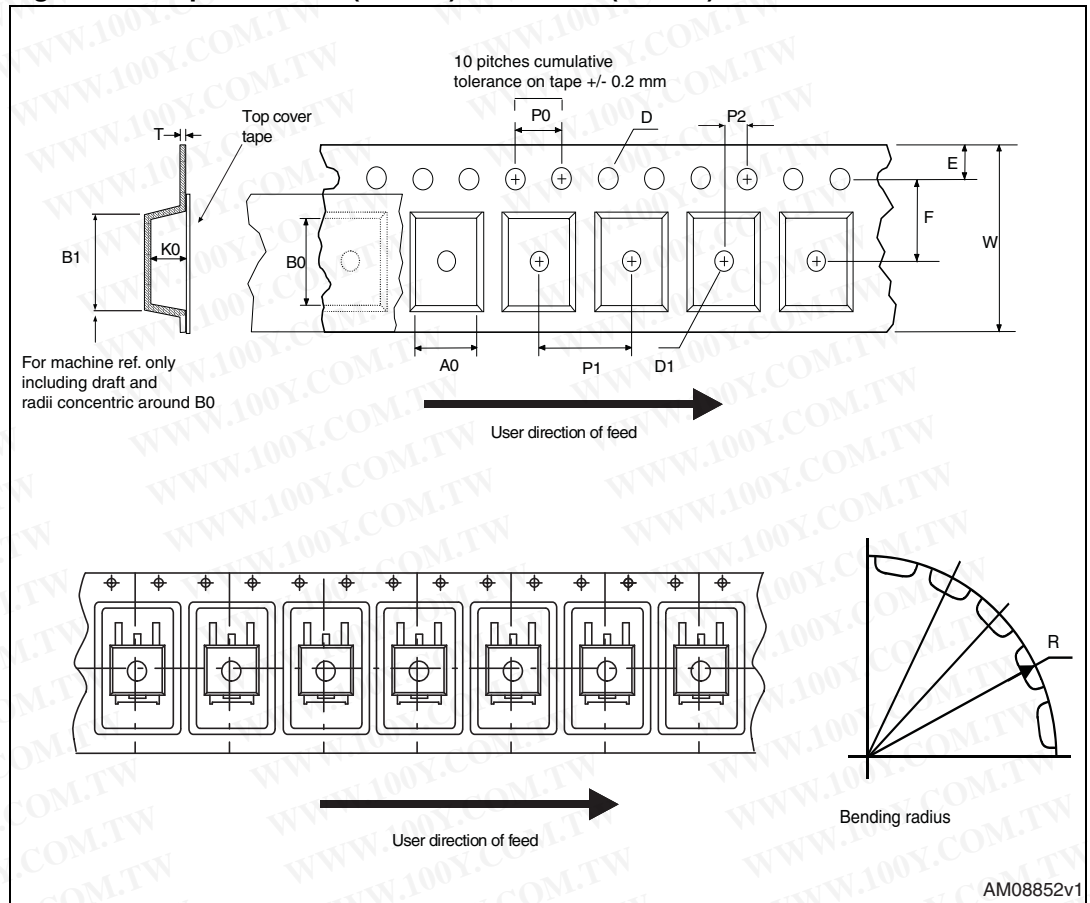
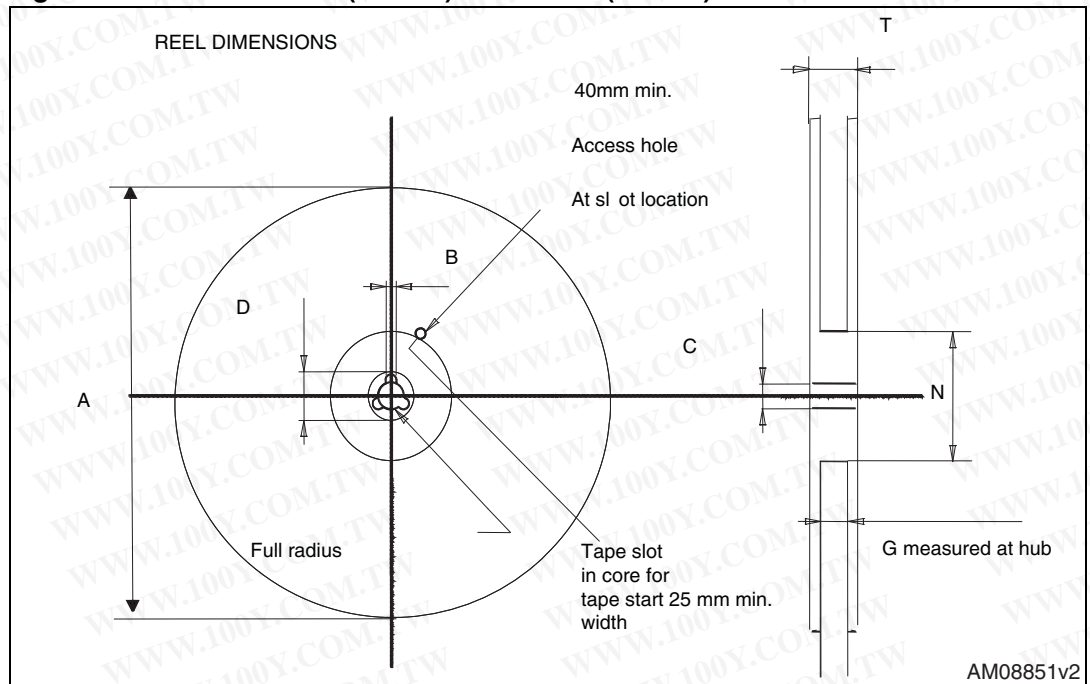


Figure 33. Reel for DPAK (TO-252) and D²PAK (TO-263)



6 Revision history

Table 16. Document revision history

Date	Revision	Changes
31-May-2011	1	First release
20-Mar-2012	2	Added new package: D ² PAK – Table 1: Device summary , Section 4: Package mechanical data and Section 5: Packaging mechanical data have been modified. Minor text changes.

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