CSD16401Q5 25-V N-Channel NexFET™ Power MOSFET

1 Features

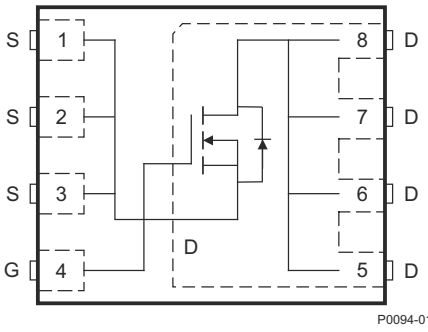
- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- SON 5-mm × 6-mm Plastic Package

2 Applications

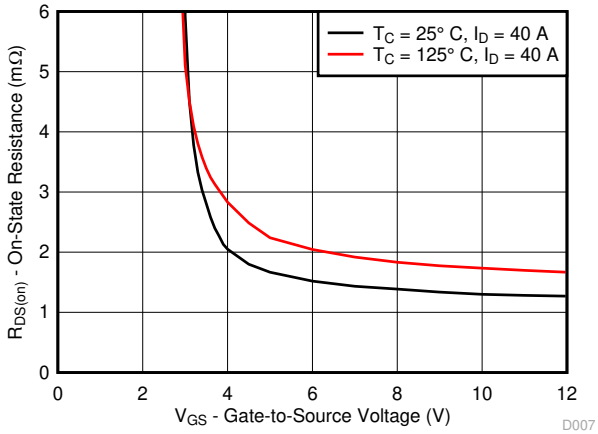
- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems
- Optimized for Synchronous FET Applications

3 Description

This 25-V, 1.3-mΩ, 5-mm × 6-mm SON NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.



Top View



$R_{DS(ON)}$ vs V_{GS}

Product Summary

T_A = 25°C		VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	25		V
Q_g	Gate Charge, Total (4.5 V)	21		nC
Q_{gd}	Gate Charge, Gate-to-Drain	5.2		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V	1.8	mΩ
		V_{GS} = 10 V	1.3	
$V_{GS(th)}$	Threshold Voltage	1.5		V

Device Information(1)

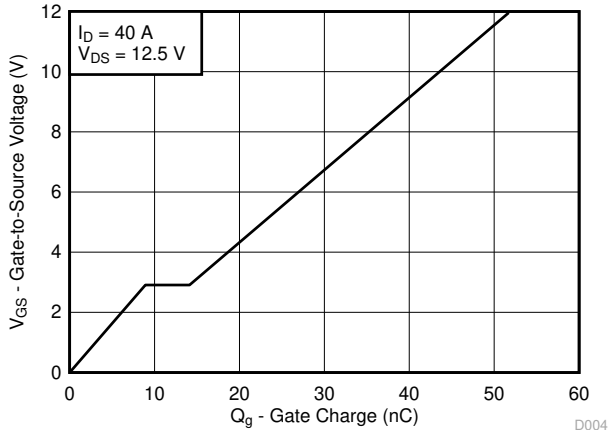
DEVICE	MEDIA	QTY	PACKAGE	SHIP
CSD16401Q5	13-Inch Reel	2500	SON 5.00-mm × 6.00-mm Plastic Package	Tape and Reel

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	25	V
V_{GS}	Gate-to-Source Voltage	–12 to 16	V
I_D	Continuous Drain Current (Package Limited)	100	A
	Continuous Drain Current (Silicon Limited), T_C = 25°C	261	
	Continuous Drain Current(1)	38	
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	240	A
P_D	Power Dissipation(1)	3.1	W
	Power Dissipation, T_C = 25°C	156	
T_J, T_{stg}	Operating Junction, Storage Temperature	–55 to 150	°C
E_{AS}	Avalanche Energy, Single Pulse I_D = 100 A, L = 0.1 mH, R_G = 25 Ω	500	mJ

(1) $R_{\theta JA}$ = 40°C/W on 1-in² (6.45-cm²) Cu 2-oz (0.071-mm) thick on 0.06-in (1.52-mm) thick FR4 PCB.
(2) Max $R_{\theta JC}$ = 0.8°C/W, pulse duration ≤ 100 µs, duty cycle ≤ 1%.



Gate Charge

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (January 2018) to Revision D (October 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision B (August 2015) to Revision C (January 2018)	Page
• Added V_{DS} = 5 V to Figure 5-3	4

Changes from Revision A (September 2010) to Revision B (August 2015)	Page
• Added part number to title	1
• Enhanced *Description*	1
• Added *Device and Documentation Support* section and *Mechanical, Packaging, and Orderable Information* section	1
• Updated pulsed current	1
• Updated Figure 5-1 to a normalized $R_{\theta JC}$ curve	4
• Updated the SOA in Figure 5-10	4

Changes from Revision * (August 2009) to Revision A (September 2010)	Page
• Deleted environmental bullets from Features list	1

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

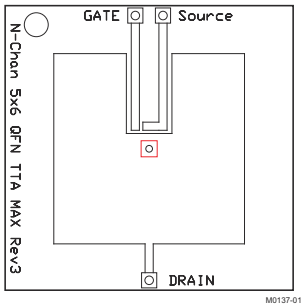
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 µA	25			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 20 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = –12 V to 16 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.2	1.5	1.9	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 4.5 V, I_D = 40 A		1.8	2.3	mΩ
		V_{GS} = 10 V, I_D = 40 A		1.3	1.6	
g_{fs}	Transconductance	V_{DS} = 15 V, I_D = 40 A		168		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = 12.5 V, f = 1 MHz		3150	4100	pF
C_{OSS}	Output capacitance			2530	3300	pF
C_{RSS}	Reverse transfer capacitance			175	230	pF
R_g	Series gate resistance			1.2	2.4	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 12.5 V, ID = 40 A		21	29	nC
Q_{gd}	Gate charge, gate-to-drain			5.2		nC
Q_{gs}	Gate charge, gate-to-source			8.3		nC
Qg(th)	Gate charge at Vth			4.8		nC
Q_{OSS}	Output charge	V_{DS} = 15 V, V_{GS} = 0 V		55		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 12.5 V, V_{GS} = 4.5 V, I_D = 40 A R_G = 2 Ω		16.6		ns
t_r	Rise time			30		ns
$t_{d(off)}$	Turnoff delay time			20		ns
t_f	Fall time			12.7		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_S = 40 A, V_{GS} = 0 V		0.85	1	V
Q_{rr}	Reverse recovery charge	V_{DD} = 15 V, I_F = 40 A, di/dt = 300 A/µs		72		nC
t_{rr}	Reverse recovery time	V_{DD} = 15 V, I_F = 40 A, di/dt = 300 A/µs		45		ns

5.2 Thermal Information

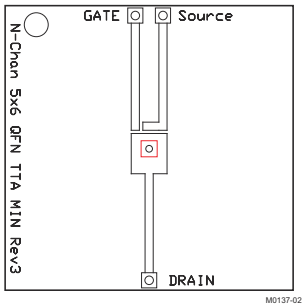
T_A = 25°C (unless otherwise noted)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case(1)			0.8	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient(1) (2)			50	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in (2.54-cm) square, 2-oz(0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 board. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1 in^2 (6.45 cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 in^2 (6.45 cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on minimum pad area of 2-oz (0.071-mm) thick Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise noted)

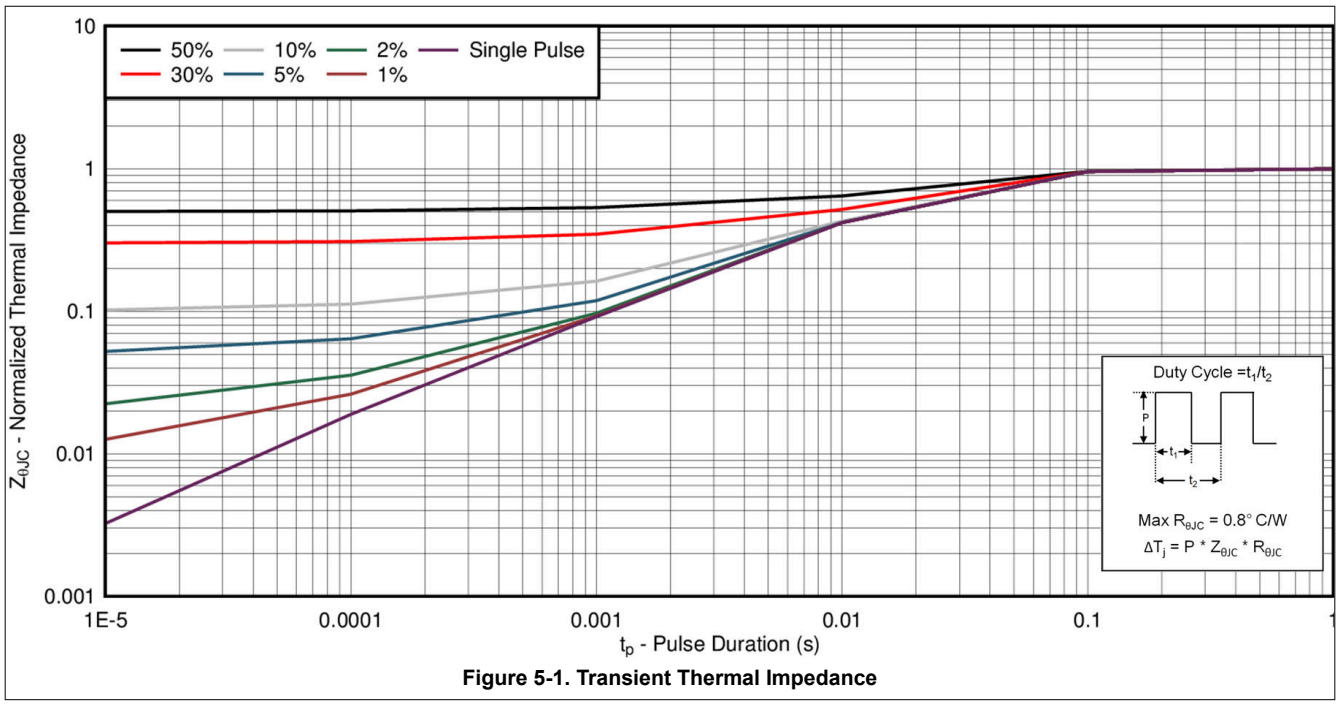


Figure 5-1. Transient Thermal Impedance

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise noted)

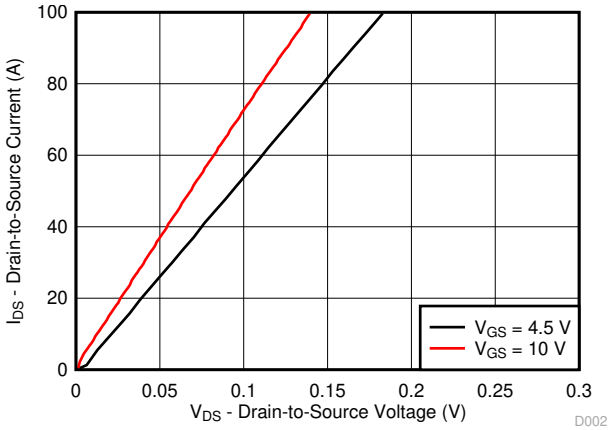
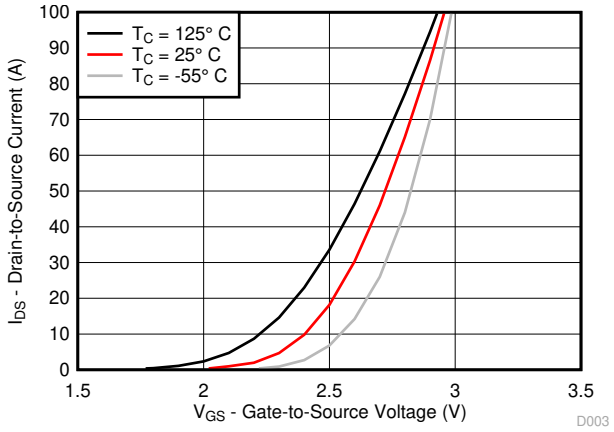
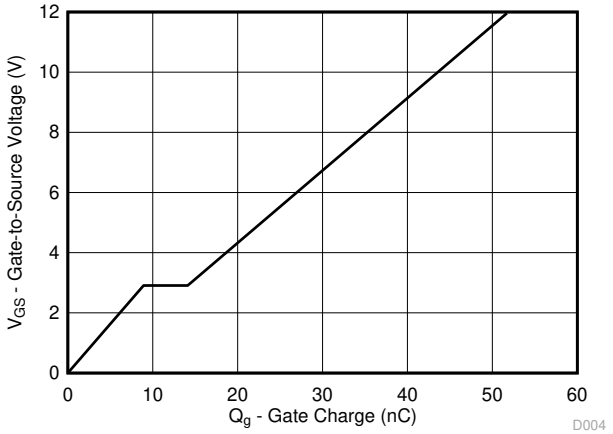


Figure 5-2. Saturation Characteristics



V_{DS} = 5 V

Figure 5-3. Transfer Characteristics



I_D = 40 A V_{DS} = 12.5 V

Figure 5-4. Gate Charge

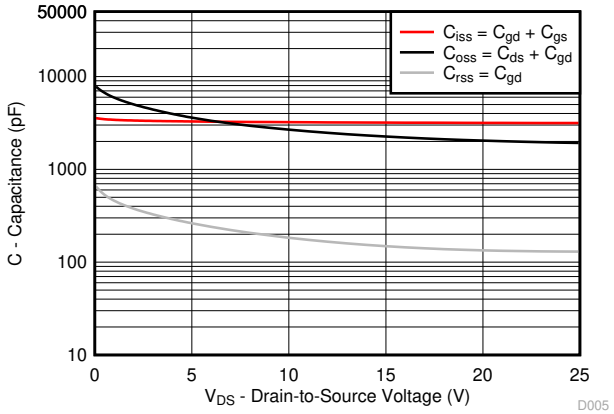
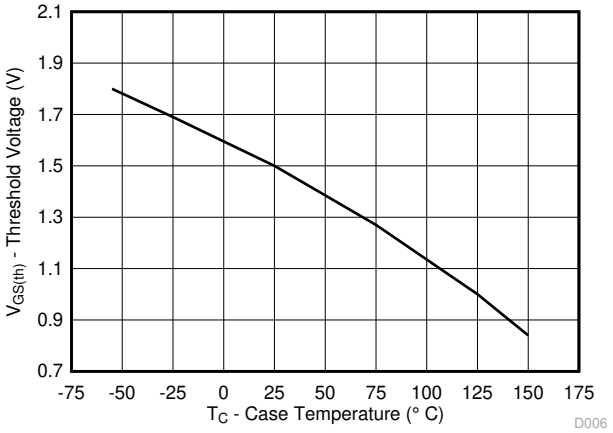


Figure 5-5. Capacitance



I_D = 250 µA

Figure 5-6. Threshold Voltage vs Temperature

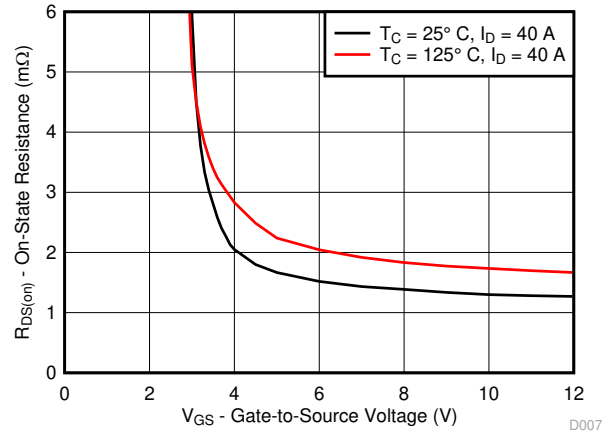
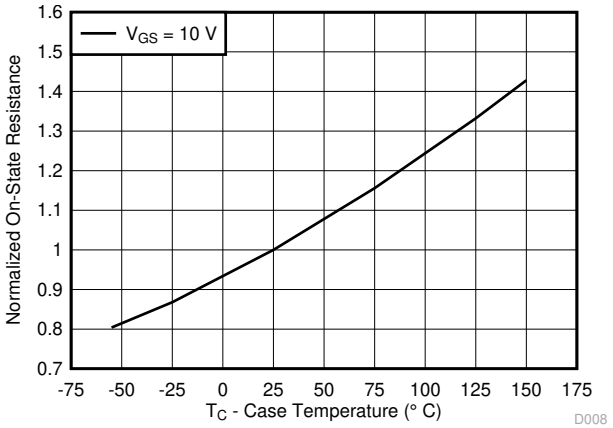


Figure 5-7. On-Resistance vs Gate Voltage

5.3 Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise noted)



I_D = 40 A

Figure 5-8. On-Resistance vs Temperature

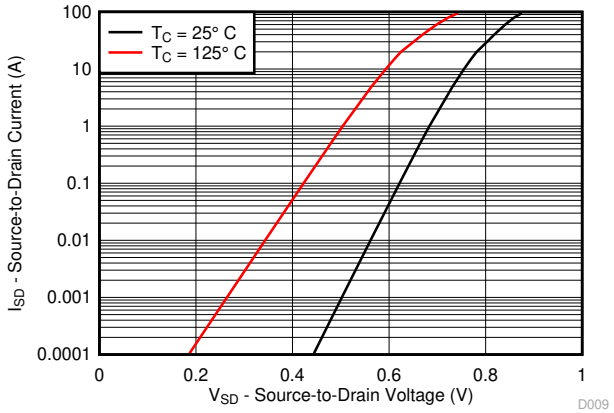
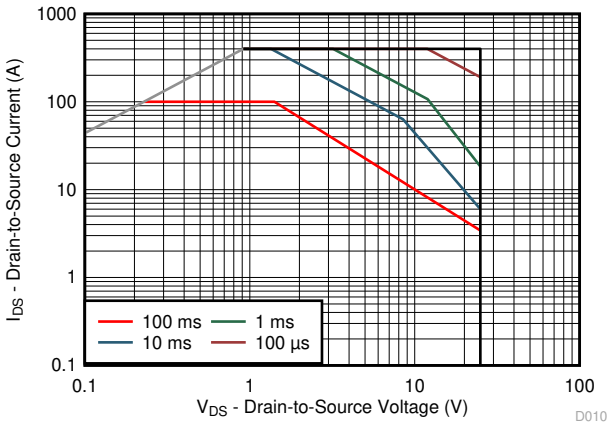


Figure 5-9. Typical Diode Forward Voltage



Single pulse, max $R_{\theta JC}$ = 0.8°C/W

Figure 5-10. Maximum Safe Operating Area

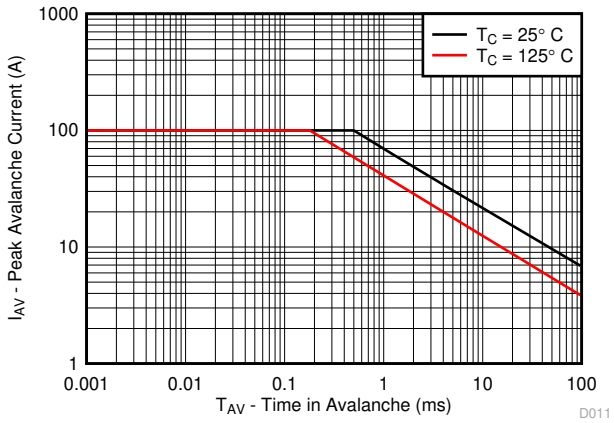


Figure 5-11. Single-Pulse Unclamped Inductive Switching

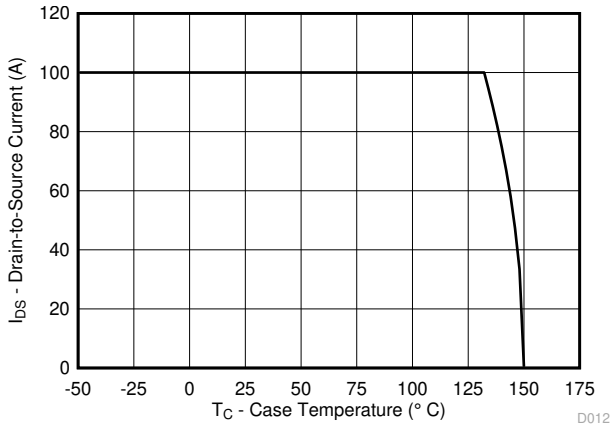


Figure 5-12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

6.3 Trademarks

NexFET™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16401Q5	ACTIVE	VSON-CLIP	DQH	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16401	Samples
CSD16401Q5T	ACTIVE	VSON-CLIP	DQH	8	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16401	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

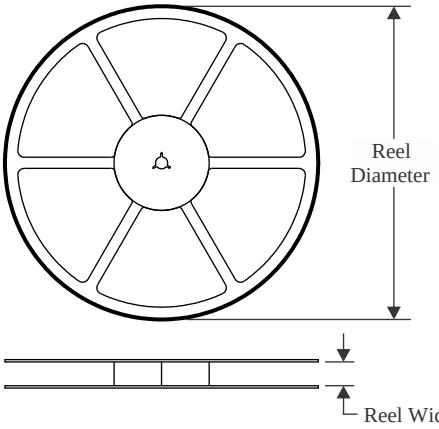
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

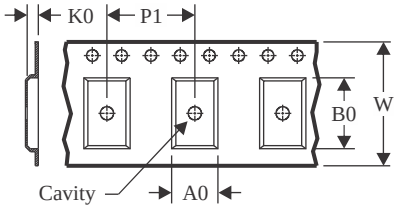
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

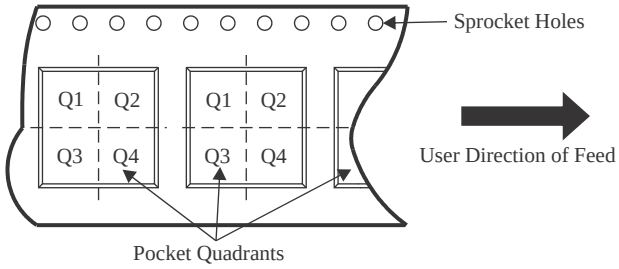


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

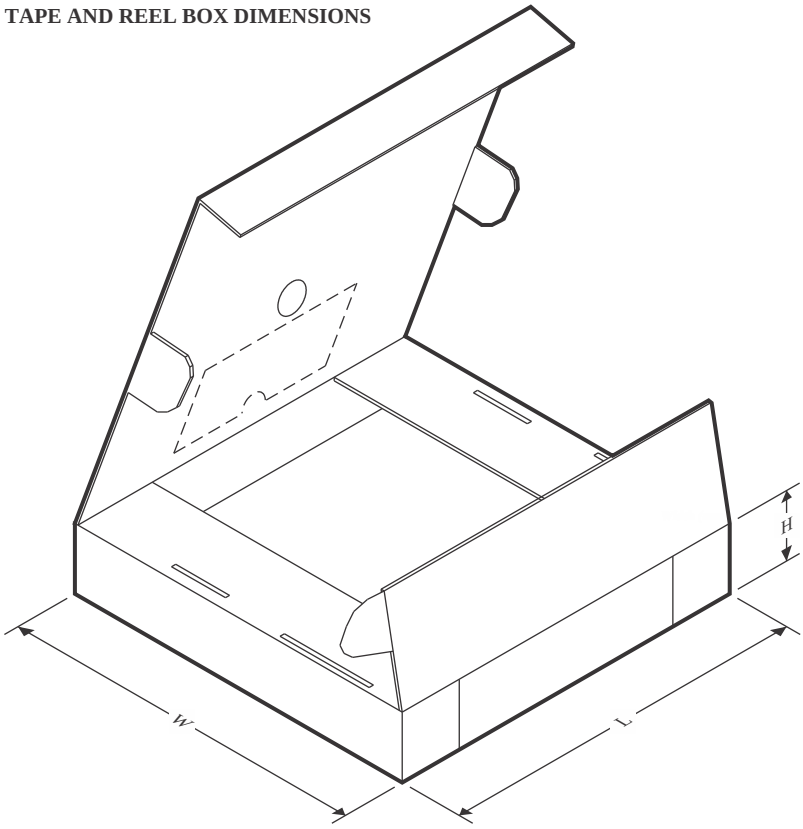
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16401Q5T	VSON-CLIP	DQH	8	250	178.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

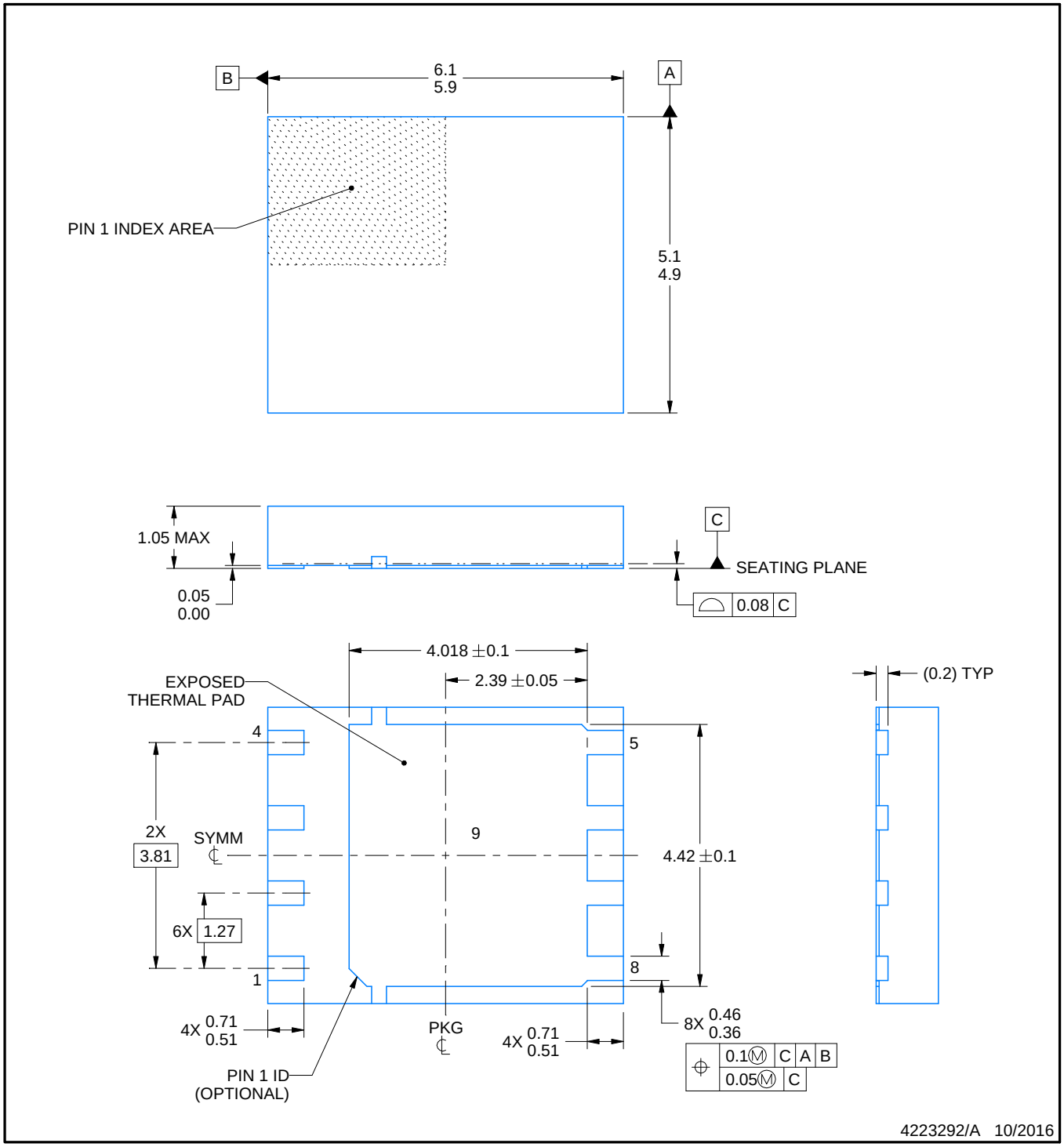
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16401Q5T	VSON-CLIP	DQH	8	250	180.0	180.0	79.0

PACKAGE OUTLINE

DQH0008A

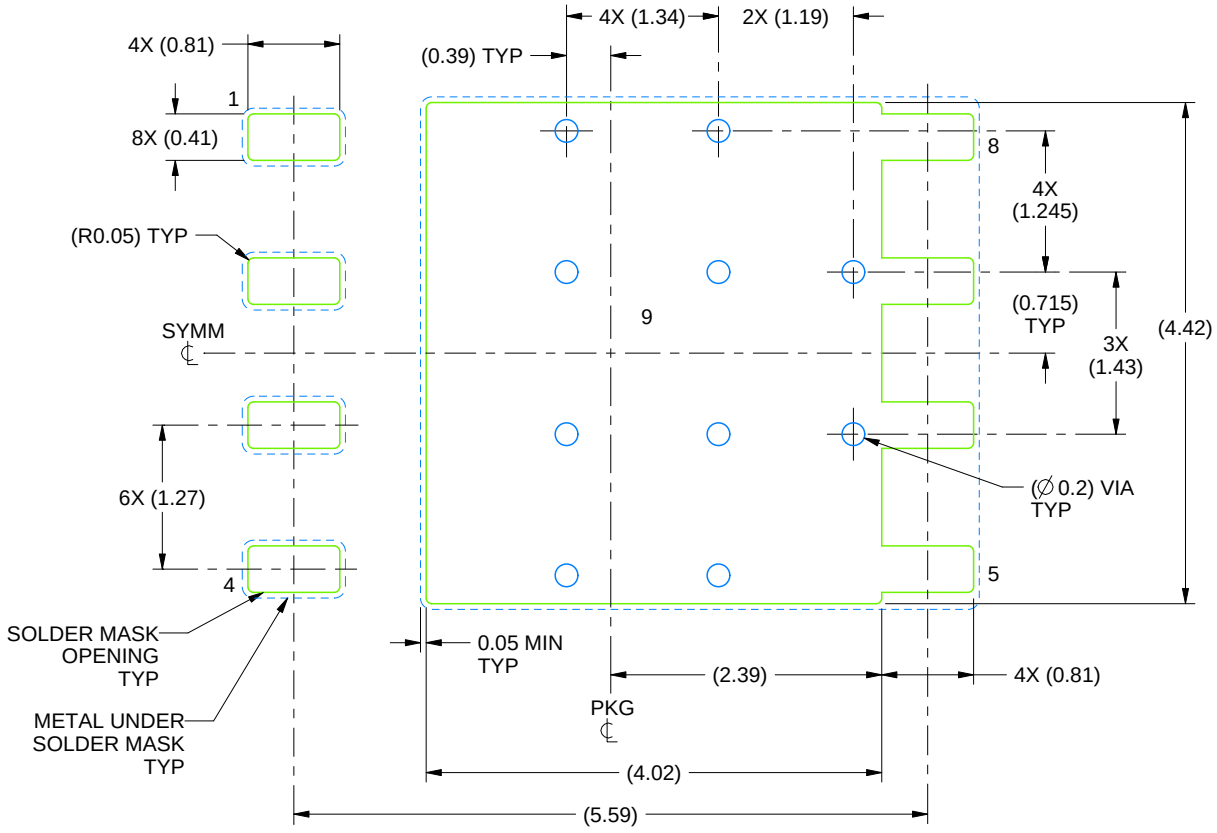
VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:15X

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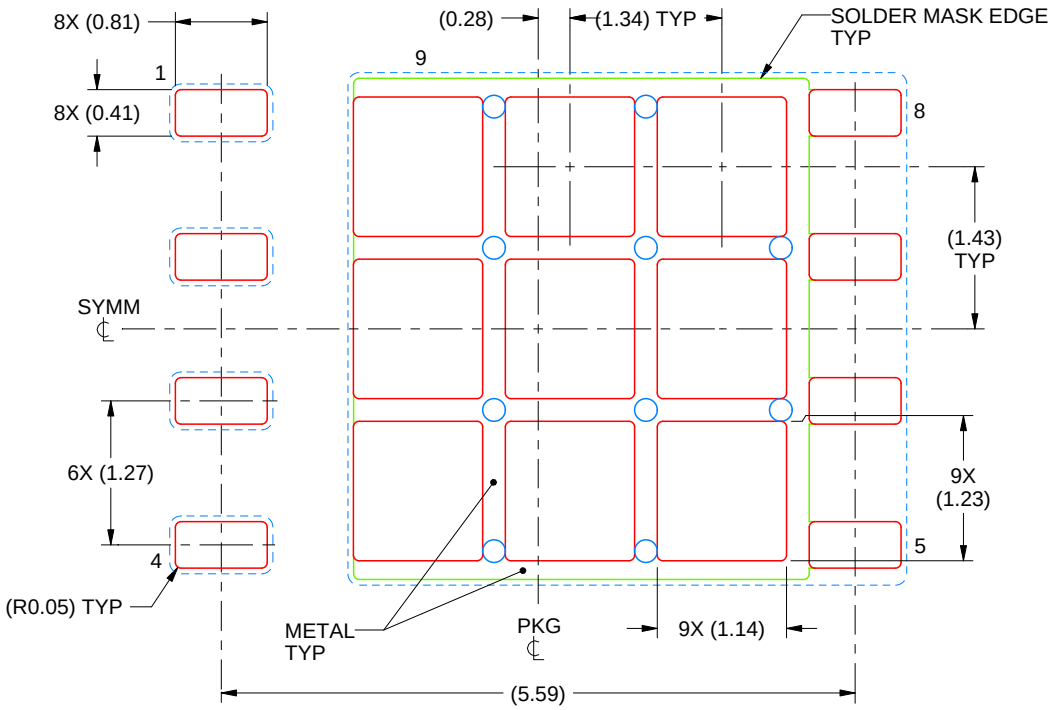
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.