

650V Cascode GaN FET in TO-247 (source tab)

Description

The TPH3205WSB 650V, 49mΩ gallium nitride (GaN) FET is a normally-off device. Transphorm GaN FETs offer better efficiency through lower gate charge, faster switching speeds, and smaller reverse recovery charge, delivering significant advantages over traditional silicon (Si) devices.

Transphorm is a leading-edge wide band gap supplier with world-class innovation and a portfolio of fully-qualified GaN transistors that enables increased performance and reduced overall system size and cost.

Related Literature

- [AN0009](#): Recommended External Circuitry for GaN FETs
- [AN0003](#): Printed Circuit Board Layout and Probing

Ordering Information

Part Number	Package	Package Configuration
TPH3205WSB	3 Lead TO-247	Common Source



Features

- Easy to drive—compatible with standard gate drivers
- Low conduction and switching losses
- Low Q_{rr} of 136nC—no free-wheeling diode required
- GSD pin layout improves high speed design
- JEDEC-qualified GaN technology
- RoHS compliant and Halogen-free

Benefits

- Increased efficiency through fast switching
- Increased power density
- Reduced system size and weight
- Enables more efficient topologies—easy to implement bridgeless totem-pole designs
- Lower BOM cost

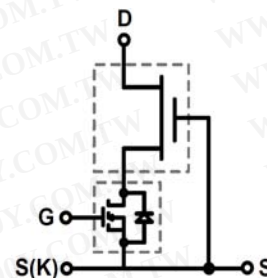
Applications

- Renewable energy
- Industrial
- Telecom and datacom
- Servo motors

Key Specifications

V_{DS} (V) min	650
V_{TDS} (V) max	800
$R_{DS(on)}$ (mΩ) max*	60
Q_{rr} (nC) typ	136
Q_g (nC) typ	28

* Dynamic $R_{DS(on)}$



Cascode Device Structure

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-34970699
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

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Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise stated)

Symbol	Parameter		Limit Value	Unit
I _{D25°C}	Continuous drain current @T _C =25°C ^a		35.2	A
I _{D100°C}	Continuous drain current @T _C =100°C ^a		22.3	A
I _{DM}	Pulsed drain current (pulse width: 10μs)		150	A
V _{DSS}	Drain to source voltage		650	V
V _{TDS}	Transient drain to source voltage ^b		800	V
V _{GSS}	Gate to source voltage		±18	V
P _{D25°C}	Maximum power dissipation		125	W
T _C	Operating temperature	Case	-55 to +150	°C
T _J		Junction	-55 to +150	°C
T _S	Storage temperature		-55 to +150	°C
T _{CSOLD}	Soldering peak temperature ^c		260	°C

Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Junction-to-case	1	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-ambient	40	$^\circ\text{C/W}$

Notes:

- For high current operation, see application note AN0009
- In off-state, spike duty cycle $D < 0.01$, spike duration $< 1\mu\text{s}$
- For 10 sec., 1.6mm from the case

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Electrical Parameters (T_C=25 °C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
V _{DSS-MAX}	Maximum drain-source voltage	650	—	—	V	V _{GS} =0V
V _{GS(th)}	Gate threshold voltage	1.6	2.1	2.6	V	V _{DS} =V _{GS} , I _D =0.7mA
R _{DS(on)}	Drain-source on-resistance (T _J =25 °C) ^a	—	49	60	mΩ	V _{GS} =8V, I _D =22A, T _J =25 °C
	Drain-source on-resistance (T _J =150 °C) ^a	—	105	—		V _{GS} =8V, I _D =22A, T _J =150 °C
I _{DSS}	Drain-to-source leakage current (T _J =25 °C)	—	4	40	μA	V _{DS} =650V, V _{GS} =0V, T _J =25 °C
	Drain-to-source leakage current (T _J =150 °C)	—	15	—		V _{DS} =650V, V _{GS} =0V, T _J =150 °C
I _{GSS}	Gate-to-source forward leakage current	—	—	100	nA	V _{GS} =18V
	Gate-to-source reverse leakage current	—	—	-100		V _{GS} =-18V
C _{ISS}	Input capacitance	—	2200	—	pF	V _{GS} =0V, V _{DS} =400V, f=1MHz
C _{OSS}	Output capacitance	—	135	—		
C _{RSS}	Reverse transfer capacitance	—	23	—		
C _{O(er)}	Output capacitance, energy related ^b	—	190	—	pF	V _{GS} =0V, V _{DS} =0V to 400V
C _{O(tr)}	Output capacitance, time related ^c	—	300	—		
Q _g	Total gate charge	—	28	42	nC	V _{DS} =400V, V _{GS} =0V to 8V, I _D =22A
Q _{gs}	Gate-source charge	—	10	—		
Q _{gd}	Gate-drain charge	—	6	—		
t _{d(on)}	Turn-on delay	—	36	—	ns	V _{DS} =400V, V _{GS} =0V to 8V, I _D =22A, R _G =4Ω including driver output resistance (See Figure 13)
t _r	Rise time	—	7.6	—		
T _{d(off)}	Turn-off delay	—	40	—		
t _f	Fall time	—	8.6	—		
Reverse Device Characteristics						
I _S	Reverse current	—	—	22	A	V _{GS} =0V, T _C =100 °C ≤50% Duty Cycle
V _{SD}	Reverse voltage ^a	—	2.0	2.4	V	V _{GS} =0V, I _S =22A, T _J =25 °C
		—	1.5	1.7		V _{GS} =0V, I _S =11A, T _J =25 °C
t _{rr}	Reverse recovery time	—	40	—	ns	I _S =22A, V _{DD} =400V,
Q _{rr}	Reverse recovery charge	—	136	—	nC	di/dt=1000A/μs, T _J =25 °C

Notes:

a. Dynamic value

b. Equivalent capacitance to give same stored energy from 0V to 400V

c. Equivalent capacitance to give same charging time from 0V to 400V

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Typical Characteristics (25 °C unless otherwise stated)

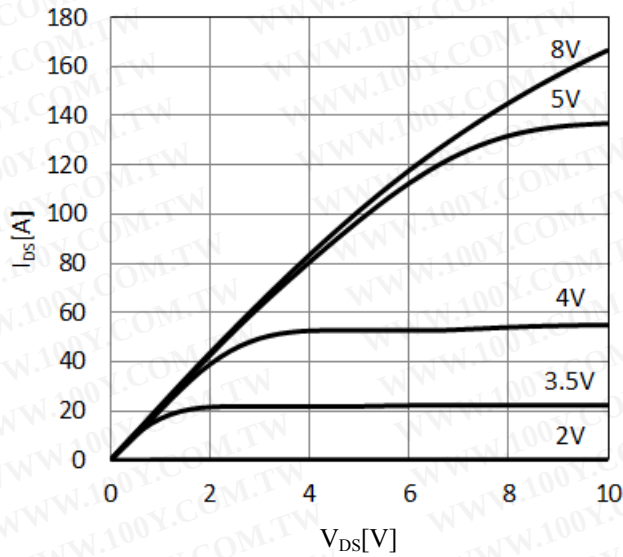


Figure 1. Typical Output Characteristics $T_J=25^\circ\text{C}$

Parameter: V_{GS}

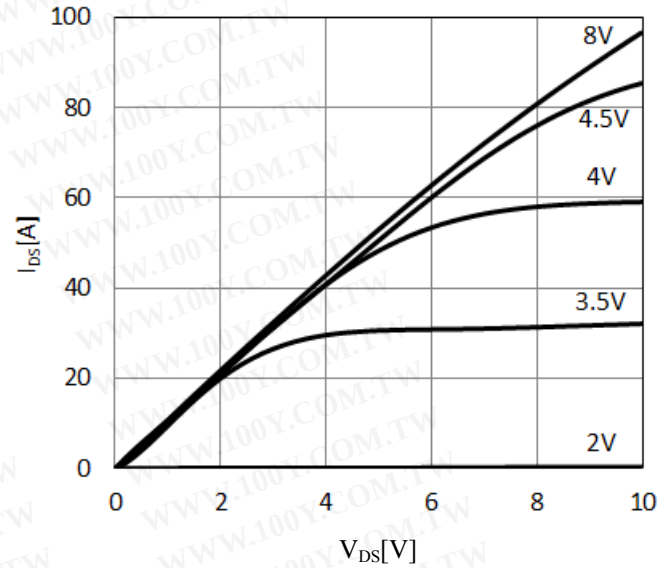


Figure 2. Typical Output Characteristics $T_J=150^\circ\text{C}$

Parameter: V_{GS}

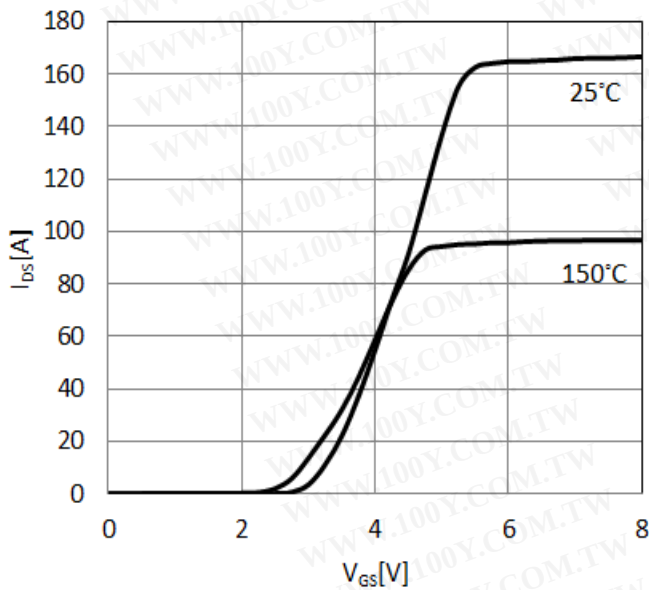


Figure 3. Typical Transfer Characteristics

$V_{DS}=10\text{V}$, parameter: T_J

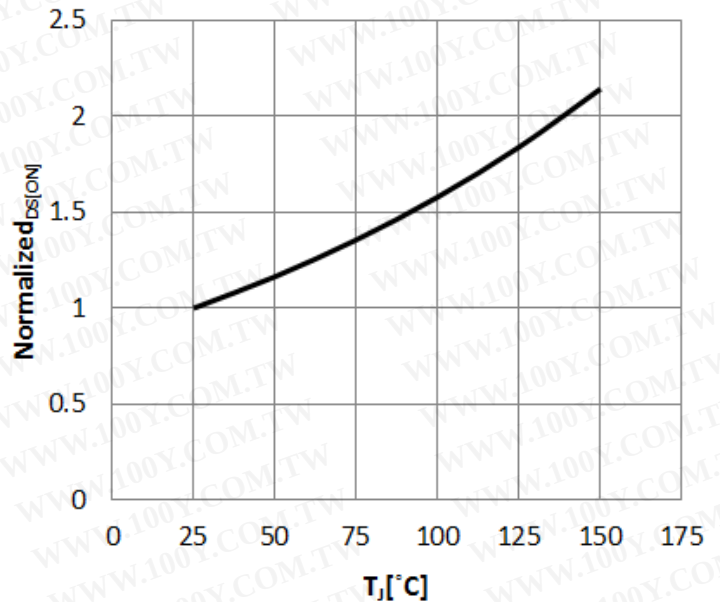


Figure 4. Normalized On-Resistance

$I_D=22\text{A}$, $V_{GS}=8\text{V}$

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Typical Characteristics (25 °C unless otherwise stated)

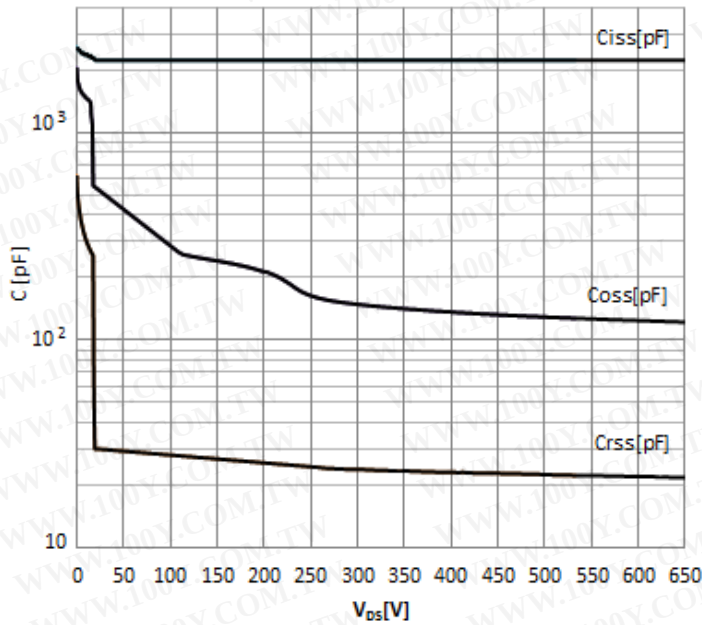


Figure 5. Typical Capacitance

$V_{GS}=0V$, $f=1MHz$

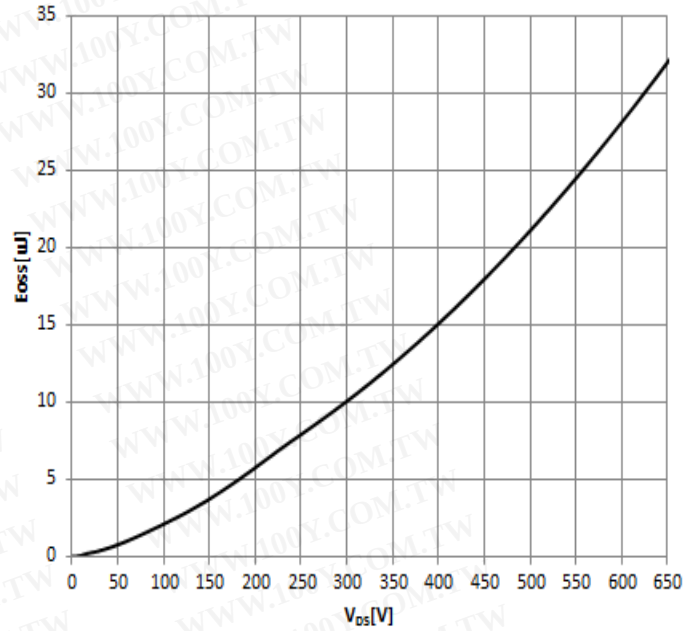


Figure 6. Typical Coss Stored Energy

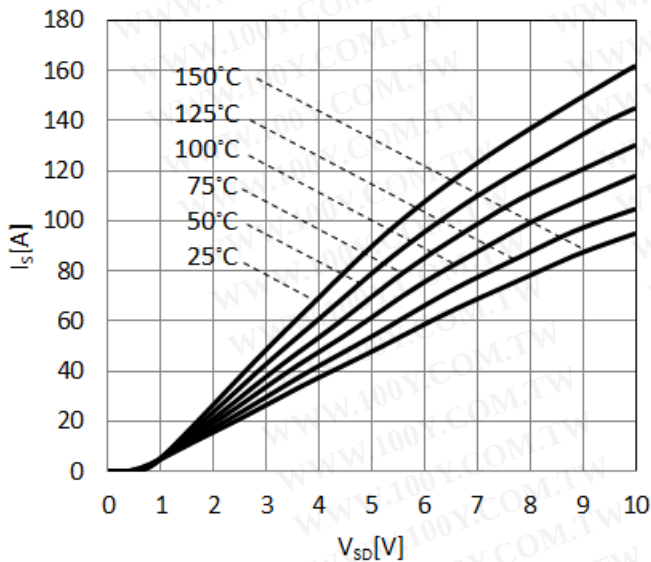


Figure 7. Forward Characteristics of Rev. Diode

$I_S=f(V_{SD})$; parameter: T_J ; pulse width = 20μs

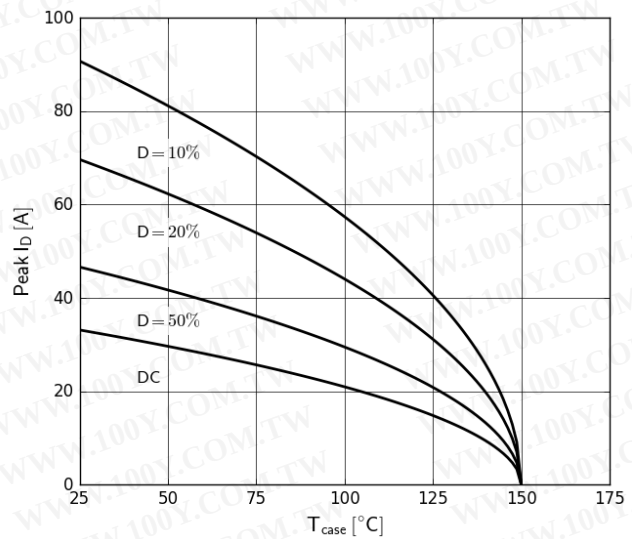


Figure 8. Current Derating

Pulse width $\leq 10\mu s$

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Typical Characteristics (25 °C unless otherwise stated)

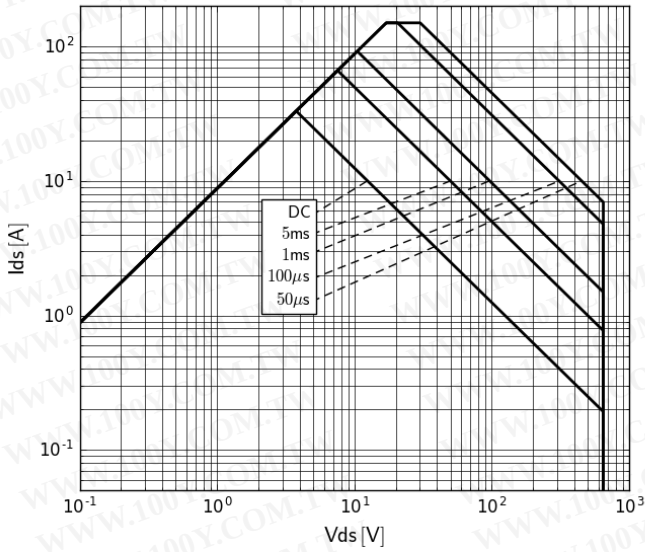


Figure 9. Safe Operating Area $T_c=25^\circ\text{C}$
(calculated based on thermal limit)

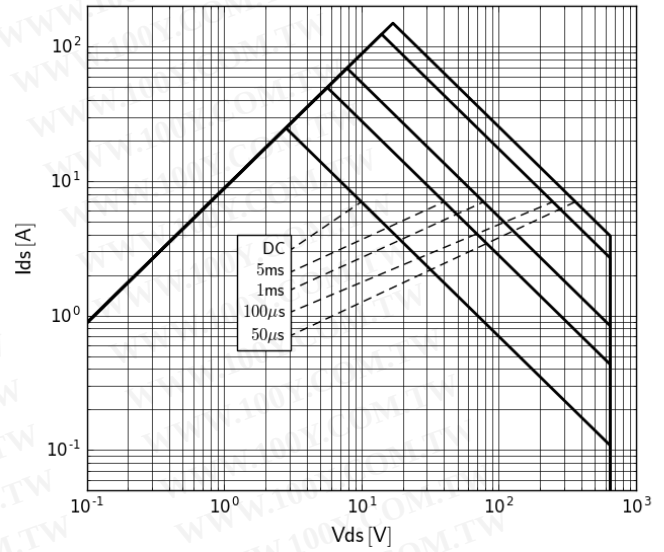


Figure 10. Safe Operating Area $T_c=80^\circ\text{C}$
(calculated based on thermal limit)

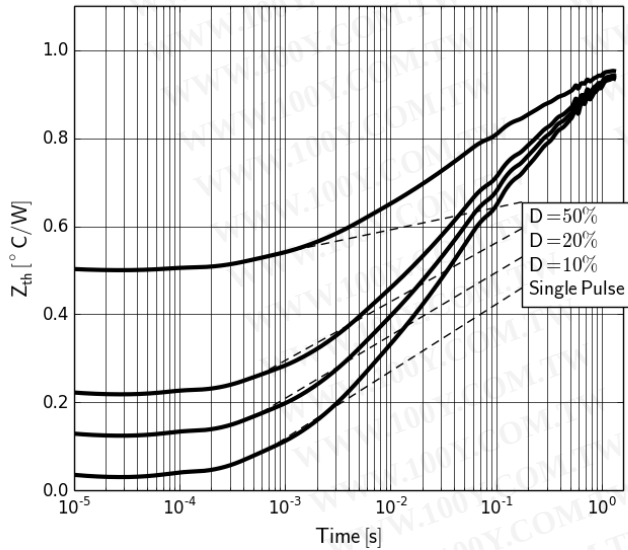


Figure 11. Transient Thermal Resistance

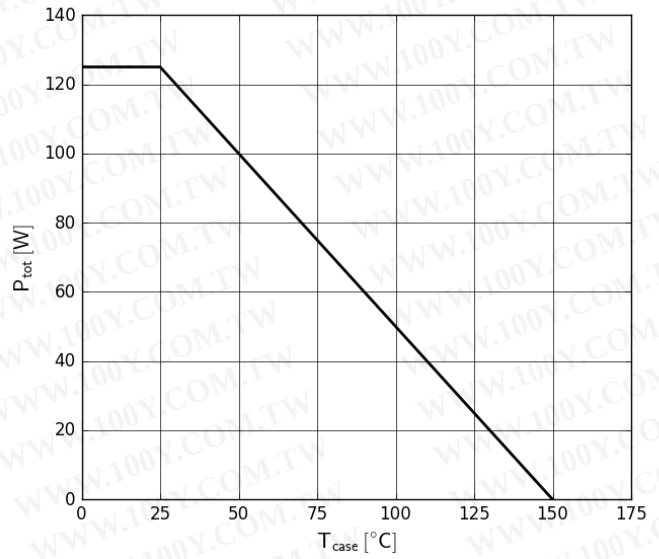


Figure 12. Power Dissipation

Test Circuits and Waveforms

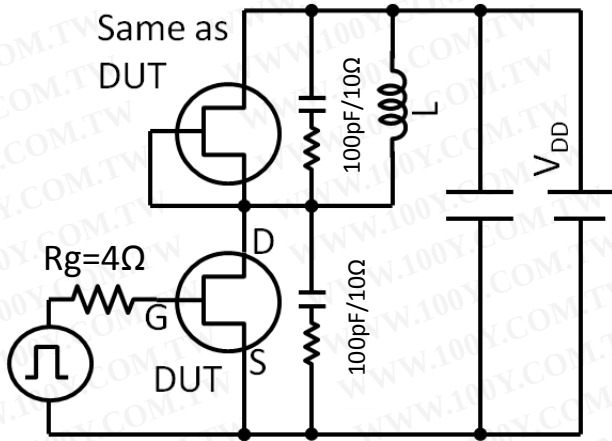


Figure 13. Switching Time Test Circuit
*See app note AN0009 for methods to ensure clean switching

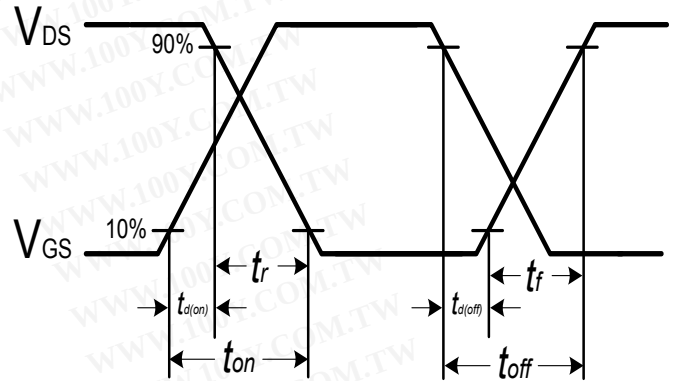


Figure 14. Switching Time Waveform

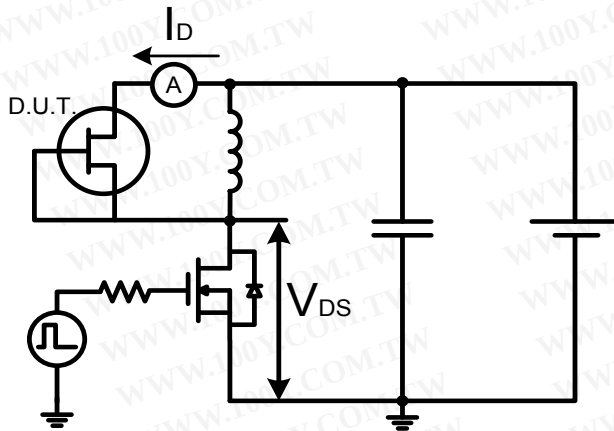


Figure 15. Test Circuit for Diode Characteristics

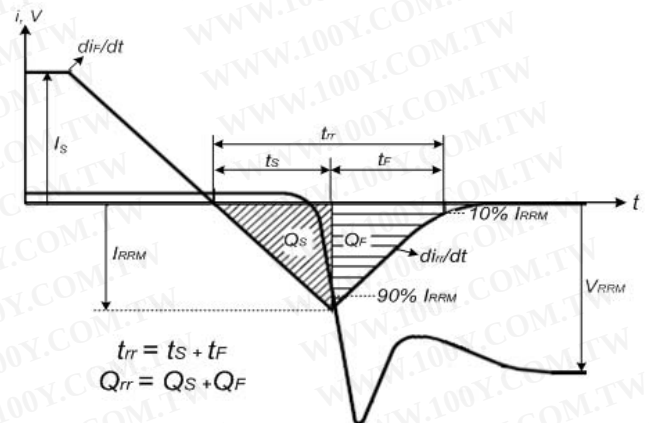


Figure 16. Diode Recovery Waveform

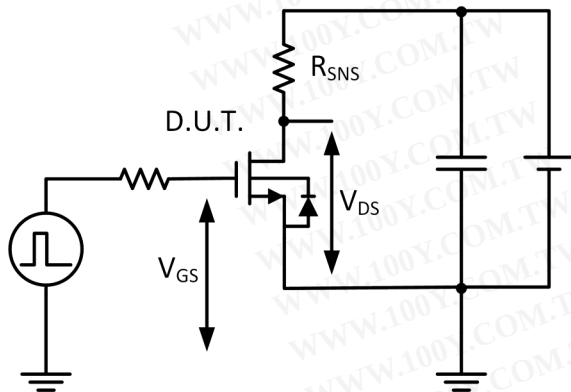


Figure 17. Test Circuit for Dynamic $R_{DS(on)}$

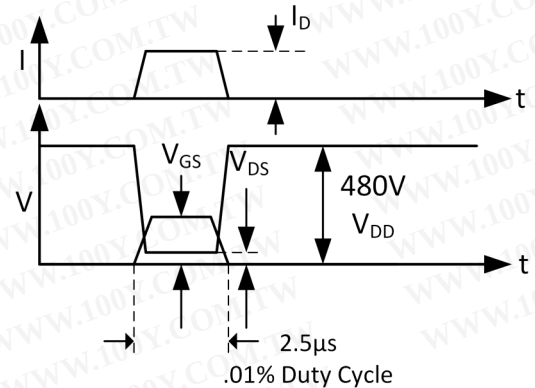
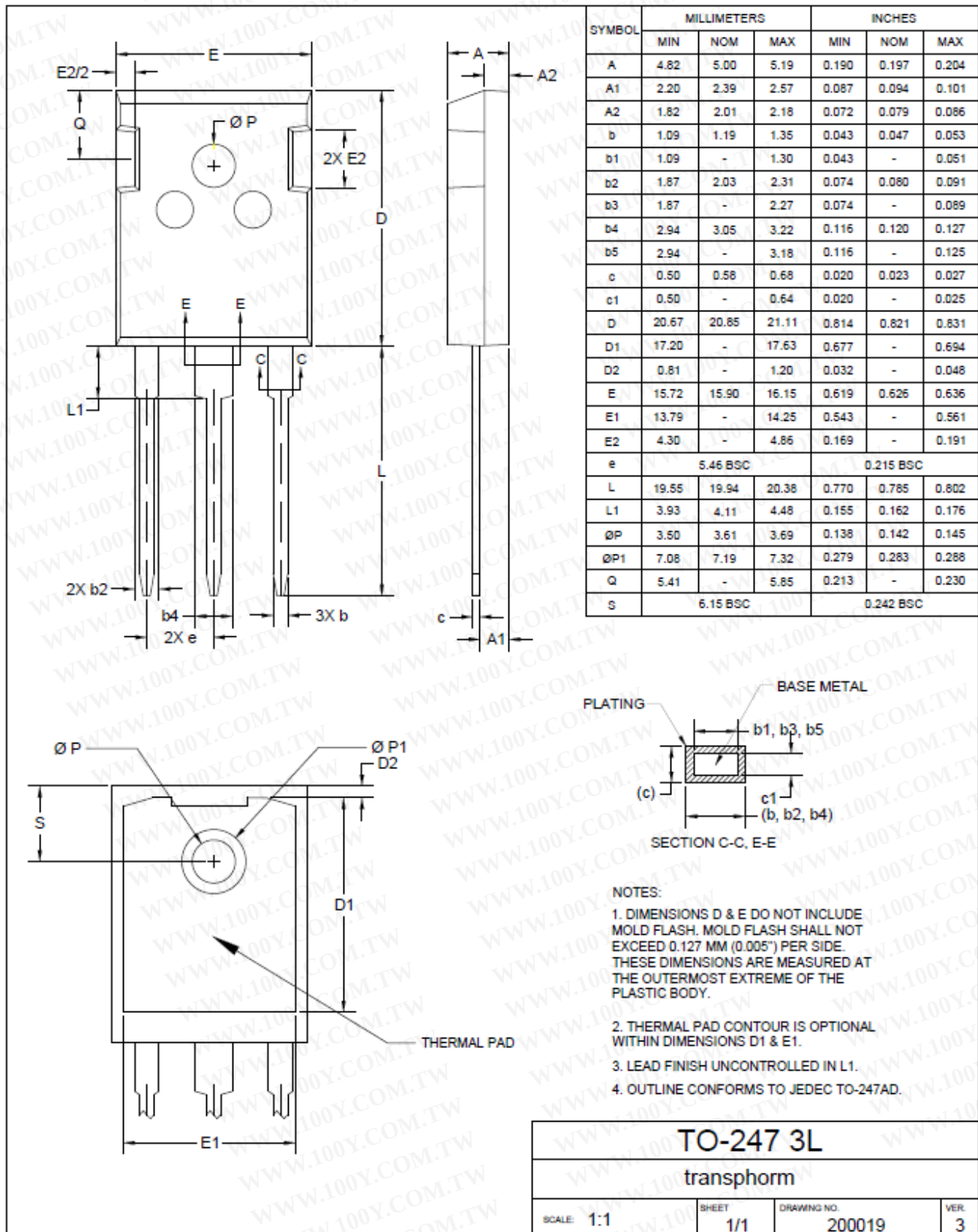


Figure 18. Dynamic $R_{DS(on)}$ Waveform

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Mechanical

3 Lead TO-247 Package



TPH3205WSB

Design Considerations

The fast switching of GaN devices reduces current-voltage cross-over losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note [Printed Circuit Board Layout and Probing for GaN Power Switches](#). The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Transphorm GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See AN0003 : Printed Circuit Board Layout and Probing	

Application Notes

- [AN0002](#): Characteristics of Transphorm GaN Power Switches
- [AN0003](#): Printed Circuit Board Layout and Probing
- [AN0004](#): Designing Hard-switched Bridges with GaN
- [AN0008](#): Drain Voltage and Avalanche Ratings for GaN FETs
- [AN0009](#): Recommended External Circuitry for GaN FETs

Evaluation Boards

- TDPS2800E2C1-KIT: 2.8kW totem-pole PFC evaluation platform
- TDPS3500E0E10-KIT: 3.5kW hard-switched half-bridge, buck, or boost evaluation platform

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Revision History

Version	Date	Change(s)
1	11/14/2016	B version integrates bleed resistor
2	12/12/2016	Formatting Changes to p. 3, revision of dynamic measurement verbiage
3	2/15/2017	Updated the package drawing

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