P-Channel 20-V (D-S) MOSFET with Schottky Diode

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 20	0.054 at V_{GS} = - 10 V	6.2	4.5 nC
	0.094 at V_{GS} = - 4.5 V	4.7	

SCHOTTKY PRODUCT SUMMARY		
V_{KA} (V)	V_f (V) Diode Forward Voltage	I_F (A)[a]
20	0.45 at 1 A	2

FEATURES

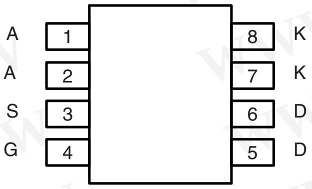
- **Halogen-free According to IEC 61249-2-21 Definition**
- LITTLE FOOT® *Plus* Schottky
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

APPLICATIONS

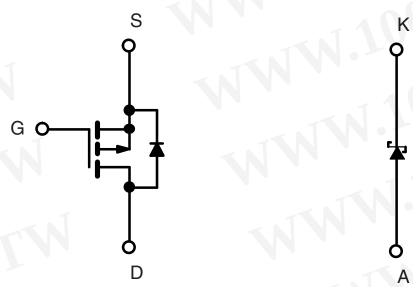
- Portable Devices
  - Ideal for Boost Circuits
  - Ideal for Buck Circuits

SO-8



Top View

Ordering Information: Si4621DY-T1-E3 (Lead (Pb)-free)
Si4621DY-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage (MOSFET)		V_{DS}	- 20	V
Reverse Voltage (Schottky)		V_{KA}	20	
Gate-Source Voltage (MOSFET)		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C) (MOSFET)	T_C = 25 °C	I_D	- 6.2	A
	T_C = 70 °C		- 5[a]	
	T_A = 25 °C		- 5[b, c]	
	T_A = 70 °C		- 4[b, c]	
Pulsed Drain Current (MOSFET)		I_{DM}	- 25	
Continuous Source-Drain Diode Current (MOSFET Diode Conduction)	T_C = 25 °C	I_S	- 2.6	
	T_A = 25 °C		1.7[b, c]	
Average Forward Current (Schottky)		I_F	2[b]	
Pulsed Forward Current (Schottky)		I_{FM}	5	
Maximum Power Dissipation (MOSFET)	T_C = 25 °C	P_D	3.1	W
	T_C = 70 °C		2	
	T_A = 25 °C		2[b, c]	
	T_A = 70 °C		1.3[b, c]	
Maximum Power Dissipation (Schottky)	T_C = 25 °C		2.7	
	T_C = 70 °C		1.7	
	T_A = 25 °C		1.6[b, c]	
	T_A = 70 °C		1[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C

VISHAY

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient (MOSFET)[b, f]	R_{thJA}	55	62.5	°C/W
Maximum Junction-to-Foot (Drain) (MOSFET)	R_{thJF}	33	40	
Maximum Junction-to-Ambient (Schottky)[b, g]	R_{thJA}	63	78	
Maximum Junction-to-Foot (Drain) (Schottky)	R_{thJF}	39	47	

Notes:
b. Surface Mounted on 1" x 1" FR4 board.
c. t = 10 s.
f. Maximum under Steady State conditions is 110 °C/W.
g. Maximum under Steady State conditions is 115 °C/W.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 250 µA		- 16		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			3.6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = - 250 µA	- 1		- 3	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 20 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 20 V, V_{GS} = 0 V, T_J = 55 °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq$ 5 V, V_{GS} = - 10 V	- 25			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 5 A		0.042	0.054	Ω
		V_{GS} = - 4.5 V, I_D = - 1.1 A		0.073	0.094	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 10 V, I_D = - 5 A		10		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 10 V, V_{GS} = 0 V, f = 1 MHz		450		pF
Output Capacitance	C_{oss}			160		
Reverse Transfer Capacitance	C_{rss}			105		
Total Gate Charge	Q_g	V_{DS} = - 10 V, V_{GS} = - 10 V, I_D = - 6.2 A		8.7	13	nC
		V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 6.2 A		4.5	6.8	
Gate-Source Charge	Q_{gs}			1.7		
Gate-Drain Charge	Q_{gd}			1.8		
Gate Resistance	R_g	f = 1 MHz		9		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 2.5 Ω $I_D \cong$ - 4 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		15	25	ns
Rise Time	t_r			60	90	
Turn-Off DelayTime	$t_{d(off)}$			22	35	
Fall Time	t_f			15	25	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 2.5 Ω $I_D \cong$ - 4 A, V_{GEN} = - 10 V, R_g = 1 Ω		5	10	
Rise Time	t_r			60	90	
Turn-Off DelayTime	$t_{d(off)}$			20	30	
Fall Time	t_f			7	15	

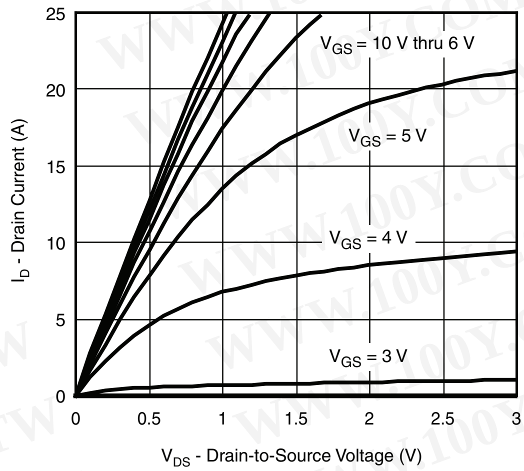
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			- 6.2	A
Pulse Diode Forward Current	I_{SM}				- 25	A
Body Diode Voltage	V_{SD}	I_S = - 1.7 A, V_{GS} = 0 V		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 1.7 A, dI/dt = 100 A/µs, T_J = 25 °C		21	40	ns
Body Diode Reverse Recovery Charge	Q_{rr}			10	20	nC
Reverse Recovery Fall Time	t_a			7		ns
Reverse Recovery Rise Time	t_b			16		ns

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

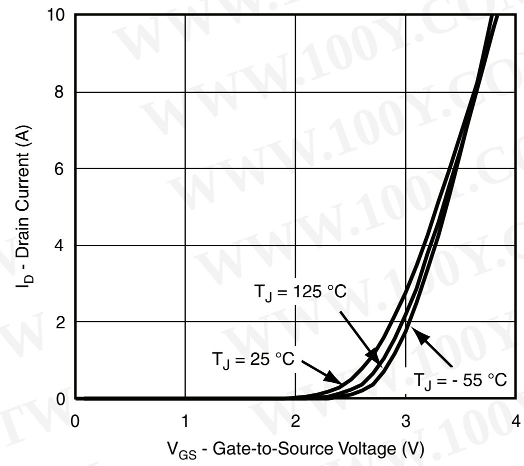
SCHOTTKY SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Forward Voltage Drop	V_F	I_F = 1 A		0.41	0.45	V
		I_F = 1 A, T_J = 125 °C		0.36	0.41	
Maximum Reverse Leakage Current	I_{rm}	V_r = 20 V		0.02	0.20	mA
		V_r = 20 V, T_J = 85 °C		0.7	7	
		V_r = 20 V, T_J = 125 °C		5	50	
Junction Capacitance	C_T	V_r = 10 V		60		pF

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

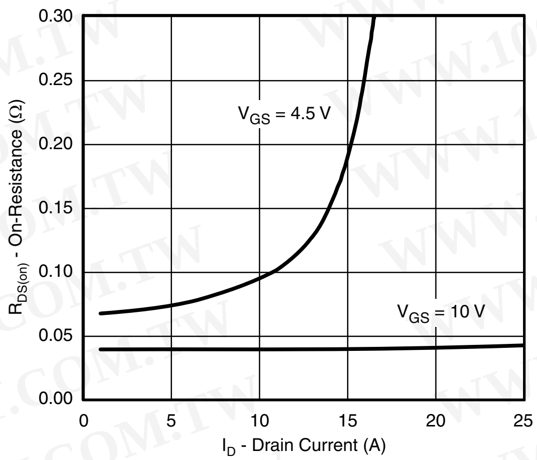
MOSFET TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



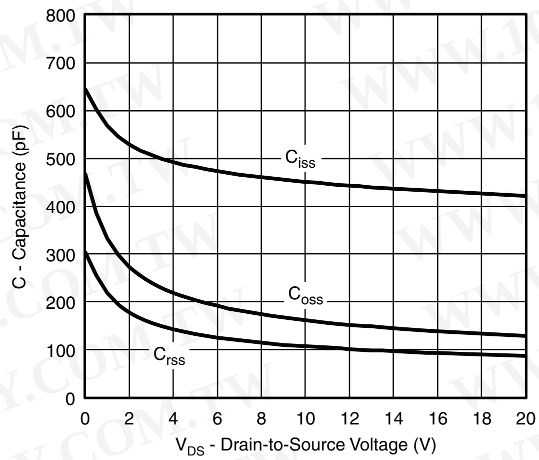
Output Characteristics



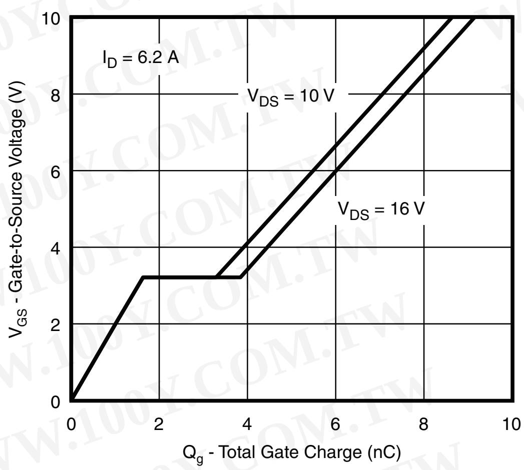
Transfer Characteristics



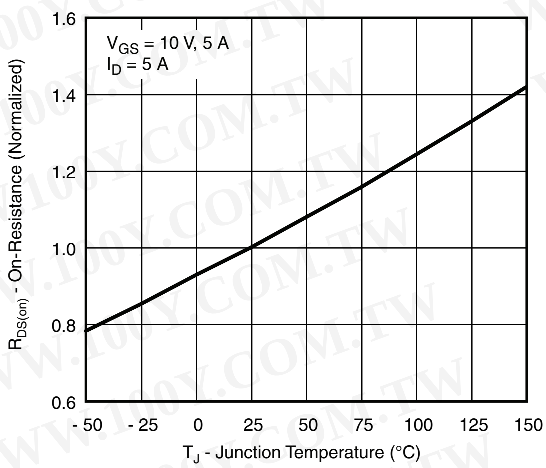
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

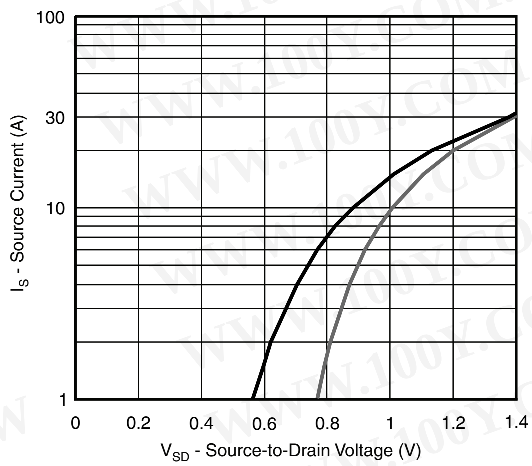


Gate Charge

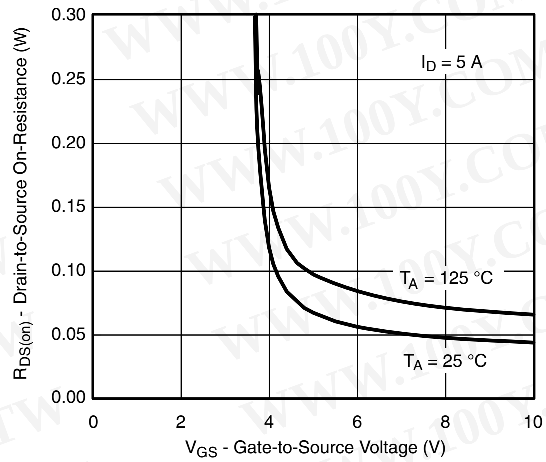


On-Resistance vs. Junction Temperature

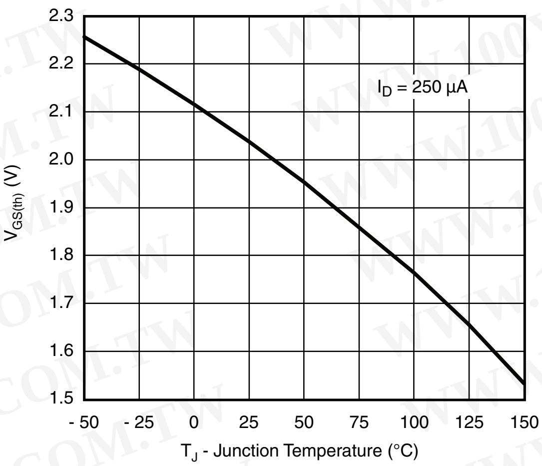
MOSFET TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



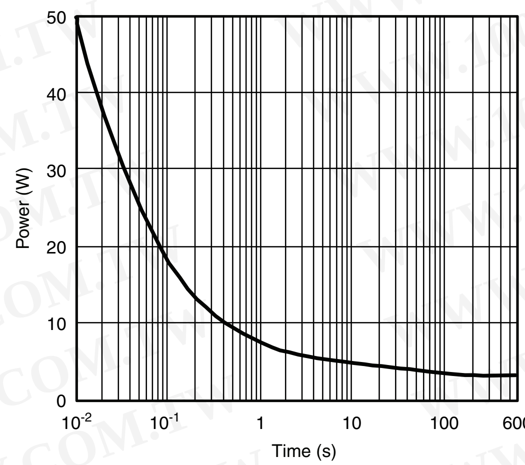
Source-Drain Diode Forward Voltage



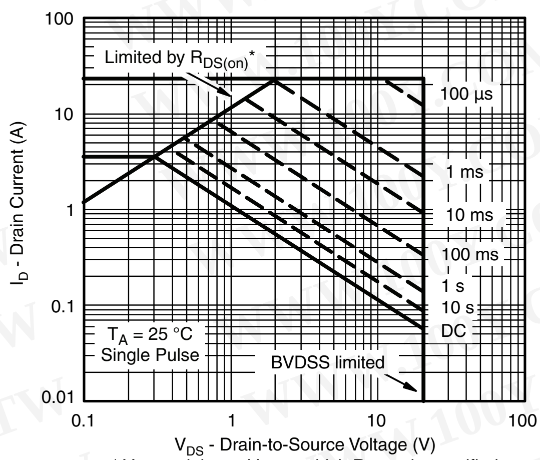
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



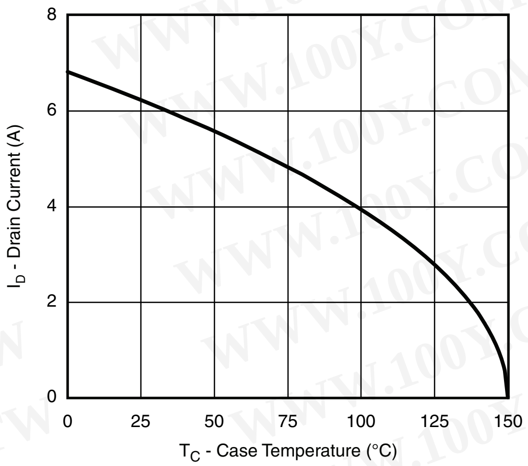
Single Pulse Power, Junction-to-Ambient



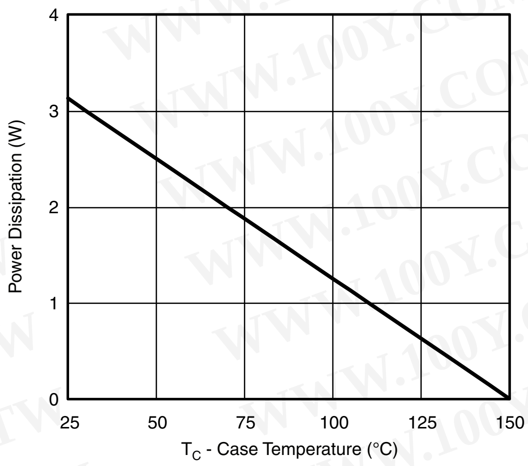
* V_{DS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case

MOSFET TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



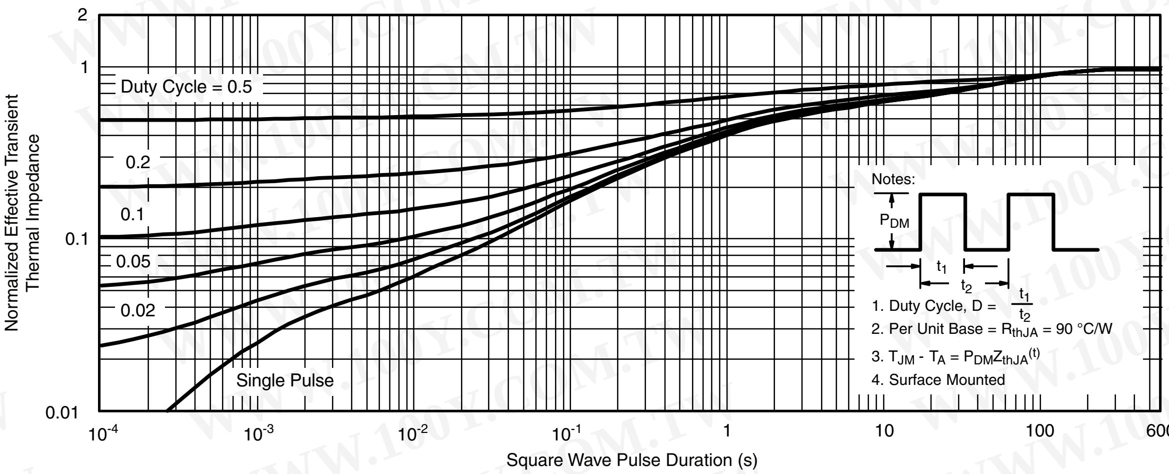
Current Derating*



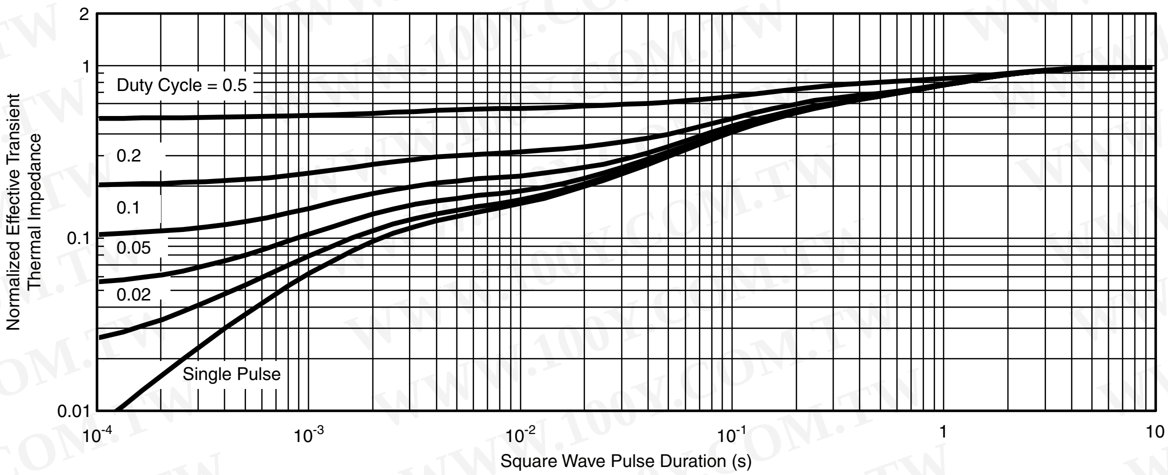
Power Derating

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

MOSFET TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

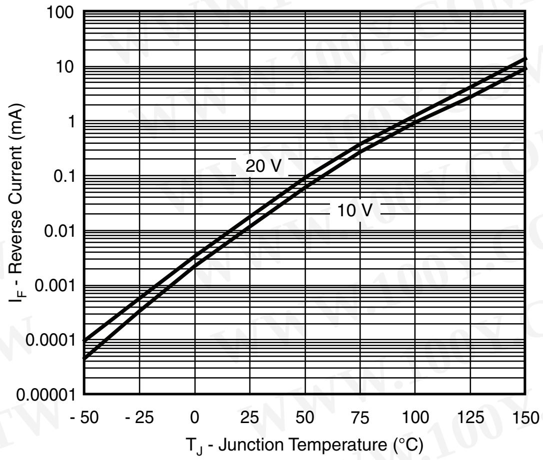


Normalized Thermal Transient Impedance, Junction-to-Ambient

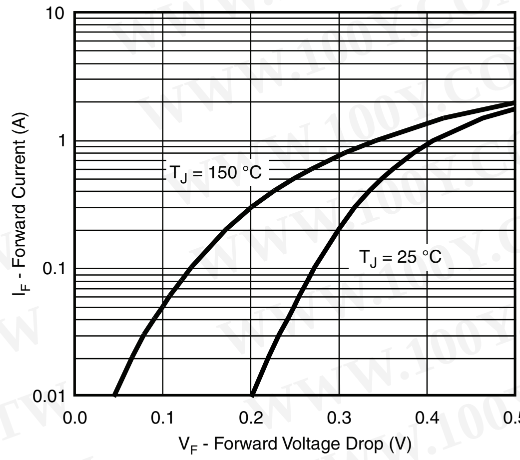


Normalized Thermal Transient Impedance, Junction-to-Foot

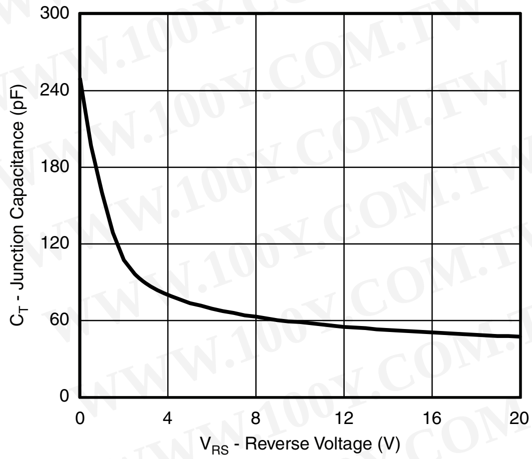
SCHOTTKY TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



Reverse Current vs. Junction Temperature

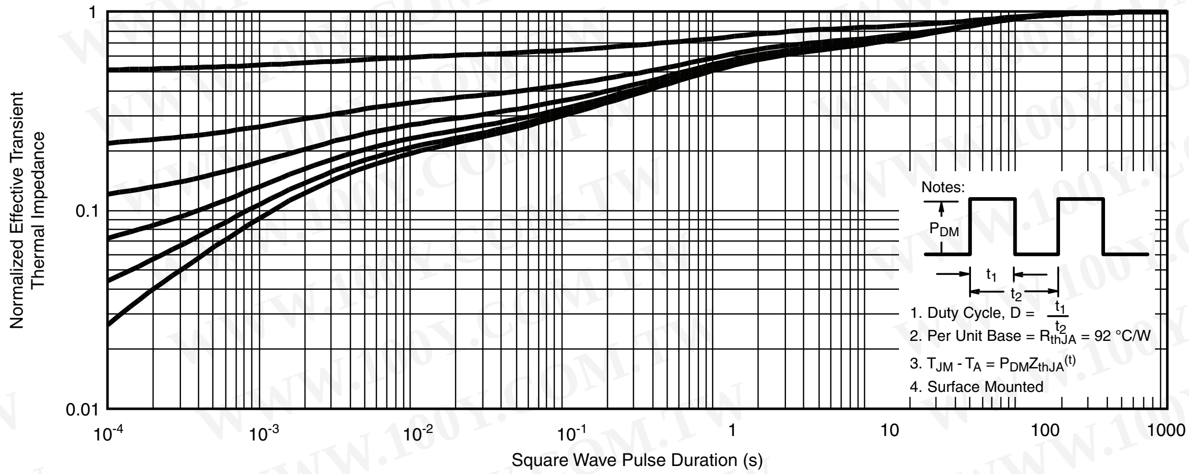


Forward Voltage Drop

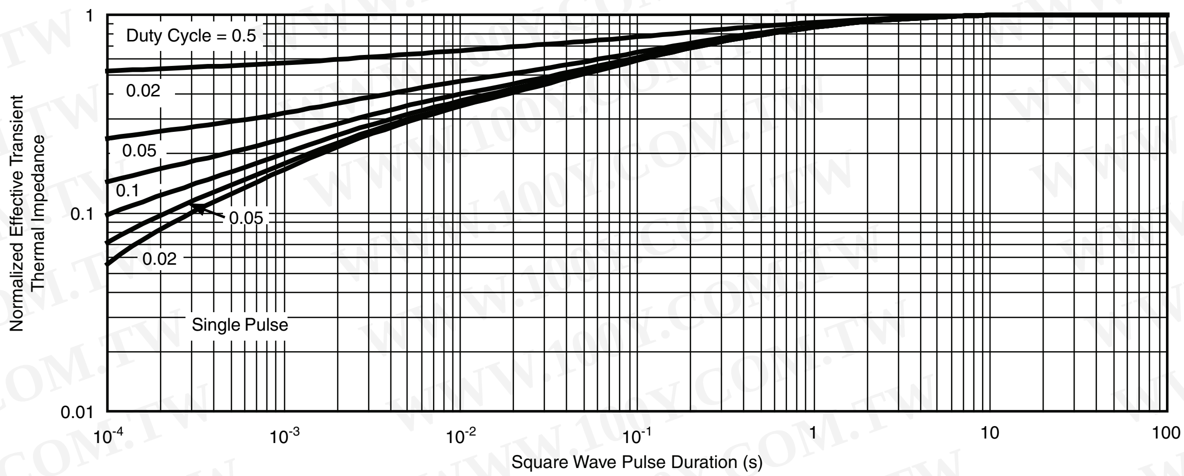


Capacitance

SCHOTTKY TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



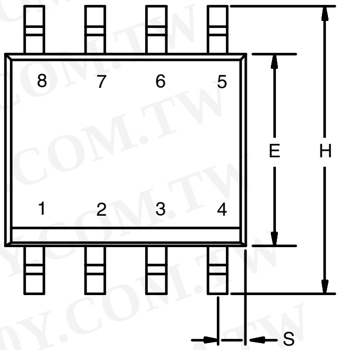
Normalized Thermal Transient Impedance, Junction-to-Ambient

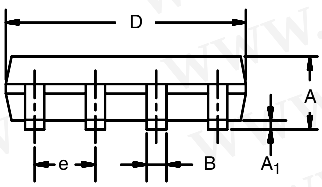


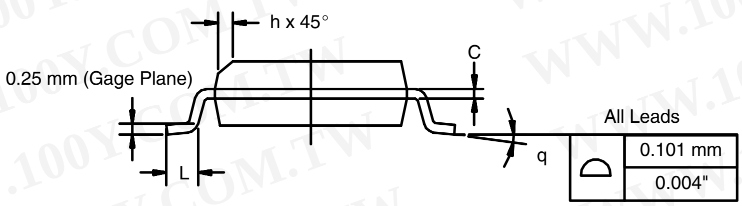
Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73855.

SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012







DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026

ECN: C-06527-Rev. I, 11-Sep-06
DWG: 5498

Mounting LITTLE FOOT®, SO-8 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/ppg?72286), for the basis of the pad design for a LITTLE FOOT SO-8 power MOSFET. In converting this recommended minimum pad to the pad set for a power MOSFET, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

In the case of the SO-8 package, the thermal connections are very simple. Pins 5, 6, 7, and 8 are the drain of the MOSFET for a single MOSFET package and are connected together. In a dual package, pins 5 and 6 are one drain, and pins 7 and 8 are the other drain. For a small-signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate. The total cross section of the copper may be adequate to carry the current required for the application, but it presents a large thermal impedance. Also, heat spreads in a circular fashion from the heat source. In this case the drain pins are the heat sources when looking at heat spread on the PC board.

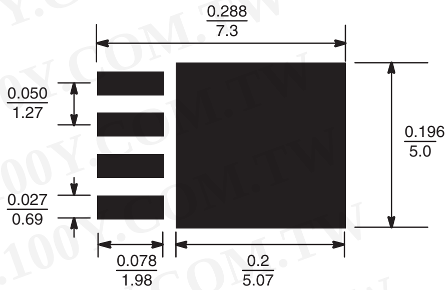


Figure 1. Single MOSFET SO-8 Pad Pattern With Copper Spreading

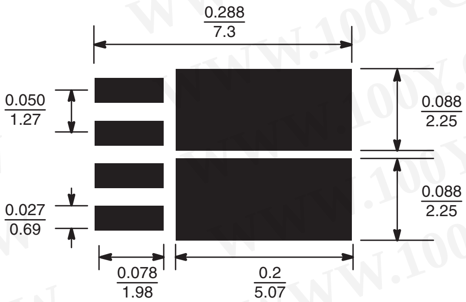


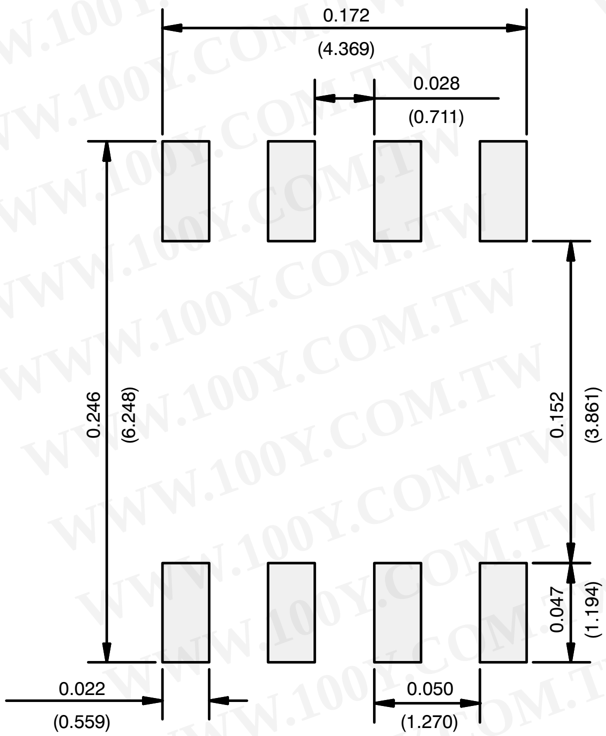
Figure 2. Dual MOSFET SO-8 Pad Pattern With Copper Spreading

The minimum recommended pad patterns for the single-MOSFET SO-8 with copper spreading (Figure 1) and dual-MOSFET SO-8 with copper spreading (Figure 2) show the starting point for utilizing the board area available for the heat-spreading copper. To create this pattern, a plane of copper overlies the drain pins. The copper plane connects the drain pins electrically, but more importantly provides planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the ambient air. These patterns use all the available area underneath the body for this purpose.

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, “thermal” connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low impedance path for heat to move away from the device.

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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Material Category Policy

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.