3 nV/√Hz Ultralow Distortion, High Speed Op Amp

AD8045

FEATURES

Ultralow distortion
SFDR
–101 dBc @ 5 MHz
–90 dBc @ 20 MHz
–63 dBc @ 70 MHz
Third-order intercept
43 dBm @ 10 MHz
Low noise
3 nV/√Hz
3 pA/√Hz
High speed
1 GHz, –3 dB bandwidth (G = +1)
1350 V/µs slew rate
7.5 ns settling time to 0.1%
Standard and low distortion pinout
Supply current: 15 mA
Offset voltage: 1.0 mV max
Wide supply voltage range: 3.3 V to 12 V

APPLICATIONS

Instrumentation
IF and baseband amplifiers
Active filters
ADC drivers
DAC buffers

CONNECTION DIAGRAMS

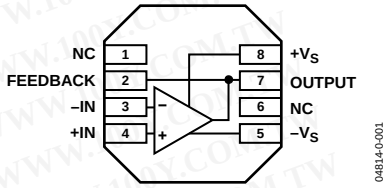

Figure 1. 8-Lead AD8045 LFCSP (CP-8)

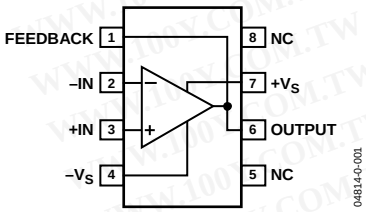

Figure 2. 8-Lead AD8045 SOIC/EP (RD-8)

GENERAL DESCRIPTION

The AD8045 is a unity gain stable voltage feedback amplifier with ultralow distortion, low noise, and high slew rate. With a spurious-free dynamic range of –90 dBc @ 20 MHz, the AD8045 is an ideal solution in a variety of applications, including ultrasound, ATE, active filters, and ADC drivers. ADI's proprietary next generation XFCB process and innovative architecture enables such high performance amplifiers.

The AD8045 features a low distortion pinout for the LFCSP, which improves second harmonic distortion and simplifies the layout of the circuit board.

The AD8045 has 1 GHz bandwidth, 1350 V/µs slew rate, and settles to 0.1% in 7.5 ns. With a wide supply voltage range (3.3 V to 12 V) and low offset voltage (200 µV), the AD8045 is an ideal candidate for systems that require high dynamic range, precision, and high speed.

The AD8045 amplifier is available in a 3 mm × 3 mm LFCSP and the standard 8-lead SOIC. Both packages feature an exposed paddle that provides a low thermal resistance path to the PCB. This enables more efficient heat transfer, and increases reliability. The AD8045 works over the extended industrial temperature range (–40°C to +125°C).

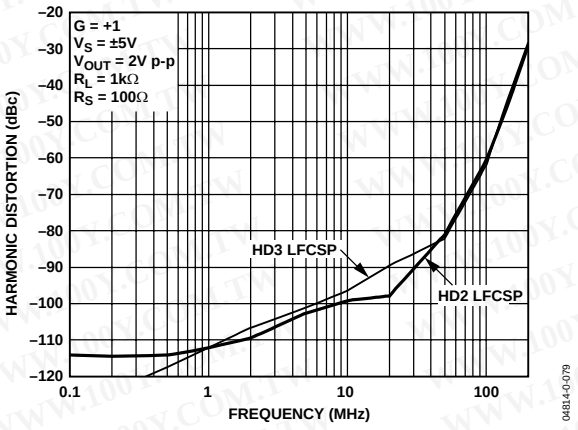

Figure 3. Harmonic Distortion vs. Frequency for Various Packages

Rev. A

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7/04—Revision 0: Initial Version

SPECIFICATIONS WITH ±5 V SUPPLY

T_A = 25°C, G = +1, R_S = 100 Ω, R_L = 1 kΩ to ground, unless noted otherwise. Exposed paddle must be floating or connected to $-V_S$.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.2 V p-p		1000		MHz
	G = +1, V_{OUT} = 2 V p-p	300	350		
	G = +2, V_{OUT} = 0.2 V p-p	320	400		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_{OUT} = 2 V p-p, R_L = 150 Ω		55		MHz
Slew Rate	G = +1, V_{OUT} = 4 V step	1000	1350		V/µs
Settling Time to 0.1%	G = +2, V_{OUT} = 2 V step		7.5		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion (dBc) HD2/HD3	f_C = 5 MHz, V_{OUT} = 2 V p-p				
	LFCSP		−102/−101		dBc
	SOIC		−106/−101		dBc
	f_C = 20 MHz, V_{OUT} = 2 V p-p				
	LFCSP		−98/−90		dBc
	SOIC		−97/−90		dBc
	f_C = 70 MHz, V_{OUT} = 2 V p-p				
	LFCSP		−71/−71		dBc
	SOIC		−60/−71		dBc
Input Voltage Noise	f = 100 kHz		3		nV/√Hz
Input Current Noise	f = 100 kHz		3		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.01		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.01		Degrees
DC PERFORMANCE					
Input Offset Voltage			0.2	1.0	mV
Input Offset Voltage Drift	See Figure 54		8		µV/°C
Input Bias Current			2	6.3	µA
Input Bias Current Drift			8		nA/°C
Input Bias Offset Current			0.2	1.3	µA
Open-Loop Gain	V_{OUT} = −3 V to +3 V	62	64		dB
INPUT CHARACTERISTICS					
Input Resistance	Common-mode/differential		3.6/1.0		MΩ
Input Capacitance	Common-mode		1.3		pF
Input Common-Mode Voltage Range			±3.8		V
Common-Mode Rejection	V_{CM} = ±1 V	−83	−91		dB
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time	V_{IN} = ±3 V, G = +2		8		ns
Output Voltage Swing	R_L = 1 kΩ	−3.8 to +3.8	−3.9 to +3.9		V
	R_L = 100 Ω	−3.4 to +3.5	−3.6 to +3.6		V
Output Current			70		mA
Short-Circuit Current	Sinking/sourcing		90/170		mA
Capacitive Load Drive	30% overshoot, G = +2		18		pF
POWER SUPPLY					
Operating Range		±1.65	±5	±6	V
Quiescent Current			16	19	mA
Positive Power Supply Rejection	$+V_S$ = +5 V to +6 V, $-V_S$ = −5 V	−61	−68		dB
Negative Power Supply Rejection	$+V_S$ = +5 V, $-V_S$ = −5 V to −6 V	−66	−73		dB

SPECIFICATIONS WITH +5 V SUPPLY

T_A = 25°C, G = +1, R_S = 100 Ω, R_L = 1 kΩ to midsupply, unless otherwise noted. Exposed paddle must be floating or connected to $-V_S$.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.2 V p-p		900		MHz
	G = +1, V_{OUT} = 2 V p-p	160	200		MHz
	G = +2, V_{OUT} = 0.2 V p-p	320	395		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_{OUT} = 2 V p-p, R_L = 150 Ω		60		MHz
Slew Rate	G = +1, V_{OUT} = 2 V step	480	1060		V/µs
Settling Time to 0.1%	G = +2, V_{OUT} = 2 V step		10		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion (dBc) HD2/HD3	f_C = 5 MHz, V_{OUT} = 2 V p-p				
	LFCSP		−89/−83		dBc
	SOIC		−92/−83		dBc
	f_C = 20 MHz, V_{OUT} = 2 V p-p				
	LFCSP		−81/−70		dBc
	SOIC		−83/−70		dBc
	f_C = 70 MHz, V_{OUT} = 2 V p-p				
	LFCSP		−57/−46		dBc
	SOIC		−57/−46		dBc
Input Voltage Noise	f = 100 kHz		3		nV/√Hz
Input Current Noise	f = 100 kHz		3		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.01		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.01		Degrees
DC PERFORMANCE					
Input Offset Voltage			0.5	1.4	mV
Input Offset Voltage Drift	See Figure 54		7		µV/°C
Input Bias Current			2	6.6	µA
Input Bias Current Drift			7		nA/°C
Input Bias Offset Current			0.2	1.3	µA
Open-Loop Gain	V_{OUT} = 2 V to 3 V	61	63		dB
INPUT CHARACTERISTICS					
Input Resistance	Common-mode/differential		3/0.9		MΩ
Input Capacitance	Common-mode		1.3		pF
Input Common-Mode Voltage Range			1.2 to 3.8		V
Common-Mode Rejection	V_{CM} = 2 V to 3 V	−78	−94		dB
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time	V_{IN} = −0.5 V to +3 V, G = +2		10		ns
Output Voltage Swing	R_L = 1 kΩ	2.2 to 3.7	1.1 to 4.0		V
	R_L = 100 Ω	2.5 to 3.5	1.2 to 3.8		V
Output Current			55		mA
Short-Circuit Current	Sinking/sourcing		70/140		mA
Capacitive Load Drive	30% overshoot, G = +2		15		pF
POWER SUPPLY					
Operating Range		3.3	5	12	V
Quiescent Current			15	18	mA
Positive Power Supply Rejection	$+V_S$ = +5 V to +6 V, $-V_S$ = 0 V	−65	−67		dB
Negative Power Supply Rejection	$+V_S$ = +5 V, $-V_S$ = 0 V to −1 V	−70	−73		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	12.6 V
Power Dissipation	See Figure 4
Common-Mode Input Voltage	$-V_S - 0.7$ V to $+V_S + 0.7$ V
Differential Input Voltage	$\pm V_S$
Exposed Paddle Voltage	$-V_S$
Storage Temperature	−65°C to +125°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
SOIC	80	30	°C/W
LFCSP	93	35	°C/W

Maximum Power Dissipation

The maximum safe power dissipation for the AD8045 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8045. Exceeding a junction temperature of 175°C for an extended period of time can result in changes in silicon devices, potentially causing degradation or loss of functionality.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the die due to the AD8045 drive at the output. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S).

$$P_D = \textit{Quiescent Power} + (\textit{Total Drive Power} - \textit{Load Power})$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L}$$

RMS output voltages should be considered. If R_L is referenced to $-V_S$, as in single-supply operation, the total drive power is $V_S \times I_{OUT}$. If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply.

$$P_D = (V_S \times I_S) + \frac{(V_S/4)^2}{R_L}$$

In single-supply operation with R_L referenced to $-V_S$, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads and exposed paddle from metal traces, through holes, ground, and power planes reduce θ_{JA}.

Figure 4 shows the maximum safe power dissipation in the package versus the ambient temperature for the exposed paddle SOIC (80°C/W) and LFCSP (93°C/W) package on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

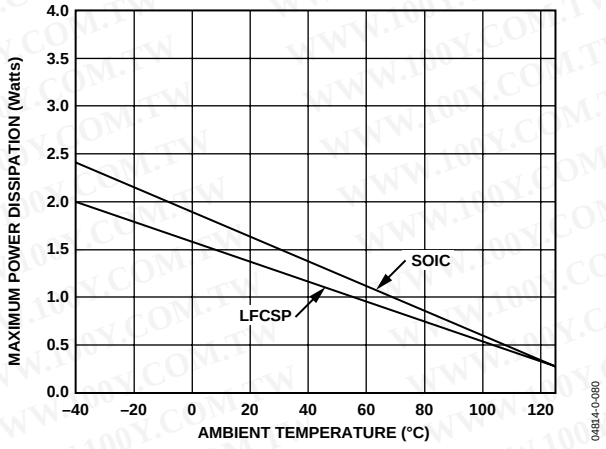

Figure 4. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation and loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

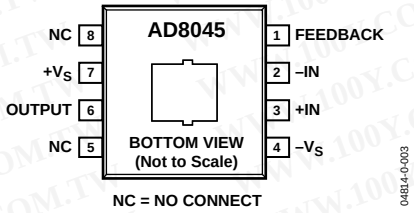

Figure 5. SOIC Pin Configuration

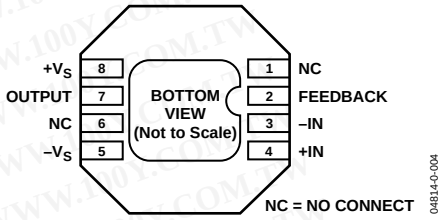

Figure 6 . 8-Lead LFCSP Pin Configuration

Note: The exposed paddle must be connected to $-V_S$ or it must be electrically isolated (floating).

Table 5. 8-Lead SOIC Pin Function Descriptions

Pin No.	Mnemonic	Description
1	FEEDBACK	Feedback Pin
2	–IN	Inverting Input
3	+IN	Noninverting Input
4	$-V_S$	Negative Supply
5	NC	NC
6	OUTPUT	Output
7	$+V_S$	Positive Supply
8	NC	NC
9	Exposed Paddle	Must Be Connected to $-V_S$ or Electrically Isolated

Table 6. 8-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connect
2	FEEDBACK	Feedback Pin
3	–IN	Inverting Input
4	+IN	Noninverting Input
5	$-V_S$	Negative Supply
6	NC	No Connect
7	OUTPUT	Output
8	$+V_S$	Positive Supply
9	Exposed Paddle	Must Be Connected to $-V_S$ or Electrically Isolated

TYPICAL PERFORMANCE CHARACTERISTICS

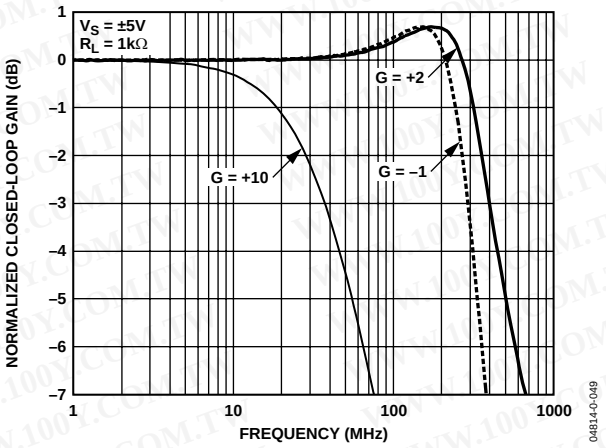

Figure 7. Small Signal Frequency Response for Various Gains

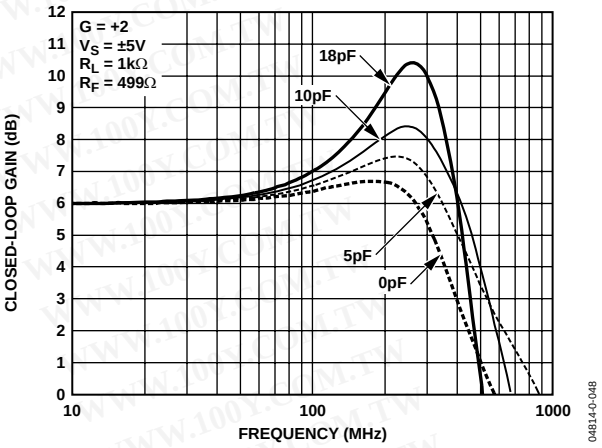

Figure 10. Small Signal Frequency Response for Various Capacitive Loads

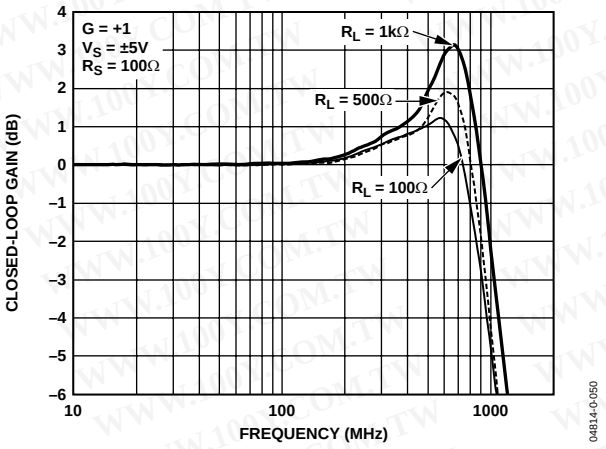

Figure 8. Small Signal Frequency Response for Various Loads

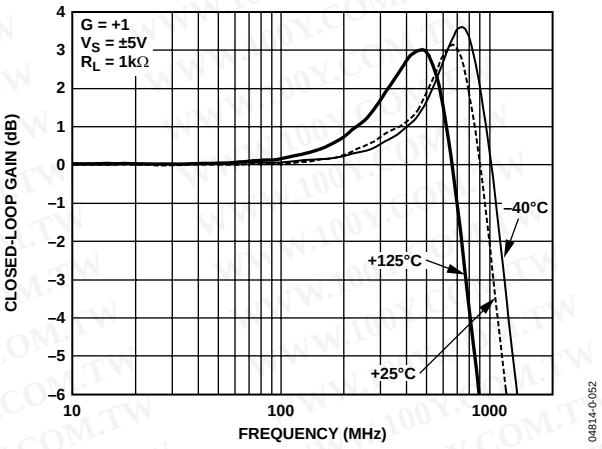

Figure 11. Small Signal Frequency Response for Various Temperatures

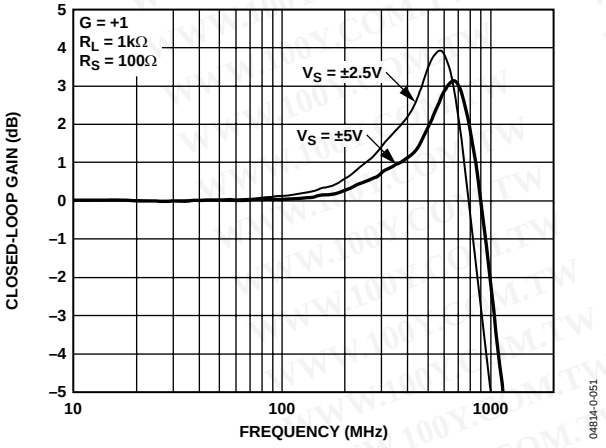

Figure 9. Small Signal Frequency Response for Various Supplies

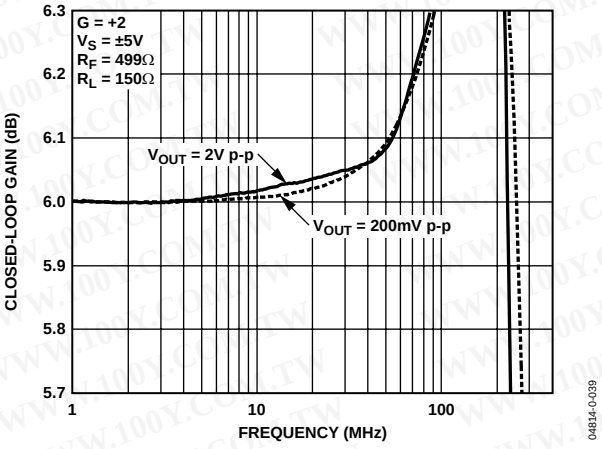

Figure 12. 0.1 dB Flatness vs. Frequency for Various Output Voltages

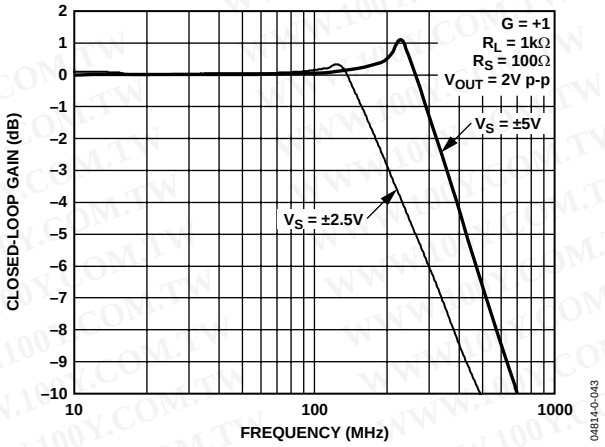

Figure 13. Large Signal Frequency Response for Various Supplies

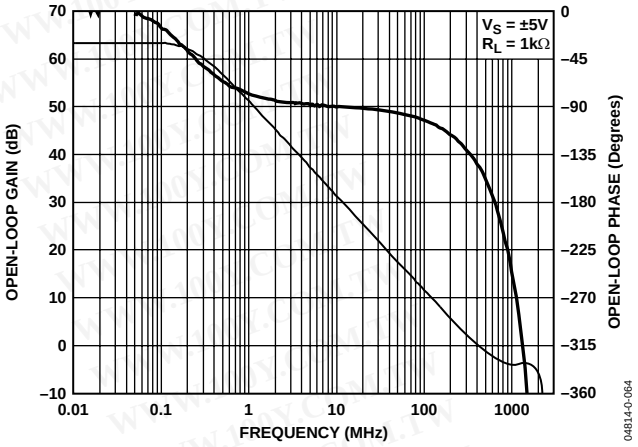

Figure 16. Open-Loop Gain and Phase vs. Frequency

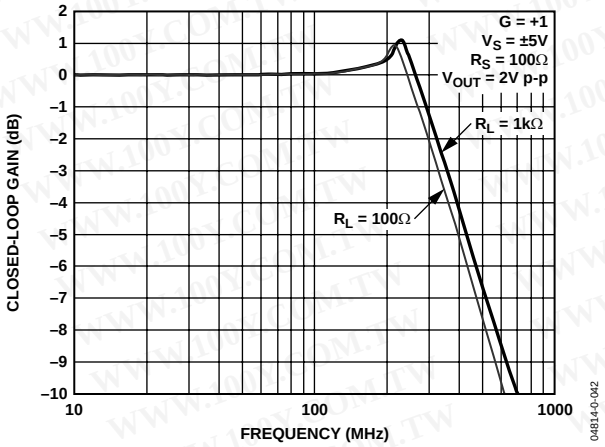

Figure 14. Large Signal Frequency Response for Various Loads

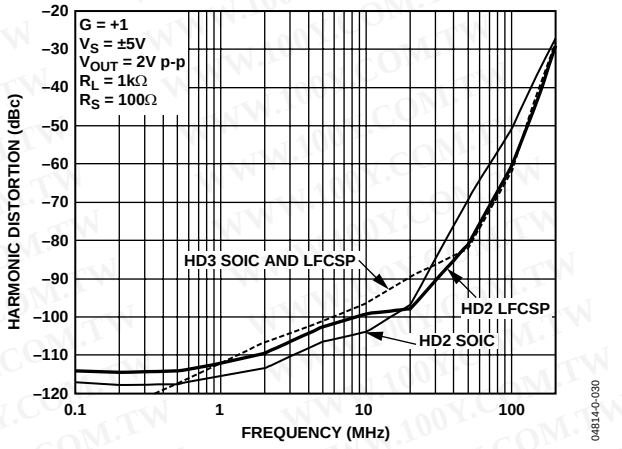

Figure 17. Harmonic Distortion vs. Frequency for Various Packages

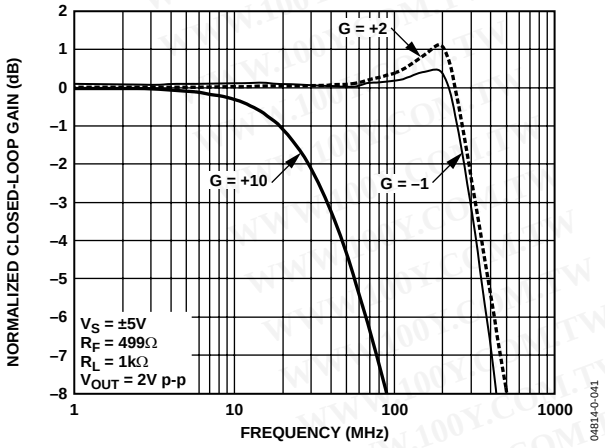

Figure 15. Large Signal Frequency Response for Various Gains

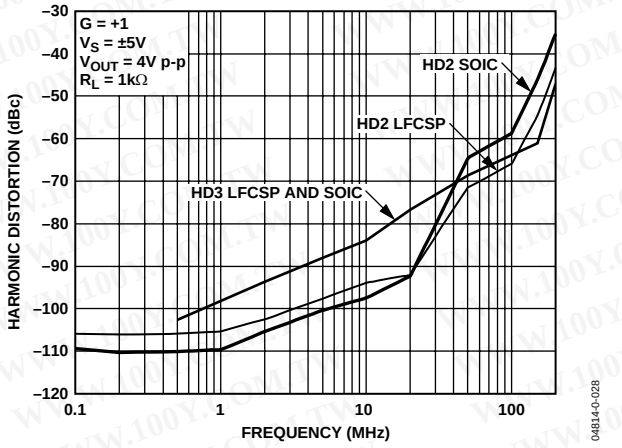

Figure 18. Harmonic Distortion vs. Frequency for Various Packages

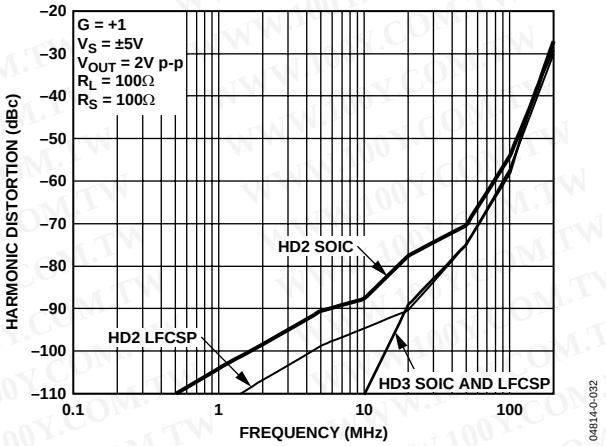

Figure 19. Harmonic Distortion vs. Frequency for Various Packages

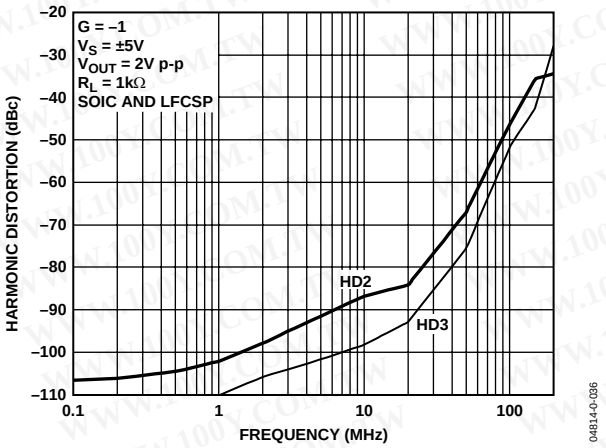

Figure 20. Harmonic Distortion vs. Frequency for Various Packages

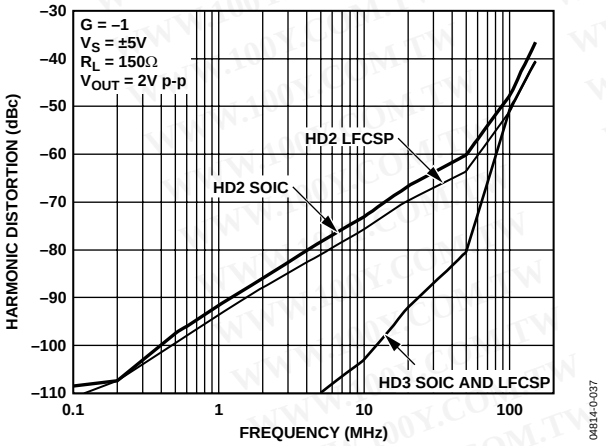

Figure 21. Harmonic Distortion vs. Frequency for Various Packages

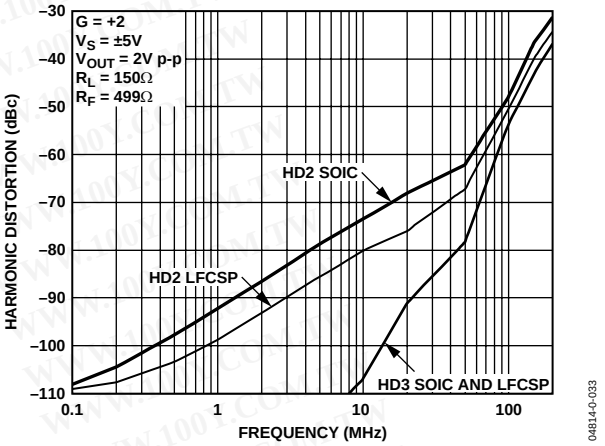

Figure 22. Harmonic Distortion vs. Frequency for Various Packages

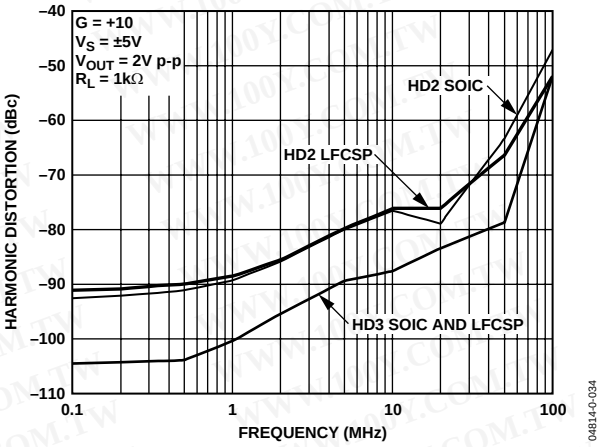

Figure 23. Harmonic Distortion vs. Frequency for Various Packages

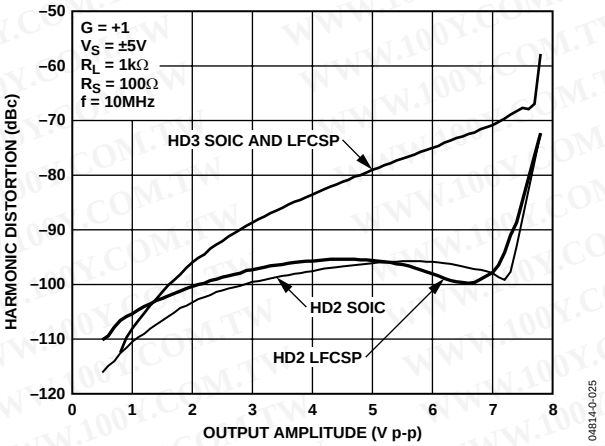

Figure 24. Harmonic Distortion vs. Output Voltage for Various Packages

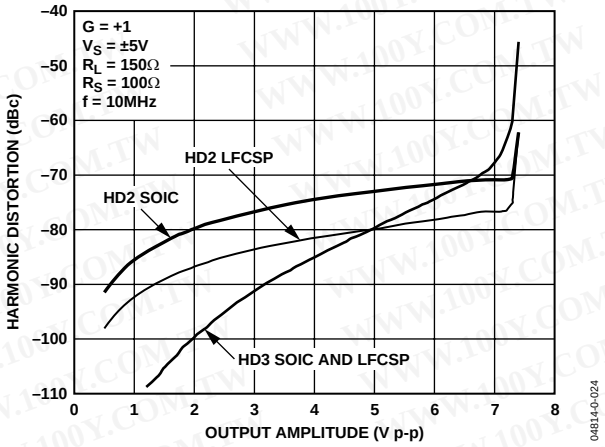

Figure 25. Harmonic Distortion vs. Output Voltage for Various Packages

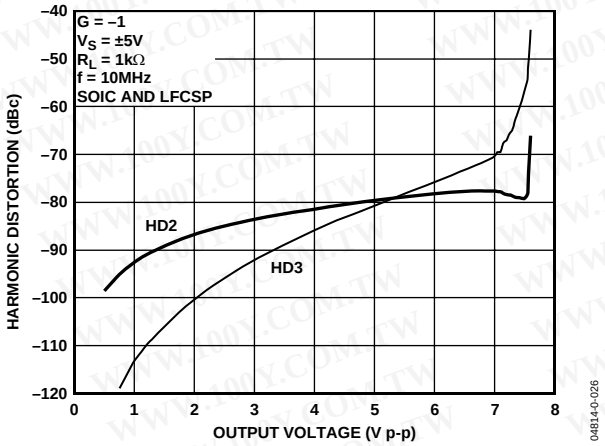

Figure 26. Harmonic Distortion vs. Output Voltage

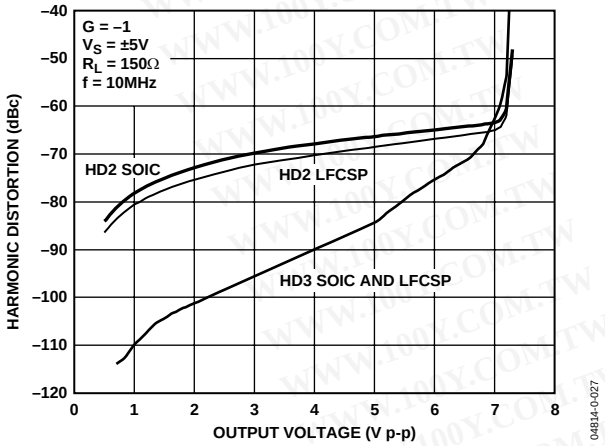

Figure 27. Harmonic Distortion vs. Output Voltage

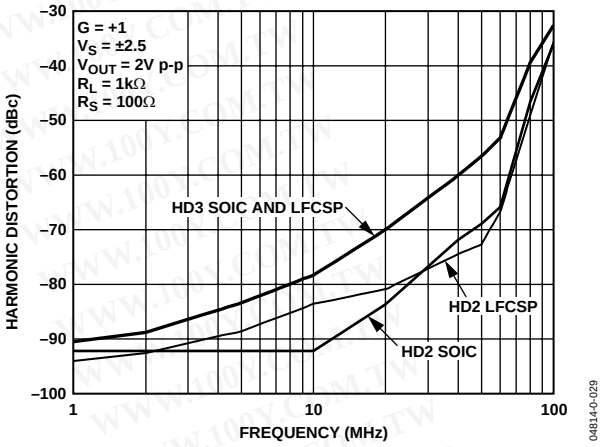

Figure 28. Harmonic Distortion vs. Frequency for Various Packages

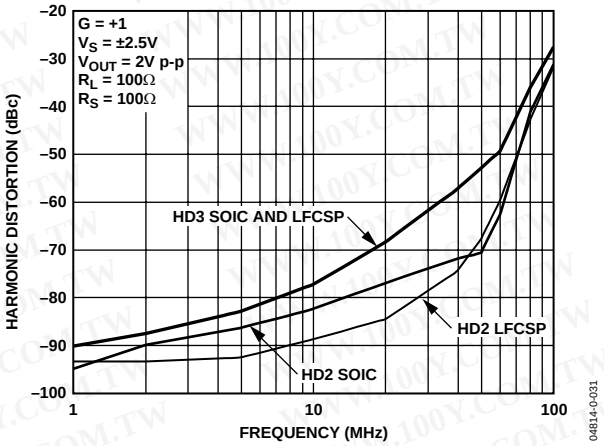

Figure 29. Harmonic Distortion vs. Frequency for Various Packages

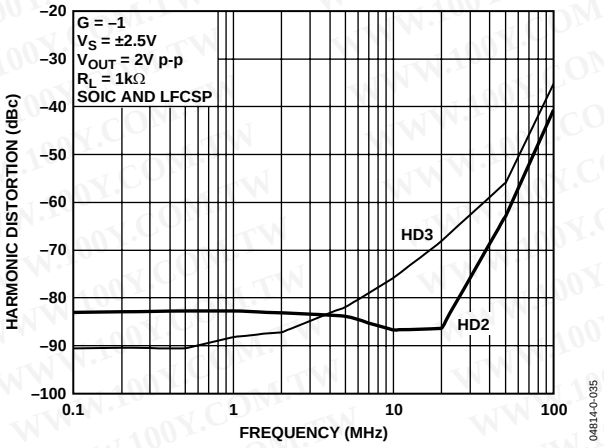

Figure 30. Harmonic Distortion vs. Frequency for Various Packages

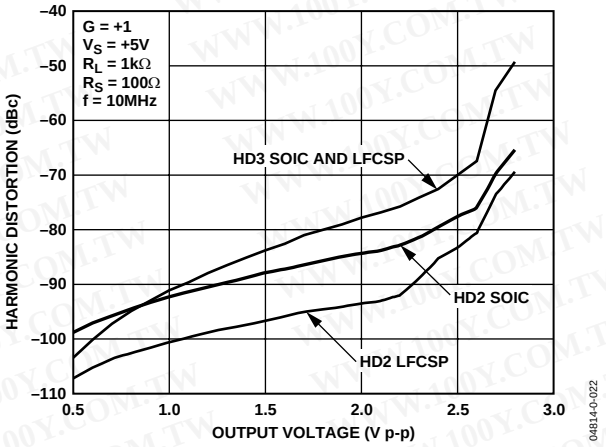

Figure 31. Harmonic Distortion vs. Output Voltage for Various Packages

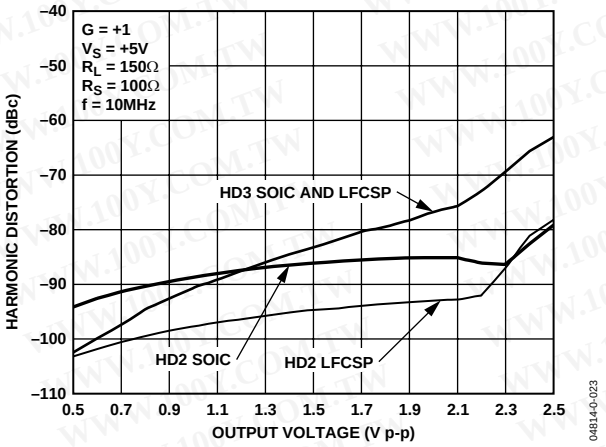

Figure 32. Harmonic Distortion vs. Output Voltage for Various Packages

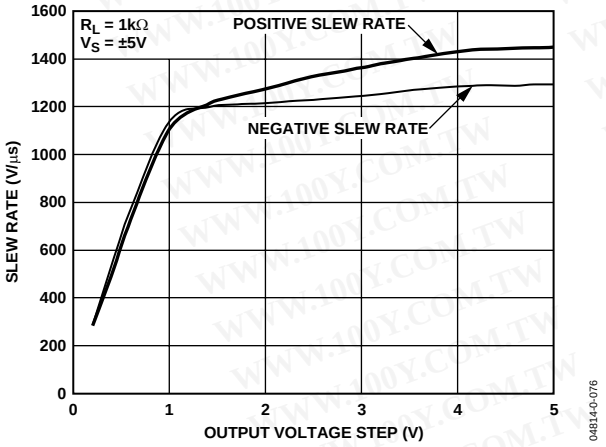

Figure 33. Slew Rate vs. Output Voltage

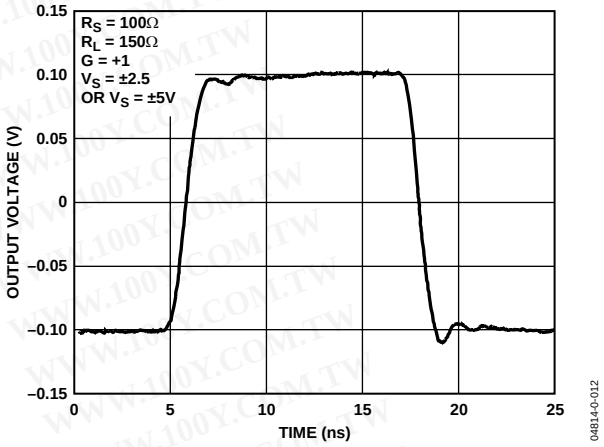

Figure 34. Small Signal Transient Response for Various Supplies and Loads

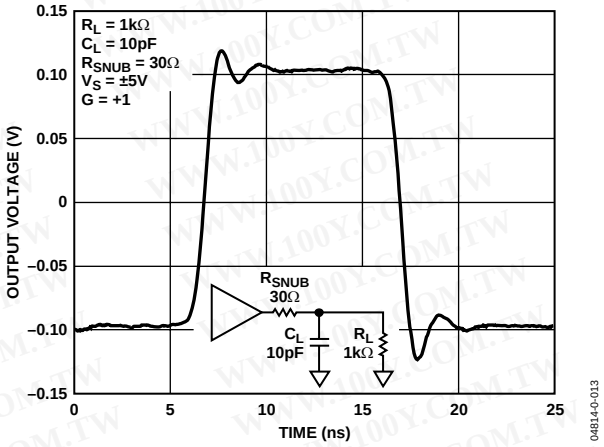

Figure 35. Small Signal Transient Response for Various Supplies and Loads

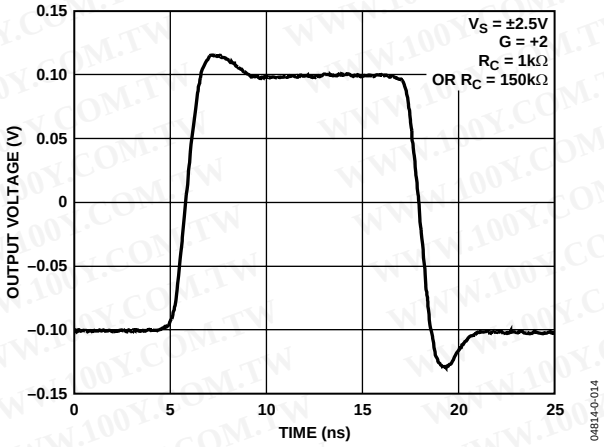

Figure 36. Small Signal Transient Response for Various Loads

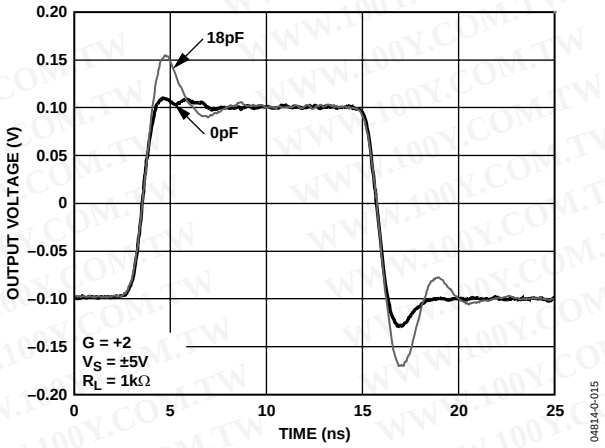

Figure 37. Small Signal Transient Response with Capacitive Load

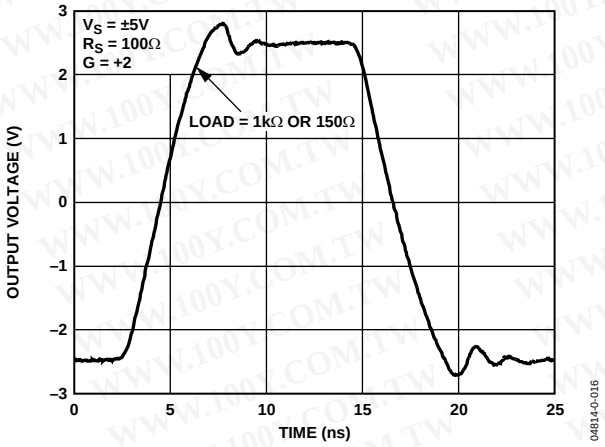

Figure 38. Large Signal Transient Response for Various Loads

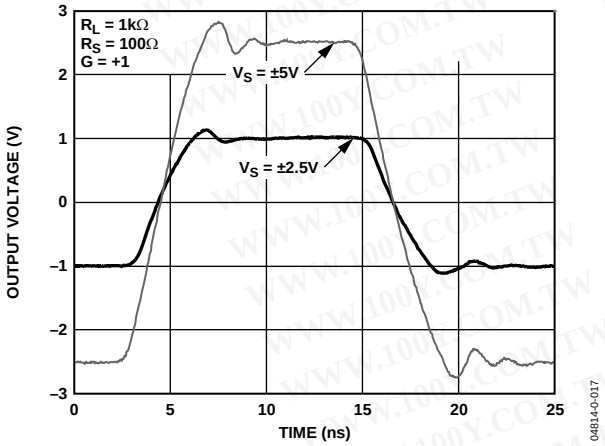

Figure 39. Large Signal Transient Response for Various Supplies

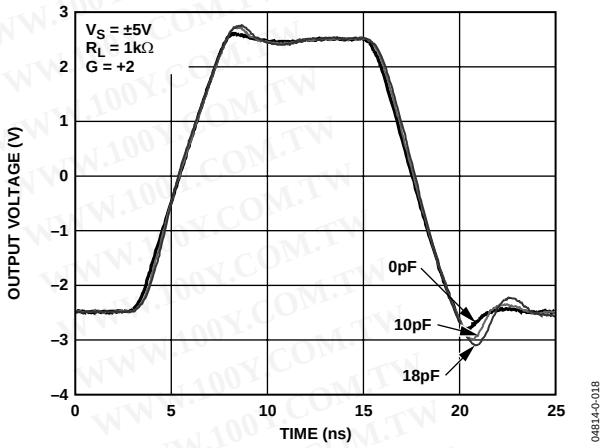

Figure 40. Large Signal Transient Response with Capacitive Load

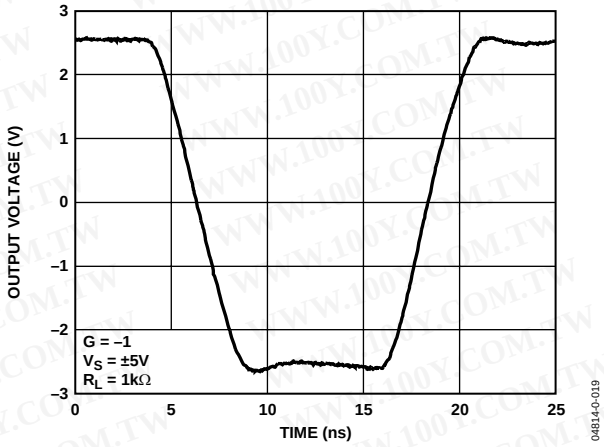

Figure 41. Large Signal Transient Response, Inverting

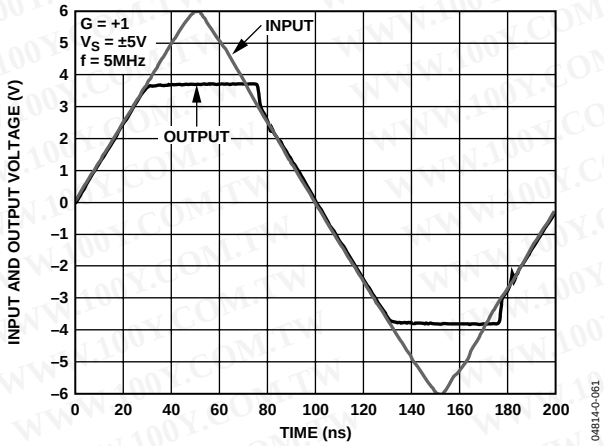

Figure 42. Input Overdrive Recovery

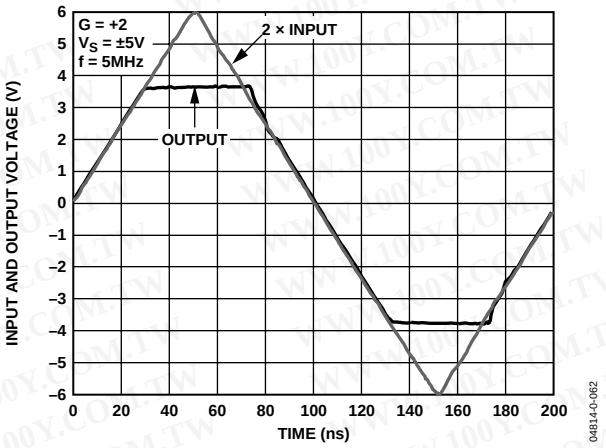

Figure 43. Output Overdrive Recovery

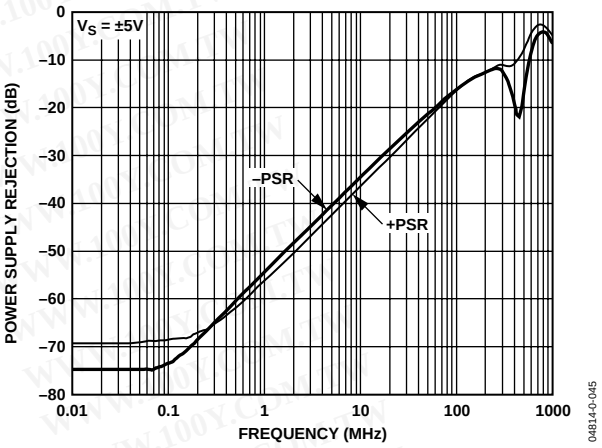

Figure 46. Power Supply Rejection vs. Frequency

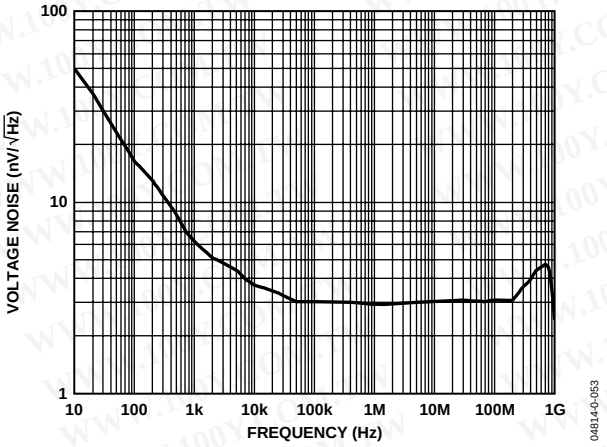

Figure 44. Voltage Noise vs. Frequency

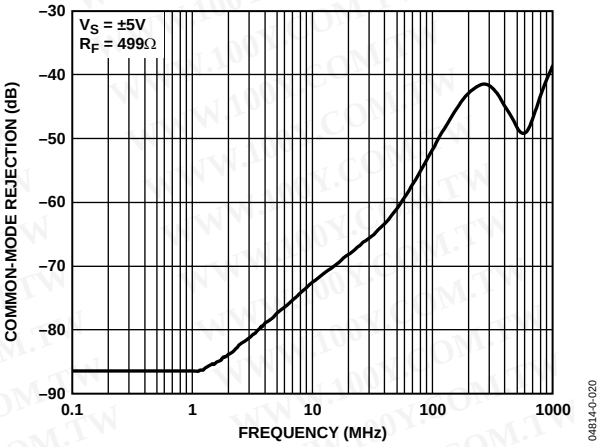

Figure 47. Common-Mode Rejection vs. Frequency

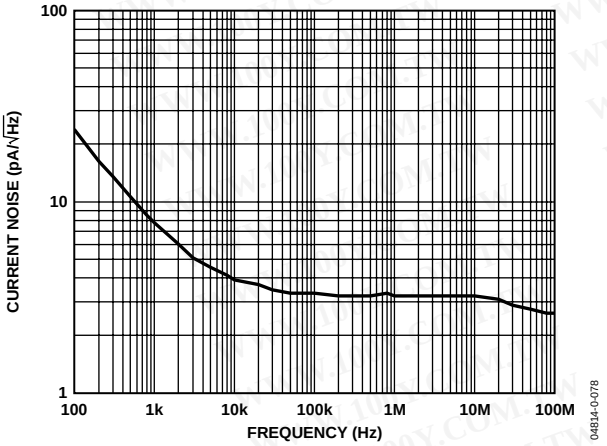

Figure 45. Current Noise vs. Frequency

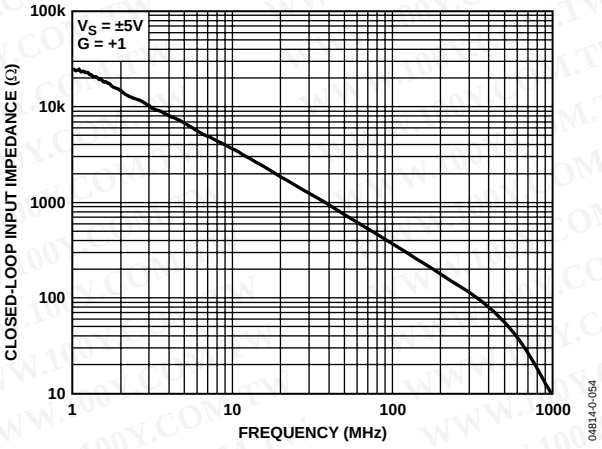

Figure 48. Input Impedance vs. Frequency

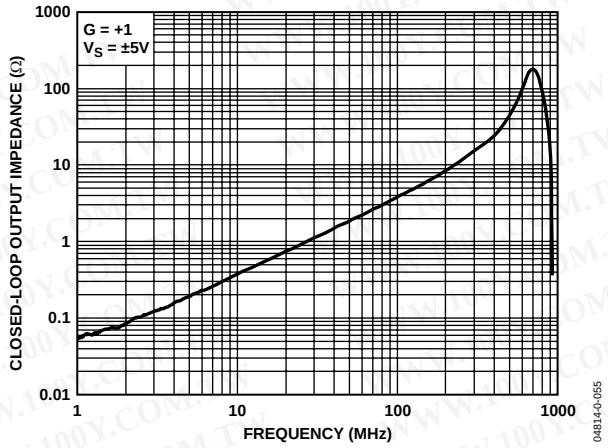

Figure 49. Output Impedance vs. Frequency

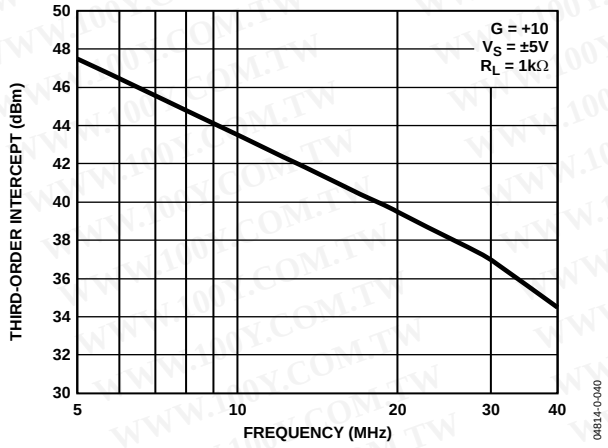

Figure 50. Third-Order Intercept vs. Frequency

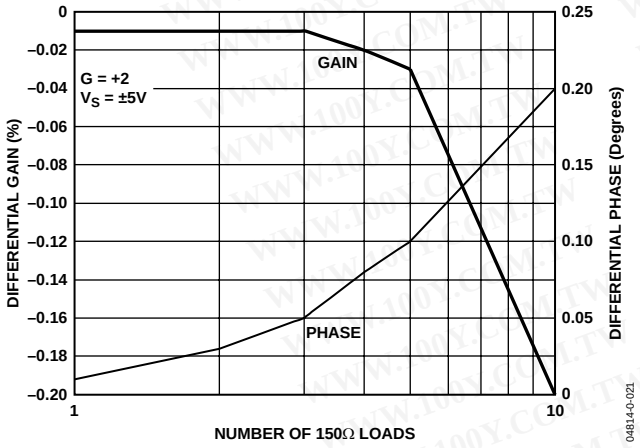

Figure 51. Differential Gain and Phase vs. Number of 150 Ω Loads

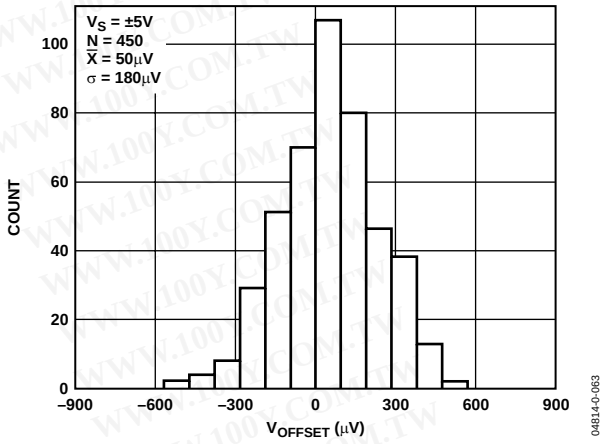

Figure 52. V_{OS} Distribution for V_S = ±5 V

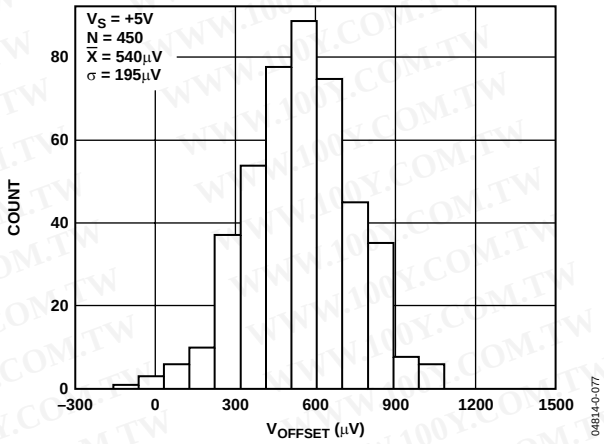

Figure 53. V_{OS} Distribution for V_S = +5 V

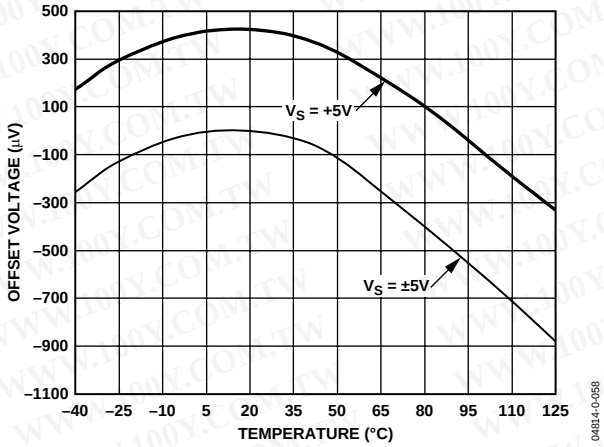

Figure 54. Offset Voltage vs. Temperature for Various Supplies

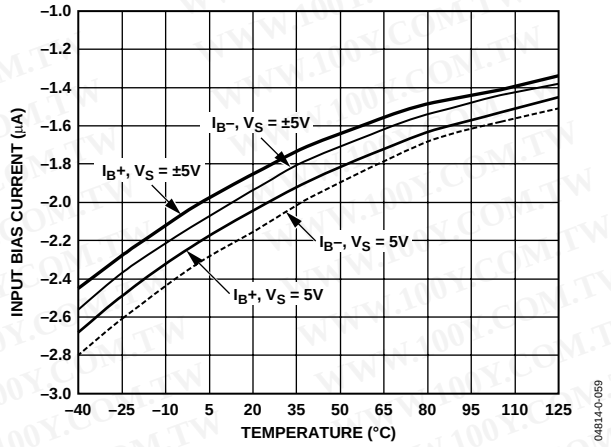

Figure 55. Input Bias Current vs. Temperature for Various Supplies

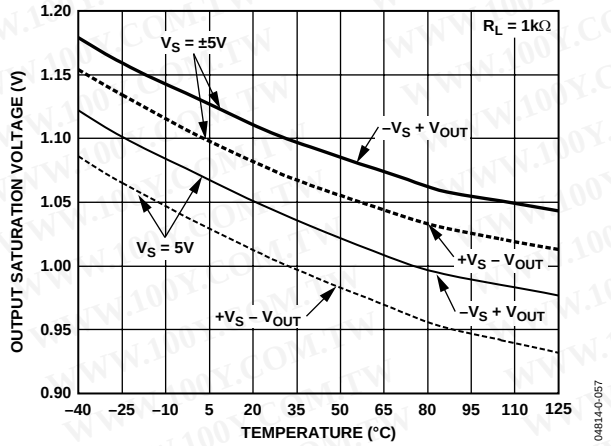

Figure 56. Output Saturation Voltage vs. Temperature for Various Supplies

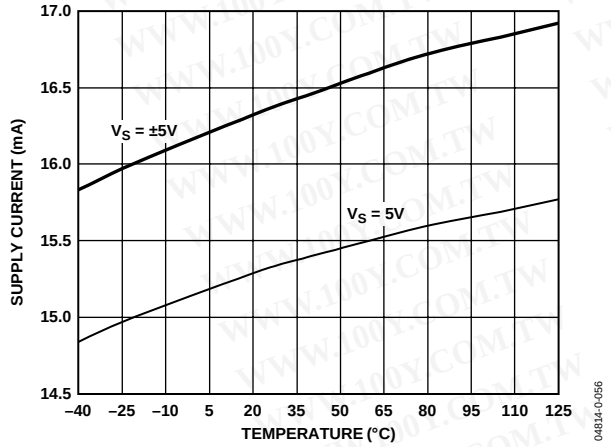

Figure 57. Supply Current vs. Temperature for Various Supplies

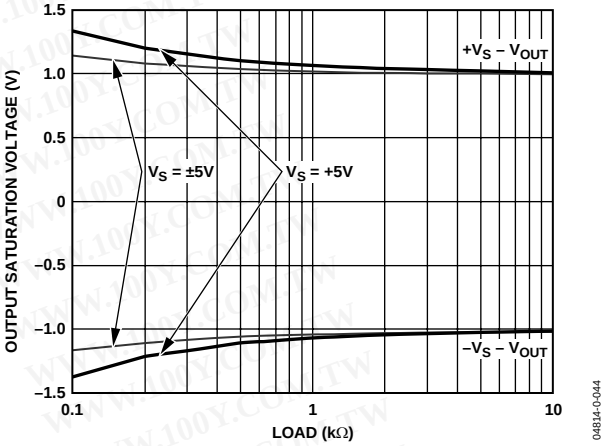

Figure 58. Output Saturation Voltage vs. Load for Various Supplies

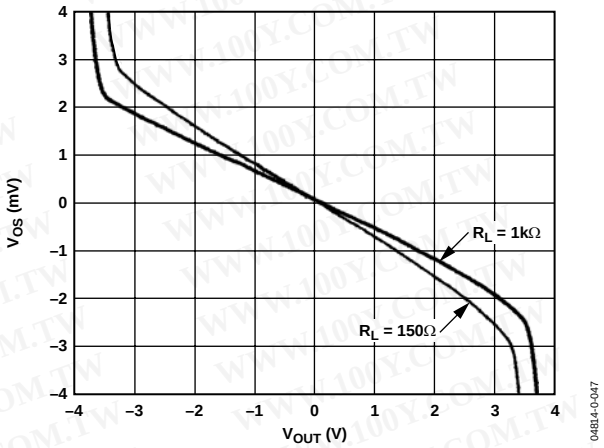

Figure 59. Input Offset Voltage vs. Output Voltage for Various Loads

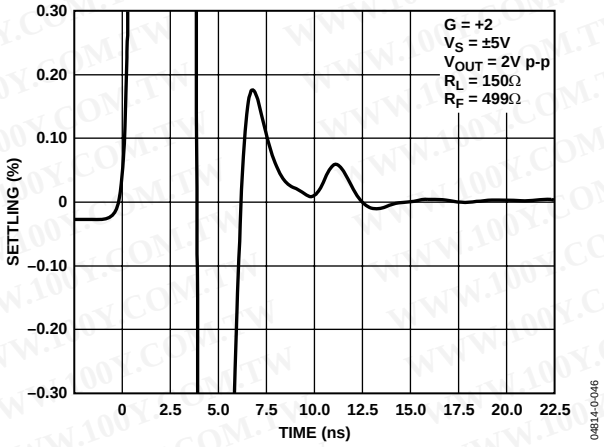

Figure 60. Short Term 0.1% Settling Time

CIRCUIT CONFIGURATIONS

WIDEBAND OPERATION

Figure 61 and Figure 62 show the recommended circuit configurations for noninverting and inverting amplifiers. In unity gain (G = +1) applications, R_S helps to reduce high frequency peaking. It is not needed for any other configurations. For more information on layout, see the Printed Circuit Board Layout section.

The resistor at the output of the amplifier, labeled R_{SNUB}, is used only when driving large capacitive loads. Using R_{SNUB} improves stability and minimizes ringing at the output. For more information, see the Driving Capacitive Loads section.

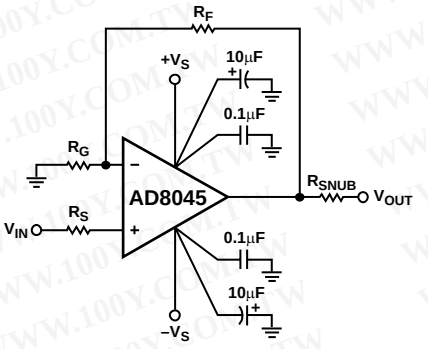

Figure 61. Noninverting Configuration

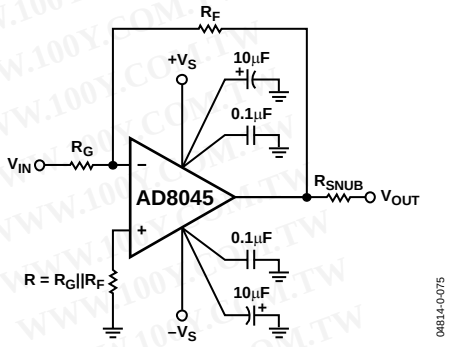

Figure 62. Inverting Configuration

THEORY OF OPERATION

The AD8045 is a high speed voltage feedback amplifier fabricated on ADI's second generation eXtra Fast Complementary Bipolar (XFCB) process. An H-bridge input stage is used to attain a 1400 V/µs slew rate and low distortion in addition to a low 3 nV/√Hz input voltage noise. Supply current and offset voltage are laser trimmed for optimum performance.

FREQUENCY RESPONSE

The AD8045's open-loop response over frequency can be approximated by the integrator response shown in Figure 63.

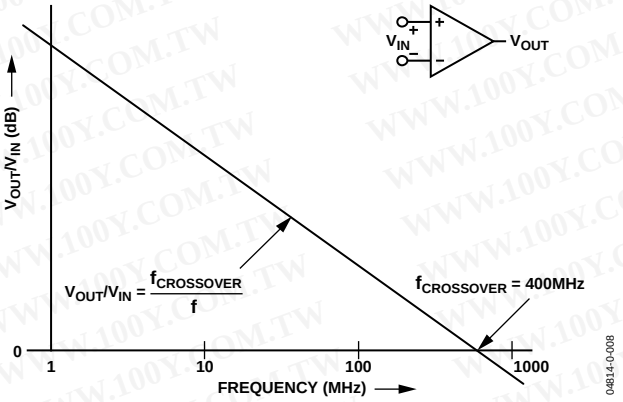

Figure 63. Open-Loop Response

The closed-loop transfer function for the noninverting configuration is shown in Figure 64 and is written as

$$\frac{V_{OUT}}{V_{IN}} = \frac{2\pi \times f_{CROSSOVER} \times (R_G + R_F)}{(R_F + R_G)s + 2\pi \times f_{CROSSOVER} \times R_G}$$

where:

s is $(2\pi j)f$.

$f_{CROSSOVER}$ is the frequency where the amplifier's open-loop gain equals 1 (0 dB).

DC gain is therefore

$$\frac{V_{OUT}}{V_{IN}} = \frac{(R_G + R_F)}{R_G}$$

Closed-loop −3 dB bandwidth equals

$$\frac{V_{OUT}}{V_{IN}} = f_{CROSSOVER} \times \frac{R_G}{(R_G + R_F)}$$

The closed-loop bandwidth is inversely proportional to the noise gain of the op amp circuit, $(R_F + R_G)/R_G$. This simple model can be used to predict the −3 dB bandwidth for noise gains above +2. The actual bandwidth of circuits with noise gains at or below +2 is higher due to the influence of other poles present in the real op amp.

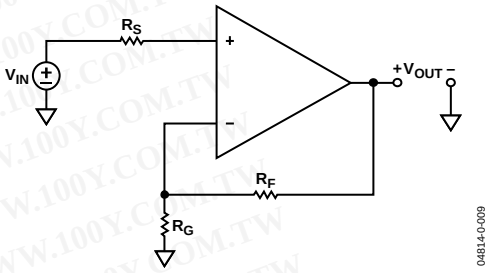

Figure 64. Noninverting Configuration

DC ERRORS

Figure 65 shows the dc error contributions. The total output error voltage is

$$V_{OUT(ERROR)} = -I_{B^+} R_S \left(\frac{R_G + R_F}{R_G}\right) + I_{B^-} R_F + V_{OS} \left(\frac{R_G + R_F}{R_G}\right)$$

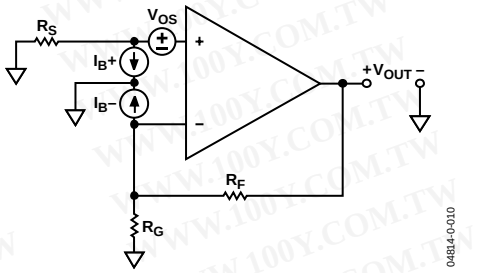

Figure 65. Amplifier DC Errors

The voltage error due to $I_{B}+$ and $I_{B}-$ is minimized if $R_S = R_F||R_G$. To include the effects of common-mode and power supply rejection, model V_{OS} as

$$V_{OS} = V_{OS_{nom}} + \frac{\Delta V_S}{PSR} + \frac{\Delta V_{CM}}{CMR}$$

where:

$V_{os_{nom}}$ is the offset voltage at nominal conditions.

ΔV_S is the change in the power supply voltage from nominal conditions.

PSR is the power supply rejection.

C*MR* is the common-mode rejection.

ΔV_{CM} is the change in common-mode voltage from nominal conditions.

OUTPUT NOISE

Figure 66 shows the contributors to the noise at the output of a noninverting configuration.

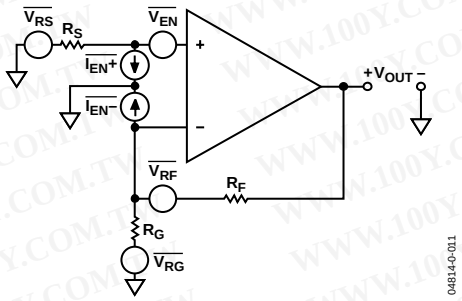

Figure 66. Amplifier DC Errors

$\overline{Ven}$, $\overline{\text{IN+}}$, and $\overline{\text{IN–}}$ are due to the amplifier. V_{R_F}, V_{R_G}, and V_{R_S} are due to the feedback network resistors. R_G and R_F, and source resistor, R_S. Total output voltage noise, $\overline{V_{OUT\_EN}}$, is the rms sum of all the contributions.

$$\overline{V_{OUT\_EN}} = \sqrt{(G_n \times \overline{Ven})^2 + (\overline{IN+} \times R_S \times G_n)^2 + (\overline{IN-} \times R_F \| R_G \times G_n)^2 + 4kTR_f + 4kTR_G(G_n)^2 + 4kTR_S(G_n)^2}$$

where:

G_n is the noise gain $\left(\frac{R_F + R_G}{R_G}\right)$.

$\overline{Ven}$ is the op amp input voltage noise.

$\overline{IN}$ is the op amp input current noise.

Table 7 lists the expected output voltage noise spectral density for several gain configurations.

Table 7. Noise and Bandwidth for Various Gains

Gain	R_F	R_G	R_S	–3 dB Bandwidth[1]	Output Noise (nV/√Hz)
+1	0	–	100	1 GHz	3.3
+2	499	499	0	400 MHz	7.4
+5	499	124	0	90 MHz	16.4
+10	499	56	0	40 MHz	31
–1	499	499	N/A	300 MHz	7.4

[1] R_L = 1 kΩ.

APPLICATIONS

LOW DISTORTION PINOUT

The AD8045 LFCSP package features Analog Devices new low distortion pinout. The new pinout provides two advantages over the traditional pinout. First, improved second harmonic distortion performance, which is accomplished by the physical separation of the noninverting input pin and the negative power supply pin. Second, the simplification of the layout due to the dedicated feedback pin and easy routing of the gain set resistor back to the inverting input pin. This allows a compact layout, which helps to minimize parasitics and increase stability.

The traditional SOIC pinout has been slightly modified as well to incorporate a dedicated feedback pin. Pin 1, previously a no connect pin on the amplifier, is now a dedicated feedback pin. The new pinout reduces parasitics and simplifies the board layout.

Existing applications that use the traditional SOIC pinout can take full advantage of the outstanding performance offered by the AD8045. An electrical insulator may be required if the SOIC rests on the ground plane or other metal trace. This is covered in more detail in the Exposed Paddle section of this data sheet. In existing designs, which have Pin 1 tied to ground or to another potential, simply lift Pin 1 of the AD8045 or remove the potential on the Pin 1 solder pad. The designer does not need to use the dedicated feedback pin to provide feedback for the AD8045. The output pin of the AD8045 can still be used to provide feedback to the inverting input of the AD8045.

HIGH SPEED ADC DRIVER

When used as an ADC driver, the AD8045 offers results comparable to transformers in distortion performance. Many ADC applications require that the analog input signal be dc-coupled and operate over a wide frequency range. Under these requirements, operational amplifiers are very effective interfaces to ADCs. An op amp interface provides the ability to amplify and level shift the input signal to be compatible with the input range of the ADC. Unlike transformers, operational amplifiers can be operated over a wide frequency range down to and including dc.

Figure 67 shows the AD8045 as a dc-coupled differential driver for the AD9244, a 14-bit 65 MSPS ADC. The two amplifiers are configured in noninverting and inverting modes. Both amplifiers are set with a noise gain of +2 to provide better bandwidth matching. The inverting amplifier is set for a gain of –1, while the noninverting is set for a gain of +2. The noninverting input is divided by 2 in order to normalize its output and make it equal to the inverting output.

This dc-coupled differential driver is best suited for ±5 V operation in which optimum distortion performance is required and the input signal is ground referenced.

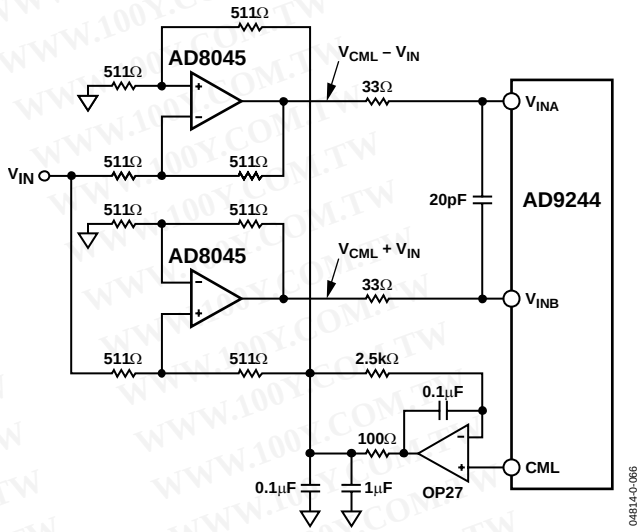

Figure 67. High Speed ADC Driver

The outputs of the AD8045s are centered about the AD9244's common-mode range of 2.5 V. The common-mode reference voltage from the AD9244 is buffered and filtered via the OP27 and fed to the noninverting resistor network used in the level shifting circuit.

The spurious-free dynamic range (SFDR) performance is shown in Figure 68. Figure 69 shows a 50 MHz single-tone FFT performance.

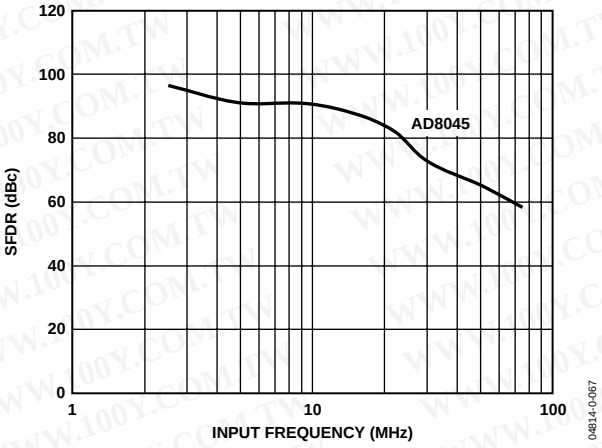

Figure 68. SFDR vs. Frequency

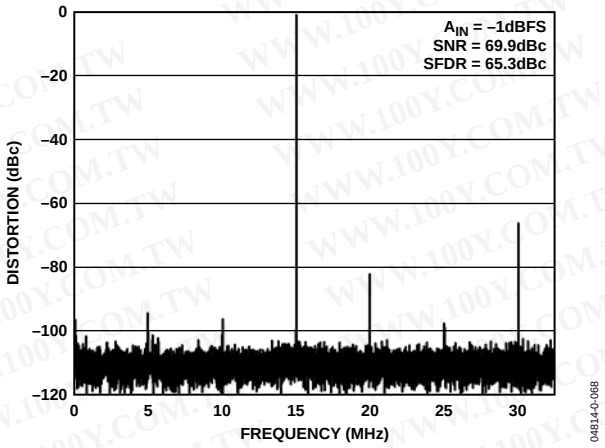

Figure 69. Single-Tone FFT, F_{IN} = 50 MHz, Sample Rate = 65 MSPS Shown in the First Nyquist Zone

90 MHZ ACTIVE LOW-PASS FILTER (LPF)

Active filters are used in many applications such as antialiasing filters and high frequency communication IF strips.

With a 400 MHz gain bandwidth product and high slew rate, the AD8045 is an ideal candidate for active filters. Figure 70 shows the frequency response of the 90 MHz LPF. In addition to the bandwidth requirements, the slew rate must be capable of supporting the full power bandwidth of the filter. In this case, a 90 MHz bandwidth with a 2 V p-p output swing requires at least 1200 V/µs. This performance is achievable only at 90 MHz because of the AD8045's wide bandwidth and high slew rate.

The circuit shown in Figure 73 is a 90 MHz, 4-pole, Sallen-Key, LPF. The filter comprises two identical cascaded Sallen-Key LPF sections, each with a fixed gain of G = +2. The net gain of the filter is equal to G = +4 or 12 dB. The actual gain shown in Figure 70 is only 6 dB. This is due to the output voltage being divided in half by the series matching termination resistor, R_T, and the load resistor.

Setting the resistors and capacitors equal to each other greatly simplifies the design equations for the Sallen-Key filter. The corner frequency, or −3 dB frequency, can be described by the equation

$$f_c = \frac{1}{2\pi RC}$$

The quality factor, or *Q*, is shown in the equation

$$Q = \frac{1}{3-K}$$

The gain, or *K*, of the circuits are

$$First\ Stage\ K = \frac{R3}{R4} + 1,\ Second\ Stage\ K = \frac{R8}{R7} + 1$$

Resistor values are kept low for minimal noise contribution, offset voltage, and optimal frequency response. Due to the low capacitance values used in the filter circuit, the PCB layout and minimization of parasitics is critical. A few picofarads can detune the filters corner frequency, f_c. The capacitor values shown in Figure 73 actually incorporate some stray PCB capacitance.

Capacitor selection is critical for optimal filter performance. Capacitors with low temperature coefficients, such as NPO ceramic capacitors and silver mica, are good choices for filter elements.

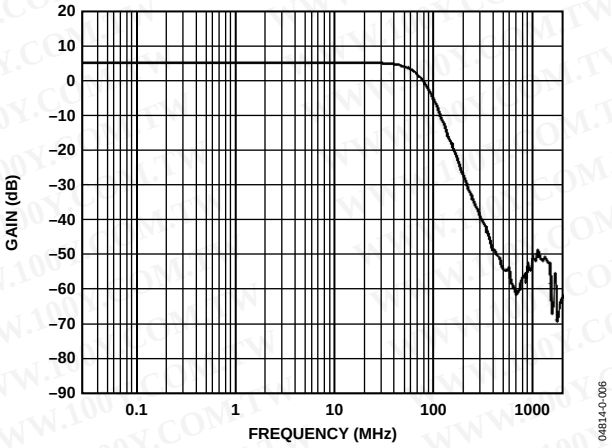

Figure 70. 90 MHz Low-Pass Filter Response

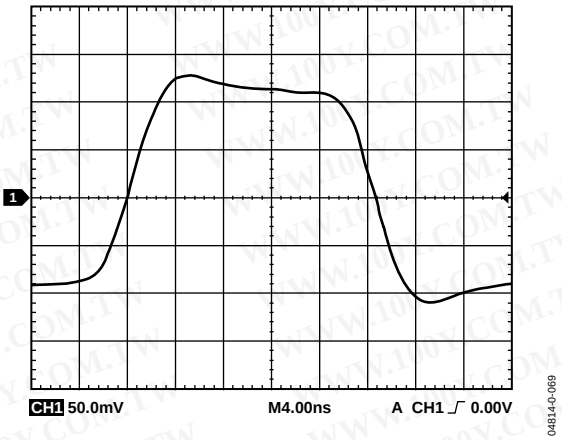

Figure 71. Small Signal Transient Response of 90 MHz LPF

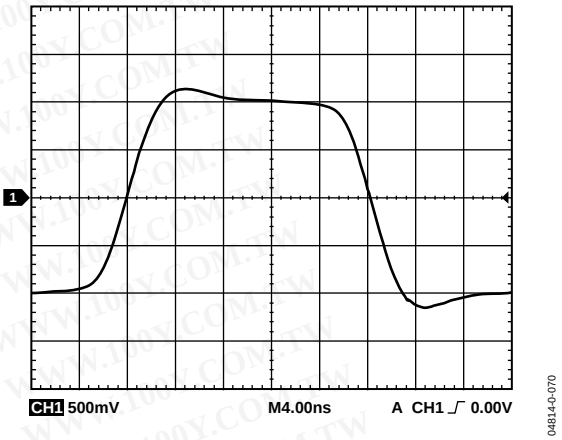

Figure 72. Large Signal Transient Response of 90 MHz LPF

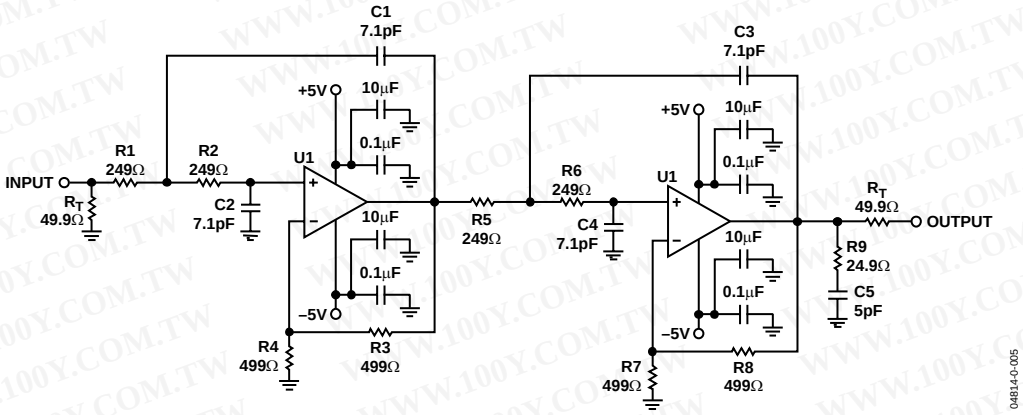

Figure 73. 4-Pole, 90 MHz, Sallen-Key Low-Pass Filter

PRINTED CIRCUIT BOARD LAYOUT

Laying out the printed circuit board (PCB) is usually the last step in the design process and often proves to be one of the most critical. A brilliant design can be rendered useless because of a poor or sloppy layout. Since the AD8045 can operate into the RF frequency spectrum, high frequency board layout considerations must be taken into account. The PCB layout, signal routing, power supply bypassing, and grounding all must be addressed to ensure optimal performance.

SIGNAL ROUTING

The AD8045 LFCSP features the new low distortion pinout with a dedicated feedback pin and allows a compact layout. The dedicated feedback pin reduces the distance from the output to the inverting input, which greatly simplifies the routing of the feedback network.

When laying out the AD8045 as a unity gain amplifier, it is recommended that a short, but wide, trace between the dedicated feedback pin and the inverting input to the amplifier be used to minimize stray parasitic inductance.

To minimize parasitic inductances, ground planes should be used under high frequency signal traces. However, the ground plane should be removed from under the input and output pins to minimize the formation of parasitic capacitors, which degrades phase margin. Signals that are susceptible to noise pickup should be run on the internal layers of the PCB, which can provide maximum shielding.

POWER SUPPLY BYPASSING

Power supply bypassing is a critical aspect of the PCB design process. For best performance, the AD8045 power supply pins need to be properly bypassed.

A parallel connection of capacitors from each of the power supply pins to ground works best. Paralleling different values and sizes of capacitors helps to ensure that the power supply pins "see" a low ac impedance across a wide band of frequencies. This is important for minimizing the coupling of noise into the amplifier. Starting directly at the power supply pins, the smallest value and sized component should be placed on the same side of the board as the amplifier, and as close as possible to the amplifier, and connected to the ground plane. This process should be repeated for the next larger value capacitor. It is recommended for the AD8045 that a 0.1 µF ceramic 0508 case be used. The 0508 offers low series inductance and excellent high frequency performance. The 0.1 µF case provides low impedance at high frequencies. A 10 µF electrolytic capacitor should be placed in parallel with the 0.1 µF. The 10 µf capacitor provides low ac impedance at low frequencies. Smaller values of electrolytic capacitors may be used depending on the circuit requirements. Additional smaller value capacitors help to provide a low impedance path for unwanted noise out to higher frequencies but are not always necessary.

Placement of the capacitor returns (grounds), where the capacitors enter into the ground plane, is also important. Returning the capacitors grounds close to the amplifier load is critical for distortion performance. Keeping the capacitors distance short, but equal from the load, is optimal for performance.

In some cases, bypassing between the two supplies can help to improve PSRR and to maintain distortion performance in crowded or difficult layouts. It is brought to the designer's attention here as another option to improve performance.

Minimizing the trace length and widening the trace from the capacitors to the amplifier reduce the trace inductance. A series inductance with the parallel capacitance can form a tank circuit, which can introduce high frequency ringing at the output. This additional inductance can also contribute to increased distortion due to high frequency compression at the output. The use of vias should be minimized in the direct path to the amplifier power supply pins since vias can introduce parasitic inductance, which can lead to instability. When required, use multiple large diameter vias because this lowers the equivalent parasitic inductance.

GROUNDING

The use of ground and power planes is encouraged as a method of proving low impedance returns for power supply and signal currents. Ground and power planes can also help to reduce stray trace inductance and to provide a low thermal path for the amplifier. Ground and power planes should not be used under any of the pins of the AD8045. The mounting pads and the ground or power planes can form a parasitic capacitance at the amplifiers input. Stray capacitance on the inverting input and the feedback resistor form a pole, which degrades the phase margin, leading to instability. Excessive stray capacitance on the output also forms a pole, which degrades phase margin.

EXPOSED PADDLE

The AD8045 features an exposed paddle, which lowers the thermal resistance by 25% compared to a standard SOIC plastic package. The exposed paddle of the AD8045 is internally connected to the negative power supply pin. Therefore, when laying out the board, the exposed paddle must either be connected to the negative power supply or left floating (electrically isolated). Soldering the exposed paddle to the negative power supply metal ensures maximum thermal transfer. Figure 74 and Figure 75 show the proper layout for connecting the SOIC and LFCSP exposed paddle to the negative supply.

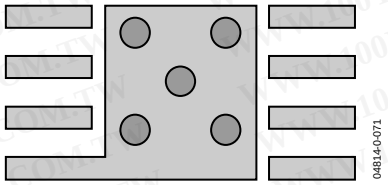

Figure 74. SOIC Exposed Paddle Layout

The use of thermal vias or "heat pipes" can also be incorporated into the design of the mounting pad for the exposed paddle. These additional vias help to lower the overall theta junction to ambient (θ_{JA}). Using a heavier weight copper on the surface to which the amplifier's exposed paddle is soldered can greatly reduce the overall thermal resistance "seen" by the AD8045.

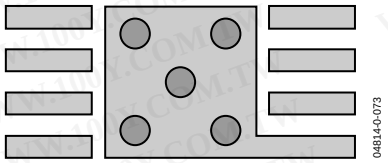

Figure 75. LFCSP Exposed Paddle Layout

For existing designs that want to incorporate the AD8045, electrically isolating the exposed paddle is another option. If the exposed paddle is electrically isolated, the thermal dissipation is primarily through the leads, and the thermal resistance of the package now approaches 125°C/W, the standard SOIC θ_{JA}. However, a thermally conductive and electrically isolated pad material may be used. A thermally conductive spacer, such as the Bergquist Company's Sil-Pad, is an excellent solution to this problem. Figure 76 shows a typical implementation using thermal pad material.

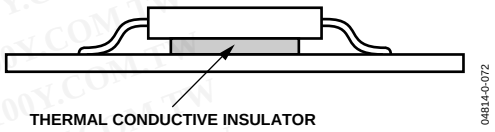

Figure 76. SOIC with Thermal Conductive Pad Material

The thermal pad provides high thermal conductivity but isolates the exposed paddle from ground or other potential. It is recommended, when possible, to solder the paddle to the negative power supply plane or trace for maximum thermal transfer.

Note that soldering the paddle to ground shorts the negative power supply to ground and can cause irreparable damage to the AD8045.

DRIVING CAPACITIVE LOADS

In general, high speed amplifiers have a difficult time driving capacitive loads. This is particularly true in low closed-loop gains, where the phase margin is the lowest. The difficulty arises because the load capacitance, C_L, forms a pole with the output resistance, R_O, of the amplifier. The pole can be described by the equation

$$f_P = \frac{1}{2\pi R_O C_L}$$

If this pole occurs too close to the unity gain crossover point, the phase margin degrades. This is due to the additional phase loss associated with the pole.

The AD8045 output can drive 18 pF of load capacitance directly, in a gain of +2 with 30% overshoot, as shown in Figure 37. Larger capacitance values can be driven but must use a snubbing resistor (R_{SNUB}) at the output of the amplifier, as shown in Figure 61 and Figure 62. Adding a small series resistor, R_{SNUB}, creates a zero that cancels the pole introduced by the load capacitance. Typical values for R_{SNUB} can range from 25 Ω to 50 Ω. The value is typically arrived at empirically and based on the circuit requirements.

OUTLINE DIMENSIONS

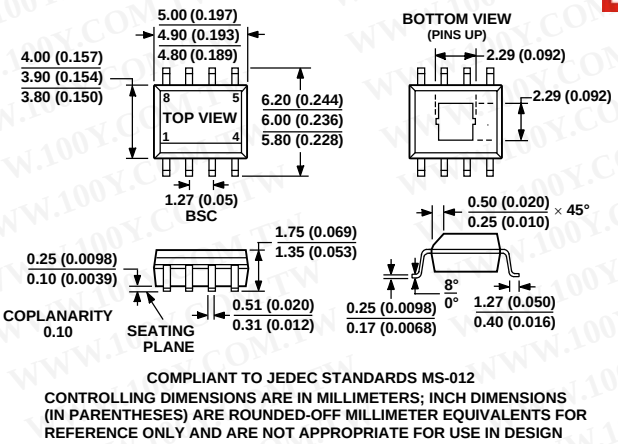

Figure 77. 8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP], Narrow Body (RD-8-1)—Dimensions shown in millimeters and (inches)

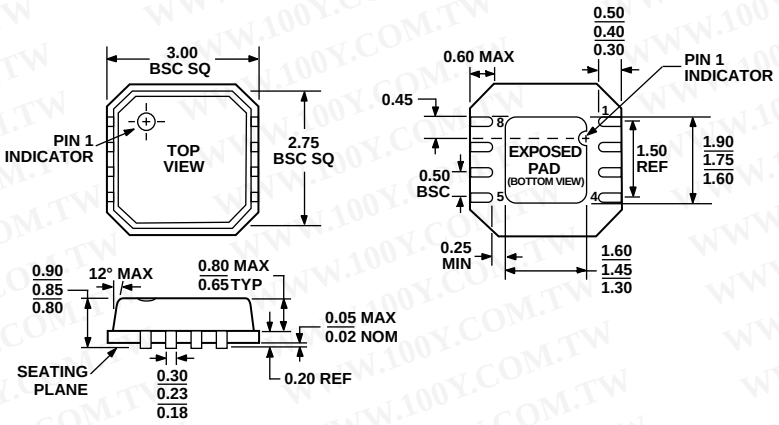

Figure 78. 8-Lead Lead Frame Chip Scale Package [LFCSP], 3 mm × 3 mm Body (CP-8-2)—Dimensions shown in millimeters

ORDERING GUIDE

Model	Minimum Ordering Quantity	Temperature Range	Package Description	Package Option	Branding
AD8045ARD	1	–40°C to +125°C	8-Lead SOIC_N_EP	RD-8-1	
AD8045ARD-REEL	2,500	–40°C to +125°C	8-Lead SOIC_N_EP	RD-8-1	
AD8045ARD-REEL7	1,000	–40°C to +125°C	8-Lead SOIC_N_EP	RD-8-1	
AD8045ARDZ[1]	1	–40°C to +125°C	8-Lead SOIC_N_EP	RD-8-1	
AD8045ARDZ-REEL[1]	2,500	–40°C to +125°C	8-Lead SOIC_N_EP	RD-8-1	
AD8045ARDZ-REEL7[1]	1,000	–40°C to +125°C	8-Lead SOIC_N_EP	RD-8-1	
AD8045ACP-R2	250	–40°C to +125°C	8-Lead LFCSP	CP-8-2	H8B
AD8045ACP-REEL	5,000	–40°C to +125°C	8-Lead LFCSP	CP-8-2	H8B
AD8045ACP-REEL7	1,500	–40°C to +125°C	8-Lead LFCSP	CP-8-2	H8B
AD8045ACPZ-R2[1]	250	–40°C to +125°C	8-Lead LFCSP	CP-8-2	H8B
AD8045ACPZ-REEL[1]	5,000	–40°C to +125°C	8-Lead LFCSP	CP-8-2	H8B
AD8045ACPZ-REEL7[1]	1,500	–40°C to +125°C	8-Lead LFCSP	CP-8-2	H8B

[1] Z = Pb-free part.

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