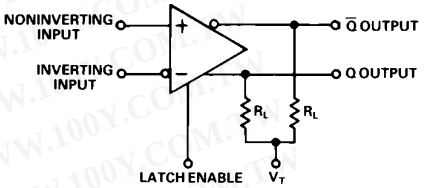
Ultrafast Comparators

AD96685/AD96687

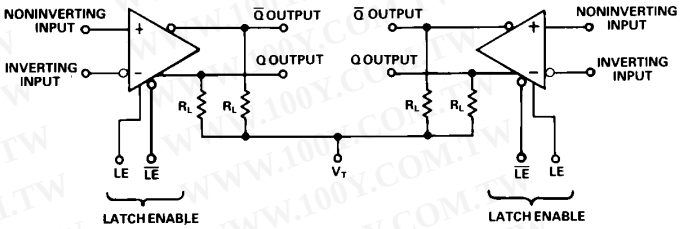
FEATURES
Fast: 2.5 ns Propagation Delay
Low Power: 118 mW per Comparator
Packages: DIP, TO-100, SOIC, PLCC
Power Supplies: +5 V, –5.2 V
Logic Compatibility: ECL
MIL-STD-883 Versions Available
50 ps Delay Dispersion

APPLICATIONS
High Speed Triggers
High Speed Line Receivers
Threshold Detectors
Window Comparators
Peak Detectors

AD96685 FUNCTIONAL BLOCK DIAGRAM



AD96687 FUNCTIONAL BLOCK DIAGRAM



THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50Ω – 200Ω CONNECTED TO –2.0V, OR 200Ω – 2000Ω

GENERAL DESCRIPTION

The AD96685 and AD96687 are ultrafast voltage comparators. The AD96685 is a single comparator with 2.5 ns propagation delay; the AD96687 is an equally fast dual comparator. Both devices feature 50 ps propagation delay dispersion which is a particularly important characteristic of high speed comparators. It is a measure of the difference in propagation delay under differing overdrive conditions.

A fast, high precision differential input stage permits consistent propagation delay with a wide variety of signals in the common-mode range from –2.5 V to +5 V. Outputs are complementary digital signals fully compatible with ECL 10 K and 10 KH logic families. The outputs provide sufficient drive current to directly drive transmission lines terminated in 50 Ω to –2 V. A level sensitive latch input is included which permits tracking, track-hold, or sample-hold modes of operation.

The AD96685 and AD96687 are available in both industrial, –25°C to +85°C, and military temperature ranges. Industrial range devices are available in 16-pin DIP, SOIC, and 20-lead PLCC; additionally, the AD96685 is available in a 10-pin, TO-100 metal can.

REV. C

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

AD96685/AD96687–SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) . . . . . +6.5 V
Negative Supply Voltage ($-V_S$) . . . . . –6.5 V
Input Voltage Range[2] . . . . . ±5 V
Differential Input Voltage . . . . . 5.5 V
Latch Enable Voltage . . . . . $-V_S$ to 0 V
Output Current . . . . . 30 mA
Operating Temperature Range[3]
AD96685/87/BH/BQ/BP/BR . . . . . –25°C to +85°C
AD96685/87/TQ . . . . . –55°C to +125°C
Storage Temperature Range . . . . . –55°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering Temperature (10 sec) . . . . . +300°C

EXPLANATION OF TEST LEVELS

Test Level
I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C; 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ELECTRICAL CHARACTERISTICS (Positive Supply Voltage = +5.0 V; Negative Supply Voltage = –5.2 V, unless otherwise noted)

			Industrial Temp. Range –25°C to +85°C						Military Temp. Range –55°C to +125°C						
			AD96685BH/BQ/BP/BR			AD96687BQ/BP/BR			AD96685TQ			AD96687TQ			
Parameter	Temp	Test Level	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
INPUT CHARACTERISTICS															
Input Offset Voltage[4]	+25°C	I		1	2		1	2		1	2		1	2	mV
	Full	VI			3			3			3			3	mV
Input Offset Drift	Full	V		20			20			20			20		µV/°C
Input Bias Current	+25°C	I		7	10		7	10		7	10		7	10	µA
	Full	VI			13			13			16			16	µA
Input Offset Current	+25°C	I		0.1	1.0		0.1	1.0		0.1	1.0		0.1	1.0	µA
	Full	VI			1.2			1.2			1.2			1.2	µA
Input Resistance	+25°C	V		200			200			200			200		kΩ
Input Capacitance	+25°C	V		2			2			2			2		pF
Input Voltage Ranges	Full	VI	–2.5		+5.0	–2.5		+5.0	–2.5		+5.0	–2.5		+5.0	V
Common-Mode Rejection Ratio	Full	VI	80	90		80	90		80	90		80	90		dB
ENABLE INPUT															
Logic "1" Voltage	Full	VI	–1.1			–1.1			–1.1			–1.1			V
Logic "0" Voltage	Full	VI			–1.5			–1.5			–1.5			–1.5	V
Logic "1" Current	Full	VI			40			40			40			40	µA
Logic "0" Current	Full	VI			5			5			5			5	µA
DIGITAL OUTPUTS[6]															
Logic "1" Voltage	Full	VI	–1.1			–1.1			–1.1			–1.1			V
Logic "0" Voltage	Full	VI			–1.5			–1.5			–1.5			–1.5	V
SWITCHING PERFORMANCES															
Propagation Delays[7]															
Input to Output HIGH	+25°C	IV		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Input to Output LOW	+25°C	IV		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Latch Enable to Output HIGH	+25°C	IV		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Latch Enable to Output LOW	+25°C	IV		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Dispersions[8]	+25°C	V		50			50			50			50		ps
Latch Enable															
Minimum Pulse Width	+25°C	IV		2.0	3.0		2.0	3.0		2.0	3.0		2.0	3.0	ns
Minimum Setup Time	+25°C	IV		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0	ns
Minimum Hold Time	+25°C	IV		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0	ns
POWER SUPPLY[9]															
Positive Supply Current (+5.0 V)	Full	VI		8	9		15	18		8	9		15	18	mA
Negative Supply Current (–5.2 V)	Full	VI		15	18		31	36		15	18		31	36	mA
Power Supply Rejection Ratio[10]	Full	VI	60	70		60	70		60	70		60	70		dB

NOTES
[1]Absolute maximum ratings are limiting values, may be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Under no circumstances should the input voltages exceed the supply voltages .
[3]Typical thermal impedances . . .
AD96685 Metal Can θ_{JA} = 172°C/W; θ_{JC} = 52°C/W
AD96685 Ceramic θ_{JA} = 115°C/W; θ_{JC} = 57°C/W
AD96685 SOIC θ_{JA} = 170°C/W; θ_{JC} = 60°C/W
AD96685 PLCC θ_{JA} = 88°C/W; θ_{JC} = 45°C/W
AD96687 Ceramic θ_{JA} = 115°C/W; θ_{JC} = 57°C/W
AD96687 SOIC θ_{JA} = 92°C/W; θ_{JC} = 47°C/W
AD96687 PLCC θ_{JA} = 81°C/W; θ_{JC} = 45°C/W
[4]R_S = 100 Ω.
[5]Input Voltage Range can be extended to –3.3 V if $-V_S$ = –6.0 V.
[6]Outputs terminated through 50 Ω to –2.0 V.
[7]Propagation delays measured with 100 mV pulse (10 mV overdrive), to 50% transition point of the output.
[8]Change in propagation Delay from 100 mV to 1 V input overdrive.
[9]Supply voltages should remain stable within ±5% for normal operation.
[10]Measured at ±5% of $+V_S$ and $-V_S$.

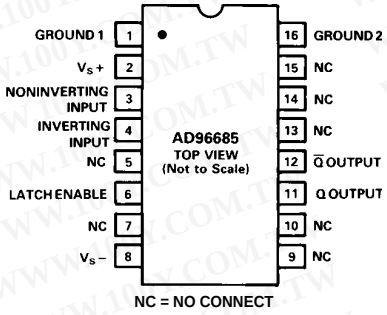
Specifications subject to change without notice.

FUNCTIONAL DESCRIPTION

Pin Name	Description
$+V_S$	Positive supply terminal, nominally +5.0 V.
NONINVERTING INPUT	Noninverting analog input of the differential input stage. The NONINVERTING INPUT must be driven in conjunction with the INVERTING INPUT.
INVERTING INPUT	Inverting analog input of the differential input stage. The INVERTING INPUT must be driven in conjunction with the NONINVERTING INPUT.
LATCH ENABLE	In the "compare" mode (logic HIGH), the output will track changes at the input of the comparator. In the "latch" mode (logic LOW), the output will reflect the input state just prior to the comparator being placed in the "latch" mode. $\overline{\text{LATCH ENABLE}}$ must be driven in conjunction with LATCH ENABLE for the AD96687.
$\overline{\text{LATCH ENABLE}}$	In the "compare" mode (logic LOW), the output will track changes at the input of the comparator. In the "latch" mode (logic HIGH), the output will reflect the input state just prior to the comparator being placed in the "latch" mode. LATCH ENABLE must be driven in conjunction with $\overline{\text{LATCH ENABLE}}$ for the AD96687.
$-V_S$	Negative supply terminal, nominally –5.2 V.
Q	One of two complementary outputs. Q will be at logic HIGH if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE and LATCH ENABLE (AD96687 only) for additional information.
$\overline{Q}$	One of two complementary outputs. $\overline{Q}$ will be at logic LOW if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE and LATCH ENABLE (AD96687 only) for additional information.
GROUND 1	One of two grounds, but primarily associated with the digital ground. Both grounds should be connected together near the comparator.
GROUND 2	One of two grounds, but primarily associated with the analog ground. Both grounds should be connected together near the comparator.

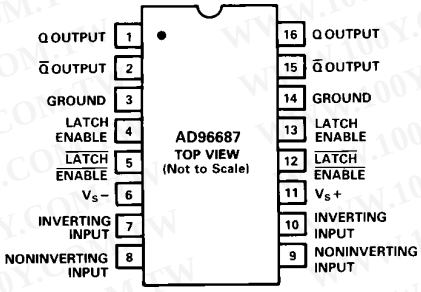
PIN DESIGNATIONS

AD96685BQ/TQ/BR

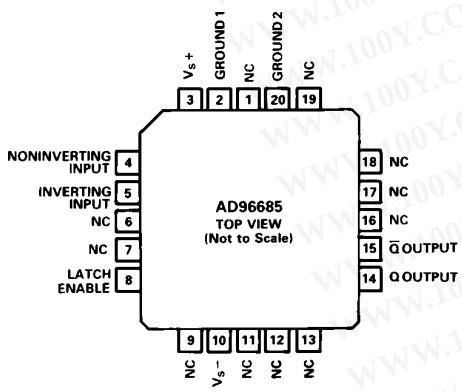


NC = NO CONNECT

AD96687BQ/TQ/BR

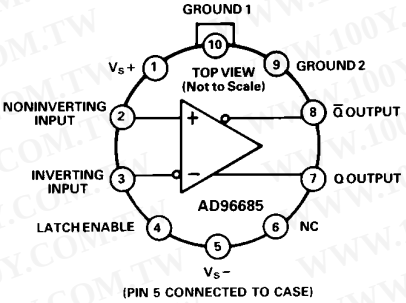


AD96685BP



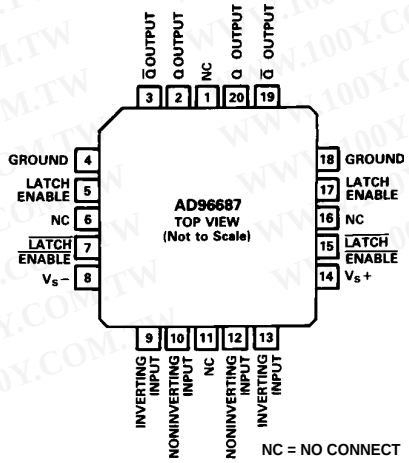
NC = NO CONNECT

AD96685BH



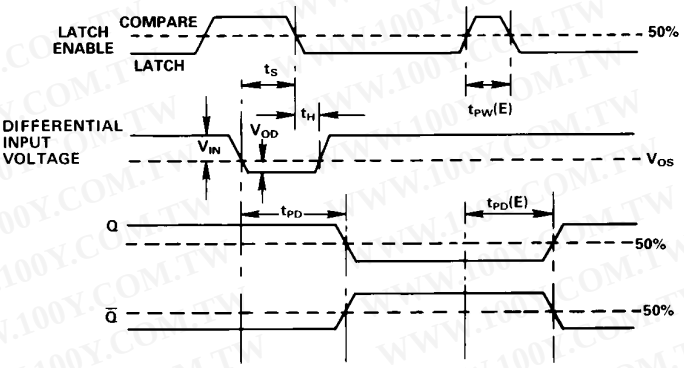
(PIN 5 CONNECTED TO CASE)

AD96687BP



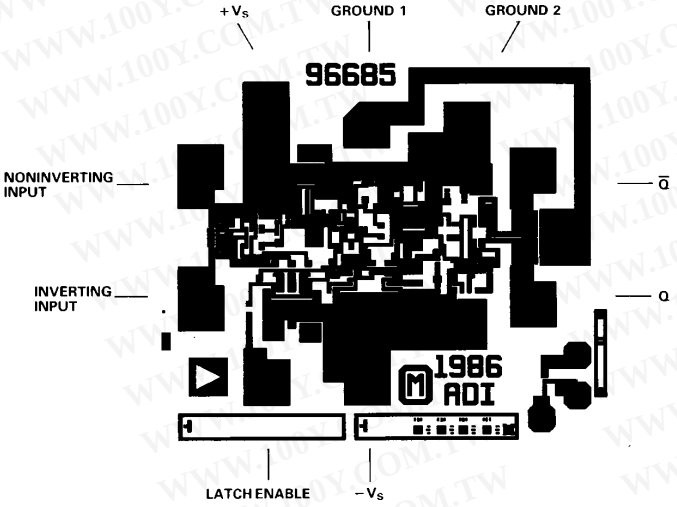
NC = NO CONNECT

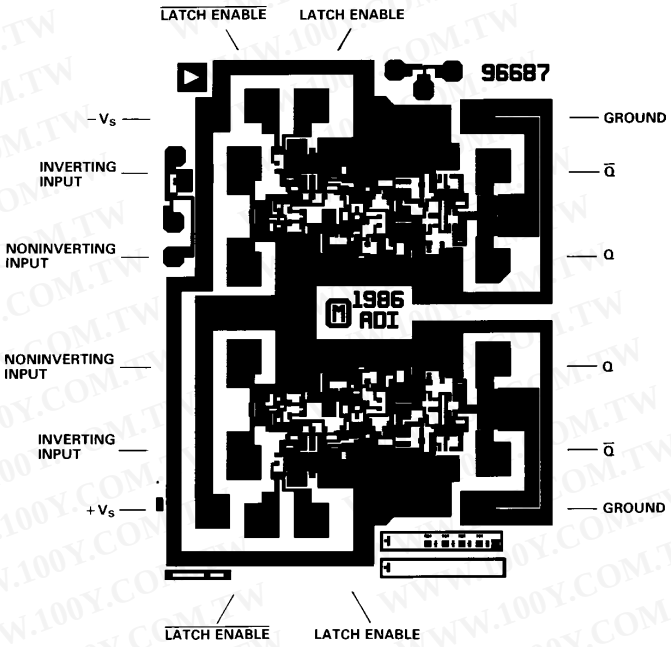
SYSTEM TIMING DIAGRAM



t_S – Minimum Setup Time
t_H – Minimum Hold Time
t_{PD} – Input to Output Delay
$t_{PD}(E)$ – LATCH ENABLE to Output Delay
$t_{PW}(E)$ – Minimum LATCH ENABLE Pulse Width
V_{OS} – Input Offset Voltage
V_{OD} – Overdrive Voltage

DIE LAYOUT AND MECHANICAL INFORMATION





Die Dimensions (AD96685)	44 × 50 × 15 (±2) mils
Pad Dimensions	4 × 4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil, Aluminum; Ultrasonic Bonding or 1 mil, Gold, Gold Ball Bonding

Die Dimensions (AD96687)	77 × 60 × 15 (±2) mils
Pad Dimensions	4 × 4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil, Aluminum; Ultrasonic Bonding or 1 mil, Gold, Gold Ball Bonding

ORDERING GUIDE

Model	Type	Temperature Range	Description	Package Options
AD96685BH	Single	–25°C to +85°C	10-Pin Can, Industrial	H-10A
AD96685BP	Single	–25°C to +85°C	20-Pin PLCC, Industrial	P-20A
AD96685BQ	Single	–25°C to +85°C	16-Pin DIP, Industrial	Q-16
AD96685BR	Single	–25°C to +85°C	16-Pin SOIC, Industrial	R-16A
AD96685BP-REEL	Single	–25°C to +85°C	20-Pin PLCC, Industrial	P-20A
AD96685TQ	Single	–55°C to +125°C	16-Pin DIP, Extended Temperature	Q-16
AD96687BP	Dual	–25°C to +85°C	20-Pin PLCC, Industrial	P-20A
AD96687BQ	Dual	–25°C to +85°C	16-Pin DIP, Industrial	Q-16
AD96687BR	Dual	–25°C to +85°C	16-Pin SOIC, Industrial	R-16A
AD96687BR-REEL	Dual	–25°C to +85°C	16-Pin SOIC, Industrial	R-16A
AD96687TQ	Dual	–55°C to +125°C	16-Pin DIP, Extended Temperature	Q-16

APPLICATIONS INFORMATION

The AD96685/87 comparators are very high speed devices. Consequently, high speed design techniques must be employed to achieve the best performance. The most critical aspect of any AD96685/87 design is the use of a low impedance ground plane.

Another area of particular importance is power supply decoupling. Normally, both power supply connections should be separately decoupled to ground through 0.1 µF ceramic and 0.001 µF mica capacitors. The basic design of comparator circuits makes the negative supply somewhat more sensitive to variations. As a result more attention should be placed on insuring a "clean" negative supply.

The LATCH ENABLE input is active LOW (latched). If the latching function is not used, the LATCH ENABLE input should be grounded (ground is an ECL logic HIGH). The $\overline{\text{LATCH ENABLE}}$ input of the AD96687 should be tied to –2.0 V or left "floating," to disable the latching function. An alternate use of the LATCH ENABLE input is as a hysteresis control input. By varying the voltage at the LATCH ENABLE input for the AD96685 and the differential voltage between both latch inputs for the AD96687, small variations in the hysteresis can be achieved.

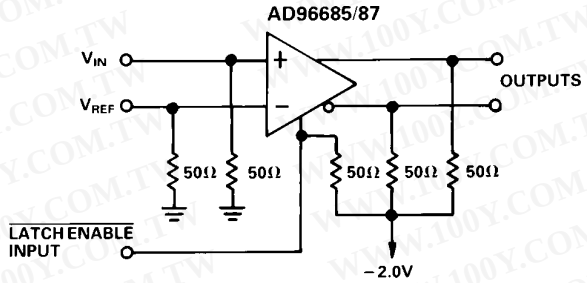
Occasionally, one of the two comparator stages within the AD96687 will not be used. The inputs of the unused comparator should not be allowed to "float." The high internal gain may cause the output to oscillate (possibly affecting the other comparator which is being used) unless the output is forced into a fixed state. This is easily accomplished by insuring that the two inputs are at least one diode drop apart, while also grounding the LATCH ENABLE input.

The best performance will be achieved with the use of proper ECL terminations. The open-emitter outputs of the AD96685/87 are designed to be terminated through 50 Ω resistors to –2.0 V, or any other equivalent ECL termination. If high speed ECL signals must be routed more than a few centimeters, MicroStrip or StripLine techniques may be required to insure proper transition times and prevent output ringing.

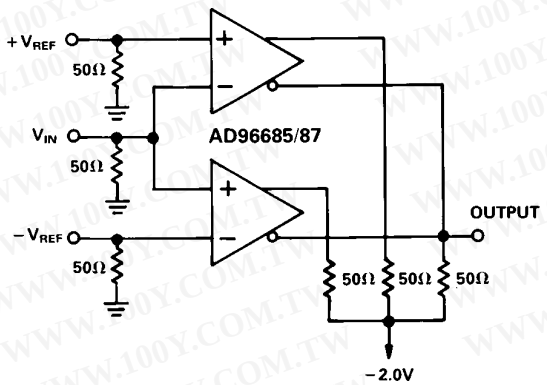
The AD96685/87 have been specifically designed to reduce propagation delay dispersion over an input overdrive range of 100 mV to 1 V. Propagation delay dispersion is the change in propagation delay which results from a change in the degree of overdrive (how far the switching point is exceeded by the input). The overall result is a higher degree of timing accuracy since the AD96685/87 is far less sensitive to input variations than most comparator designs.

Typical Applications

HIGH SPEED SAMPLING CIRCUIT



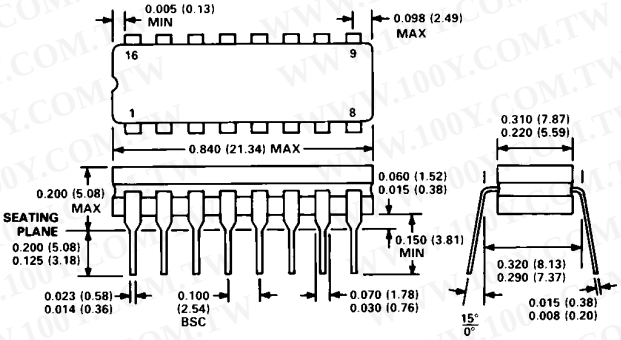
HIGH SPEED WINDOW COMPARATOR



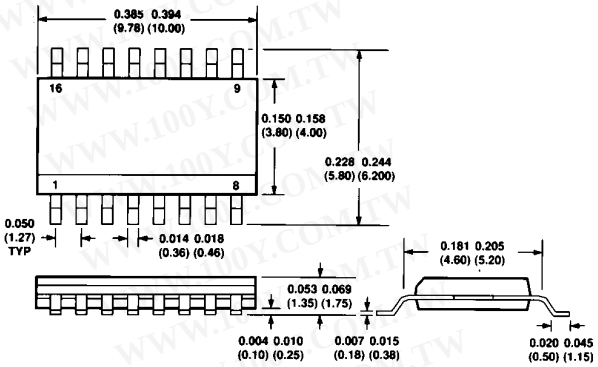
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

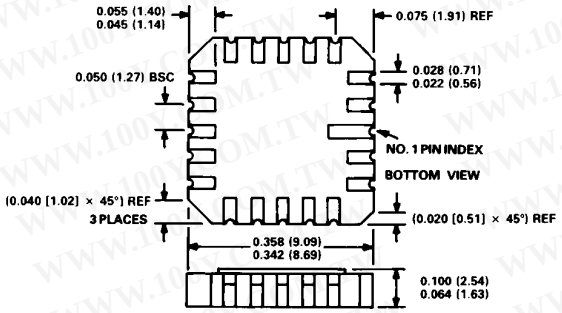
16-Pin Ceramic DIP



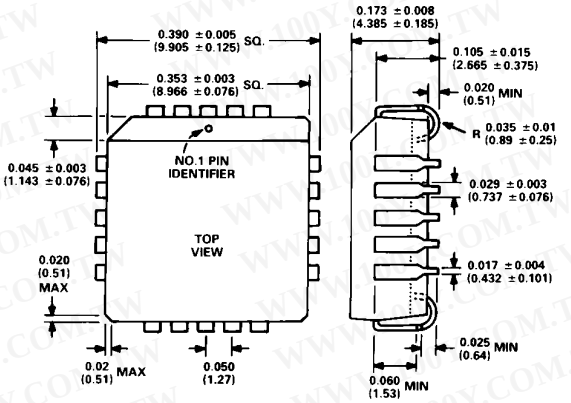
16-Pin SOIC



20-Pin LCC



20-Pin PLCC



10-Pin TO-100 Metal Can