

# Dual Ultrafast Voltage Comparator

# ADCMP565

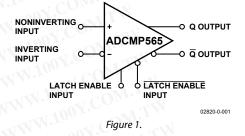
#### **FEATURES**

300 ps propagation delay input to output 50 ps propagation delay dispersion Differential ECL compatible outputs Differential latch control Robust input protection Input common-mode range –2.0 V to +3.0 V Input differential range ±5 V Power supply sensitivity greater than 65 dB 200 ps minimum pulsewidth 5 GHz equivalent input rise time bandwidth Typical output rise/fall of 160 ps SPT 9689 replacement

#### **APPLICATIONS**

High speed instrumentation Scope and logic analyzer front ends Window comparators High speed line receivers and signal restoration Threshold detection Peak detection High speed triggers Patient diagnostics Disk drive read channel detection Hand-held test instruments Zero-crossing detectors Clock drivers Automatic test equipment

#### FUNCTIONAL BLOCK DIAGRAM



#### **GENERAL DESCRIPTION**

The ADCMP565 is an ultrafast voltage comparator fabricated on Analog Devices' proprietary XFCB process. The device features 300 ps propagation delay with less than 50 ps overdrive dispersion. Overdrive dispersion, a particularly important characteristic of high speed comparators, is a measure of the difference in propagation delay under differing overdrive conditions.

A fast, high precision differential input stage permits consistent propagation delay with a wide variety of signals in the common-mode range from -2.0 V to +3.0 V. Outputs are complementary digital signals fully compatible with ECL 10 K and 10 KH logic families. The outputs provide sufficient drive current to directly drive transmission lines terminated in 50  $\Omega$  to -2 V. A latch input is included, which permits tracking, track-and-hold, or sample-and-hold modes of operation.

The ADCMP565 is available in a 20-lead PLCC package.

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#### Rev. 0

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### TABLE OF CONTENTS

	WW
TABLE OF CONTENTS	
Specifications	
Absolute Maximum Ratings5	
Thermal Considerations5	
ESD Caution	
Pin Configuration and Function Descriptions	
Timing Information	Ту
Application Information9	O
Clock Timing Recovery9	
REVISION HISTORY	
The second standard s	

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NN	WW.100Y.CO.	
	Optimizing High Speed Performance	9
	Comparator Propagation Delay Dispersion	9
	Comparator Hysteresis	
	Minimum Input Slew Rate Requirement	
	Typical Application Circuits	11
1	Typical Performance Characteristics	12
C	Outline Dimensions	14
	Ordering Guide	14

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# REVISION HISTORY

WWW.100Y.COM.TW **Revision 0: Initial Version** WWW.10

#### **SPECIFICATIONS**

.COM.TW Table 1. ADCMP565 ELECTRICAL CHARACTERISTICS ( $V_{CC} = +5.0$  V,  $V_{FF} = -5.2$  V,  $T_A = 25^{\circ}$ C, unless otherwise noted.)

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$\begin{array}{ c                                   $	Parameter	Symbol	Condition	Min	Тур	Max	Unit
Input Differential Voltage-5+5Vinput Offset Voltage Cannel Matching $V_{0x}$ -6.0 $\pm 1.5$ $\pm 6.0$ $\# V^{12}$ Offset Voltage Tempco $D_{0x}/dr$ -6.0 $\pm 1.5$ $\pm 6.0$ $\# V^{12}$ Input Bias Current $D_{0x}/dr$ -5.0 $\pm 0.5$ $\mu X$ Input Resistance, Differential Mode $I_{0x}$ -5.0 $\pm 0.5$ $\mu X$ Input Resistance, Common ModeCis-5.0 $\pm 0.5$ $\mu X$ Open Loop GainCis-5.0 $\pm 0.5$ $\mu X$ Common-Mode Rejection RatioCMRR $V_{ex} = -2.0$ V to $\pm 3.0$ V $-2.0$ 0VLATCH HABLE CHARACTERISTICS $\pm 1.0$ $\mu X$ $\pm 1.0$ $\mu X$ Latch Fnable Differential Input Voltage $V_{ex}$ $-2.0$ 0VInput Resistance, Common Mode Range $V_{ex}$ $250$ mV overdrive $-50$ $V$ Latch Fnable Differential Input Voltage $V_{ex}$ $250$ mV overdrive $-50$ $ps$ Latch Fnable Differential Input Voltage $V_{ex}$ $250$ mV overdrive $-1.0$ $-6.8$ $V$ Latch Fuble Differential Input Voltage $V_{ex}$ $250$ mV overdrive $250$ mV overdrive $ps$ Latch Fuble Differential Input Voltage $V_{ex}$ $250$ mV overdrive $1.08$ $-0.81$ $V$ Utry Urbut Delay $V_{ex}$ $250$ mV overdrive $1.08$ $-0.81$ $V$ Output Voltage—Input Latch Fuble Differential Fuble $V_{ex}$ $250$ mV overdrive $1.08$ $-0.81$ $V$ Out	DC INPUT CHARACTERISTICS (See Note)	WT	WWWWWWWY.CO	WTA			
input Offset Voltage Channel Matching         Vox         -6.0         ±1.5         ±6.0         mV           Input Offset Voltage Tempco         DVox/dr         -0.0         +1.0         +8         mV           Input Bias Current         Inc         -1.0.0         +2.4         +4.0.0         µA           Input Offset Voltage Tempco         DVox/dr         -1.0.0         +2.4         +4.0.0         µA           Input Capacitance         Cx         -5.0         ±0.5         +5.0         µA           Input Capacitance, Differential Mode         -5.0         ±0.5         +5.0         µA           Open Loop Gain         Cmmon-Mode Rejection Ratio         CMR         Vox         -2.0 V to +3.0 V         69         dB           Latch Enable Common-Mode Range         Vox         -2.0 V to +3.0 V         -10         +6         +1.0         µA           Input Low Current         ±0.0 V         -10         +6         +1.0         µA           Latch Enable Common-Mode Range         Vox         250 mV overdrive         280         ps           Latch Fulls Width         tx_c         250 mV overdrive         280         ps           Latch Houls Width         tx_c         250 mV overdrive         150         p	Input Common-Mode Range	V <sub>CM</sub>	VW. IOC	-2.0		+3.0	V
Input Offset Voltage Channel Matching         DVm/dr        8         +1         +8         mV           Offset Voltage Tempco         bic         -10.0         +24         +40.0         µA/C           Input Bias Current         bic         -5.0         ±0.5         +5.0         µA           Input Cristic Current         crist         -5.0         ±0.5         +5.0         µA           Input Resistance, Common Mode         -5.0         ±0.5         +5.0         µA           Open Loop Gain         Cm         60         60         48           Common-Mode Rejection Ratio         CMR         Von         -2.0         0         V           Latch Enable Common-Mode Range         Von         -2.0         0         V         0.4         ±0.0         PS           Latch Enable Differential Input Voltage         Von         -2.0         -10         +6         +10         µA           Latch Enable Differential Input Voltage         Von         250 mV overdrive         250         ps         ps           Latch Hold Time         ts         250 mV overdrive         250         ps         -1.61         ps           DUTPUT CHARACTERISTICS         Von         250 mV overdrive         10	Input Differential Voltage	WT.M	W 1 1001.0	-5		+5	V
Offset Voltage Tempo         DVcs/dr         μ//C         -10.0         5.0         μ///C           Input Bias Current         Inc         -10.0         +24         +40.0         μ//C           Input Offset Current         -5.0         ±0.5         +5.0         µ//C           Input Capacitance         Cri         -5.0         ±0.5         +5.0         µ//C           Open Loop Gain         Cri         -60.         40         60.         40           Common-Mode Rejection Ratio         CMRR         V <sub>CM</sub> = -2.0 V to +3.0 V         69         dB           Latch Enable Common-Mode Range         V <sub>LCM</sub> -2.0         0         V         41.0         mV           Latch Enable Common-Mode Range         V <sub>LCM</sub> -2.0         0.4         2.0         V           Latch Enable Common-Mode Range         V <sub>LCM</sub> -0.0         0.4         2.0         V           Input High Current         0         0.0 V         -10         +6         +10         µA           Input Law Current         ts         250 mV overdrive         280         ps         10         ps           Latch Fuble Differential Input Voltage         ts         250 mV overdrive         150         ps <td>Input Offset Voltage</td> <td>Vos</td> <td>WWW 100Y.</td> <td>-6.0</td> <td>±1.5</td> <td>+6.0</td> <td>mV</td>	Input Offset Voltage	Vos	WWW 100Y.	-6.0	±1.5	+6.0	mV
Input Bias Current         Inc         -10.0         +24         +40.0         μA           Input Dirac Bias Current Tempco         Input Organization Control         -5.0         ±0.5         +5.0         µA           Input Capacitance         Crv         -5.0         ±0.5         +5.0         µA           Input Resistance, Differential Mode         Crv         -60         40         60         KD           Common-Mode Region         CMRR         Vicm         -2.0         V to +3.0 V         69         dB           Hysteresis         Vicm         -2.0 V to +3.0 V         69         dB         BB         Wicm         -2.0 V         0.4         2.0         V           Latch Enable Differential Input Voltage         Vicm         @ 0.0 V         -10         +6         +10         µA           Input High Current         @ 0.0 V         -10         +6         +10         µA           Latch Enable Differential Input Voltage         ts.         250 mV overdrive         50         ps           Latch Didu Time         ts.         250 mV overdrive         10         ps           Latch Didu Time         ts.         250 mV overdrive         10         ps           DUTUT CHARCE TENSTICS	Input Offset Voltage Channel Matching	ON.	WWW.100	-8	+1	+8	mV
Input Bias Current Tempco Input Capacitance17 $nA^{AC}$ Input CapacitanceCm $\pm 5.0$ $\pm 0.3$ $\mu A^{AC}$ Input Resistance, Differential Mode Input Resistance, Common Mode Open Loop GainCMRR $V_{CM} = -2.0 V to +3.0 V$ $600$ KQOpen Loop GainCMRR $V_{CM} = -2.0 V to +3.0 V$ $69$ $dB$ $B$ Carmon-Mode Rejection RatioCMRR $V_{CM} = -2.0 V to +3.0 V$ $69$ $dB$ $B$ Hysteresis $U_{CM}$ $U_{CM}$ $-2.0$ $0$ $V$ Latch Enable Common-Mode Range $V_{CM}$ $U_{CM}$ $2.0$ $0$ $V$ Latch Enable Differential Input Voltage $W_{1D}$ $W_{1D}$ $0.0 V$ $-10$ $+6$ $+10$ $\mu A$ Input Low Current $W_{1D}$ <td>Offset Voltage Tempco</td> <td>DVos/d<sub>T</sub></td> <td>W 1,100 1</td> <td>Mo</td> <td>5.0</td> <td></td> <td>μV/°C</td>	Offset Voltage Tempco	DVos/d <sub>T</sub>	W 1,100 1	Mo	5.0		μV/°C
Input Offset Current Input Capacitance, Differential Mode Input Resistance, Common Mode Open Loop Gain Common-Mode Rejection Ratio Hysteresis $-5.0$ $\pm 0.5$ $\pm 5.0$ $\mu A$ pF pF G0 $K\Omega$ G0Common-Mode Rejection Ratio HysteresisCMRR $V_{CM} = -2.0 V to +3.0 V$ $60$ <	Input Bias Current	Івс	WWW TOO	-10.0	+24	+40.0	μA
$\begin{array}{ c c c c c } \mbox{Input Offset Current} & C_{\rm H} & -5.0 & \pm 0.5 & \pm 5.0 & \mu A \\ \mbox{Input Capacitance, Differential Mode} & -5.0 & \pm 0.5 & \pm 5.0 & \mu A \\ \mbox{Input Resistance, Common Mode} & -7.0 $	Input Bias Current Tempco	COM.	NWW-10	A CON	17		nA/°C
Input Capacitance         Gw         1.75         pF           Input Resistance, Offferential Mode         100         KΩ           Open Loop Gain         60         KΩ           Common-Mode Rejection Ratio         CMRR         V <sub>CW</sub> = -2.0 V to +3.0 V         69         dB           Hysteresis         -1.0         +1.0         mV         mV           LATCH ENABLE CHARACTERISTICS         -2.0         0         V           Latch Enable Common-Mode Range         V <sub>LOM</sub> -2.0         0         V           Input High Current         @ 0.0 V         -10         +6         +10         µA           Input High Current         @ 0.0 V         -10         +6         +10         µA           Latch Setup Time         ts         250 mV overdrive         250         ps           Latch Nulse Width         tr,         250 mV overdrive         260         ps           Latch Hule Width         tr,         250 mV overdrive         10         ps           Output Voltage—High Level         Vort         ECL 50 Ω to -2.0 V         -1.08         -0.81         V           Output Voltage—High Level         Vort         ECL 50 Ω to -2.0 V         -1.95         -0.61         ps <tr< td=""><td></td><td>T.Mon</td><td>N.10</td><td>-5.0</td><td>±0.5</td><td>+5.0</td><td>μA</td></tr<>		T.Mon	N.10	-5.0	±0.5	+5.0	μA
Input Resistance, Common Mode Open Loop Gain Common-Mode Rejection RatioCMRR $V_{CM} = -2.0 V \text{ to } +3.0 V$ $600$ $60$ 69 $dB$ 69LATCH ENABLE CHARACTERISTICS Latch Enable Differential Input Voltage Input High Current Latch Setup Time $V_{CM}$ $-2.0$ $0$ $V$ Input High Current Input Low Current $\emptyset$ 0.0 V $-10$ $+6$ $+10$ $\mu A$ Input Low Current Latch Setup Time $t_s$ $250 \text{ mV overdrive}$ $260$ $ps$ Latch Output Delay Latch Pulse Width $t_r$ $250 \text{ mV overdrive}$ $280$ $ps$ DUTPUT CHARACTERISTICS Output Voltage—High Level With Rise Time Fall Time $V_{OH}$ $ECL 50 \Omega \text{ to } -2.0 V$ $-1.08$ $-0.81$ Output Voltage—High Level Propagation Delay $V_{OH}$ $ECL 50 \Omega \text{ to } -2.0 V$ $-1.08$ $-0.81$ $V$ Output Voltage—Low Level Righ Transition to Falling Transition Propagation Delay Dispersion vs. Duty Cycle $10 \text{ Voerdrive}$ $310$ $ps$ Propagation Delay Dispersion vs. Duty Cycle $1 \text{ MHz}_1 \text{ In stw, tr}$ $\pm10$ $ps$ Propagation Delay Dispersion vs. Solew Rate $1 \text{ MHz}_1 \text{ In stw, tr}$ $\pm10$ $ps$ Propagation Delay Dispersion vs. Solew Rate $0 \text{ Vol V Vswing}_1$ $50$ $ps$ Propagation Delay Dispersion vs. Solew Rate $0 \text{ Vol V Vswing}_1$ $500$ $ps$ Propagation Delay Dispersion vs. Solew Rate $0 \text{ Vol V Vswing}_1$ $500$ $ps$ Propagation Delay Dispersion vs. Solew Rate $0  Vol V Vswing$	Input Capacitance	CIN	CN WWW	NOY.CO	1.75		
Open Loop Gain Common-Mode Rejection Ratio HysteresisCMRR $V_{CM} = -2.0 V \text{ to } +3.0 V$ $60$ dB dB dBLATCH ENABLE CHARACTERISTICS Latch Enable Offreential Input Voltage Upt Usy $V_{LOM}$ $-2.0$ $0$ $V$ LATCH ENABLE CHARACTERISTICS Latch Enable Offreential Input Voltage Upt Usy $0.0 V$ $-10$ $+6$ $+10$ $\mu A$ Latch Enable Offreential Input Voltage Latch Enable Offreential Input Voltage $\psi_{CD}$ $0.4$ $2.0$ $V$ Input High Current Latch Pulse Widthtrices Erock Trices Erock $250 \text{ mV overdrive}$ $280$ $ps$ Latch Pulse Width Latch Hold Timetrices Erock Trices Erock $250 \text{ mV overdrive}$ $100$ $ps$ OUTPUT CHARACTERISTICS Output Voltage—Low Level Rise Time Propagation Delay Propagation Delay Propagation Delay Dispersion vs. Duty Cycle $V_{Ov}$ $ECL 50 \Omega \text{ to } -2.0 V$ $-1.08$ $-0.81$ $V$ $V$ Propagation Delay Dispersion vs. Duty Cycletro $20\% \text{ to } 80\%$ $145$ $ps$ Propagation Delay Dispersion vs. Duty Cycle $10 \text{ MHz}$ $300 \text{ vpririve}$ $310$ $ps$ Propagation Delay Dispersion vs. Common-Mode Voltage $10 \text{ Vo visining}$ $50 \text{ mV to } 1.5 V$ $50 \text{ mp}$ $ps$ Propagation Delay Dispersion vs. Common-Mode Voltage $8W$ $0V \text{ to } 1 \text{ swing}$ $5000 \text{ mV to } 1.5 V$ $50 \text{ mp}$ $ps$ Propagation Delay Dispersion vs. Common-Mode Voltage $8W$ $0V \text{ to } 1 \text{ swing}$ $5000 \text{ mV to } 1.5 V$ $50 \text{ mV to } 1.5 V$	Input Resistance, Differential Mode	CONT.	WWW.		100		kΩ
Common-Mode Rejection Ratio HysteresisCMRR $V_{CM} = -2.0 V \text{ to } +3.0 V$ $69$ $\pm 1.0$ $dB$ mVLATCH ENABLE CHARACTERISTICS Latch Enable Common-Mode Range Latch Public Width Latch Setup Time Latch Output Voltage $V_{CM}$ $-2.0$ $0$ $V$ Input Low Current Latch Dube Width Latch Voltage $@ 0.0 V$ $-10$ $+6$ $+10$ $µA$ $µA$ Latch Output Delay Latch Puble Width tree Latch Puble Width Latch Puble Width tree $t_{RC}$ $250 \text{ mV overdrive}$ $280$ $ps$ OUTPUT CHARACTERISTICS Output Voltage—High Level Noutput Voltage—Low Level Rise Time Propagation Delay $V_{OH}$ $ECL 50 \Omega \text{ to } -2.0 V$ $-1.08$ $-0.81$ $V$ $V$ Output Voltage—High Level Propagation Delay Dispersion vs. Duty Cycle $V_{OH}$ $ECL 50 \Omega \text{ to } -2.0 V$ $-1.08$ $-0.81$ $V$ $V$ Propagation Delay Dispersion vs. Duty Cycle $Tro<$ $1 \text{ Voverdrive}$ $310$ $ps$ Propagation Delay Dispersion vs. Duty Cycle $20 \text{ mV to } 1.5 V$ $50$ $ps$ Propagation Delay Dispersion vs. Slew Rate $1 \text{ MHz}$ 1 ns tw, tr $\pm 10$ $ps$ Propagation Delay Dispersion vs. Slew Rate $250 \text{ mV to } 1.5 V$ $50$ $ps$ Propagation Delay Dispersion vs. Duty Cycle $20 \text{ mV to } 1.5 V$ $50$ $ps$ Propagation Delay Dispersion vs. Slew Rate $1 \text{ MHz}$ 1 ns tw, tr $\pm 10$ $ps$	Input Resistance, Common Mode	ON. ON	W	100 1	600		kΩ
Hysteresis±1.0±1.0mVLATCH ENABLE CHARACTERISTICSV.cot-2.00.42.0VLatch Enable Differential Input VoltageV.D0.42.0VInput High Current@ 0.0 V-10+6+10µAInput Low Current@ -2.0 V-10+6+10µALatch Setup Timets250 mV overdrive50psLatch Output Delaytr.or, troot250 mV overdrive10psLatch Hold Timetr250 mV overdrive10psOUTPUT CHARACTERISTICStr.or, troot250 mV overdrive10psOutput Voltage—High LevelVortECL 50 Ω to -2.0 V-1.08-0.81VOutput Voltage—Low LevelVortECL 50 Ω to -2.0 V-1.95-1.61VRise Timetr20% to 80%145pssspsAC PERFORMANCEtro1 V overdrive310pspsPropagation Delaytro20 mV overdrive375pspsPropagation Delay TempcoPro20 mV to 1.5 V50pspsPropagation Delay Dispersion vs.1 MHz, 1 ns to, tr±10pspsPropagation Delay Dispersion vs.20 mV to 1.5 V50pspsPropagation Delay Dispersion vs.10 HHz, 1 ns to, tr±10pspsPropagation Delay Dispersion vs.20 mV to 1.5 V50pspsPropagation Delay Dispersion vs.20 mV to 1.5 V50 <td></td> <td>INV.CON</td> <td>WW WIT</td> <td>1001.0</td> <td>60</td> <td></td> <td>dB</td>		INV.CON	WW WIT	1001.0	60		dB
Hysteresiswith $\pm 1.0$ mVLATCH ENABLE CHARACTERISTICS Latch Enable Common-Mode Range Latch Enable Differential Input VoltageV.co.t $-2.0$ $0.4$ $2.0$ VInput High Current Input Low Current@ $0.0$ V $-10$ $+6$ $+10$ $\mu$ AInput Low Current Latch Stepup Timets $250$ mV overdrive $50$ $ps$ Latch fulles Widthtrice, troct $250$ mV overdrive $280$ $ps$ Latch fulles Widthtri, $250$ mV overdrive $10$ $ps$ Latch Hold Timetri $250$ mV overdrive $10$ $ps$ OUTPUT CHARACTERISTICS Output Voltage—Low LevelVortECL 50 $\Omega$ to $-2.0$ V $-1.08$ $-0.81$ VOutput Voltage—Low LevelVortECL 50 $\Omega$ to $-2.0$ V $-1.08$ $-0.81$ VRise Timetr<	Common-Mode Rejection Ratio	CMRR	$V_{CM} = -2.0 \text{ V to } +3.0 \text{ V}$	. Voor	69		dB
LATCH ENABLE CHARACTERISTICSV.cm-2.00VLatch Enable Differential Input VoltageV.cm0.42.0VInput High Current@ 0.0 V-10+6+10µAInput Low Current@ 0.0 V-10+6+10µALatch Setup Timets250 mV overdrive250psLatch Voluput Delayts.ow, tetox250 mV overdrive150psLatch Hold Timetri250 mV overdrive10psOUTPUT CHARACTERISTICSVOHECL 50 Ω to -2.0 V-1.08-0.81VOutput Voltage—Ligh LevelVOHECL 50 Ω to -2.0 V-1.95-1.61VOutput Voltage—Ligh LevelVOHta20% to 80%160psAC PERFORMANCEtro1 V overdrive310pspsPropagation DelayTero20 mV overdrive375psps/°CPropagation DelayTero20 mV overdrive310psps/°CPropagation DelayTero1 MHz, 1 ns te, tr±10psPropagation Delay Dispersion vs.0.04 to 1.5 V50pspsDuty CyclePropagation Delay Dispersion vs.0.0410psPropagation Delay Dispersion vs.0.041.5 V50psSlew Rate20 mV to 1.5 V50pspsPropagation Delay Dispersion vs.0.041.0 V swing, 2.09% to 80%, S0 ps and 600 ps te, tr, tr50psPropagation Delay Dispersion vs. <t< td=""><td></td><td>11001.</td><td>1.1.</td><td>N.100 1</td><td>±1.0</td><td></td><td>mV</td></t<>		11001.	1.1.	N.100 1	±1.0		mV
$ \begin{array}{c c c c c c c } \mbox{Latch Enable Common-Mode Range} & V_{LOM} & & & & & & & & & & & & & & & & & & &$		1001.0	NN NT	1005	- Al	TW	
Latch Enable Differential Input Voltage Input High CurrentVLD0.42.0VInput Low Current@ 0.0 V-10+6+10µAInput Low Current250 mV overdrive50psLatch Setup Timets250 mV overdrive280psLatch Vulse Widthtr.250 mV overdrive150psLatch Hold Timetr.250 mV overdrive150psOUTPUT CHARACTERISTICStr.250 mV overdrive10-0.81VOutput Voltage—High LevelVor.ECL 50 Ω to -2.0 V-1.08-0.81VOutput Voltage—Low LevelVor.ECL 50 Ω to -2.0 V-1.95-1.61VRise Timetr.20% to 80%160pspsFall Timetr.20% to 80%145psPropagation Delaytro1 V overdrive310psPropagation Delaytro1 V overdrive310psPropagation Delay Dispersion vs.1 MHz, 1 ns te, tr±10psPropagation Delay Dispersion vs. Overdrive20 mV to 1.5 V50psPropagation Delay Dispersion vs.20 mV to 1.5		VICM	CM. WW	-2.0		0	v
Input High Current Input Low Currentww-10+6+10μALatch Setup Timets250 mV overdrive50psLatch Output Delaytrion, triot250 mV overdrive150psLatch Hold Timetri250 mV overdrive150psOUTPUT CHARACTERISTICStri250 mV overdrive10psOutput Voltage—High LevelVoritECL 50 Ω to -2.0 V-1.08-0.81VOutput Voltage—Low LevelVoritECL 50 Ω to -2.0 V-1.95-1.61VRise Timetri20% to 80%160pspsFropagation Delaytro1 V overdrive310psPropagation Delay Skew— Channel O Channeltro1 V overdrive310psPropagation Delay Dispersion vs. Duty Cycleps1 MHz, 1 ns tw, tr±10psPropagation Delay Dispersion vs. Skew Rate50 mV to 1.5 V50psPropagation Delay Dispersion vs. Skew Rate20 mV to 1.5 V50psPropagation Delay Dispersion vs. Skew Rate1 MHz, 1 ns tw, tr±10psPropagation Delay Dispersion vs. Skew Rate50 mV to 1.5 V50psPropagation Delay Dispersion vs. Skew Rate50 ps tw, tr, 1 V swing, 20% to 80%,5000psPropagation Delay Dispersion vs. Common-Mode VoltageBW0 V to 1 V swing, 20% to 80%,5000MHz			ON. I				
Input Low Current Latch Setup Time $(                                    $		YooX.	@ 0.0 V		+6		
Latch Setup Timets250 mV overdrive50psLatch to Output Delaytruch, truck250 mV overdrive280psLatch Pulse Widthtrl250 mV overdrive150psLatch Hold Timetrl250 mV overdrive10psOUTPUT CHARACTERISTICS-0.81VOutput Voltage—Low LevelVortECL 50 Ω to -2.0 V-1.08-0.81VRise Timetr20% to 80%160psFall Timetr20% to 80%145psAC PERFORMANCEtro1 V overdrive310psPropagation Delaytro1 V overdrive375psPropagation Delay Tempcotro1 V overdrive375psPropagation Delay Tempcotro1 MHz, 1 ns tr, tr±10psPropagation Delay Dispersion vs.1 MHz, 1 ns tr, tr±10psPropagation Delay Dispersion vs. Overdrive20 mV to 1.5 V50psPropagation Delay Dispersion vs.20 mV to 1.5 V50psPropagation Delay Dispersion vs.20 mV to 1.5 V50psSlew Rate20 mV to 1.5 V50psPropagation Delay Dispersion vs.20 mV to 1.5 V <td></td> <td>WW.Los</td> <td></td> <td></td> <td></td> <td></td> <td>-</td>		WW.Los					-
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	Equivalent Input Rise Time Bandwidth	BW	0 V to 1 V swing, 20% to 80%,	N.COM	5000		MHz

Ра	rameter	Symbol	Condition	Min	Тур	Max	Unit
AC	PERFORMANCE (continued)	COM.	N. M. M.	ON.	1		
	Toggle Rate	WT.IN	>50% output swing	T.Mo-	5		Gbps
	Minimum Pulse Width	PW	$\Delta t_{PD}$ from 10 ns to 200 ps < ±50 ps	COM.	200		ps
	Unit to Unit Propagation Delay Skew	Y.M.TV	N N 1007	M	±10		ps
PO	WER SUPPLY	N.COm	NN NN	1.00	WT		
	Positive Supply Current	lv <sub>cc</sub>	@ +5.0 V	10	13	18	mA
	Negative Supply Current	Iv <sub>EE</sub>	@ -5.2 V	60	70	80	mA
	Positive Supply Voltage	Vcc	Dual	4.75	5.0	5.25	V
	Negative Supply Voltage	VEE	Dual	-4.96	-5.2	-5.45	V
	Power Dissipation	N. JOU CO	Dual, without load	370	435	490	mW
	Power Dissipation	W 1001.	Dual, with load	V.100 1.	550		mW
	Power Supply Sensitivity—Vcc	PSSv <sub>cc</sub>	WW WILL	×100Y	67		dB
	Power Supply Sensitivity—V <sub>EE</sub>	PSSv <sub>FF</sub>	WW WW	N.1	83		dB

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### **ABSOLUTE MAXIMUM RATINGS**

	Parameter	Rating
Supply Voltages	Positive Supply Voltage (V <sub>cc</sub> to GND)	–0.5 V to +6.0 V
	Negative Supply Voltage ( $V_{EE}$ to GND)	-6.0 V to +0.5 V
	Ground Voltage Differential	-0.5 V to +0.5 V
Input Voltages	Input Common-Mode Voltage	-3.0 V to +4.0 V
	Differential Input Voltage	-7.0 V to +7.0 V
	Input Voltage, Latch Controls	V <sub>EE</sub> to 0.5 V
Output	Output Current	30 mA
Temperature	Operating Temperature, Ambient	-40°C to +85°C
	Operating Temperature, Junction	125°C
	Storage Temperature Range	-55°C to +125°C

Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ESD CAUTION**

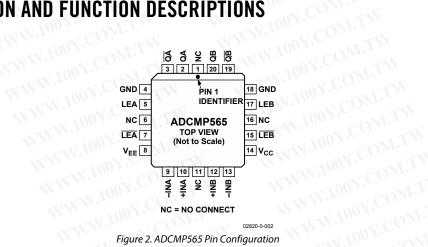
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

#### THERMAL CONSIDERATIONS

The ADCMP565 20-lead PLCC package option has a  $\theta_{JA}$  (junction-to-ambient thermal resistance) of 89.4°C/W in still air.



# 100X.COM.TW PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



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Pin No.	OCMP565 Pin Des Mnemonic	Function
1	NC	No Connect. Leave pin unconnected.
2	QA	One of two complementary outputs for Channel A. QA will be at logic high if the analog voltage at the noninverting input is greater than the analog voltage at the inverting input (provided the comparator is in the compare mode). See the LEA description (Pin 5) for more information.
3	QA	One of two complementary outputs for Channel A. QA will be at logic low if the analog voltage at the noninverting input is greater than the analog voltage at the inverting input (provided the comparator is in the compare mode). See the LEA description (Pin 5) for more information.
4	GND	Analog Ground
5	LEA	One of two complementary inputs for Channel A Latch Enable. In the compare mode (logic high), the output will track changes at the input of the comparator. In the latch mode (logic low), the output will reflect the input state just prior to the comparator's being placed in the latch mode. LEA must be driven in conjunction with LEA.
6	NC	No Connect. Leave pin unconnected or attach to GND (internally connected to GND).
7	LEA	One of two complementary inputs for Channel A Latch Enable. In the compare mode (logic low), the output will track changes at the input of the comparator. In the latch mode (logic high), the output will reflect the input state just prior to the comparator's being placed in the latch mode. LEA must be driven in conjunction with LEA.
8	V <sub>EE</sub>	Negative Supply Terminal
9	-INA	Inverting analog input of the differential input stage for Channel A. The inverting A input must be driver in conjunction with the noninverting A input.
10	+INA	Noninverting analog input of the differential input stage for Channel A. The noninverting A input must be driven in conjunction with the inverting A input.
11	NC	No Connect. Leave pin unconnected.
12	+INB	Noninverting analog input of the differential input stage for Channel B. The noninverting B input must be driven in conjunction with the inverting B input.
13	-INB	Inverting analog input of the differential input stage for Channel B. The inverting B input must be driven in conjunction with the noninverting B input.
14	Vcc	Positive Supply Terminal
15	LEB	One of two complementary inputs for Channel B Latch Enable. In the compare mode (logic low), the output will track changes at the input of the comparator. In the latch mode (logic high), the output will reflect the input state just prior to the comparator's being placed in the latch mode. LEB must be driven in conjunction with LEB.
16	NC	No Connect. Leave pin unconnected or attach to GND (internally connected to GND).
17	LEB	One of two complementary inputs for Channel B Latch Enable. In the compare mode (logic high), the output will track changes at the input of the comparator. In the latch mode (logic low), the output will reflect the input state just prior to the comparator's being placed in the latch mode. LEB must be driven in conjunction with LEB.

## WWW.100Y.COM.TW OY.COM.TW Table 3. ADCMP565 Pin Descriptions

CNID	
GND	Analog Ground
QB	One of two complementary outputs for Channel B. QB will be at logic low if the analog voltage at the noninverting input is greater than the analog voltage at the inverting input (provided the comparator in the compare mode). See the LEB description (Pin 17) for more information.
QB	One of two complementary outputs for Channel B. QB will be at logic high if the analog voltage at the noninverting input is greater than the analog voltage at the inverting input (provided the comparator in the compare mode). See the LEB description (Pin 17) for more information.
TW V	in the compare mode). See the LEB description (Pin 17) for more information.
	QB

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#### TIMING INFORMATION

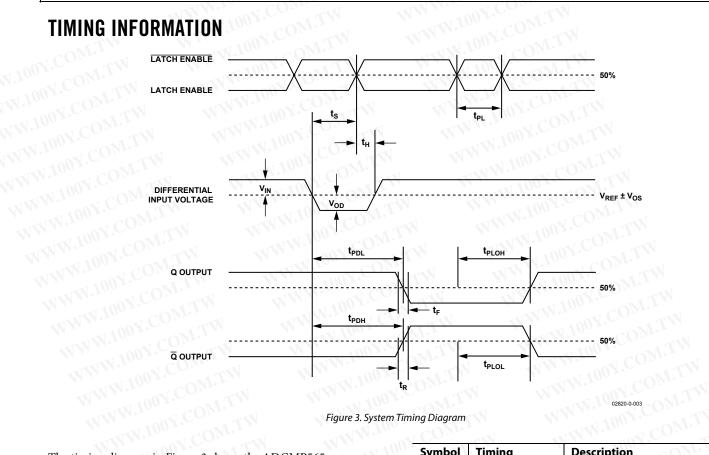


Figure 3. System Timing Diagram

The timing diagram in Figure 3 shows the ADCMP565 compare and latch features. Table 4 describes the terms in the diagram.

Symbol	Timing	Description
tрdн	Input to output high delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output low-to-high transition
<b>t</b> PDL	Input to output low delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output high-to-low transition
<b>t</b> PLOH	Latch enable to output high delay	Propagation delay measured from the 50% point of the Latch Enable signal low-to-high transition to the 50% point of an output low- to-high transition
<b>t</b> <sub>PLOL</sub>	Latch enable to output low delay	Propagation delay measured from the 50% point of the Latch Enable signal low-to-high transition to the 50% point of an output high- to-low transition

Symbol	Timing	Description
H N.COM N.CO	Minimum hold time	Minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged to be acquired and held at the outputs
t <sub>PL</sub>	Minimum latch enable pulse width	Minimum time that the Latch Enable signal must be high to acquire an input signal change
ts N.100X N.100	Minimum setup time	Minimum time before the negative transition of the Latch Enable signal that an input signal change must be present to be acquired and held at the outputs
R	Output rise time	Amount of time required to transition from a low to a high output as measured at the 20% and 80% points
FWW	Output fall time	Amount of time required to transition from a high to a low output as measured at the 20% and 80% points
/od	Voltage overdrive	Difference between the differential input and reference input voltages

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### **APPLICATION INFORMATION**

The ADCMP565 comparators are very high speed devices. Consequently, high speed design techniques must be employed to achieve the best performance. The most critical aspect of any ADCMP565 design is the use of a low impedance ground plane. A ground plane, as part of a multilayer board, is recommended for proper high speed performance. Using a continuous conductive plane over the surface of the circuit board can create this, allowing breaks in the plane only for necessary signal paths. The ground plane provides a low inductance ground, eliminating any potential differences at different ground points throughout the circuit board caused by ground bounce. A proper ground plane also minimizes the effects of stray capacitance on the circuit board.

It is also important to provide bypass capacitors for the power supply in a high speed application. A 1  $\mu$ F electrolytic bypass capacitor should be placed within 0.5 inches of each power supply pin to ground. These capacitors will reduce any potential voltage ripples from the power supply. In addition, a 10 nF ceramic capacitor should be placed as close as possible from the power supply pins on the ADCMP565 to ground. These capacitors act as a charge reservoir for the device during high frequency switching.

The LATCH ENABLE input is active low (latched). If the latching function is not used, the LATCH ENABLE input should be grounded (ground is an ECL logic high), and the complementary input, LATCH ENABLE, should be tied to -2.0 V. This will disable the latching function.

Occasionally, one of the two comparator stages within the ADCMP565 will not be used. The inputs of the unused comparator should not be allowed to float. The high internal gain may cause the output to oscillate (possibly affecting the comparator that is being used) unless the output is forced into a fixed state. This is easily accomplished by ensuring that the two inputs are at least one diode drop apart, while also appropriately connecting the LATCH ENABLE and LATCH ENABLE inputs as described above.

The best performance is achieved with the use of proper ECL terminations. The open emitter outputs of the ADCMP565 are designed to be terminated through 50  $\Omega$  resistors to -2.0 V, or any other equivalent ECL termination. If a -2.0 V supply is not available, an 82  $\Omega$  resistor to ground and a 130  $\Omega$  resistor to -5.2 V provide a suitable equivalent. If high speed ECL signals must be routed more than a centimeter, microstrip or stripline techniques may be required to ensure proper transition times and prevent output ringing.

#### **CLOCK TIMING RECOVERY**

Comparators are often used in digital systems to recover clock timing signals. High speed square waves transmitted over a distance, even tens of centimeters, can become distorted due to stray capacitance and inductance. Poor layout or improper termination can also cause reflections on the transmission line, further distorting the signal waveform. A high speed comparator can be used to recover the distorted waveform while maintaining a minimum of delay.

#### **OPTIMIZING HIGH SPEED PERFORMANCE**

As with any high speed comparator amplifier, proper design and layout techniques should be used to ensure optimal performance from the ADCMP565. The performance limits of high speed circuitry can easily be a result of stray capacitance, improper ground impedance, or other layout issues.

Minimizing resistance from source to the input is an important consideration in maximizing the high speed operation of the ADCMP565. Source resistance in combination with equivalent input capacitance could cause a lagged response at the input, thus delaying the output. The input capacitance of the ADCMP565 in combination with stray capacitance from an input pin to ground could result in several picofarads of equivalent capacitance. A combination of 3 k $\Omega$  source resistance and 5 pF of input capacitance yields a time constant of 15 ns, which is significantly slower than the sub 500 ps capability of the ADCMP565. Source impedances should be significantly less than 100  $\Omega$  for best performance.

Sockets should be avoided due to stray capacitance and inductance. If proper high speed techniques are used, the ADCMP565 should be free from oscillation when the comparator input signal passes through the switching threshold.

#### COMPARATOR PROPAGATION DELAY DISPERSION

The ADCMP565 has been specifically designed to reduce propagation delay dispersion over an input overdrive range of 100 mV to 1 V. Propagation delay overdrive dispersion is the change in propagation delay that results from a change in the degree of overdrive (how far the switching point is exceeded by the input). The overall result is a higher degree of timing accuracy since the ADCMP565 is far less sensitive to input variations than most comparator designs.

Propagation delay dispersion is a specification that is important in critical timing applications such as ATE, bench instruments, and nuclear instrumentation. Overdrive dispersion is defined

as the variation in propagation delay as the input overdrive conditions are changed (Figure 4). For the ADCMP565, overdrive dispersion is typically 50 ps as the overdrive is changed from 100 mV to 1 V. This specification applies for both positive and negative overdrive since the ADCMP565 has equal delays for positive and negative going inputs.

The 50 ps propagation delay dispersion of the ADCMP565 offers considerable improvement of the 100 ps dispersion of other similar series comparators.

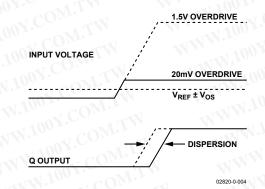


Figure 4. Propagation Delay Dispersion

#### **COMPARATOR HYSTERESIS**

The addition of hysteresis to a comparator is often useful in a noisy environment or where it is not desirable for the comparator to toggle between states when the input signal is at the switching threshold. The transfer function for a comparator with hysteresis is shown in Figure 5. If the input voltage approaches the threshold from the negative direction, the comparator will switch from a 0 to a 1 when the input crosses  $+V_H/2$ . The new switching threshold becomes  $-V_H/2$ . The comparator will remain in a 1 state until the threshold  $-V_H/2$  is crossed coming from the positive direction. In this manner, noise centered on 0 V input will not cause the comparator to switch states unless it exceeds the region bounded by  $\pm V_H/2$ .

Positive feedback from the output to the input is often used to produce hysteresis in a comparator (Figure 9). The major problem with this approach is that the amount of hysteresis varies with the output logic levels, resulting in a hysteresis that is not symmetrical around zero.

Another method to implement hysteresis is generated by introducing a differential voltage between the LATCH ENABLE and LATCH ENABLE inputs (Figure 10). Hysteresis generated in this manner is independent of output swing and is symmetrical around zero. The variation of hysteresis with input voltage is shown in Figure 6.

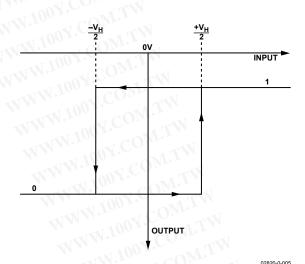
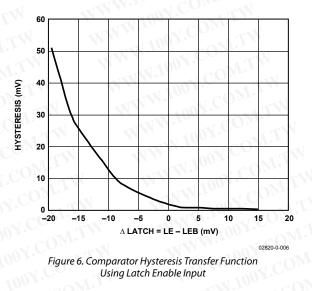


Figure 5. Comparator Hysteresis Transfer Function

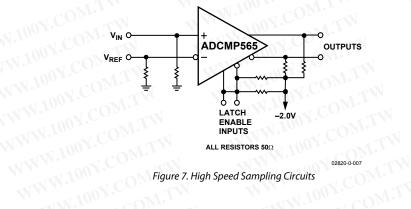


#### MINIMUM INPUT SLEW RATE REQUIREMENT

As for all high speed comparators, a minimum slew rate must be met to ensure that the device does not oscillate when the input crosses the threshold. This oscillation is due in part to the high input bandwidth of the comparator and the parasitics of the package. Analog Devices recommends a slew rate of 5 V/ $\mu$ s or faster to ensure a clean output transition. If slew rates less than 5 V/ $\mu$ s are used, then hysteresis should be added to reduce the oscillation.

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#### **TYPICAL APPLICATION CIRCUITS**



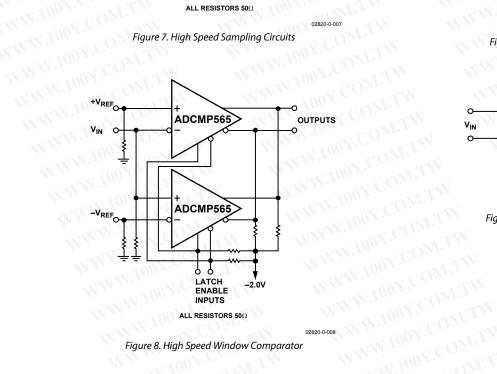


Figure 8. High Speed Window Comparator

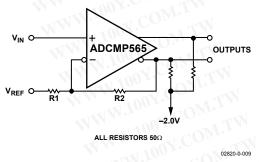
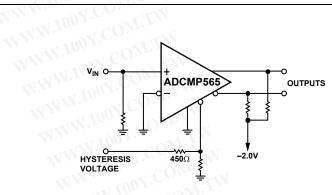


Figure 9. Hysteresis Using Positive Feedback WWW.100Y.COM



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ALL RESISTORS 50Ω UNLESS OTHERWISE NOTED

Figure 10. Hysteresis Using Latch Enable Input

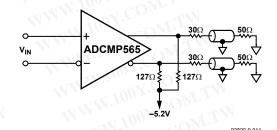
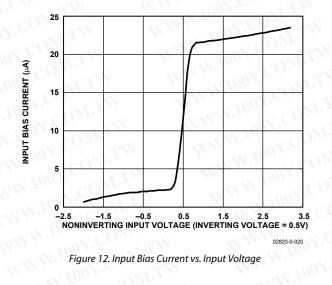
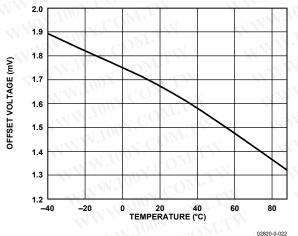


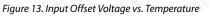
Figure 11. How to Interface an ECL Output to an Instrument with a 50  $\Omega$  to Ground Input

## **TYPICAL PERFORMANCE CHARACTERISTICS**

(V<sub>CC</sub> = +5.0 V, V<sub>EE</sub> = -5.2 V, T<sub>A</sub> =  $25^{\circ}$ C, unless otherwise noted.)







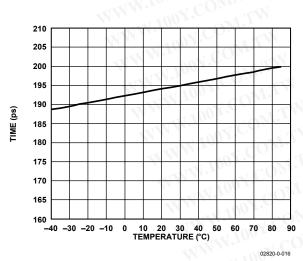
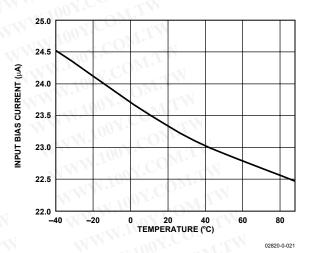
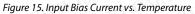
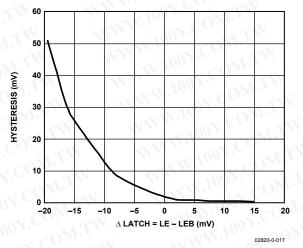


Figure 14. Rise Time vs. Temperature









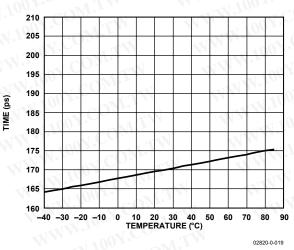
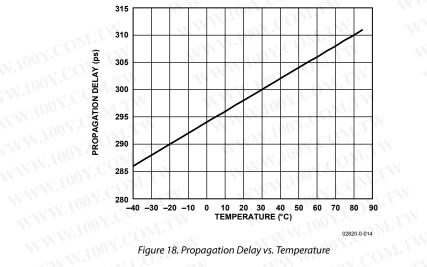
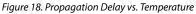


Figure 17. Fall Time vs. Temperature

Rev. 0 | Page 12 of 16





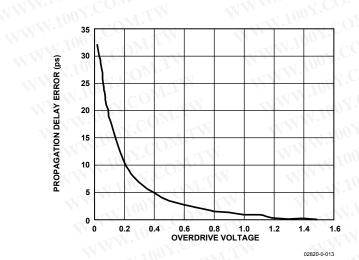


Figure 19. Propagation Delay Error vs. Overdrive Voltage

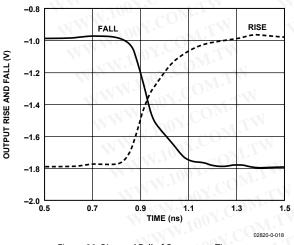
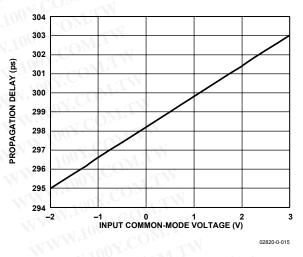


Figure 20. Rise and Fall of Outputs vs. Time WWW.100Y.COM.TW



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Figure 21. Propagation Delay vs. Common-Mode Voltage

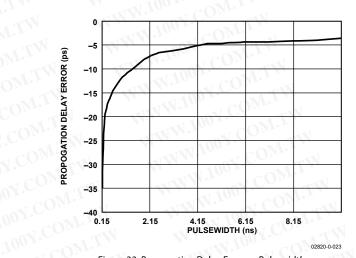
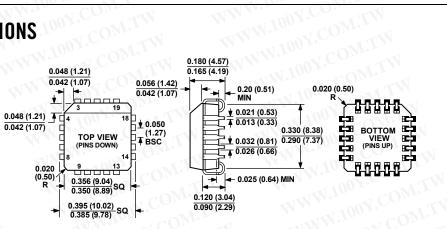


Figure 22. Propagation Delay Error vs. Pulsewidth

### **OUTLINE DIMENSIONS**



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Figure 23. 20-Lead Plastic Leaded Chip Carrier [PLCC] (P-20) Dimensions shown in inches and (millimeters)

# WW.100X.COM.TW **ORDERING GUIDE**

Model	Temperature Range	Package Description	Package Option
ADCMP565BP	-40°C to +85°C	20-Lead PLCC	P-20



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