élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

# EL2018/EL2018C

*Fast, High Voltage Comparator with Transparent Latch*



## Features

- Fast response time – 20 ns
- Wide input differential voltage range — 24 V on ±15 V supplies
- Precision input stage – $V_{OS}$ = 1 mV
- Low input bias current – $I_B$ = 100 nA
- Low input offset current – $I_{OS}$ = 30 nA
- ±4.5 V to ±18 V supplies
- 3 State TTL and CMOS compatible output
- No supply current glitch during switching
- High voltage gain – 40 V/mV
- 50% power reduction in shutdown mode
- Input and latch remain active in shutdown mode
- P/N compatible with industry standard comparators

## Applications

- Analog to digital converters
- ATE pin receiver
- Precision crystal oscillators
- Zero crossing detector
- Window detector
- Pulse width modulation generator
- "Go/no-go" detector

## Ordering Information

| Part No. | Temp. Range | Pkg. | Outline# |
|---|---|---|---|
| EL2018CH | −25 to +85°C | TO-99 | MDP0004 |
| EL2018CH/E+ | −25 to +85°C | TO-99 | MDP0004 |
| EL2018CJ | −25 to +85°C | Cerdip | MDP0010 |
| EL2018CJ/E+ | −25 to +85°C | Cerdip | MDP0010 |
| EL2018CN | −25 to +85°C | P-DIP | MDP0006 |
| EL2018CN/E+ | −25 to +85°C | P-DIP | MDP0006 |
| EL2018H | −55 to +125°C | TO-99 | MDP0004 |
| EL2018H/883B | −55 to +125°C | TO-99 | MDP0004 |
| EL2018J | −55 to +125°C | Cerdip | MDP0010 |
| EL2018J/883B | −55 to +125°C | Cerdip | MDP0010 |

## General Description

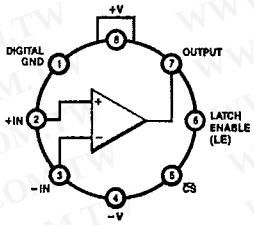
The EL2018 represents a quantum leap forward in comparator speed, accuracy and functionality. Manufactured with Elantec's proprietary Dielectric Isolation (DI) process, this device uses fast PNP and NPN transistors in the signal path. A unique circuit design gives the inputs the ability to handle large common mode and differential mode signals, yet retain high speed and excellent accuracy. Careful design of the front end insures the part maintains speed and accuracy when operating with a mix of small and large signals. The three-state output stage is designed to be TTL compatible for any power supply combination, yet it draws a constant current and does not generate glitches. When the output is disabled, the supply current consumption drops by 50%, but the input stage and latch remain active.

The EL2018 is available in 8 pin Cerdip, 8 pin plastic DIP, and 8 pin metal can packages.

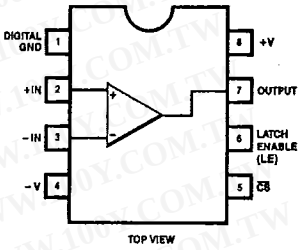
Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, see: *Elantec's Military Processing-Monolithic Products.*

## Connection Diagrams

**To-99 Metal Can**




**8-Pin CerDIP**
**8-Pin Plastic DIP**



# EL2018/EL2018C

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## Absolute Maximum Ratings ($T_A$ = 25°C)

| | | |
|---|---|---|
| $V_S$ | Supply Voltage | ±18 V |
| $V_{IN}$ | Input Voltage | $+V_S$ to $-V_S$ |
| $\Delta V_{IN}$ | Differential Input Voltage | Limited only by Power Supplies |
| $I_{IN}$ | Input Current (Pins 1, 2 or 3) | ± 10 mA |
| $I_{INS}$ | Input Current (Pins 5 or 6) | ±5 mA |
| $P_D$ | Maximum Power Dissipation (Note 4 – See Curves) | |
| | Cerdip | 1.5 Watts |
| | Metal Can | 1.0 Watt |
| | Plastic Dip | 1.25 Watts |
| $I_{OP}$ | Peak Output Current | 50 mA |
| $I_O$ | Continuous Output Current | 25 mA |
| $T_A$ | Operating Temperature Range: | |
| | EL2018 | −55°C to +125°C |
| | EL2018C | −25°C to +85°C |
| $T_J$ | Operating Junction Temperature | |
| | Ceramic Dip Package, Metal Can Package | +175°C |
| | Plastic Dip Package | +150°C |
| $T_{ST}$ | Storage Temperature | −65°C to +150°C |
| | Lead Temperature (Soldering, 5 Seconds) | +300°C |

**Important Note:** All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX 77 Series system. Unless otherwise noted, all tests are pulse tests, therefore $T_J = T_C = T_A$.

I 100% production tested and QA sample tested per QA test plan QCX0002,
II 100% production tested at $T_A$ = 25°C, and QA sample tested at $T_A$ = 25°C, $T_{MAX}$ and $T_{MIN}$ per QA test plan QCX0002.
III QA sample tested per QA test plan QCX0002.
IV Parameter is guaranteed (but not tested) by Design and Characterization Data
V Parameter is typical value at $T_A$ = 25°C for information purposes only.

## DC Electrical Characteristics $V_S$ = ±15 Volts unless otherwise specified

| Parameter | Description | Temp. | Min. | Typ. | Max. | Test Level EL2018 | Test Level EL2018C | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{os}$ | Input Offset Voltage (Note 1) | 25°C | | 1.0 | 3 | I | I | mV |
| | $V_{CM}$ = 0V, $V_O$ = 1.4 V | $T_{MIN}$,$T_{MAX}$ | | | 5 | I | III | mV |
| $I_B$ | Input Bias Current | 25°C | | 100 | 300 | I | I | nA |
| | $V_{CM}$ = 0V, pin 2 or 3 | $T_{MIN}$,$T_{MAX}$ | | | 500 | I | III | nA |
| $I_{os}$ | Input offset Current | 25°C | | 30 | 150 | I | I | nA |
| | $V_{CM}$ = 0V | $T_{MIN}$,$T_{MAX}$ | | | 250 | I | III | nA |
| CMRR | Common Mode Rejection Ratio | 25°C | 85 | 105 | | I | I | dB |
| | (Note 2) | $T_{MIN}$,$T_{MAX}$ | 80 | | | I | III | dB |
| PSRR | Power Supply Rejection Ratio | 25°C | 85 | 100 | | I | I | dB |
| | (Note 3) | $T_{MIN}$,$T_{MAX}$ | 80 | | | I | III | dB |
| $V_{CM}$ | Common Mode Input Range | 25°C | ±12 | ±13 | | I | I | V |
| | | $T_{MIN}$,$T_{MAX}$ | ±12 | | | I | III | V |
| $A_v$ | Voltage Gain | 25°C | 15 | 40 | | I | I | V/mV |
| | $V_{out}$ = 0.8 to 2.0 V | $T_{MIN}$,$T_{MAX}$ | 10 | | | I | III | V/mV |
| $V_{ol}$ | Output Voltage logic low | 25°C | 0 | 0.15 | 0.4 | I | I | V |
| | $I_{ol}$ = 0 mA to 8 mA | $T_{MIN}$,$T_{MAX}$ | 0 | | 0.4 | I | III | V |
| $V_{oh}$ | Output Voltage logic High | | | | | | | |
| | Vs = ±15 V | 25°C | 3.5 | 4.0 | 4.5 | I | I | V |
| | Vs = ±15 V | $T_{MIN}$,$T_{MAX}$ | 3.5 | | 4.5 | I | III | V |
| | Vs = ±5 V | 25°C | 2.7 | 3.0 | 3.3 | I | I | V |
| | Vs = ±5 V | $T_{MIN}$ | 2.4 | | 3.5 | I | III | V |
| | Vs = ±5 V | $T_{MAX}$ | 2.4 | | 3.05 | I | III | V |

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## DC Electrical Characteristics — (Continued)

| Parameter | Description | Temp. | Min. | Typ. | Max. | Test Level EL2018 | Test Level EL2018C | Units |
|---|---|---|---|---|---|---|---|---|
| Vodis1 | Vout Range, Disabled, $I_{ol}$ = −1mA | | | | | | | |
| | Vs = ±15 V | 25°C | 4.8 | | | I | I | V |
| | Vs = ±15 V | $T_{MIN}$,$T_{MAX}$ | 4.6 | | | I | III | V |
| | Vs = ±5 V | 25°C | | 3.5 | | V | V | V |
| Vodis2 | Vout Range, Disabled, $I_{ol}$ = +1mA | | | | | | | |
| | Vs = ±5 to ±15 | ALL | −0.3 | −1 | | I | II | V |
| $V_{inh}$ | LE or $\overline{CS}$ inputs | 25°C | 2.0 | | | I | I | V |
| | Logic High Input Voltage | $T_{MIN}$,$T_{MAX}$ | 2.0 | | | I | III | V |
| $V_{inl}$ | LE or $\overline{CS}$ inputs | 25°C | | | 0.8 | I | I | V |
| | Logic Low Input Voltage | $T_{MIN}$,$T_{MAX}$ | | | 0.8 | I | III | V |
| $I_{in}$ | LE or $\overline{CS}$ inputs | 25°C | | | ±200 | I | I | μA |
| | Logic Input Current $V_{in}$ = 0V to 5V | $T_{MIN}$,$T_{MAX}$ | | | ±300 | I | III | μA |
| $I_{s+en}$ | Positive supply current Enabled | 25°C | | 8.4 | 10 | I | I | mA |
| | | $T_{MIN}$,$T_{MAX}$ | | | 11 | I | III | mA |
| $I_{s+dis}$ | Positive supply current Disabled | 25°C | | 4.7 | 6 | I | I | mA |
| | | $T_{MIN}$,$T_{MAX}$ | | | 7 | I | III | mA |
| $I_{s-en}$ | Negative supply current Enabled | 25°C | | 13.0 | 17 | I | I | mA |
| | | $T_{MIN}$,$T_{MAX}$ | | | 18 | I | III | mA |
| $I_{s-dis}$ | Negative supply current Disabled | 25°C | | 5.0 | 6.5 | I | I | mA |
| | | $T_{MIN}$,$T_{MAX}$ | | | 6.5 | I | III | mA |

## AC Electrical Characteristics $V_S$ = ± 15 Volts, $T_A$ = 25°C

| Parameter | Description | Min | Typ | Max | Test Level EL2018 | Test Level EL2018C | Units |
|---|---|---|---|---|---|---|---|
| $T_{pd}$ | Propagation Delay, 5 mV overdrive | | 20 | 30 | I | III | ns |
| $T_s$ | Setup Time | | 6 | 12 | I | III | ns |
| $T_h$ | Hold Time | | −2 | 0 | I | III | ns |
| $T_{un}$ | Unlatch Time | | 23 | 30 | I | III | ns |
| $T_{mpw}$ | Minimum clock pulse width | | 12 | | V | V | ns |
| $T_{en}$ | Output 3-State enable delay | | 30 | 50 | I | III | ns |
| $T_{dis}$ | Output 3-State disable delay | | 50 | 200 | I | III | ns |

Note 1: $V_{out}$ = 1.4 V
Note 2: $V_{cm}$ = +12 V to −12 V
Note 3: $V_s$ = ±5 V to ±15 V
Note 4: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the Typical Performance curves for more details.

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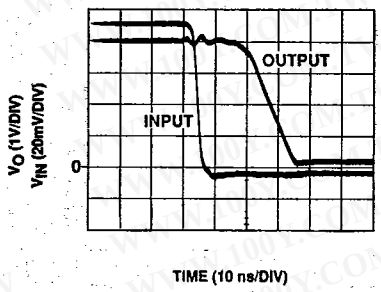
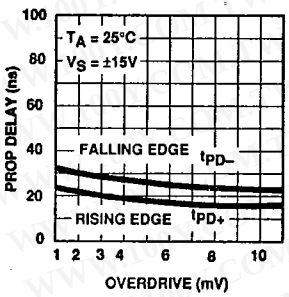
## Typical AC Performance Curves

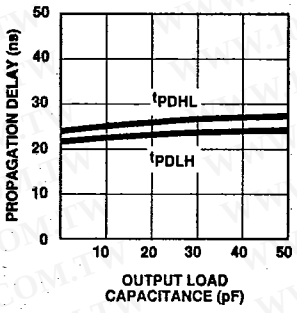
**Propagation Delay (–) 5 mV Overdrive**



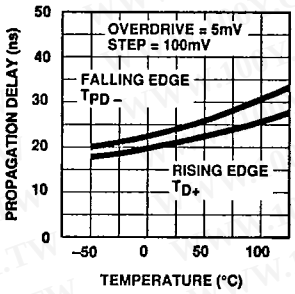

**Propagation Delay vs Overdrive**



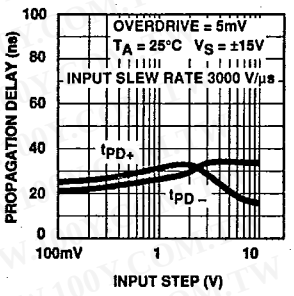

**Propagation Delay vs Load Capacitance**



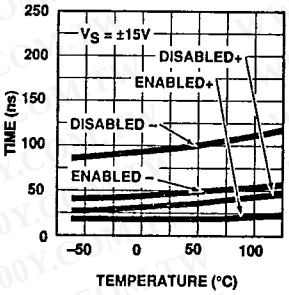

**Propagation Delay vs Temperature**




**Propagation Delay vs Input Step**




**Enabled/ Disabled Time vs Temperature**



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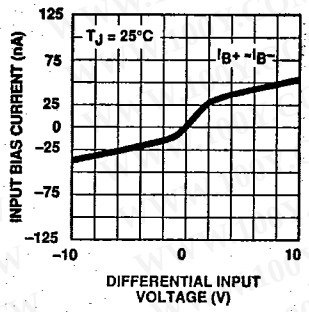
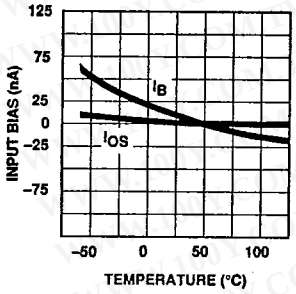
## Typical AC Performance Curves — (Continued)

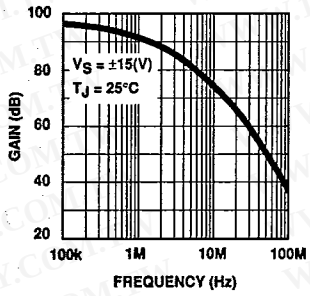
**Input Bias Current vs Differential Input Voltage**



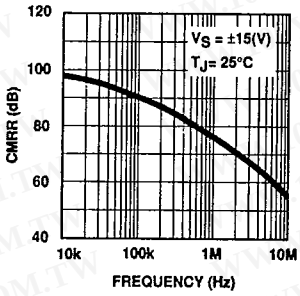

**Input Bias Current vs Temperature**



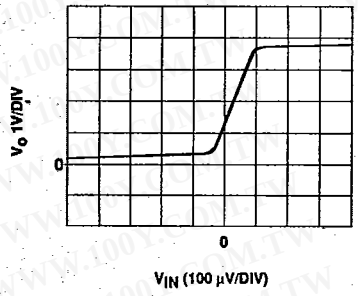

**Open-Loop Gain vs Frequency**



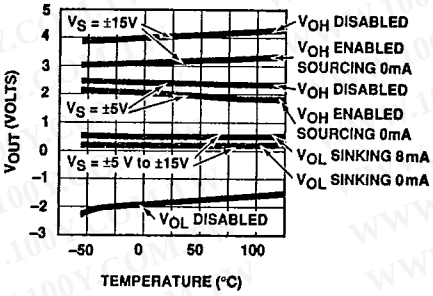

**CMRR vs Frequency**




**$V_O/V_I$ Transfer Characteristic**




**$V_{OUT}$ vs Temperature**



# EL2018/EL2018C

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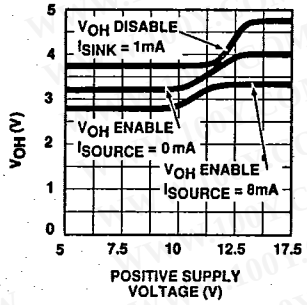
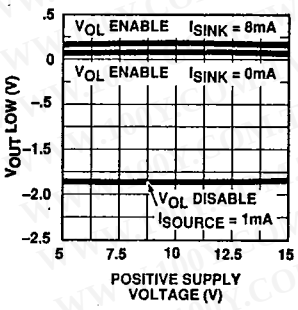
## Typical AC Performance Curves — (Continued)

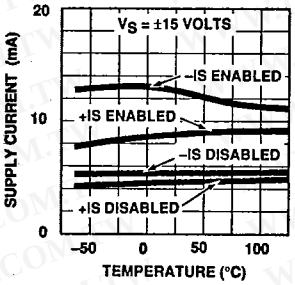
**$V_{OH}$ vs Positive Supply Voltage**



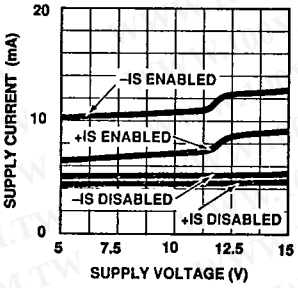

**$V_{OL}$ vs Positive Supply Voltage**



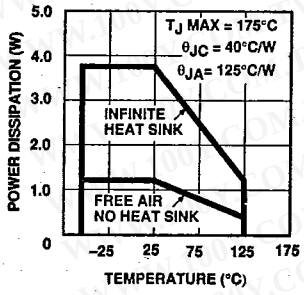

**Supply Current vs Temperature**



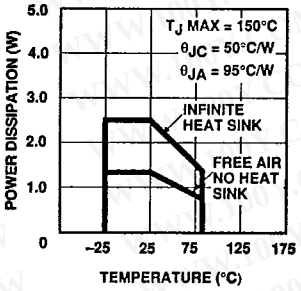

**Supply Current vs Supply Voltage**



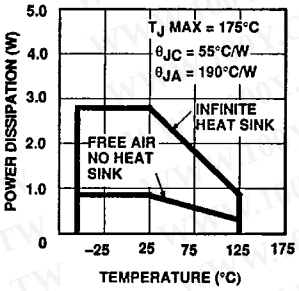

**8-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature**




**8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature**




**8-Lead TO-99 Metal Can Maximum Power Dissipation vs Ambient Temperature**

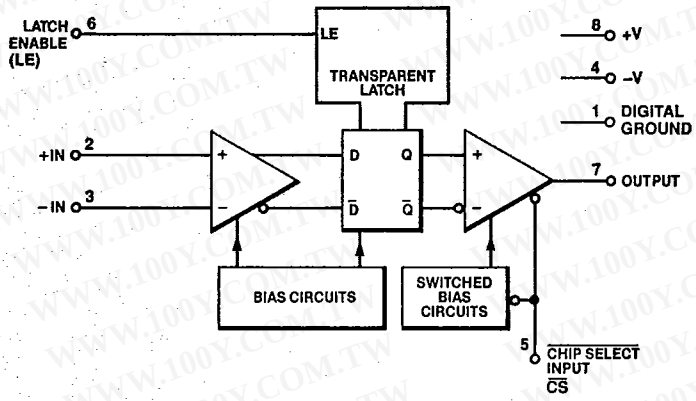


# EL2018/EL2018C

*Fast, High Voltage Comparator with Transparent Latch*



## Block Diagram




## Function Table

| INPUTS (time n–1) | | | | Internal Q | Notes | OUTPUT |
|---|---|---|---|---|---|---|
| +IN | –IN | $\overline{CS}$ | LE | | | |
| + | – | L | L | H | Normal Comparator Operation | H |
| – | + | L | L | L | | L |
| + | – | H | L | H | Internal Normal Comparator Operation | High Z |
| – | + | H | L | L | Output Power Down Mode | High Z |
| X | X | L | H | Qn–1 | Data Retained in latch | Qn–1 |
| X | X | H | H | Qn–1 | Data Retained in latch Power Down Mode | High Z |

## Application Hints

### Device Overview

The EL2018 is the first comparator of its kind. It is capable of 24 V differential signals, yet has excellent accuracy, linearity and voltage gain. It even has a 3-state output feature that reduces the power supply currents 50% when the output is disabled, yet the input stage and latch remain active. This extremely fast and accurate device is built with the proprietary Elantec Complementary Bipolar Dielectric Isolation Process, which is immune to power sequencing and latch up problems.

### Power Supplies

The EL2018 will work with ±5 V to ±18 V supplies or any combination between (Example +12 V & –5 V). The supplies should be well bypassed with good high frequency capacitors (.01 μF monolithic ceramic recommended) close to the power supply leads. Good ground plane construction techniques enhance stability, and the lead from pin 1 to ground should be short.

### Front end

The EL2018 uses schottky diodes to make a "bullet proof" front end with very low input bias currents, even if the two inputs are tied to very large differential voltages (±24 V). The transfer function of the EL2018 is linear, and the output is stable when in the linear region.

The large common mode range (±12 V minimum) and differential voltage handling ability (±24 V min.) of the device make it useful in ATE applications without the need for an input attenuator with its associated delay.

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## Application Hints

**Recovery from large overdrives**
Timing accuracy is excellent for all signals within the common mode range of the device (±12 V with ±15 V supply). When the common mode range is exceeded the input stage will saturate, input bias currents increase and it may take as much as 200 nS for the device to recover to normal operation after the inputs are returned to the common mode range. If signals greater than the common mode range of the device are anticipated, the inputs should be diode clamped to remain within the common mode range of the device.

**Input slew rate**
All comparators have input slew rate limitations. The EL2018 operates normally with any input slew rate up to 300 V/μs. Input signal slew rates over 300 V/μs induce offset voltages of 5 to 20 mV. This induced offset voltage settles out in about 20 ns, 20 times faster than previous high voltage comparators.

**Latch**
The EL2018 contains a "transparent" latch. A "transparent" latch acts as an amplifier when the LE input is low and it "latches" and holds the value it had just before the LE transition from low to high.

It is possible to make an oscillation resistant design by putting a short duration "0" on the LE input whenever you wish to make a comparison. This gates the comparator on only for a brief instant, long enough to compare, but not long enough to oscillate. The minimum duration of this pulse is specified by the minimum clock width parameter in the AC electrical tables.

The $\overline{CS}$ input may be left floating and still produce a guaranteed logic "0" input (active). Floating the LE input will normally produce a logic "0" input also, but operation is not guaranteed.

Proper RF technique suggests that these inputs be grounded or pulled to ground if they are not used.

**Output stage**
The output stage of the EL2018 is a pair of complementary emitter followers operating as a linear amplifier. This makes the output stage of the EL2018 glitch free, and improves accuracy and stability when operating with small signals.

**3-State Output, Power Saving Feature**
The EL2018 has an output stage which can be put into a high impedance "3-state" mode. When it is in this mode, the input stage and latch remain active, yet the device dissipates only 50% of the power used when the output is active. This has advantages in a large ATE system where there may be 1000 comparators, but only 10% are in use at any one time.

Due to the power saving feature and linear output stage, the EL2018 does not have a standard TTL 3-state output stage. As such one must be careful when using the 3-state feature with devices other than other EL2018's or EL2019's. When operating from ±15 V supplies the 3-state feature is compatible with all TTL families, however CMOS families may conflict on high outputs. Since the output stage of the EL2018 turns on faster than it turns off, a 50Ω to 100Ω resistor in series with the output will limit fault currents between devices with minimum impact on logic drive capability.

**System design considerations**
The most common problem users have with high speed comparators is oscillations due to output to input feedback. This can be avoided by using a ground plane, proper supply bypassing, and routing the inputs and outputs away from each other. Since the EL2018 has a gain bandwidth product of about 40 GHz, layout and bypassing are important to a successful system design. A unique alternative to the EL2018 is the EL2019, with its edge triggered master slave flip flop.

**Device Functions**
The various operating states of the EL2018 are described in the function table above.

# EL2018/EL2018C

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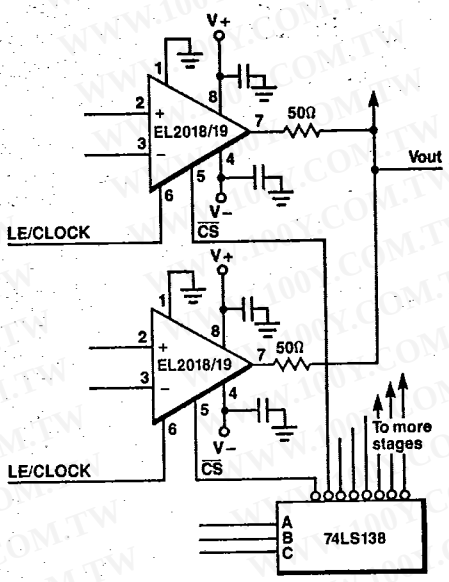
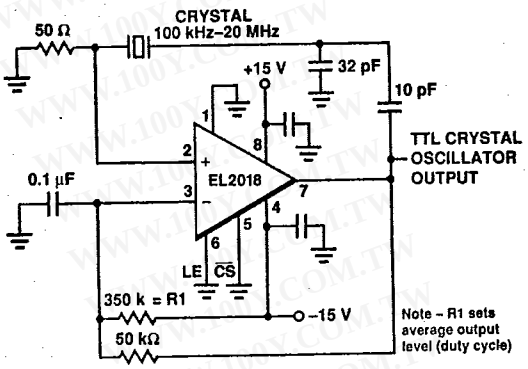
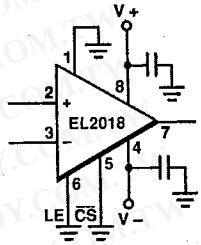
## Typical Applications



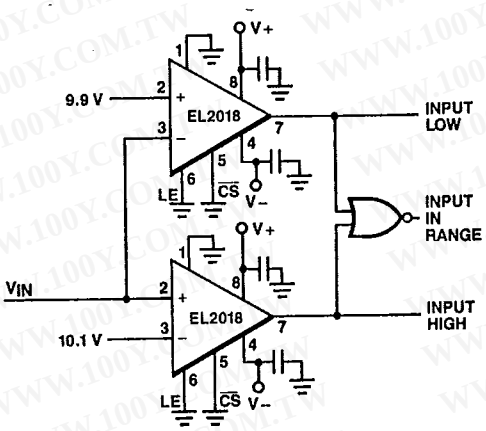

Using the Power Down/ 3 State Feature




Series Resonant Crystal Oscillator




Using the EL2018 in the Transparent Mode (latch not used)

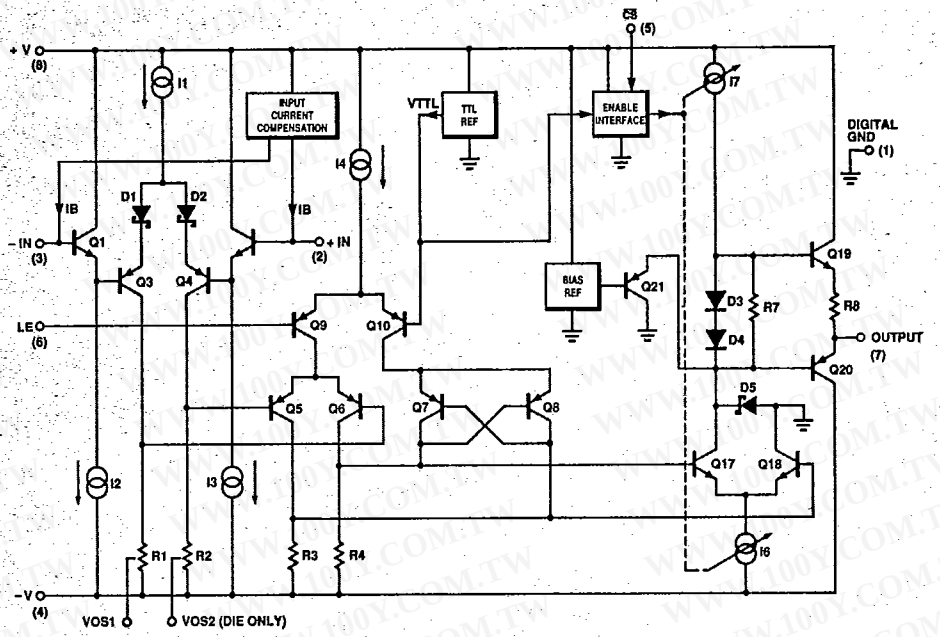



A Wide Input Range Window Comparator ($V_{IN}$ Range +12 V to −12 V with $V_S$ = ±15 V

# EL2018/EL2018C

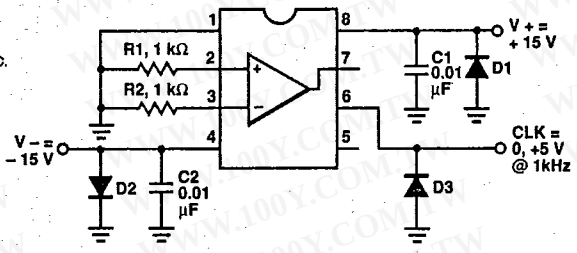
*Fast, High Voltage Comparator with Transparent Latch*

## Equivalent Schematic

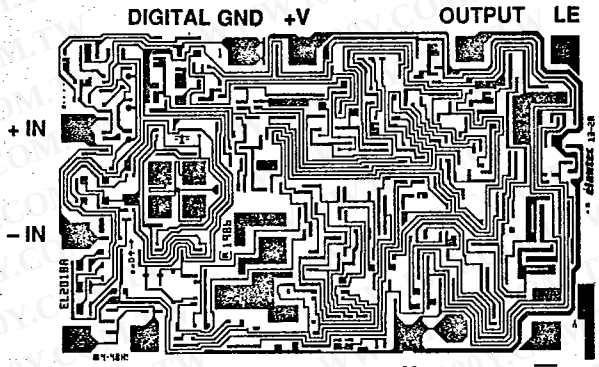



## Burn-In Circuit

PIN NUMBERS ARE FOR DIP PACKAGES.
ALL PACKAGES USE THE SAME SCHEMATIC.




## Die Layout




DIE SIZE: 97 x 62 MILS