CA3290, CA3290A

November 1996

BiMOS Dual Voltage Comparators with MOSFET Input, Bipolar Output

Features

- **MOSFET Input Stage**
  - **Very High Input Impedance (Z_{IN}). . . . . . . 1.7TΩ (Typ)**
  - **Very Low Input Current at V+ = 5V . . . . . 3.5pA (Typ)**
  - **Wide Common Mode Input Voltage Range (V_{ICR}) Can Be Swung 1.5V (Typ) Below Negative Supply Voltage Rail**
  - **Virtually Eliminates Errors Due to Flow of Input Currents**
- **Output Voltage Compatible with TTL, DTL, ECL, MOS, and CMOS Logic Systems in Most Applications**

Applications

- **High Source Impedance Voltage Comparators**
- **Long Time Delay Circuits**
- **Square Wave Generators**
- **A/D Converters**
- **Window Comparators**

Description

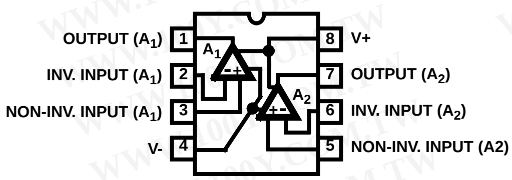
The CA3290A and CA3290 types consist of a dual voltage comparator on a single monolithic chip. The common mode input voltage range includes ground even when operated from a single supply. The low supply current drain makes these comparators suitable for battery operation; their extremely low input currents allow their use in applications that employ sensors with extremely high source impedances. Package options are shown in the table below.

Ordering Information

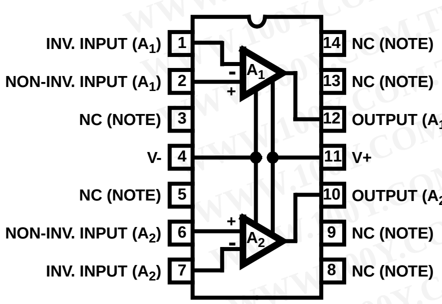
PART NUMBER	TEMP RANGE (^oC)	PACKAGE	PKG. NO.
CA3290AE	-55 to 125	8 Ld PDIP	E8.3
CA3290AE1	-55 to 125	14 Ld PDIP	E14.3
CA3290AT	-55 to 125	8 Pin Metal Can	T8.C
CA3290E	-55 to 125	8 Ld PDIP	E8.3
CA3290T	-55 to 125	8 Pin Metal Can	T8.C

Pinouts

CA3290/A (PDIP)
TOP VIEW

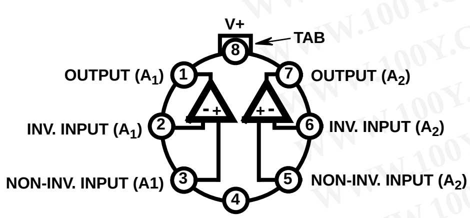


CA3290A (PDIP)
TOP VIEW



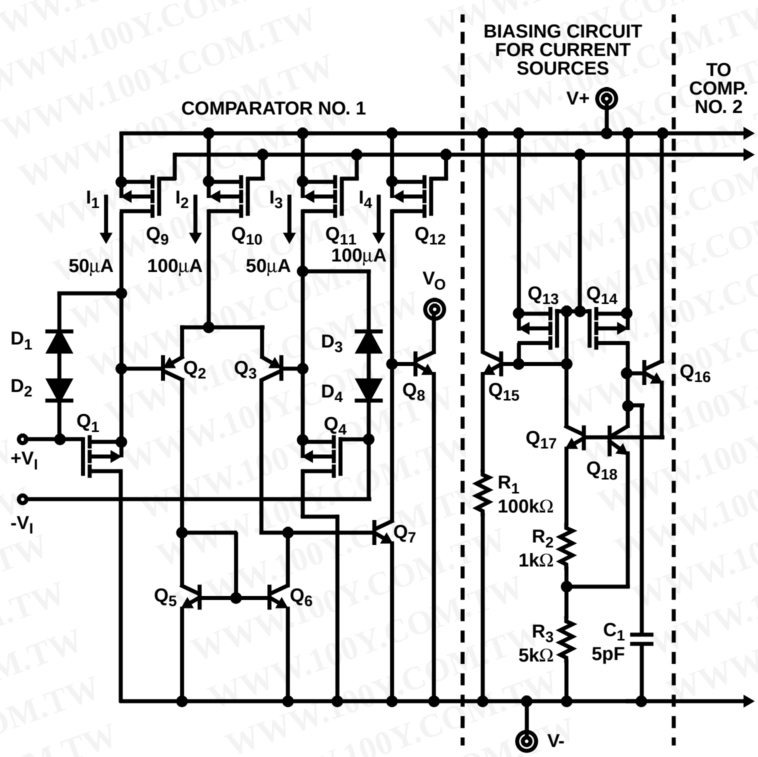
NOTE: Tie to GND or V+ for best Input/Output Isolation.

CA3290A, CA3290 (METAL CAN)
TOP VIEW



Schematic Diagram

(ONLY ONE IS SHOWN)



Absolute Maximum Ratings

Supply Voltage
- Single Supply . . . . +36V
- Dual Supply . . . . ±18V

Differential Input Voltage . . . . 36V or [(V+ - V-) +5V] (whichever is less)

DC Input Voltage . . . . V+ +5V to V- -5V

Output to V- Short Circuit Duration (Note 1) . . . . Continuous

Input Current 1mA

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
14 Lead PDIP Package	100	N/A
8 Lead PDIP Package	120	N/A
8 Pin Metal Can Package	155	67

Maximum Junction Temperature (Can) . . . . 175°C

Maximum Junction Temperature (Plastic Package) . . . . 150°C

Maximum Storage Temperature Range . . . . -65°C to 150°C

Maximum Lead Temperature (Soldering 10s) . . . . 300°C

Operating Conditions

Temperature Range . . . . -55 to 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Short circuits from the output to V+ can cause excessive heating and eventual destruction of the device.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

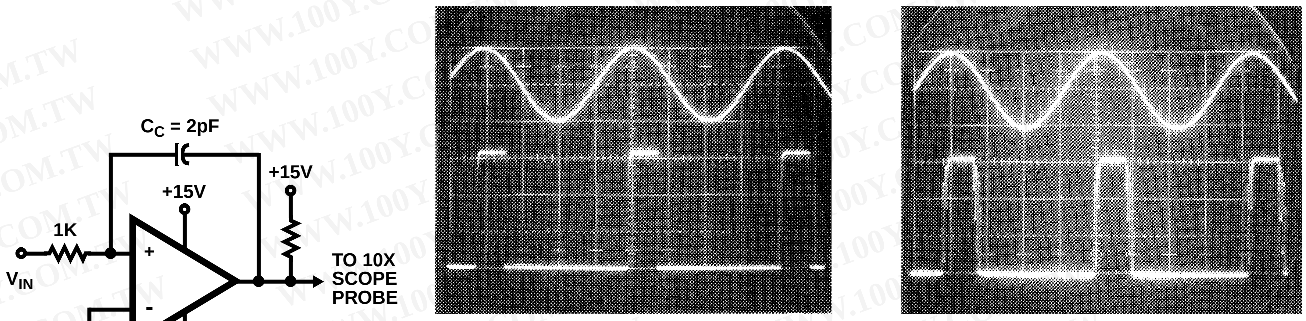
V- = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	CA3290A			CA3290			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	V_{CM} = V_O = 1.4V, V+ = 5V	Full	-	4.5	-	-	8.5	-	mV
		V_{CM} = V_O = 0V, V+ = +15V, V- = -15V	Full	-	8.5	-	-	8.5	-	mV
		V_{CM} = V_O = 1.4V, V+ = 5V	25	-	4.0	10	-	7.5	20	mV
		V_{CM} = V_O = 0V, V+ = +15V, V- = -15V	25	-	4.0	10	-	7.5	20	mV
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$			-	8	-	-	8	-	µV/°C
Input Offset Current	I_{IO}	V_{CM} = 1.4V, V+ = 5V	Full	-	2	28	-	2	32	nA
		V_{CM} = 0V, V+ = +15V, V- = -15V	Full	-	7	28	-	7	32	nA
		V_{CM} = 1.4V, V+ = 5V	25	-	2	25	-	2	30	pA
		V_{CM} = 0V, V+ = +15V, V- = -15V	25	-	7	25	-	7	30	pA
Input Current	I_I	V_{CM} = 1.4V, V+ = 5V	125	-	2.8	45	-	2.8	55	nA
		V_{CM} = 0V, V+ = +15V, V- = -15V	125	-	13	45	-	13	55	nA
		V_{CM} = 1.4V, V+ = 5V	25	-	3.5	40	-	3.5	50	pA
		V_{CM} = 0V, V+ = +15V, V- = -15V	25	-	12	40	-	12	50	pA

Electrical Specifications V- = 0V, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (^{o}C)	CA3290A			CA3290			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current	I+	R_L = ∞, V+ = 5V	-55	-	0.85	1.0	-	0.85	1.6	mA
		R_L = ∞, V+ = 30V	-55	-	1.62	3.0	-	1.62	3.5	mA
		R_L = ∞, V+ = 5V	25	-	0.8	1.4	-	0.8	1.4	mA
		R_L = ∞, V+ = 30V	25	-	1.35	3.0	-	1.35	3.0	mA
Voltage Gain	A_{OL}	R_L = 15kΩ, V+ = +15V, V- = -15V	Full	-	150	-	-	150	-	V/mV
				-	103	-	-	103	-	dB
		R_L = 15kΩ, V+ = +15V, V- = -15V	25	25	800	-	25	800	-	V/mV
				88	118	-	88	118	-	dB
Saturation Voltage	V_{SAT}	I_{SINK} = 4mA, V+ = 5V, $+V_I$ = 0V, $-V_I$ = 1V	125	-	0.22	0.7	-	0.22	0.7	V
		I_{SINK} = 4mA, V+ = 5V, $+V_I$ = 0V, $-V_I$ = 1V	-55	-	0.1	-	-	0.1	-	V
		I_{SINK} = 4mA, V+ = 5V, $+V_I$ = 0V, $-V_I$ = 1V	25	-	0.12	0.4	-	0.12	0.4	V
Output Leakage Current	I_{OL}	V+ = 15V	Full	-	65	-	-	65	-	nA
		V+ = 36V	Full	-	130	1k	-	130	1k	nA
		V+ = 15V	25	-	100	-	-	100	-	pA
		V+ = 36V	25	-	500	-	-	500	-	pA
Common Mode Input Voltage Range	V_{ICR}	V_O = 1.4V, V+ = 5V	25	V+-3.5 V-	V+-3.1 V- -1.5	-	V+-3.5 V-	V+-3.1 V- -1.5	-	V
		V_O = 0V, V+ = +15V, V- = -15V	25	V+-3.8 V-	V+-3.4 V- -1.6	-	V+-3.8 V-	V+-3.4 V- -1.6	-	V
Common Mode Rejection Ratio	CMRR	V+ = +15V, V- = -15V	25	-	44	562	-	44	562	μV/V
		V+ = 5V	25	-	100	562	-	100	562	μV/V
Power Supply Rejection Ratio	PSRR	V+ = +15V, V- = -15V	25	-	15	316	-	15	316	μV/V
Output Sink Current		V_O = 1.4V, V+ = 5V	25	6	30	-	6	30	-	mA
Response Time Rising Edge	t_r	R_L = 5.1kΩ, V+ = 15V	25	-	1.2	-	-	1.2	-	μs
Response Time Falling Edge	t_f	R_L = 5.1kΩ, V+ = 15V	25	-	200	-	-	200	-	ns
Large Signal Response Time		R_L = 5.1kΩ, V+ = 15V	25	-	500	-	-	500	-	ns
		R_L = 5.1kΩ, V+ = 5V	25	-	400	-	-	400	-	ns

Test Circuits and Waveforms



WITH C_C
Top Trace ≈ 4.5mV/Div. = V_{IN}
Bottom Trace = 10V/Div. = V_{OUT}
Time Scale = 5µs/Div.

WITHOUT C_C
Top Trace ≈ 4.5mV/Div.
Bottom Trace = 10V/Div.
Time Scale = 5µs/Div.

FIGURE 1. PARASITIC OSCILLATIONS TEST CIRCUIT AND WAVEFORMS

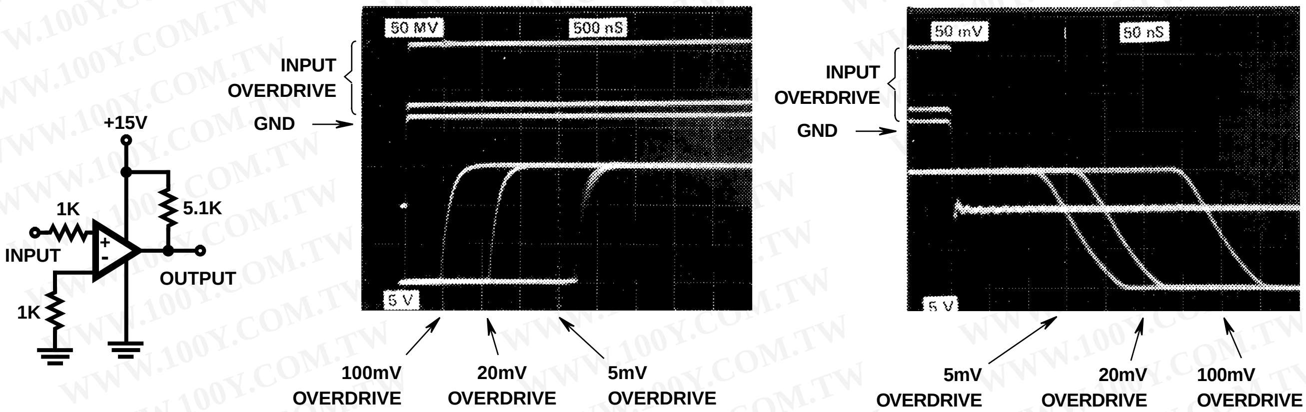


FIGURE 2. NON-INVERTING COMPARATOR RESPONSE TIME TEST CIRCUIT AND WAVEFORMS

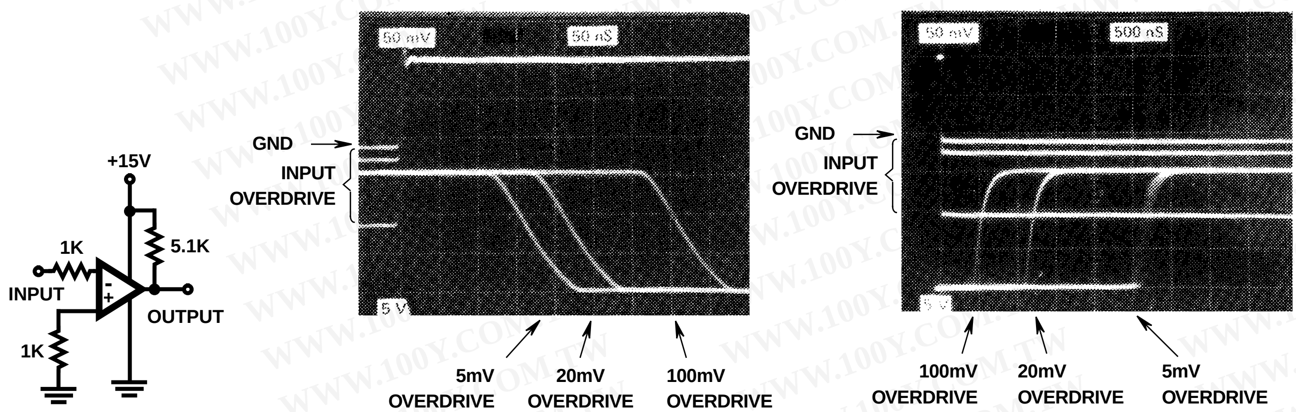


FIGURE 3. INVERTING COMPARATOR RESPONSE TIME TEST CIRCUIT AND WAVEFORMS

Circuit Description

The Basic Comparator

Figure 4 shows the basic circuit diagram for one of the two comparators in the CA3290. It is generically similar to the industry type "139" comparators, with PMOS transistors replacing PNP transistors as input stage elements. Transistors Q_1 through Q_4 comprise the differential input stage, with Q_5 and Q_6 serving as a mirror connected active load and differential-to-single-ended converter. The differential input at Q_1 and Q_4 is amplified so as to toggle Q_6 in accordance with the input signal polarity. For example, if $+V_{IN}$ is greater than $-V_{IN}$, Q_1, Q_2, and current mirror transistors Q_5 and Q_6 will be turned off; Transistors Q_3, Q_4, and Q_7 will be turned on, causing Q_8 to be turned off. The output is pulled positive when a load resistor is connected between the output and V+.

In essence, Q_1 and Q_4 function as source followers to drive Q_2 and Q_3, respectively, with zener diodes D_1 through D_4 providing gate oxide protection against input voltage transients (e.g., static electricity). The current flow in Q_1 and Q_4 is established at approximately 50µA by constant current sources I_1 and I_3, respectively. Since Q_1 and Q_4 are operated with a constant current load, their gate-to-source voltage drops will be effectively constant as long as the input voltages are within the common-mode range.

As a result, the input offset voltage ($V_{GS(Q1)} + V_{BE(Q2)} - V_{BE(Q3)} - V_{GS(Q4)}$) will not be degraded when a large differential DC voltage is applied to the device for extended periods of time at high temperatures.

Additional voltage gain following the first stage is provided by transistors Q_7 and Q_8. The collector of Q_8 is open, offering the user a wide variety of options in applications. An additional discrete transistor can be added if it becomes necessary to boost the output sink current capability.

The detailed schematic diagram for one comparator and the common current source biasing is shown on the front page. PMOS transistors Q_9 through Q_{12} are the current source elements identified in Figure 4 as I_1 through I_4, respectively. Their gate source potentials (V_{GS}) are supplied by a common bus from the biasing circuit shown in the right hand portion of the Schematic Diagram. The currents supplied by Q_{10} and Q_{12} are twice those supplied by Q_9 and Q_{11}. The transistor geometries are appropriately scaled to provide the requisite currents with common V_{GS} applied to Q_9 through Q_{12}.

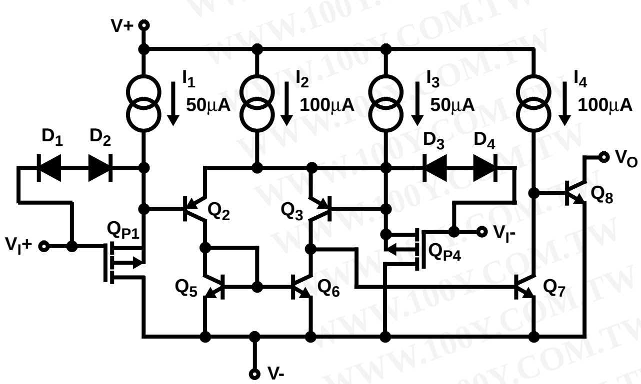


FIGURE 4. BASIC CIRCUIT DIAGRAM FOR ONE OF THE TWO COMPARATORS

Operating Considerations

Input Circuit

The use of MOS transistors in the input stage of the CA3290 series circuits provides the user with the following features for comparator applications:

1. Ultra high input impedance (≅1.7TΩ);
2. The availability of common mode rejection for input signals at potentials below that of the negative power supply rail;
3. Retention of the in phase relationship of the input and output signals for input signals below the negative rail.

Although the CA3290 employs rugged bipolar (zener) diodes for protection of the input circuit, the input terminal currents should not exceed 1mA. Appropriate series connected limiting resistors should be used in circuits where greater current flows might exist, allowing the signal input voltage to be greater than the supply voltage without damaging the circuit.

Output Circuit

The output of the CA3290 is the open collector of an n-p-n transistor, a feature providing flexibility in a broad range of comparator applications. An output ORing function can be implemented by parallel connection of the open collectors. An output pull-up resistor can be connected to a power supply having a voltage range within the rating of the particular CA3290 in use; the magnitude of this voltage may be set at a value which is independent of that applied to the V+ terminal of the CA3290.

Parasitic Oscillations

The ideal comparator has, among other features, ultra high input impedance, high gain, and wide bandwidth. These desirable characteristics may, however, produce parasitic oscillations unless certain precautions are observed to minimize the stray capacitive coupling between the input and output terminals. Parasitic oscillations manifest themselves during the output voltage transition intervals as the comparator switches states. For high source impedances, stray capacitance can induce parasitic oscillations. The addition of a small amount (1mV to 10mV) of positive feedback (hysteresis) produces a faster transition, thereby reducing the likelihood of parasitic oscillations. Furthermore, if the input signal is a pulse waveform, with relatively rapid rise and fall times, parasitic tendencies are reduced.

When dual comparators, like the CA3290, are packaged in an 8 lead configuration, the output terminal of each comparator is adjacent to an input terminal. The lead-to-lead capacitance is approximately 1pF, which may be sufficient to cause undesirable feedback effects in certain applications. Circuit factors such as impedance levels, supply voltage, switching rate, etc., may increase the possibility of parasitic oscillations. To minimize this potential oscillatory condition, it is recommended that for source impedances greater than 1kΩ a capacitor (≥1pF - 2pF) be connected between the appropriate input terminal and the output terminal. (See Figure 1.)

The CA3290A is also supplied in a 14 lead dual-in-line plastic package. To minimize the possibility of parasitic oscillations the input and output terminals are positioned on opposite sides of the package. In addition, there are two leads between the output terminal of each comparator and its corresponding inverting input terminal, reducing the input/output coupling significantly. These leads (8, 9, 13, 14) should be tied to either the V+ or V- supply rail. If either comparator is unused, its input terminals should also be tied to either the V+ or V- supply rail.

Typical Applications

Light Controlled One-Shot Timer

In Figure 5 one comparator (A_1) of the CA3290 is used to sense a change in photo diode current. The other comparator (A_2) is configured as a one-shot timer and is triggered by the output of A_1. The output of the circuit will switch to a low state for approximately 60 seconds after the light source to the photo diode has been interrupted. The circuit operates at normal room lighting levels. The sensitivity of the circuit may be adjusted by changing the values of R_1 and R_2. The ratio of R_1 to R_2 should be constant to insure constant reverse voltage bias on the photo diode.

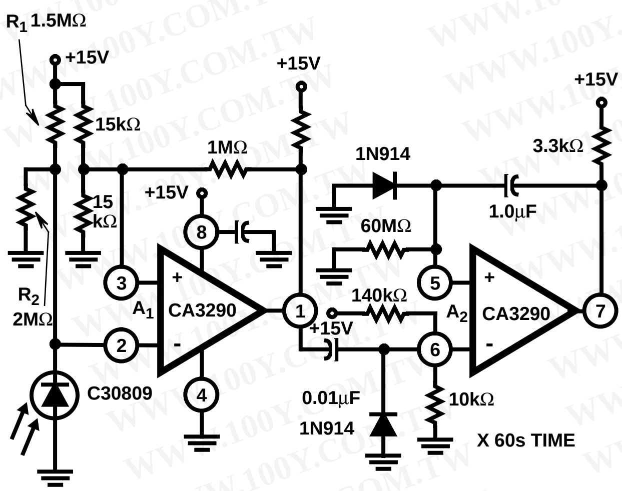


FIGURE 5. LIGHT CONTROLLED ONE-SHOT TIMER

Low-Frequency Multivibrator

In this application, one half of the CA3290 is used as a conventional multivibrator circuit. Because of the extremely high input impedance of this device, large values of timing resistor (R_1) may be used for long time delays with relatively small leakage timing capacitors. The second half of the CA3290 is used as an output buffer to insure that the multivibrator frequency will not be affected by output loading. R_P is the parallel combination of the two 1MΩ resistors connected between +15V and GND.

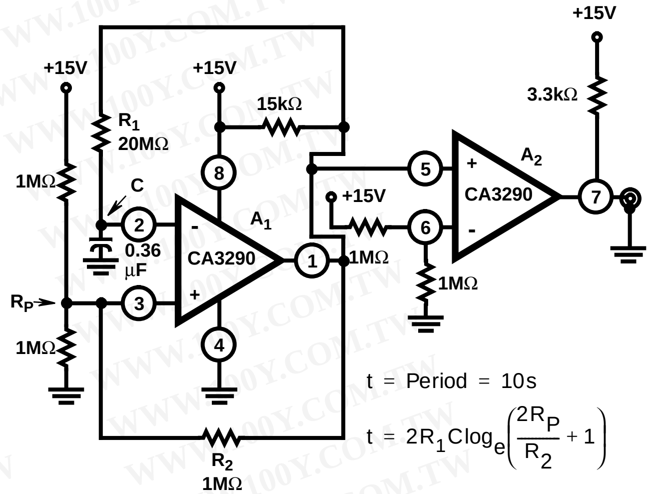


FIGURE 6. LOW FREQUENCY MULTIVIBRATOR

Window Comparator

Both halves of the CA3290 can be used in a high input impedance window comparator as shown in Figure 7. The LED will be turned "on" whenever the input signal is above the lower limit (V_L) but below the upper limit (V_U), as determined by the $R_1/R_2/R_3$ resistor divider.

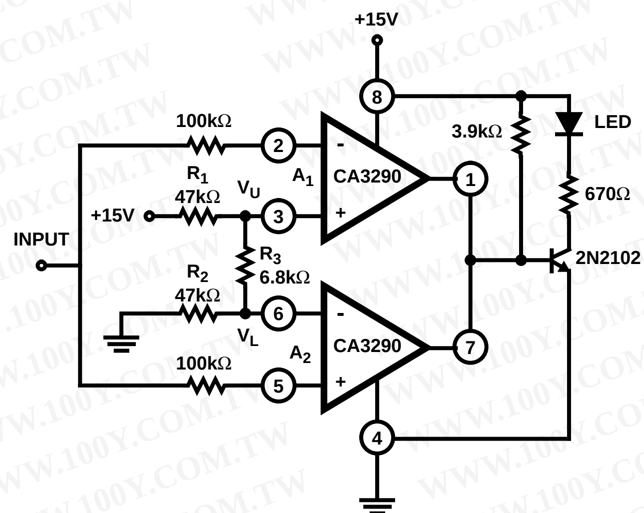


FIGURE 7. WINDOW COMPARATOR

Typical Performance Curves

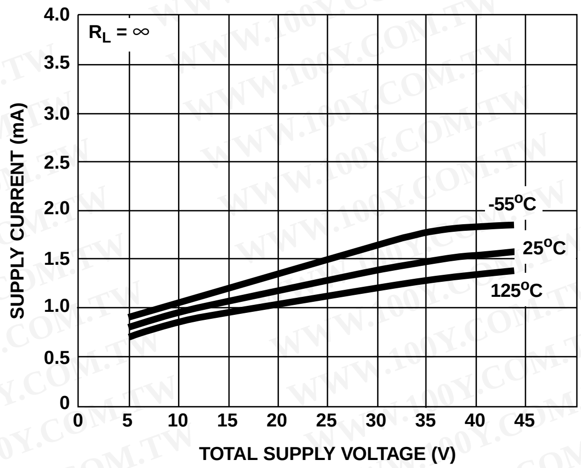


FIGURE 8. SUPPLY CURRENT vs SUPPLY VOLTAGE (BOTH AMPLIFIERS)

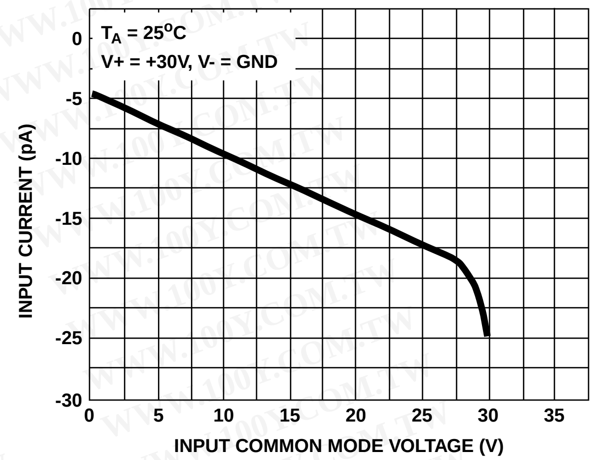


FIGURE 9. INPUT CURRENT vs INPUT COMMON MODE VOLTAGE

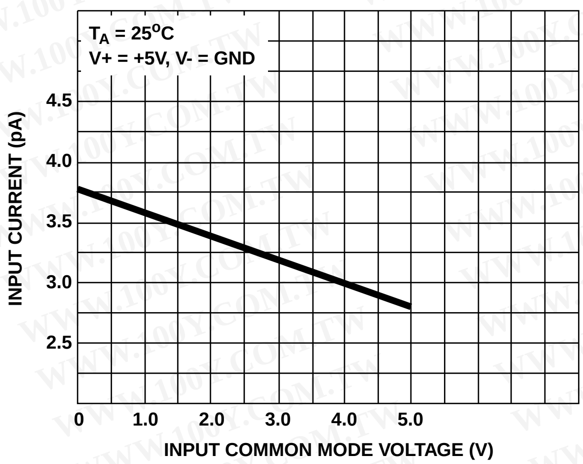


FIGURE 10. INPUT CURRENT vs INPUT COMMON MODE VOLTAGE

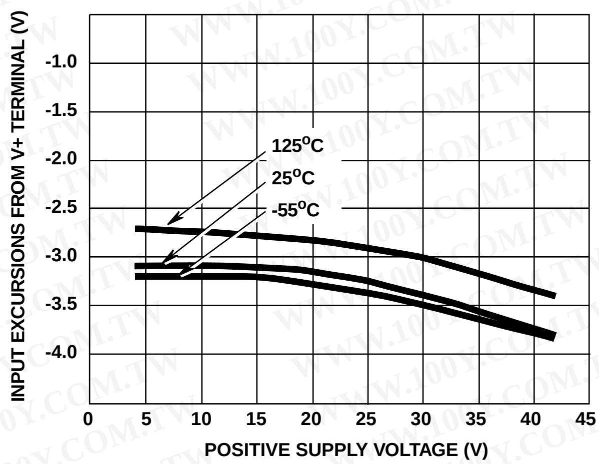


FIGURE 11. POSITIVE COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

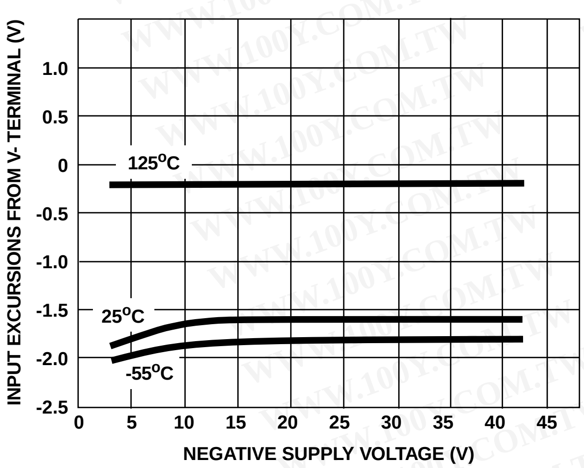


FIGURE 12. NEGATIVE COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

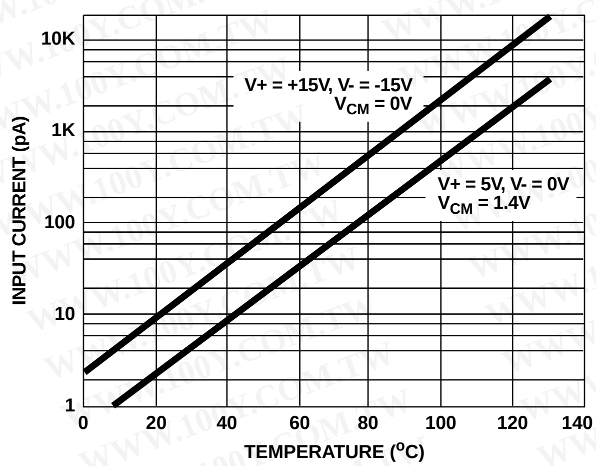


FIGURE 13. INPUT CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

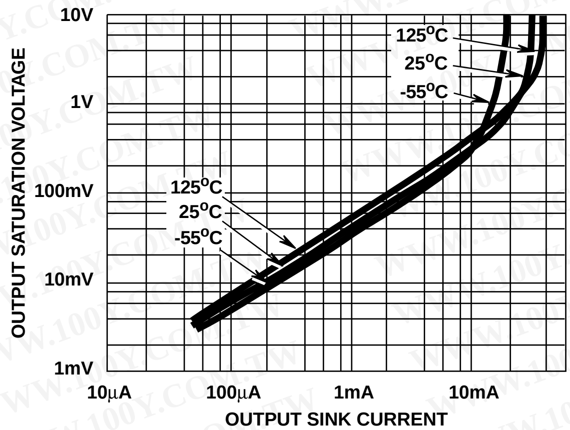
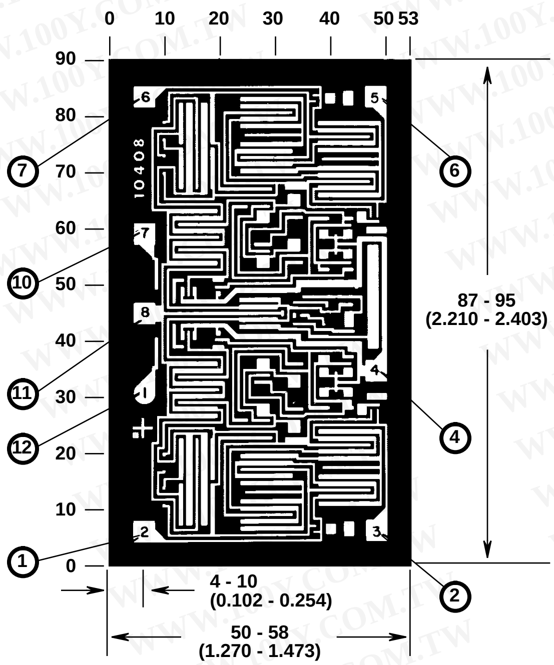


FIGURE 14. OUTPUT SATURATION VOLTAGE vs OUTPUT SINK CURRENT

Metallization Mask Layout



The photographs and dimensions of each chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7mils (0.17mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

NOTE: Numbers in pads are for 8 lead DIP and TO-5 Can and numbers outside of chip are for 14 lead DIP.