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120MHz Current Feedback Amplifier

élantec

The EL2030 is a very fast, wide bandwidth amplifier optimized for gains between -10 and +10. Built using the Elantec monolithic Complementary Bipolar process, this amplifier uses current mode feedback to achieve more bandwidth at a given gain than a conventional voltage feedback operational amplifier.

Due to its wide operating supply range (±15V) and extremely high slew rate of 2000V/µs, the EL2030 drives ±10V into 200Ω at a frequency of 30MHz, while achieving 110MHz of small signal bandwidth at A_V = +2. This bandwidth is still 95MHz for a gain of +10. On ±5V supplies the amplifier maintains a 90MHz bandwidth for A_V = +2. When used as a unity gain buffer, the EL2030 has a 120MHz bandwidth with the gain precision and low distortion of closed loop buffers.

The EL2030 features extremely low differential gain and phase, a low noise topology that reduces noise by a factor of 2 over competing amplifiers, and settling time of 40ns to 0.25% for a 10V step. The output is short circuit protected. In addition, datasheet limits are guaranteed for ±5V and ±15V supplies.

Elantec's products and facilities comply with applicable quality specifications. See Elantec document, QRA-1: Processing, Monolithic Integrated Circuits.

Features

- -3dB bandwidth = 120MHz, A_V = 1
- -3dB bandwidth = 110MHz, A_V = 2
- 0.01% differential gain and 0.01° differential phase (NTSC, PAL)
- 0.05% differential gain and 0.02° differential phase (HDTV)
- Slew rate 2000V/µs
- 65mA output current
- Drives ±10V into 200Ω load
- Characterized at ±5V and ±15V
- Low voltage noise
- Current mode feedback
- Settling time of 40ns to 0.25% for a 10V step
- Output short circuit protected
- Low cost

Applications

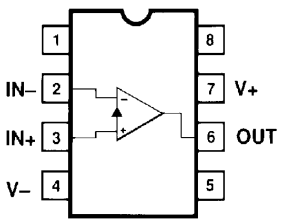
- Video gain block
- Video distribution amplifier
- HDTV amplifier
- Residue amplifiers in ADC
- Current to voltage converter
- Coax cable driver

Ordering Information

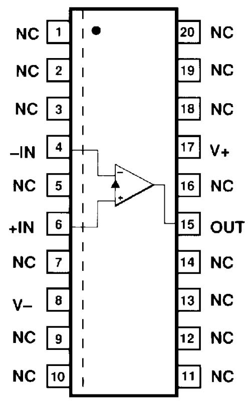
PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
EL2030CN	-40°C to +85°C	8-Pin PDIP	MDP0031
EL2030CM	-40°C to +85°C	20-Pin SOL	MDP0027

Pinouts

EL2030
(8-PIN PDIP)
TOP VIEW



EL2030
(20-PIN SOL)
TOP VIEW



NOTE: Non-Designated pins are no connects and are not electrically connected internally. Manufactured under U.S. Patent No. 4,893,091.

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V or 36V
V_{IN}	Input Voltage	±15V or V_S
V_{IN}	Differential Input Voltage	±6V
P_D	Maximum Power Dissipation	See Curves
I_{IN}	Input Current	±10mA
I_{OP}	Peak Output Current	Short Circuit Protected

Output Short Circuit Duration . . . . . Continuous

A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.

T_A	Operating Temperature Range	-40°C to +85°C
T_J	Operating Junction Temperature Plastic Packages	150°C
T_{ST}	Storage Temperature	-65°C to +150°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Open Loop DC Electrical Specifications V_S = ±15V, R_L = 200Ω, unless otherwise specified

PARAMETER	DESCRIPTION	CONDITION	TEMP	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_S = ±15V	25°C		10	20	mV
			T_{MIN}, T_{MAX}			30	mV
		V_S = ±5V	25°C		5	10	mV
			T_{MIN}, T_{MAX}			15	mV
V_{OS}/T	Offset Voltage Drift				25		µV/°C
$+I_{IN}$	+Input Current	V_S = ±5V, ±15V	25°C		5	15	µA
			T_{MIN}, T_{MAX}			25	µA
$-I_{IN}$	-Input Current	V_S = ±5V, ±15V	25°C		10	40	µA
			T_{MIN}, T_{MAX}			50	µA
$+R_{IN}$	+Input Resistance		Full	1.1	2.0		MΩ
C_{IN}	Input Capacitance		25°C		1		pF
CMRR	Common Mode Rejection Ratio (Note 1)	V_S = ±5V, ±15V	Full	50	60		dB
-ICMR	Input Current Common Mode Rejection (Note 1)		25°C		5	10	µA/V
			T_{MIN}, T_{MAX}			20	µA/V
PSRR	Power Supply Rejection Ratio (Note 2)		Full	60	70		dB
+IPSR	+Input Current Power Supply Rejection (Note 2)		25°C		0.1	0.5	µA/V
			T_{MIN}, T_{MAX}			1.0	µA/V
-IPSR	-Input Current Power Supply Rejection (Note 2)		25°C		0.5	5.0	µA/V
			T_{MIN}, T_{MAX}			8.0	µA/V
R_{OL}	Transimpedance ($V_{OUT}/(-I_{IN})$) V_{OUT} = ±10V	V_S = ±15V	25°C	88	150		V/mA
			T_{MIN}, T_{MAX}	75			V/mA
	V_{OUT} = ±2.5V (Note 3)	V_S = ±5V	25°C	80	120		V/mA
			T_{MIN}, T_{MAX}		70		V/mA
A_{VOL}	Open Loop DC Voltage Gain V_{OUT} = ±10V	V_S = ±15V	Full	60	70		dB
	V_{OUT} = ±2.5V (Note 3)	V_S = ±5V	Full	56	65		dB
V_O	Output Voltage Swing (Note 3)	V_S = ±15V	Full	12	13		V
		V_S = ±5V	Full	3	3.5		V
I_{OUT}	Output Current (Note 4)	V_S = ±15V	Full	60	65		mA
		V_S = ±5V	Full	30	35		mA

Open Loop DC Electrical Specifications $V_S = \pm15V$, $R_L = 200\Omega$, unless otherwise specified **(Continued)**

PARAMETER	DESCRIPTION	CONDITION	TEMP	MIN	TYP	MAX	UNITS
R_{OUT}	Output Resistance		25°C		5		Ω
I_S	Quiescent Supply Current		Full		15	21	mA
I_{SC}	Short Circuit Current		25°C		85		mA

NOTES:

1. $V_{CM} = \pm10V$ for $V_S = \pm15V$. For $V_S = \pm5V$, $V_{CM} = \pm2.5V$.
2. V_{OS} is measured at $V_S = \pm4.5V$ and at $V_S = \pm18V$. Both supplies are changed simultaneously.
3. $R_L = 100\Omega$.
4. For $V_S = \pm15V$, $V_{OUT} = \pm10V$. For V_S ±5V, $V_{OUT} = \pm2.5V$.

Closed Loop AC Electrical Characteristics $V_S = \pm15V$, $A_V = +2$, $R_F = 820\Omega$, $R_G = 820\Omega$ and $R_L = 200\Omega$

PARAMETER	DESCRIPTION	CONDITION	TEMP	MIN	TYP	MAX	UNITS
SR	Slew Rate (Note 1)		25°C	1200	2000		V/µs
FPBW	Full Power Bandwidth (Note 2)		25°C	19	31.8		MHz
t_R, t_F	Rise Time. Fall Time	V_{PP} = 250mV	25°C		3		ns
t_S	Settling Time to 0.25% for 10V step (Note 3)		25°C		40		ns
G	Differential Gain (Note 4)		25°C		0.01		% p-p
	Differential Phase (Note 4)		25°C		0.01		° p-p
eN	Input Spot Noise at 1kHz R_G = 101; R_F = 909		25°C		4		$nV/\sqrt{Hz}$

NOTES:

1. $V_O = \pm10V$, tested at $V_O = \pm5$. See test circuit.
2. Full Power Bandwidth is specified based on Slew Rate measurement $FPBW = SR/2\pi V_P$.
3. Settling Time measurement techniques are shown in: “Take The Guesswork Out of Settling Time Measurements', EDN, September 19, 1985. Available from the factory upon request.
4. NTSC (3.58MHz) and PAL (4.43MHz).

Typical Performance Curves

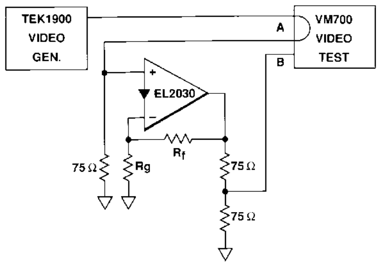
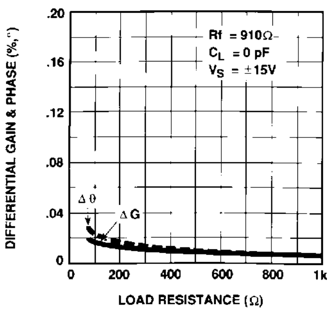
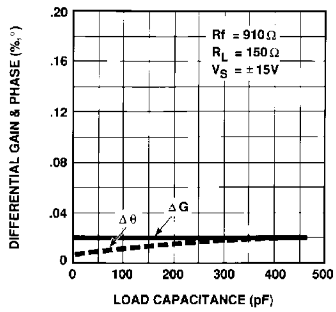


FIGURE 1. NTSC VIDEO DIFFERENTIAL GAIN AND PHASE TEST SET-UP

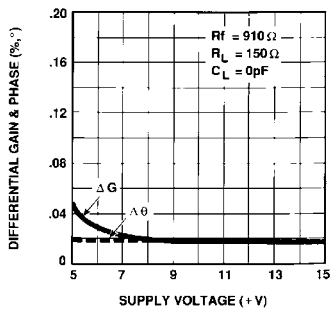
Differential Gain and Phase vs Load Resistance, Gain = +1



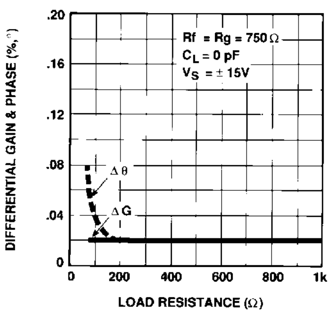
Differential Gain and Phase vs Load Capacitance, Gain = +1



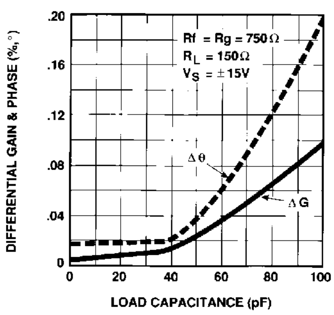
Differential Gain and Phase vs Supply Voltage, Gain = +1



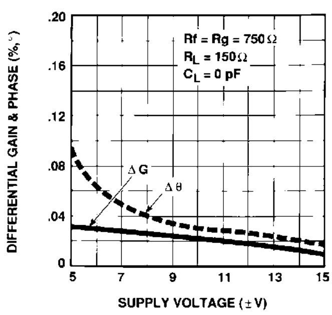
Differential Gain and Phase vs Load Resistance, Gain = +2



Differential Gain and Phase vs Load Capacitance, Gain = +2



Differential Gain and Phase vs Supply Voltage, Gain = +2



Typical Performance Curves (Continued)

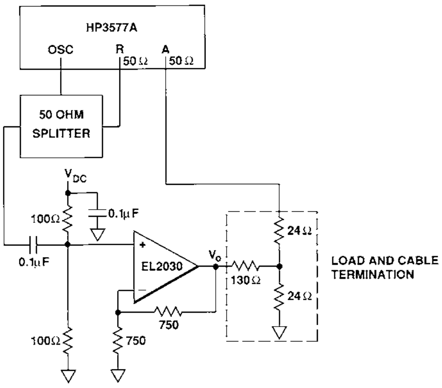
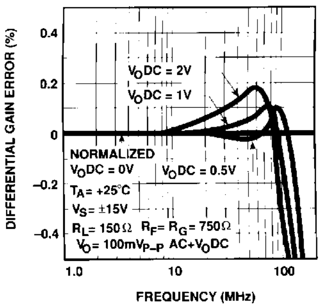
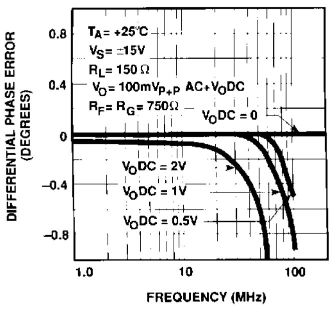


FIGURE 2. HDTV AND WIDEBAND VIDEO DIFFERENTIAL GAIN AND PHASE TEST SET-UP

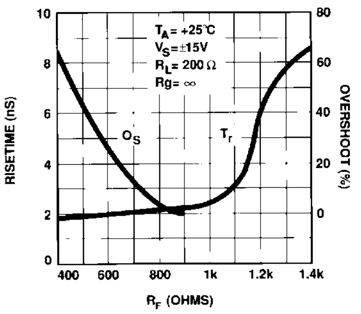
Differential Gain Error vs Frequency for Various DC Output Levels



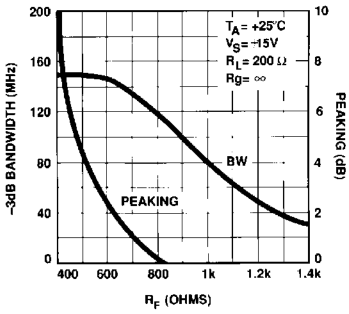
Differential Phase Error vs Frequency for Various DC Output Levels



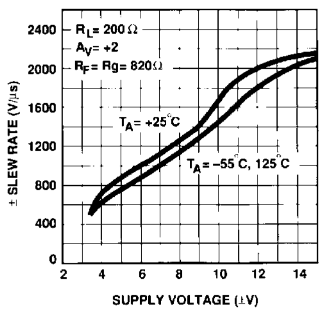
Risetime and Overshoot vs R_F for $A_V = +1$



Bandwidth and Peaking vs R_F for $A_V = +1$

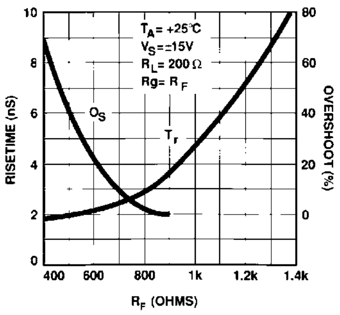


±Slew Rate vs Supply Voltage

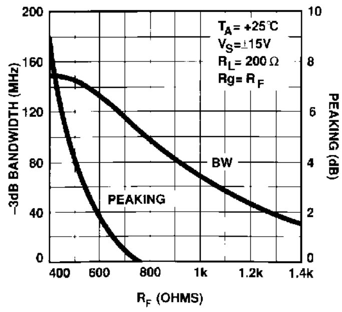


Typical Performance Curves (Continued)

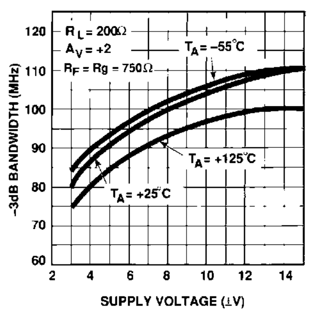
Risetime and Overshoot vs R_F for A_V = +2



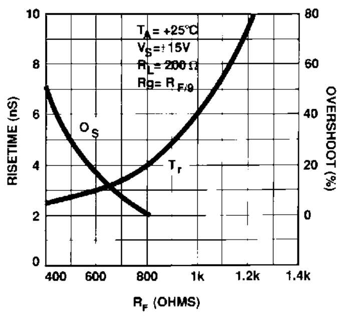
Bandwidth and Peaking vs R_F for A_V = +2



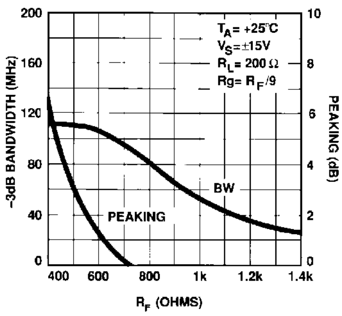
-3dB Bandwidth vs Supply Voltage



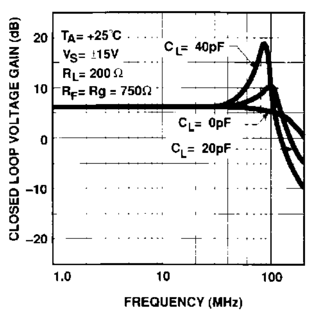
Risetime and Overshoot vs R_F for A_V = +10



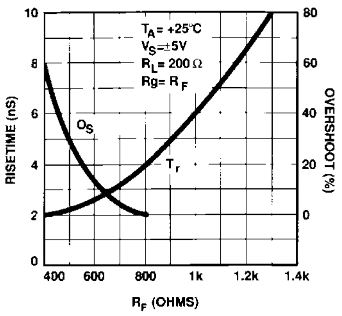
Bandwidth and Peaking vs R_F for A_V = +10



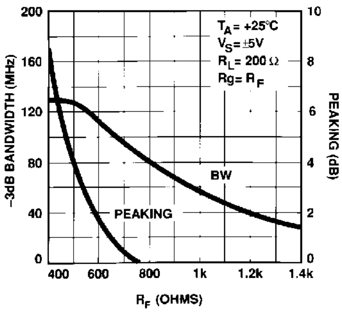
Voltage Gain vs Frequency for A_V = +2, Various Capacitive Loads



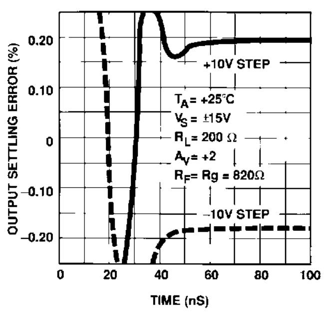
Risetime and Overshoot vs R_F for A_V = +2, V_S = ±5V



Bandwidth and Peaking vs R_F for A_V = +2, V_S = +5V

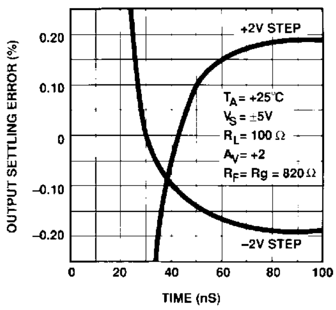


Output Settling Error vs Time

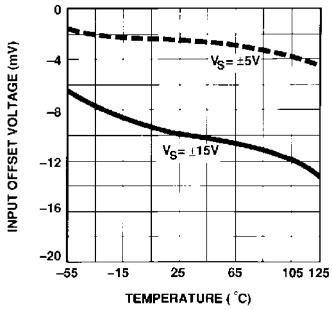


Typical Performance Curves (Continued)

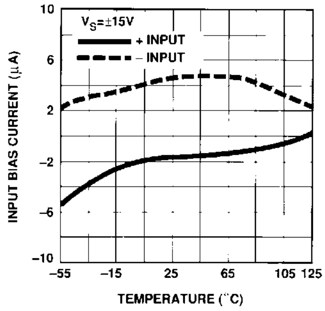
Output Settling Error vs Time, V_S = ±5V



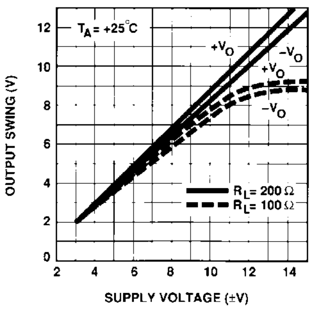
Input Offset Voltage vs Temperature



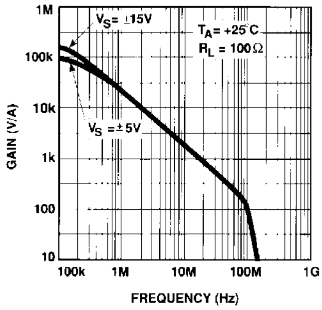
Input Bias Current vs Temperature



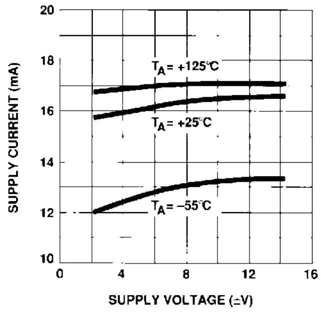
Output Swing vs Supply Voltage



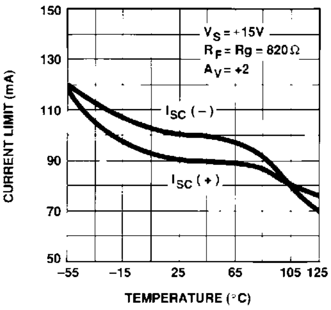
Transimpedance (R_{OL})



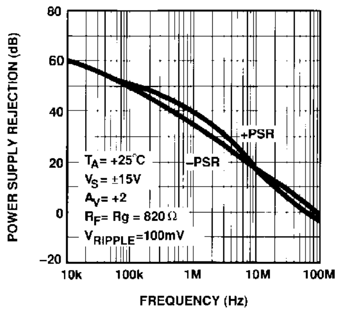
Supply Current vs Supply Voltage



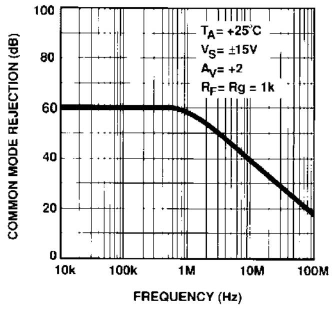
Current Limit vs Temperature



Power Supply Rejection vs Frequency

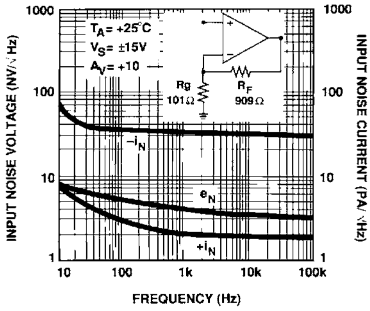


Common Mode Rejection vs Frequency

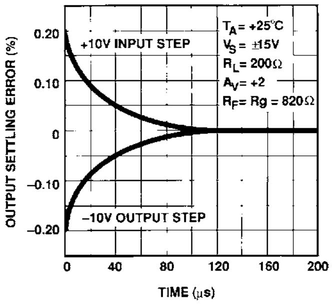


Typical Performance Curves (Continued)

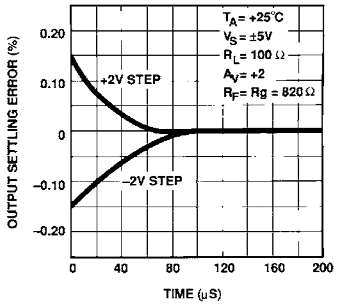
Equivalent Input Noise



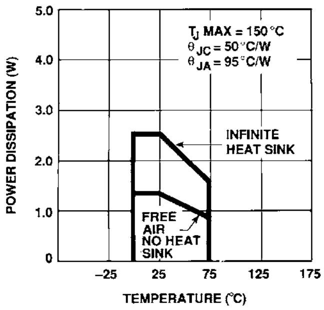
Long-Term Output Settling Error vs Time



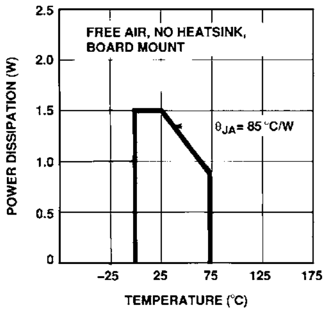
Long-Term Output Settling Error vs Time, V_S = ±5V



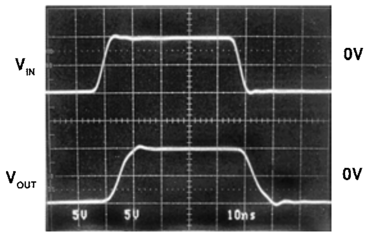
8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



20-Pin SOL Maximum Power Dissipation vs Ambient Temperature

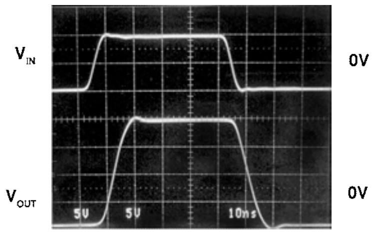


Large Signal Response



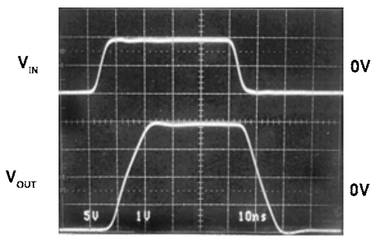
A_V = +1, R_F = 1 kΩ,
R_L = 200Ω, V_S = ±15V

Large Signal Response



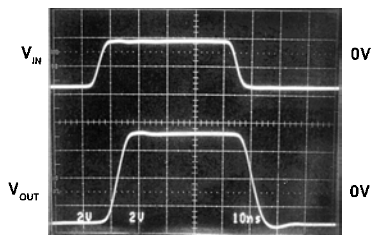
A_V = +2, R_F = R_G = 820,
R_L = 200Ω, V_S = ±15V

Large Signal Response



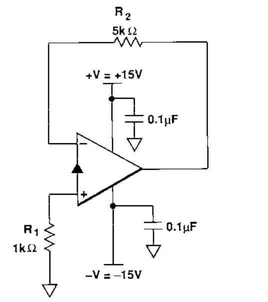
A_V = +10, R_F = 750, R_G = 82Ω,
R_L = 200Ω, V_S = ±15V

Large Signal Response



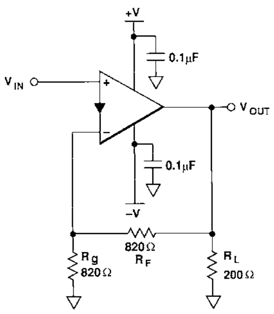
A_V = +2, R_F = R_G = 750Ω,
R_L = 200Ω, V_S = ±15V

Burn-In Circuit



ALL PACKAGES USE THE SAME SCHEMATIC

Test Circuit



Application Information

Product Description

The EL2030 is a current mode feedback amplifier similar to the industry standard EL2020, but with greatly improved AC characteristics. Most significant among these are the extremely wide bandwidth and very low differential gain and phase. In addition, the EL2030 is fully characterized and tested at ±5V and ±15V supplies.

Power Supply Bypassing/Pin Dressing

It is important to bypass the power supplies of the EL2030 with 0.1µF ceramic disc capacitors. Although the pin length is not critical, it should not be more the 1/2 inch from the IC pins. Failure to do this will result in oscillation, and possible destruction of the part. Another important detail is the pin length of the inputs. The inputs should be designed with minimum stray capacitance and short pin lengths to avoid ringing and distortion.

Latch Mode

The EL2030 can be damaged in certain circumstances resulting in catastrophic failure in which destructive supply currents flow in the device. Specifically, an input signal greater than ±5 volts at currents greater than 5mA is applied to the device when the power supply voltages are zero will result in failure of the device.

In addition, the EL2030 will be destroyed or damaged in the same way for momentary power supply voltage reversals. This could happen, for example, during a power turn on transient, or if the power supply voltages were oscillating and the positive rail were instantaneously negative with respect to the negative rail or vice versa.

Differential Gain and Differential Phase

Composite video signals contain intensity, color, hue, timing and audio information in AM, FM, and Phase Modulation. These video signals pass through many stages during their production, processing, archiving and transmission. It is important that each stage not corrupt these signals to provide a “high fidelity” image to the end viewer.

An industry standard way of measuring the distortion of a video component (or system) is to measure the amount of differential gain and phase error it introduces. A 100mV peak to peak sine wave at 3.58MHz for NTSC (4.3MHz for PAL), with 0V DC component serves as the reference. The reference signal is added to a DC offset, shifting the sine wave from 0V to 0.7V which is then applied to the device under test (DUT). The output signal from the DUT is compared to the reference signal. The Differential Gain is a measure of the change in amplitude of the sine wave and is measured in percent. The Differential Phase is a measure of the change in the phase of the sine wave and is measured in degrees. Typically, the maximum positive and negative deviations are summed to give peak differential gain and differential phase errors. The test setup in Figure 1 was used to characterize the EL2030. For higher than NTSC and PAL frequencies, an alternate Differential Gain and Phase measurement can be made using an HP3577A Network Analyzer and the setup shown in Figure 2. The frequency response is normalized to gain or phase with 0V DC at the input. From the normalized value a DC offset voltage is introduced and the Differential Gain or Phase is the deviation from the normalized value.

Video Applications

The video signals that must be transmitted for modest distances are usually amplified by a device such as the EL2030 and carried via coax cable. There are at least two ways to drive cables, single terminated and double terminated.

When driving a cable, it is important to terminate it properly to avoid unwanted signal reflections. Single termination (75Ω to ground at receive end) may be sufficient for less demanding applications. In general, a double terminated cable (75Ω in series at drive end and 75Ω to ground at receive end) is preferred since the impedance match at both ends of the line will absorb signal reflections. However, when double termination is used (a total impedance of 150Ω), the received signal is reduced by half; therefore, the amplifier is usually set at a gain of 2 or higher to compensate for attenuation.

Video signals are 1V peak-peak in amplitude, from sync tip to peak white. There are 100 IRE (0.714V) of picture (from black to peak white of the transmitted signal) and 40 IRE (0.286V) of sync in a composite video signal (140 IRE = 1V).

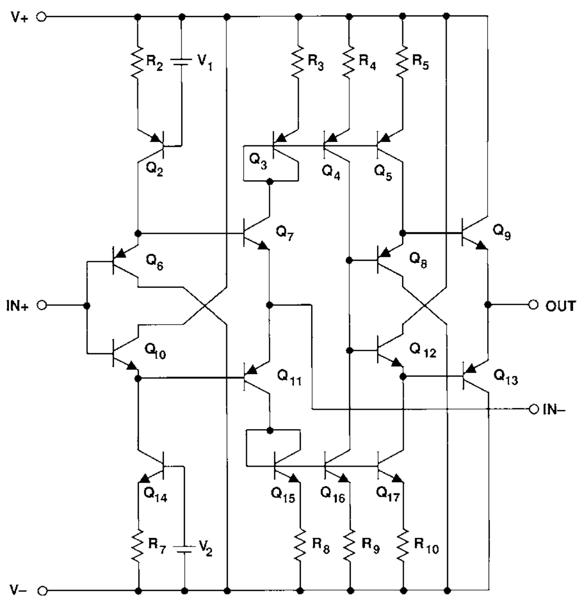
For video applications where a gain of two is used (double termination), the output of the video amplifier will be a maximum of 2V peak-peak. With ±5V power supply, the EL2030 output swing of 3.5V is sufficient to satisfy the video output swing requirements. The EL2030 can drive two double terminated coax cables under these conditions. With ±15V supplies, driving four double terminated cables is feasible.

Although the EL2030's video characteristics (differential gain and phase) are impressive with ±5V supplies at NTSC and PAL frequencies, it can be optimized when the supplies are increased to ±15V, especially at 30MHz HDTV applications. This is primarily due to a reduction in internal parasitic junction capacitance with increased power supply voltage.

The following table summarizes the behavior of the EL2030 at ±5V and ±15V for NTSC. In addition, 30MHz HDTV data is included. Refer to the differential gain and phase typical performance curves for more data.

$\pm V_S$	RLOAD	A_V	GAIN	PHASE	COMMENTS
15V	75Ω	1	0.02%	0.03°	Single terminated
15V	150Ω	1	0.02%	0.02°	Double terminated
5V	150Ω	1	0.05%	0.02°	Double terminated
15V	75Ω	2	0.02%	0.08°	Single terminated
15V	150Ω	2	0.01%	0.02°	Double terminated
5V	150Ω	2	0.03%	0.09°	Double terminated
15V	150Ω	2	0.05%	0.02°	HDTV, Double terminated

Equivalent Circuit

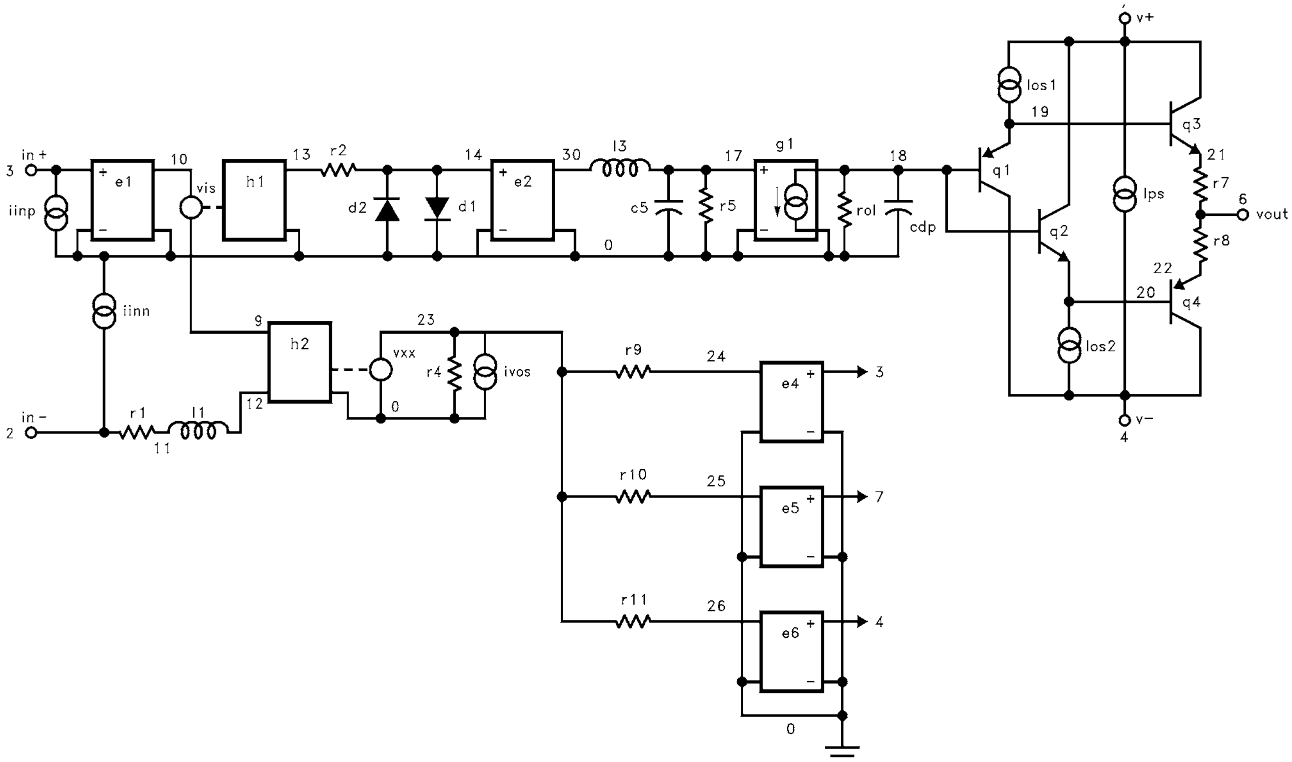


EL2030 Macromodel

```
* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:   +input
*                  |   -input
*                  |     |   +Vsupply
*                  |     |     |   -Vsupply
*                  |     |     |     |   output
*                  |     |     |     |     |
.subckt M2030      3     2     7     4     6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 50
l1 11 12 48nH
iinp 3 0 5µA
iinm 2 0 10µA
r12 3 0 2Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
*e2 30 0 14 0 0.00166666666
l3 30 17 0.5µH
c5 17 0 1pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 150K
cdp 18 0 2.8pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 2.5mA
ios2 20 4 2.5mA
*
* Supply Current
*
ips 7 4 9mA
*
* Error Terms
*
ivos 0 23 5mA
```

EL2030 Macromodel (Continued)

```
vxx 23 0 0V
e4 24 3 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 3K
r10 25 23 1K
r11 26 23 1K
*
* Models
*
.model qn npn (is=5e-15 bf=100 tf=0.1nS)
.model qp pnp (is=5e-15 bf=100 tf=0.1nS)
.model dclamp d(is=1e-30 ibv=0.266 bv=3.7 n=4)
.ends
```



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élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2030C
120 MHz Current Feedback Amplifier

Features

- −3 dB bandwidth = 120 MHz, $A_V = 1$
- −3 dB bandwidth = 110 MHz, $A_V = 2$
- 0.01% differential gain and 0.01° differential phase (NTSC, PAL)
- 0.05% differential gain and 0.02° differential phase (HDTV)
- Slew rate 2000 V/μs
- 65 mA output current
- Drives ±10V into 200Ω load
- Characterized at ±5V and ±15V
- Low voltage noise
- Current mode feedback
- Settling time of 40 ns to 0.25% for a 10V step
- Output short circuit protected
- Low cost

Applications

- Video gain block
- Video distribution amplifier
- HDTV amplifier
- Residue amplifiers in ADC
- Current to voltage converter
- Coax cable driver

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2030CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2030CM	−40°C to +85°C	20-Lead SOL	MDP0027

General Description

The EL2030 is a very fast, wide bandwidth amplifier optimized for gains between −10 and +10. Built using the Elantec monolithic Complementary Bipolar process, this amplifier uses current mode feedback to achieve more bandwidth at a given gain than a conventional voltage feedback operational amplifier.

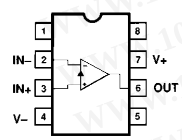
Due to its wide operating supply range (±15V) and extremely high slew rate of 2000 V/μs, the EL2030 drives ±10V into 200Ω at a frequency of 30 MHz, while achieving 110 MHz of small signal bandwidth at $A_V = +2$. This bandwidth is still 95 MHz for a gain of +10. On ±5V supplies the amplifier maintains a 90 MHz bandwidth for $A_V = +2$. When used as a unity gain buffer, the EL2030 has a 120 MHz bandwidth with the gain precision and low distortion of closed loop buffers.

The EL2030 features extremely low differential gain and phase, a low noise topology that reduces noise by a factor of 2 over competing amplifiers, and settling time of 40 ns to 0.25% for a 10V step. The output is short circuit protected. In addition, datasheet limits are guaranteed for ±5V and ±15V supplies.

Elantec's products and facilities comply with applicable quality specifications. See Elantec document, QRA-1: *Processing, Monolithic Integrated Circuits*.

Connection Diagrams

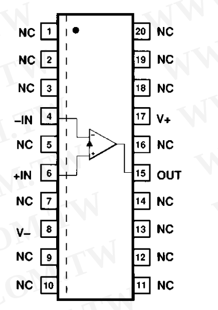
Mini DIP



2030–1

Top View

SOL



2030–3

Top View

Note: Non-designated pins are no connects and are not electrically connected internally.

Manufactured under U.S. Patent No. 4,893,091.

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V or 36V
V_{IN}	Input Voltage	±15V or V_S
ΔV_{IN}	Differential Input Voltage	±6V
P_D	Maximum Power Dissipation	See Curves
I_{IN}	Input Current	±10 mA
I_{OP}	Peak Output Current	Short Circuit Protected
	Output Short Circuit Duration (Note 1)	Continuous
T_A	Operating Temperature Range	−40°C to +85°C
T_J	Operating Junction Temperature Plastic Packages	150°C
T_{ST}	Storage Temperature	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics V_S = ±15V, R_L = 200Ω, unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level EL2030C	Units
V_{OS}	Input Offset Voltage	V_S = ±15V	25°C		10	20	I	mV
			T_{MIN}, T_{MAX}			30	III	mV
		V_S = ±5V	25°C		5	10	I	mV
			T_{MIN}, T_{MAX}			15	III	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift				25		V	µV/°C
$+I_{IN}$	+Input Current	V_S = ±5V, ±15V	25°C		5	15	I	µA
			T_{MIN}, T_{MAX}			25	III	µA
$-I_{IN}$	−Input Current	V_S = ±5V, ±15V	25°C		10	40	I	µA
			T_{MIN}, T_{MAX}			50	III	µA
$+R_{IN}$	+Input Resistance		Full	1.1	2.0		II	MΩ
C_{IN}	Input Capacitance		25°C		1		V	pF
CMRR	Common Mode Rejection Ratio (Note 2)	V_S = ±5V, ±15V	Full	50	60		II	dB
−ICMR	Input Current Common Mode Rejection (Note 2)		25°C		5	10	I	µA/V
			T_{MIN}, T_{MAX}			20	III	µA/V
PSRR	Power Supply Rejection Ratio (Note 3)		Full	60	70		II	dB
+IPSR	+Input Current Power Supply Rejection (Note 3)		25°C		0.1	0.5	II	µA/V
			T_{MIN}, T_{MAX}			1.0	III	µA/V
−IPSR	−Input Current Power Supply Rejection (Note 3)		25°C		0.5	5.0	II	µA/V
			T_{MIN}, T_{MAX}			8.0	III	µA/V

TD is 3.6in

Open Loop DC Electrical Characteristics

$V_S = \pm 15V$, $R_L = 200\Omega$, unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level EL2030C	Units
R_{OL}	Transimpedance ($\Delta V_{OUT}/\Delta(-I_{IN})$) $V_{OUT} = \pm 10V$	$V_S = \pm 15V$	25°C	88	150		II	V/mA
			T_{MIN}, T_{MAX}	75			III	V/mA
	$V_{OUT} = \pm 2.5V$ (Note 6)	$V_S = \pm 5V$	25°C	80	120		II	V/mA
			T_{MIN}, T_{MAX}		70		III	V/mA
A_{VOL}	Open Loop DC Voltage Gain $V_{OUT} = \pm 10V$	$V_S = \pm 15V$	Full	60	70		II	dB
	$V_{OUT} = \pm 2.5V$ (Note 6)	$V_S = \pm 5V$	Full	56	65		II	dB
V_O	Output Voltage Swing (Note 6)	$V_S = \pm 15V$	Full	12	13		II	V
		$V_S = \pm 5V$	Full	3	3.5		II	V
I_{OUT}	Output Current (Note 9)	$V_S = \pm 15V$	Full	60	65		II	mA
		$V_S = \pm 5V$	Full	30	35		II	mA
R_{OUT}	Output Resistance		25°C		5		V	Ω
I_S	Quiescent Supply Current		Full		15	21	II	mA
I_{SC}	Short Circuit Current		25°C		85		V	mA

Closed Loop AC Electrical Characteristics

$V_S = \pm 15V$, $A_V = +2$, $R_F = 820\Omega$, $R_G = 820\Omega$ and $R_L = 200\Omega$

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level EL2030C	Units
SR	Slew Rate (Note 7)		25°C	1200	2000		IV	V/µs
FPBW	Full Power Bandwidth (Note 4)		25°C	19	31.8		IV	MHz
t_r, t_f	Rise Time. Fall Time	$V_{pp} = 250$ mV	25°C		3		V	ns
t_s	Settling Time to 0.25% for 10V step (Note 5)		25°C		40		V	ns
ΔG	Differential Gain (Note 8)		25°C		0.01		V	% p-p
Δϕ	Differential Phase (Note 8)		25°C		0.01		V	° p-p
eN	Input Spot Noise at 1 kHz $R_G = 101$; $R_F = 909$		25°C		4		V	$nV/\sqrt{Hz}$

Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.
Note 2: $V_{CM} = \pm 10V$ for $V_S = \pm 15V$. For $V_S = \pm 5V$, $V_{CM} = \pm 2.5V$.
Note 3: V_{OS} is measured at $V_S = \pm 4.5V$ and at $V_S = \pm 18V$. Both supplies are changed simultaneously.
Note 4: Full Power Bandwidth is specified based on Slew Rate measurement FPBW = $SR/2\pi V_P$.
Note 5: Settling Time measurement techniques are shown in: "Take The Guesswork Out of Settling Time Measurements", EDN, September 19, 1985. Available from the factory upon request.
Note 6: $R_L = 100\Omega$.
Note 7: $V_O = \pm 10V$, tested at $V_O = \pm 5$. See test circuit.
Note 8: NTSC (3.58 MHz) and PAL (4.43 MHz).
Note 9: For $V_S = \pm 15V$, $V_{OUT} = \pm 10V$. For V_S ±5V, $V_{OUT} = \pm 2.5V$.

TD is 2.8in

TD is 1.9in

Typical Performance Curves

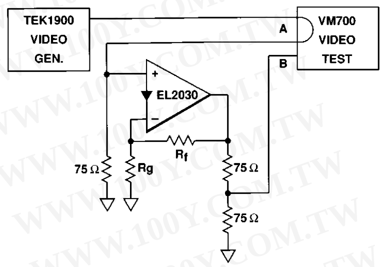
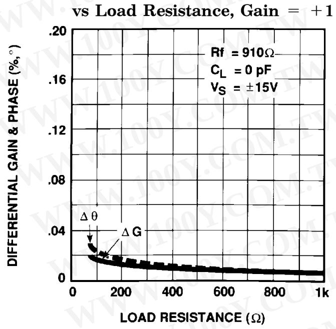
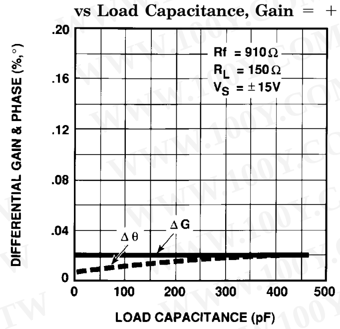


Figure 1. NTSC Video Differential Gain and Phase Test Set-Up

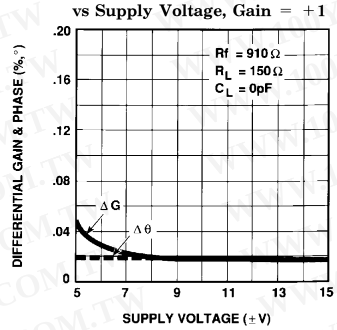
Differential Gain and Phase vs Load Resistance, Gain = +1



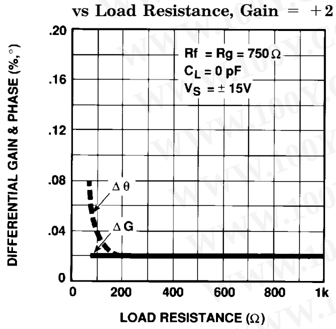
Differential Gain and Phase vs Load Capacitance, Gain = +1



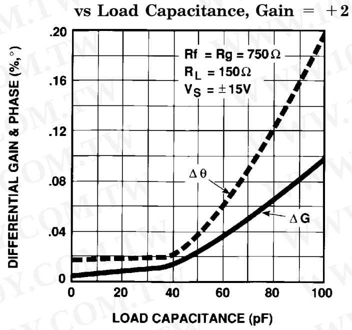
Differential Gain and Phase vs Supply Voltage, Gain = +1



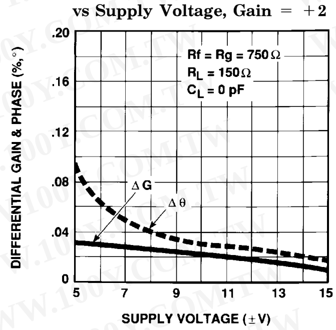
Differential Gain and Phase vs Load Resistance, Gain = +2



Differential Gain and Phase vs Load Capacitance, Gain = +2

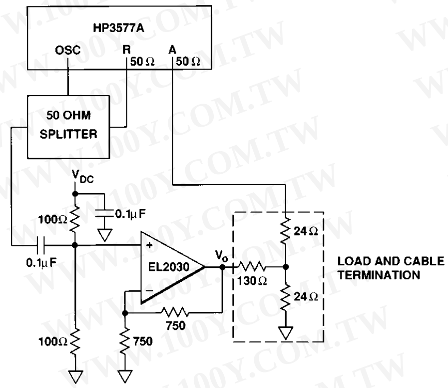


Differential Gain and Phase vs Supply Voltage, Gain = +2



2030-6

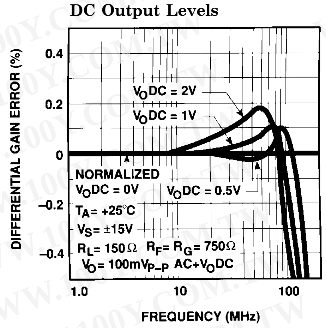
Typical Performance Curves — Contd.



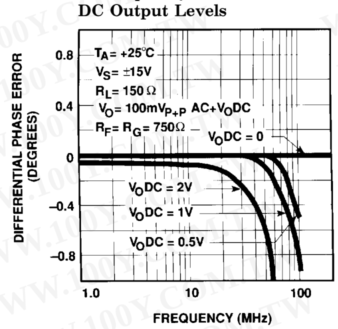
2030-7

Figure 2. HDTV and Wideband Video Differential Gain and Phase Test Set-Up

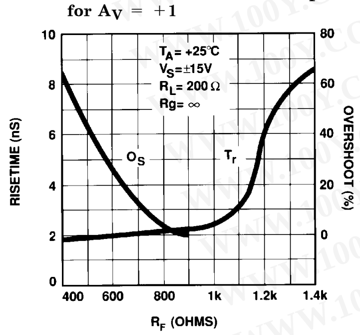
Differential Gain Error vs Frequency for Various DC Output Levels



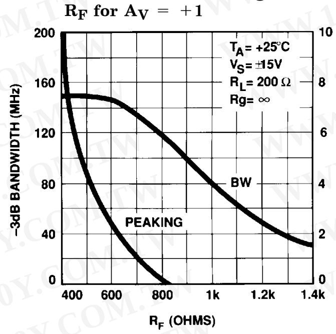
Differential Phase Error vs Frequency for Various DC Output Levels



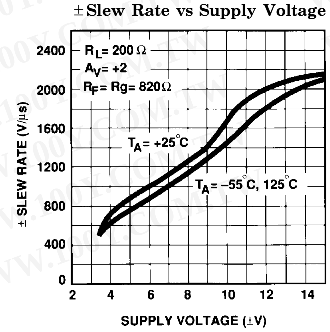
Risetime and Overshoot vs R_F for A_V = +1



Bandwidth and Peaking vs R_F for A_V = +1



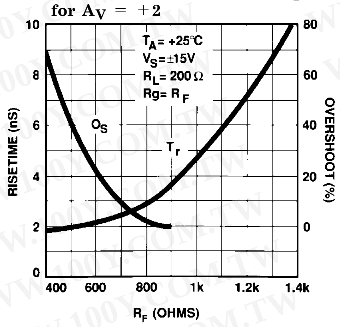
±Slew Rate vs Supply Voltage



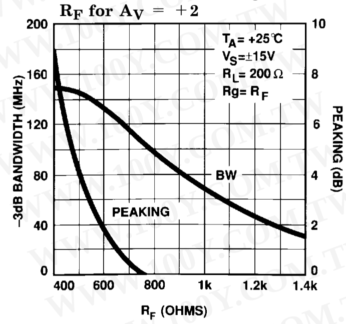
2030-8

Typical Performance Curves — Contd.

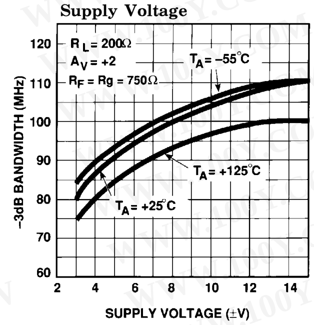
Risetime and Overshoot vs R_F for $A_V = +2$



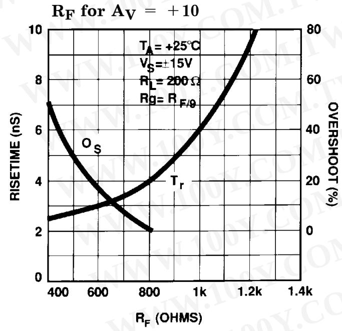
Bandwidth and Peaking vs R_F for $A_V = +2$



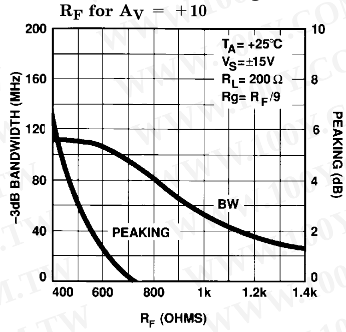
−3 dB Bandwidth vs Supply Voltage



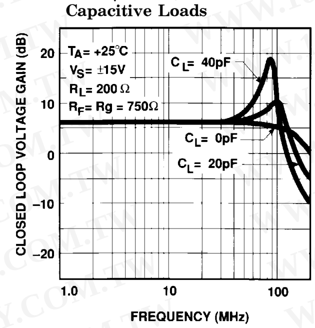
Risetime and Overshoot vs R_F for $A_V = +10$



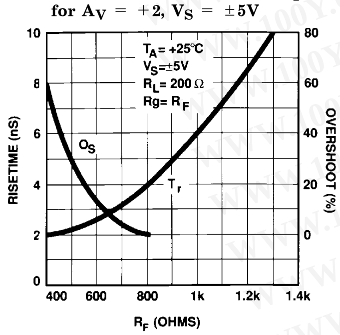
Bandwidth and Peaking vs R_F for $A_V = +10$



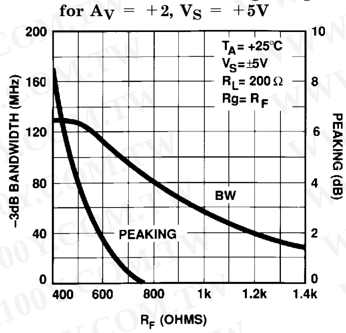
Voltage Gain vs Frequency for $A_V = +2$, various Capacitive Loads



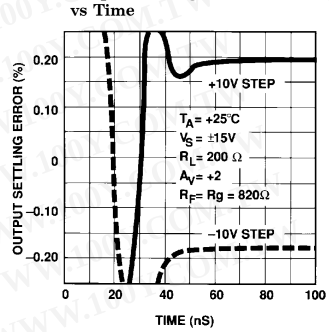
Risetime and Overshoot vs R_F for $A_V = +2$, $V_S = \pm 5V$



Bandwidth and Peaking vs R_F for $A_V = +2$, $V_S = +5V$



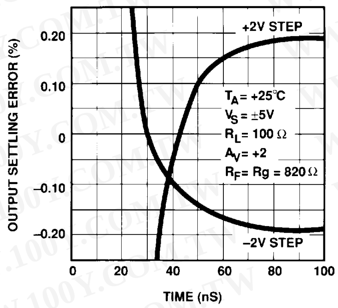
Output Settling Error vs Time



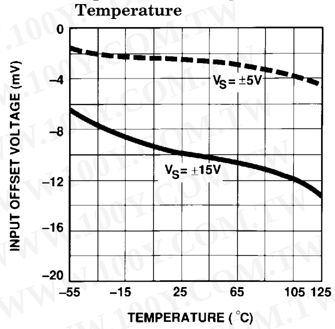
2030−9

Typical Performance Curves — Contd.

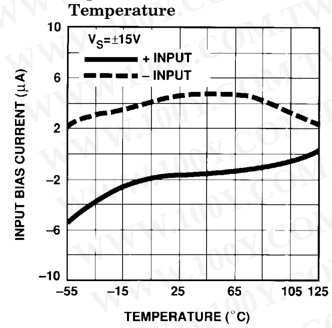
Output Settling Error vs Time, $V_S = \pm 5V$



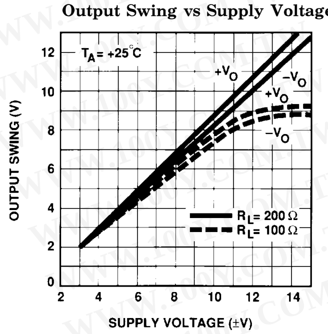
Input Offset Voltage vs Temperature



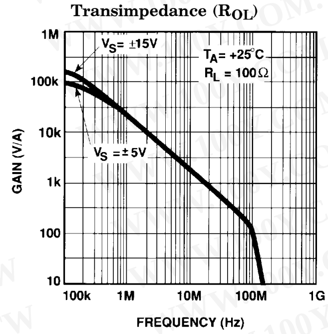
Input Bias Current vs Temperature



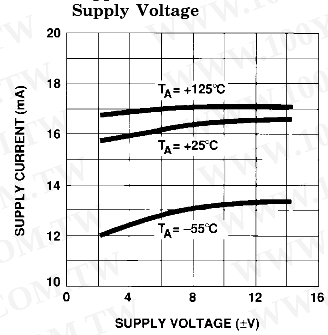
Output Swing vs Supply Voltage



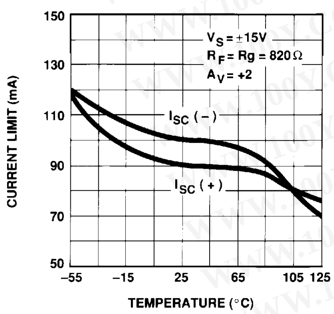
Transimpedance (R_{OL})



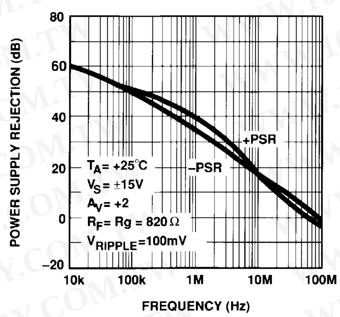
Supply Current vs Supply Voltage



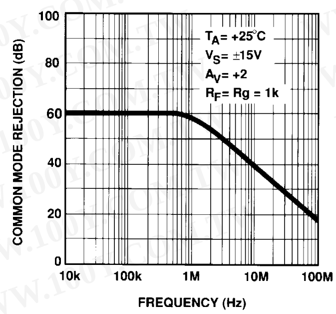
Current Limit vs Temperature



Power Supply Rejection vs Frequency



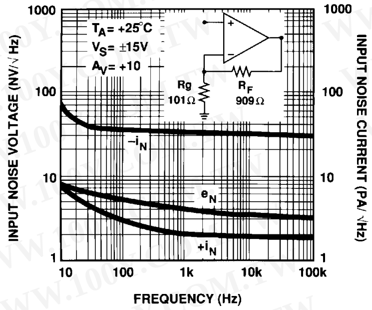
Common Mode Rejection vs Frequency



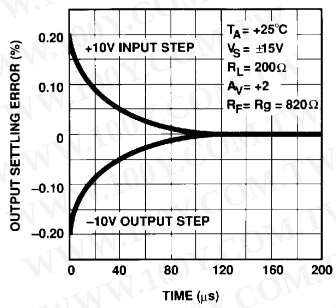
2030-10

Typical Performance Curves — Contd.

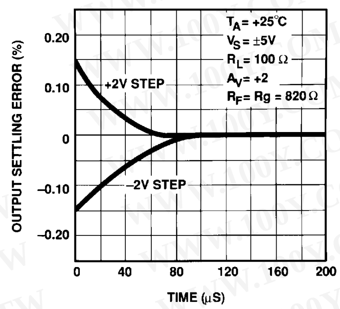
Equivalent Input Noise



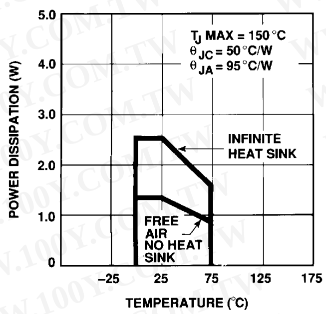
Long-Term Output Settling Error vs Time



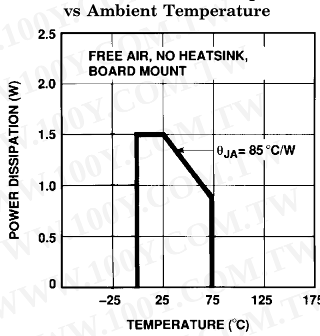
Long-Term Output Settling Error vs Time, $V_S = \pm 5V$



8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



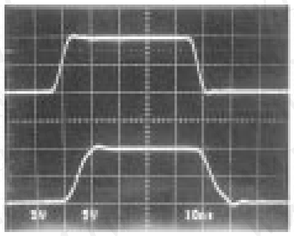
20-Lead SOL Maximum Power Dissipation vs Ambient Temperature



2030–11

Typical Performance Curves — Contd.

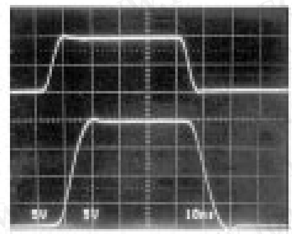
Large Signal Response



$A_V = +1$, $R_F = 1\ k\Omega$, $R_L = 200\Omega$, $V_S = \pm15V$

2030-12

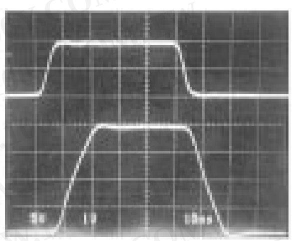
Large Signal Response



$A_V = +2$, $R_F = R_G = 820$, $R_L = 200\Omega$, $V_S = \pm15V$

2030-13

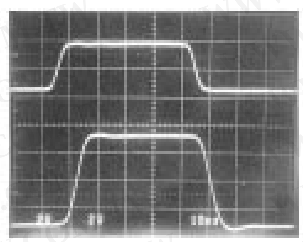
Large Signal Response



$A_V = +10$, $R_F = 750$, $R_G = 82\Omega$, $R_L = 200\Omega$, $V_S = \pm15V$

2030-14

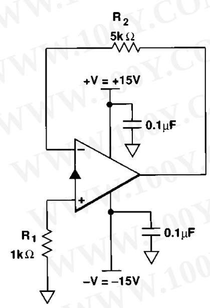
Large Signal Response



$A_V = +2$, $R_F = R_G = 750\Omega$, $R_L = 200\Omega$, $V_S = \pm15V$

2030-15

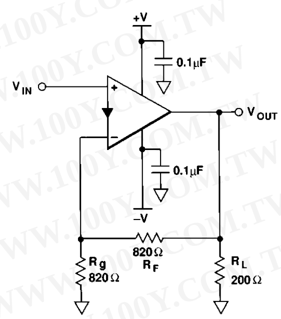
Burn-In Circuit



2030-16

ALL PACKAGES USE THE SAME SCHEMATIC.

Test Circuit



2030-17

Application Information

Product Description

The EL2030 is a current mode feedback amplifier similar to the industry standard EL2020, but with greatly improved AC characteristics. Most significant among these are the extremely wide bandwidth and very low differential gain and phase. In addition, the EL2030 is fully characterized and tested at ±5V and ±15V supplies.

Power Supply Bypassing/Lead Dressing

It is important to bypass the power supplies of the EL2030 with 0.1 μF ceramic disc capacitors. Although the lead length is not critical, it should not be more the ½ inch from the IC pins. Failure to do this will result in oscillation, and possible destruction of the part. Another important detail is the lead length of the inputs. The inputs should be designed with minimum stray capacitance and short lead lengths to avoid ringing and distortion.

Latch Mode

The EL2030 can be damaged in certain circumstances resulting in catastrophic failure in which destructive supply currents flow in the device. Specifically, an input signal greater than ±5 volts at currents greater than 5 mA is applied to the device when the power supply voltages are zero will result in failure of the device.

In addition, the EL2030 will be destroyed or damaged in the same way for momentary power supply voltage reversals. This could happen, for example, during a power turn on transient, or if the power supply voltages were oscillating and the positive rail were instantaneously negative with respect to the negative rail or vice versa.

Differential Gain and Differential Phase

Composite video signals contain intensity, color, hue, timing and audio information in AM, FM, and Phase Modulation. These video signals pass through many stages during their production, processing, archiving and transmission. It is important that each stage not corrupt these signals to provide a "high fidelity" image to the end viewer.

An industry standard way of measuring the distortion of a video component (or system) is to measure the amount of differential gain and phase error it introduces. A 100 mV peak to peak sine wave at 3.58 MHz for NTSC (4.3 MHz for PAL), with 0V DC component serves as the reference. The reference signal is added to a DC offset, shifting the sine wave from 0V to 0.7V which is then applied to the device under test (DUT). The output signal from the DUT is compared to the reference signal. The Differential Gain is a measure of the change in amplitude of the sine wave and is measured in percent. The Differential Phase is a measure of the change in the phase of the sine wave and is measured in degrees. Typically, the maximum positive and negative deviations are summed to give peak differential gain and differential phase errors. The test setup in Figure 1 was used to characterize the EL2030. For higher than NTSC and PAL frequencies, an alternate Differential Gain and Phase measurement can be made using an HP3577A Network Analyser and the setup shown in Figure 2. The frequency response is normalized to gain or phase with 0V DC at the input. From the normalized value a DC offset voltage is introduced and the Differential Gain or Phase is the deviation from the normalized value.

Video Applications

The video signals that must be transmitted for modest distances are usually amplified by a device such as the EL2030 and carried via coax cable. There are at least two ways to drive cables, single terminated and double terminated.

When driving a cable, it is important to terminate it properly to avoid unwanted signal reflections. Single termination (75Ω to ground at receive end) may be sufficient for less demanding applications. In general, a double terminated cable (75Ω in series at drive end and 75Ω to ground at receive end) is preferred since the impedance match at both ends of the line will absorb signal reflections. However, when double termination is used (a total impedance of 150Ω), the received signal is reduced by half; therefore, the amplifier is usually set at a gain of 2 or higher to compensate for attenuation.

Video Applications — Contd.

Video signals are 1V peak-peak in amplitude, from sync tip to peak white. There are 100 IRE (0.714V) of picture (from black to peak white of the transmitted signal) and 40 IRE (0.286V) of sync in a composite video signal (140 IRE = 1V).

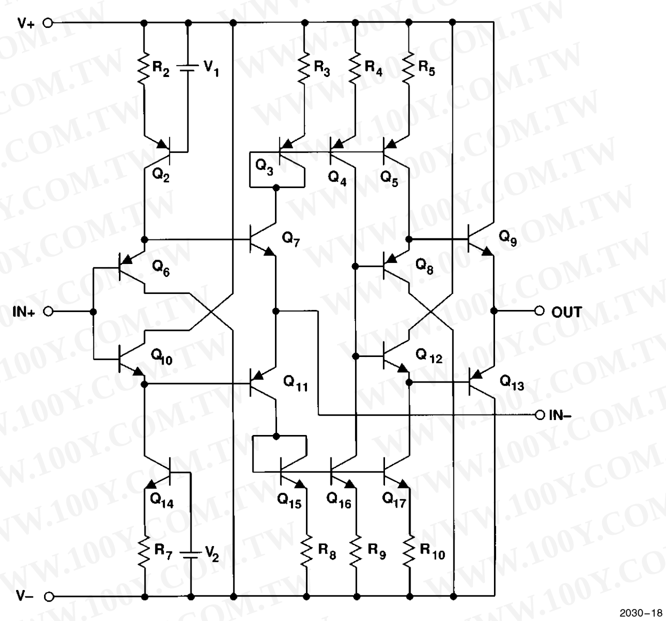
For video applications where a gain of two is used (double termination), the output of the video amplifier will be a maximum of 2V peak-peak. With ±5V power supply, the EL2030 output swing of 3.5V is sufficient to satisfy the video output swing requirements. The EL2030 can drive two double terminated coax cables under these conditions. With ±15V supplies, driving four double terminated cables is feasible.

Although the EL2030's video characteristics (differential gain and phase) are impressive with ±5V supplies at NTSC and PAL frequencies, it can be optimized when the supplies are increased to ±15V, especially at 30 MHz HDTV applications. This is primarily due to a reduction in internal parasitic junction capacitance with increased power supply voltage.

The following table summarizes the behavior of the EL2030 at ±5V and ±15V for NTSC. In addition, 30 MHz HDTV data is included. Refer to the differential gain and phase typical performance curves for more data.

$\pm V_S$	Rload	A_V	ΔGain	ΔPhase	Comments
15V	75Ω	1	0.02%	0.03°	Single terminated
15V	150Ω	1	0.02%	0.02°	Double terminated
5V	150Ω	1	0.05%	0.02°	Double terminated
15V	75Ω	2	0.02%	0.08°	Single terminated
15V	150Ω	2	0.01%	0.02°	Double terminated
5V	150Ω	2	0.03%	0.09°	Double terminated
15V	150Ω	2	0.05%	0.02°	HDTV, Double terminated

Equivalent Circuit



EL2030 Macromodel

```
* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:    +input
*                 |      -input
*                 |      |      +Vsupply
*                 |      |      |      -Vsupply
*                 |      |      |      |      output
*                 |      |      |      |      |
.subckt M2030     3      2      7      4      6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 50
l1 11 12 48nH
iinp 3 0 5µA
iinm 2 0 10µA
r12 3 0 2Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
*e2 30 0 14 0 0.00166666666
l3 30 17 0.5µH
c5 17 0 1pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 150K
cdp 18 0 2.8pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
```


TAB WIDE

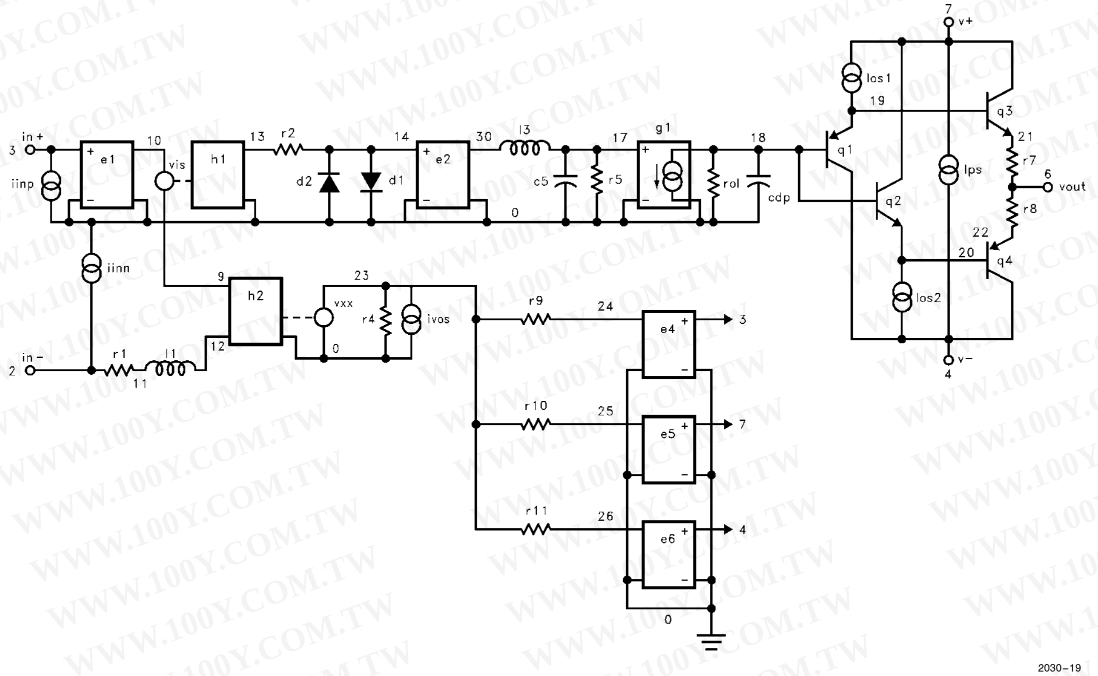
TD is 6.5in

EL2030 Macromodel — Contd.

```
ios1 7 19 2.5mA
ios2 20 4 2.5mA
*
* Supply Current
*
ips 7 4 9mA
*
* Error Terms
*
ivos 0 23 5mA
vxx 23 0 0V
e4 24 3 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 3K
r10 25 23 1K
r11 26 23 1K
*
* Models
*
.model qn npn (is=5e-15 bf=100 tf=0.1nS)
.model qp pnp (is=5e-15 bf=100 tf=0.1nS)
.model dclamp d(is=1e-30 ibv=0.266 bv=3.7 n=4)
.ends
```

TD is 3.1in

EL2030 Macromodel — Contd.



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EL2030C

120 MHz Current Feedback Amplifier

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