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19-2398; Rev 1; 7/93

MAXIM

# Ultra-Fast ECL-Output Comparator with Latch Enable



## General Description

The MAX9685 is an ultra-fast ECL comparator manufactured with a high-frequency bipolar process ($f_T$ = 6GHz) capable of very short propagation delays. This design maintains the excellent DC matching characteristics normally found only in slower comparators.

The device is pin-compatible with the AD9685 and Am6685, but exceeds their AC characteristics.

The MAX9685 has differential inputs and complementary outputs that are fully compatible with ECL-logic levels. Output current levels are capable of driving 50Ω terminated transmission lines. The ultra-fast operation makes signal processing possible at frequencies in excess of 600MHz.

A latch-enable (LE) function is provided to allow the comparator to be used in a sample-hold mode. When LE is ECL high, the comparator functions normally. When LE is driven ECL low, the outputs are forced to an unambiguous ECL-logic state, dependent on the input conditions at the time of the latch input transition. If the latch-enable function is not used, the LE pin must be connected to ground.

## Applications

High-Speed A/D Converters
High-Speed Line Receivers
Peak Detectors
Threshold Detectors
High-Speed Triggers

## Features

- **1.3ns Propagation Delay**
- **0.5ns Latch Setup Time**
- **+5V, -5.2V Power Supplies**
- **Pin-Compatible with AD9685, Am6685**
- **Available in Commercial, Extended-Industrial, and Military Temperature Ranges**
- **Available in Narrow SO Package**

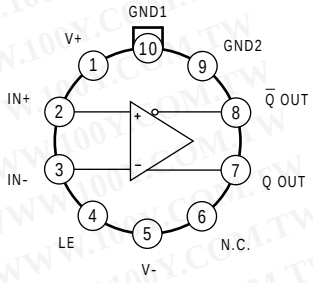
## Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE* |
|---|---|---|
| MAX9685CPE | 0°C to +70°C | 16 Plastic DIP |
| MAX9685CSE | 0°C to +70°C | 16 Narrow SO |
| MAX9685CJE | 0°C to +70°C | 16 CERDIP |
| MAX9685CTW | 0°C to +70°C | 10 TO-100 |
| MAX9685C/D | 0°C to +70°C | Dice** |
| MAX9685EPE | -40°C to +85°C | 16 Plastic DIP |
| MAX9685ESE | -40°C to +85°C | 16 Narrow SO |
| MAX9685MJE | -55°C to +125°C | 16 CERDIP |
| MAX9685MTW | -55°C to +125°C | 10 TO-100 |

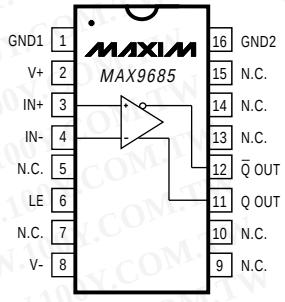
** Contact factory for availability of 20-pin PLCC.*
*** Contact factory for dice specifications.*

## Pin Configurations

TOP VIEW




**TO-100**




**DIP/SO**



Call toll free 1-800-998-8800 for free samples or literature.

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# Ultra-Fast ECL-Output Comparator with Latch Enable

## ABSOLUTE MAXIMUM RATINGS

Supply Voltages ..... ±6V
Output Short-Circuit Duration ..... Indefinite
Input Voltages ..... ±5V
Differential Input Voltages ..... 7.0V
Output Current ..... 30mA
Continuous Power Dissipation ($T_A$ = +70°C)
Plastic DIP (derate 10.53mW/°C above +70°C) ..... 842mW
Narrow SO (derate 8.70mW/°C above +70°C) ..... 696mW
CERDIP (derate 10.00mW/°C above +70°C) ..... 800mW
TO-100 (derate 6.67mW/°C above +70°C) ..... 533mW
Operating Temperature Ranges
MAX9685C_ _ ..... 0°C to +70°C
MAX9685E_ _ ..... -40°C to +85°C
MAX9685M_ _ ..... -55°C to +125°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

(V+ = +5V, V- = -5.2V, $R_L$ = 50Ω, $V_T$ = -2V, $T_A$ = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MAX9685C/E MIN | MAX9685C/E TYP | MAX9685C/E MAX | MAX9685M MIN | MAX9685M TYP | MAX9685M MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{OS}$ | $R_S$ =100Ω | $T_A$ = +25°C | -5 | | 5 | -5 | | 5 | mV |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | -7 | | 7 | -8 | | 8 | |
| Temperature Coefficient | $\Delta V_{OS}/\Delta T$ | | | | 10 | | | 15 | | µV/°C |
| Input Offset Current | $I_{OS}$ | $T_A$ = +25°C | | | | 5 | | | 5 | µA |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | | 8 | | | 12 | |
| Input Bias Current | $I_B$ | $T_A$ = +25°C | | | 10 | 20 | | 10 | 20 | µA |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | | 30 | | | 40 | |
| Input Voltage Range | $V_{CM}$ | (Note 1) | | -2.5 | | +2.5 | -2.5 | | +2.5 | V |
| Common-Mode Rejection Ratio | CMRR | | | 80 | | | 80 | | | dB |
| Power-Supply Rejection Ratio | PSRR | | | | 60 | | | 60 | | dB |
| Input Resistance | $R_{IN}$ | (Note 1) | | 60 | | | 60 | | | kΩ |
| Input Capacitance | $C_{IN}$ | | | | 3 | | | 3 | | pF |
| Logic Output High Voltage | $V_{OH}$ | MAX9685C, MAX9685M | $T_A$ = $T_{MIN}$ | -1.05 | | -0.87 | -1.16 | | -0.89 | V |
| | | | $T_A$ = $T_{MAX}$ | -0.89 | | -0.70 | 0.88 | | -0.69 | |
| | | | $T_A$ = +25°C | -0.96 | | -0.81 | -0.96 | | -0.81 | |
| | | MAX9685E | $T_A$ = $T_{MIN}$ | -1.14 | | -0.88 | | | | |
| | | | $T_A$ = $T_{MAX}$ | -0.88 | | -0.70 | | | | |
| | | | $T_A$ = +25°C | -0.96 | | -0.81 | | | | |
| Logic Output Low Voltage | $V_{OL}$ | MAX9685C, MAX9685M | $T_A$ = $T_{MIN}$ | -1.89 | | -1.69 | -1.90 | | -1.65 | V |
| | | | $T_A$ = $T_{MAX}$ | -1.83 | | -1.57 | -1.82 | | -1.55 | |
| | | | $T_A$ = +25°C | -1.85 | | -1.65 | -1.85 | | -1.65 | |
| | | MAX9685E | $T_A$ = $T_{MIN}$ | -1.90 | | -1.65 | | | | |
| | | | $T_A$ = $T_{MAX}$ | -1.83 | | -1.57 | | | | |
| | | | $T_A$ = +25°C | -1.85 | | -1.65 | | | | |
| Positive Supply Current | $I_{CC}$ | $T_A$ = +25°C | | | 16 | 22 | | 16 | 22 | mA |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | | 24 | | | 25 | |
| Negative Supply Current | $I_{EE}$ | $T_A$ = +25°C | | | 20 | 32 | | 20 | 32 | mA |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | | 36 | | | 36 | |

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## SWITCHING CHARACTERISTICS

(V+ = 5V, V- = -5.2V, $R_L$ = 50Ω, $V_T$ = -2V, $T_A$ = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MAX9685C/E | | | MAX9685M | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Input to Output High (Notes 1, 2) | $t_{pd+}$ | $T_A$ = +25°C | | 1.3 | 1.8 | | 1.3 | 1.8 | ns |
| | | $T_A$ = 0°C to +70°C | | 1.5 | 2.0 | | | | |
| | | $T_A$ = -55°C to +125°C | | | | | 1.7 | 2.4 | |
| Input to Output Low (Notes 1, 2) | $t_{pd-}$ | $T_A$ = +25°C | | 1.3 | 1.8 | | 1.3 | 1.8 | ns |
| | | $T_A$ = 0°C to +70°C | | 1.5 | 2.0 | | | | |
| | | $T_A$ = -55°C to +125°C | | | | | 1.7 | 2.4 | |
| Latch-Enable to Output High (Notes 1, 2) | $t_{pd+}(E)$ | $T_A$ = +25°C | | 1.2 | 1.7 | | 1.2 | 1.7 | ns |
| | | $T_A$ = 0°C to +70°C | | 1.4 | 2.0 | | | | |
| | | $T_A$ = -55°C to +125°C | | | | | 2.0 | 3.0 | |
| Latch-Enable to Output High (Notes 1, 2) | $t_{pd-}(E)$ | $T_A$ = +25°C | | 1.2 | 1.7 | | 1.2 | 1.7 | ns |
| | | $T_A$ = 0°C to +70°C | | 1.4 | 2.0 | | | | |
| | | $T_A$ = -55°C to +125°C | | | | | 2.0 | 3.0 | |
| Latch-Enable Pulse Width (Note 2) | $t_{pw}(E)$ | | 3.0 | 2.0 | | 3.0 | 2.0 | | ns |
| Minimum Setup Time | $t_S$ | | | 0.5 | 1.0 | | 0.5 | 1.0 | ns |
| Minimum Hold Time | $t_h$ | | | 0.5 | 1.0 | | 0.5 | 1.0 | ns |

**Note 1:** Not tested, guaranteed by design.
**Note 2:** $V_{IN}$ = 100mV, $V_{OD}$ = 10mV

## Applications Information

### Layout

Because of the MAX9685's large gain-bandwidth characteristic, special precautions need to be taken if its high-speed capabilities are to be used. A PC board with a ground plane is mandatory. Mount all decoupling capacitors as close to the power-supply pins as possible, and process the ECL outputs in microstrip fashion, consistent with the load termination of 50Ω to 120Ω. For low-impedance applications, microstrip layout at the input may also be helpful. Pay close attention to the bandwidth of the decoupling and terminating components. Chip components can be used to minimize lead inductance. An unused LE pin must be connected to ground.

### Input Slew-Rate Requirements

As with all high-speed comparators, the high gain-bandwidth product of these devices creates oscillation problems when the input traverses through the linear region. For clean switching without oscillation or steps in the output waveform, the input must meet certain minimum slew-rate requirements. The tendency of the part to oscillate is a function of the layout and source impedance of the circuit employed. Poor layout and larger source impedance will increase the minimum slew-rate requirement.

Figure 1 shows a high-speed receiver application with 50Ω input and output termination. With this configuration, in which a ground plane and microstrip PC board were used, the minimum slew rate for clean output switching is 1.6V/µs. Sine-wave inputs imply a minimum signal size of $360mV_{RMS}$ at 500kHz and $90mV_{RMS}$ at 4MHz.

$$E_{RMS} = \frac{\text{Slew Rate}}{2\sqrt{2nf}}$$

In many applications, the addition of regenerative feedback will assist the input signal through the linear region, which will lower the minimum slew-rate requirement considerably. For example, with the addition of positive feedback components $R_f$ = 1kΩ and $C_f$ = 10pF, the minimum slew-rate requirement can be reduced by a factor of four.

# Ultra-Fast ECL-Output Comparator with Latch Enable

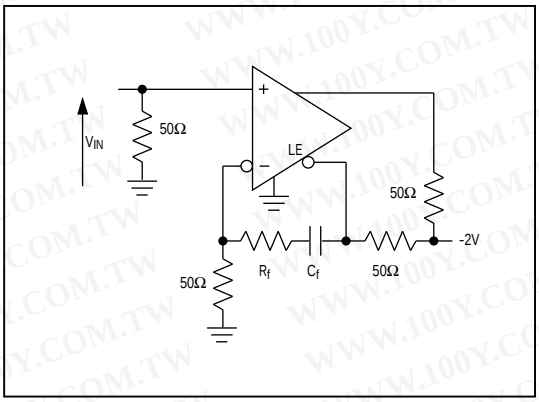


*Figure 1. Regenerative Feedback. High-speed receiver with 50Ω input and output termination.*

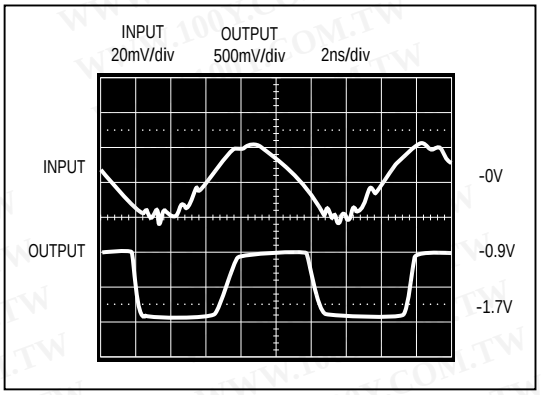


*Figure 2. As a high-speed receiver, the MAX9685 is capable of processing signals in excess of 600MHz. Figure 2 is a 100MHz example with an input signal level of 14mV$_{RMS}$.*

The timing diagram (Figure 3) illustrates the series of events that complete the compare function, under worst-case conditions.

The top line of the diagram illustrates two latch-enable pulses. Each pulse is high for the compare function and low for the latch function. The first pulse demonstrates the compare function; part of the input action takes place during the compare mode. The second pulse demonstrates a compare-function interval during which there is no change in the input.

The leading edge of the input signal (illustrated as a large-amplitude, small-overdrive pulse) switches the comparator after time interval $t_{pd}$. Output Q and $\overline{Q}$ transistors are similar in timing. The input signal must occur at time $t_S$ before the latch falling edge, and it must be maintained for time $t_h$ after the edge to be acquired. After $t_h$, the output is no longer affected by the input status until the latch is again strobed. A minimum latch pulse width of $t_{PW}(E)$ is needed for the strobe operation, and the output transitions occur after a time $t_{pd}(E)$.

### *Definition of Terms*

$V_{OS}$ Input Offset Voltage—The voltage required between the input terminals to obtain 0V differential at the output.

$V_{IN}$ Input Voltage Pulse Amplitude

$V_{OD}$ Input Voltage Overdrive

$t_{pd+}$ Input to Output High Delay—The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output low-to-high transition.

$t_{pd-}$ Input to Output Low Delay—The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output high-to-low transition.

$t_{pd+}(E)$ Latch-Enable to Output High Delay—The propagation delay measured from the 50% point of the latch-enable signal low-to-high transition to the 50% point of an output low-to-high transition.

$t_{pd-}(E)$ Latch-Enable to Output Low Delay—The propagation delay measured from the 50% point of the latch-enable signal low-to-high transition to the 50% point of an output high-to-low transition.

$t_{PW}(E)$ Minimum Latch-Enable Pulse Width—The minimum time the latch-enable signal must be high to acquire and hold an input signal.

$t_S$ Minimum Setup Time—The minimum time before the negative transition of the latch-enable pulse that an input signal must be present to be acquired and held at the outputs.

$t_h$ Minimum Hold Time—The minimum time after the negative transition of the latch-enable signal that an input signal must remain unchanged to be acquired and held at the output.



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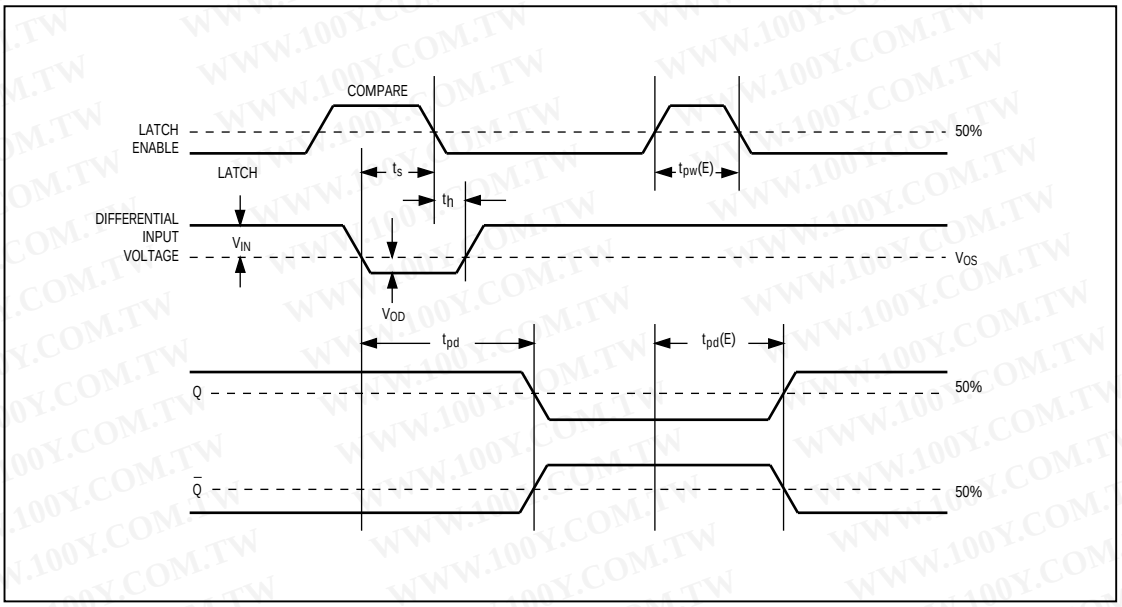


*Figure 3. Timing Diagram*

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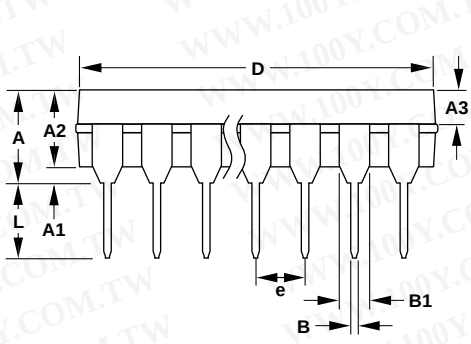
# Ultra-Fast ECL-Output Comparator with Latch Enable

## Package Information

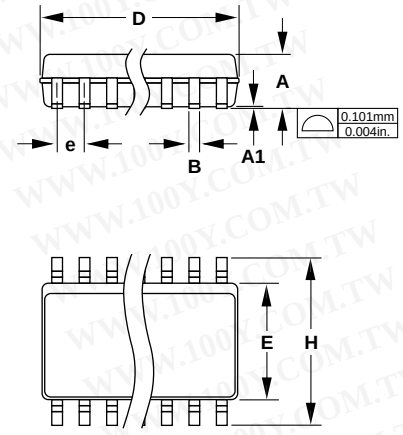



| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | – | 0.200 | – | 5.08 |
| A1 | 0.015 | – | 0.38 | – |
| A2 | 0.125 | 0.175 | 3.18 | 4.45 |
| A3 | 0.055 | 0.080 | 1.40 | 2.03 |
| B | 0.016 | 0.022 | 0.41 | 0.56 |
| B1 | 0.045 | 0.065 | 1.14 | 1.65 |
| C | 0.008 | 0.012 | 0.20 | 0.30 |
| D1 | 0.005 | 0.080 | 0.13 | 2.03 |
| E | 0.300 | 0.325 | 7.62 | 8.26 |
| E1 | 0.240 | 0.310 | 6.10 | 7.87 |
| e | 0.100 | – | 2.54 | – |
| eA | 0.300 | – | 7.62 | – |
| eB | – | 0.400 | – | 10.16 |
| L | 0.115 | 0.150 | 2.92 | 3.81 |

**Plastic DIP**
**PLASTIC**
**DUAL-IN-LINE**
**PACKAGE**
**(0.300 in.)**

| PKG. | DIM | PINS | INCHES | | MILLIMETERS | |
|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX |
| P | D | 8 | 0.348 | 0.390 | 8.84 | 9.91 |
| P | D | 14 | 0.735 | 0.765 | 18.67 | 19.43 |
| P | D | 16 | 0.745 | 0.765 | 18.92 | 19.43 |
| P | D | 18 | 0.885 | 0.915 | 22.48 | 23.24 |
| P | D | 20 | 1.015 | 1.045 | 25.78 | 26.54 |
| N | D | 24 | 1.14 | 1.265 | 28.96 | 32.13 |

21-0043A




| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.007 | 0.010 | 0.19 | 0.25 |
| E | 0.150 | 0.157 | 3.80 | 4.00 |
| e | 0.050 | | 1.27 | |
| H | 0.228 | 0.244 | 5.80 | 6.20 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

**Narrow SO**
**SMALL-OUTLINE**
**PACKAGE**
**(0.150 in.)**

| DIM | PINS | INCHES | | MILLIMETERS | |
|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX |
| D | 8 | 0.189 | 0.197 | 4.80 | 5.00 |
| D | 14 | 0.337 | 0.344 | 8.55 | 8.75 |
| D | 16 | 0.386 | 0.394 | 9.80 | 10.00 |

21-0041A

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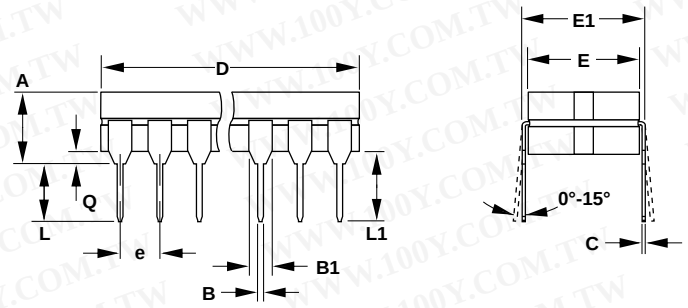
## Package Information (continued)

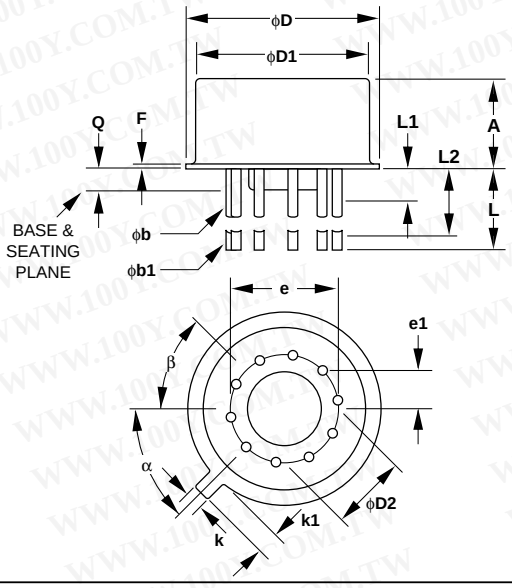



| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | – | 0.200 | – | 5.08 |
| B | 0.014 | 0.023 | 0.36 | 0.58 |
| B1 | 0.038 | 0.065 | 0.97 | 1.65 |
| C | 0.008 | 0.015 | 0.20 | 0.38 |
| E | 0.220 | 0.310 | 5.59 | 7.87 |
| E1 | 0.290 | 0.320 | 7.37 | 8.13 |
| e | 0.100 | | 2.54 | |
| L | 0.125 | 0.200 | 3.18 | 5.08 |
| L1 | 0.150 | – | 3.81 | – |
| Q | 0.015 | 0.070 | 0.38 | 1.78 |
| S | – | 0.098 | – | 2.49 |
| S1 | 0.005 | – | 0.13 | – |

| DIM | PINS | INCHES | | MILLIMETERS | |
|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX |
| D | 8 | – | 0.405 | – | 10.29 |
| D | 14 | – | 0.785 | – | 19.94 |
| D | 16 | – | 0.840 | – | 21.34 |
| D | 18 | – | 0.960 | – | 24.38 |
| D | 20 | – | 1.060 | – | 26.92 |
| D | 24 | – | 1.280 | – | 32.51 |

21-0045A

**CERDIP**
**CERAMIC DUAL-IN-LINE PACKAGE**
**(0.300 in.)**




| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.165 | 0.185 | 4.19 | 4.70 |
| φb | 0.016 | 0.019 | 0.41 | 0.48 |
| φb1 | 0.016 | 0.021 | 0.41 | 0.53 |
| φD | 0.335 | 0.375 | 8.51 | 9.40 |
| φD1 | 0.305 | 0.335 | 7.75 | 8.51 |
| φD2 | 0.110 | 0.160 | 2.79 | 4.06 |
| e | 0.230 BSC | | 5.84 BSC | |
| e1 | 0.115 BSC | | 2.92 BSC | |
| F | | 0.040 | | 1.02 |
| k | 0.027 | 0.034 | 0.69 | 0.86 |
| k1 | 0.027 | 0.045 | 0.69 | 1.14 |
| L | 0.500 | 0.750 | 12.70 | 19.05 |
| L1 | | 0.050 | | 1.27 |
| L2 | 0.250 | | 6.35 | |
| Q | 0.010 | 0.045 | 0.25 | 1.14 |
| α | 36° BSC | | 36° BSC | |
| β | 36° BSC | | 36° BSC | |

21-0023A

**10-PIN**
**TO-100 METAL CAN PACKAGE**



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