# DATA SHEET



## NE/SA5204A
## Wide-band high-frequency amplifier

Product specification

1992 Feb 25

RF Communications Handbook



PHILIPS

# Wide-band high-frequency amplifier NE/SA5204A

## DESCRIPTION

The NE/SA5204A family of wideband amplifiers replaces the NE/SA5204 family. The 'A' parts are fabricated on a rugged 2µm bipolar process featuring excellent statistical process control. Electrical performance is nomically identical to the original parts.

The NE/SA5204A is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 200MHz. The -3dB bandwidth is greater than 350MHz. This performance makes the amplifier ideal for cable TV applications. The NE/SA5204A operates with a single supply of 6V, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

The NE/SA5204A is a relaxed version of the NE5205. Minimum guaranteed bandwidth is relaxed to 350MHz and the "S" parameter Min/Max limits are specified as typicals only.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA5204A solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The standing wave ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output over the entire DC to 350MHz operating range.

Since the part is a small, monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

No external components are needed other than AC-coupling capacitors because the NE/SA5204A is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm, respectively, at 100MHz.

The part is well matched for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters, and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio, and data/video transmission in fiber optics, as well as broadband LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA5204As in series as required, without any degradation in amplifier stability.

## PIN CONFIGURATION

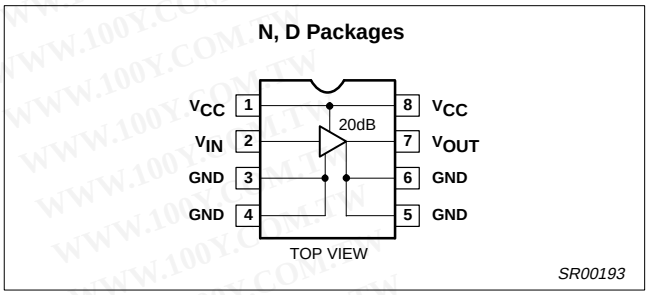



**Figure 1. Pin Configuration**

## FEATURES

- Bandwidth (min.)
  200 MHz, ±0.5dB
  350 MHz, -3dB
- 20dB insertion gain
- 4.8dB (6dB) noise figure $Z_O$=75Ω ($Z_O$=50Ω)
- No external components required
- Input and output impedances matched to 50/75Ω systems
- Surface-mount package available
- Cascadable
- 2000V ESD protection

## APPLICATIONS

- Antenna amplifiers
- Amplified splitters
- Signal generators
- Frequency counters
- Oscilloscopes
- Signal analyzers
- Broadband LANs
- Networks
- Modems
- Mobile radio
- Security systems
- Telecommunications

## ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE | DWG # |
|---|---|---|---|
| 8-Pin Plastic Dual In-Line Package (DIP) | 0 to +70°C | NE5204AN | SOT97-1 |
| 8-Pin Plastic Small Outline (SO) package | 0 to +70°C | NE5204AD | SOT96-1 |
| 8-Pin Plastic Dual In-Line Package (DIP) | –40 to +85°C | SA5204AN | SOT97-1 |
| 8-Pin Plastic Small Outline (SO) package | –40 to +85°C | SA5204AD | SOT96-1 |

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 9 | V |
| $V_{IN}$ | AC input voltage | 5 | $V_{P-P}$ |
| $T_A$ | Operating ambient temperature range | | |
| | NE grade | 0 to +70 | °C |
| | SA grade | –40 to +85 | °C |
| $P_{DMAX}$ | Maximum power dissipation[1, 2] $T_A$=25°C(still–air) | | |
| | N package | 1160 | mW |
| | D package | 780 | mW |
| $T_J$ | Junction temperature | 150 | °C |
| $T_{STG}$ | Storage temperature range | –55 to +150 | °C |
| $T_{SOLD}$ | Lead temperature (soldering 60s) | 300 | °C |

**NOTES:**
1. Derate above 25°C, at the following rates
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. See “Power Dissipation Considerations” section.

## EQUIVALENT SCHEMATIC

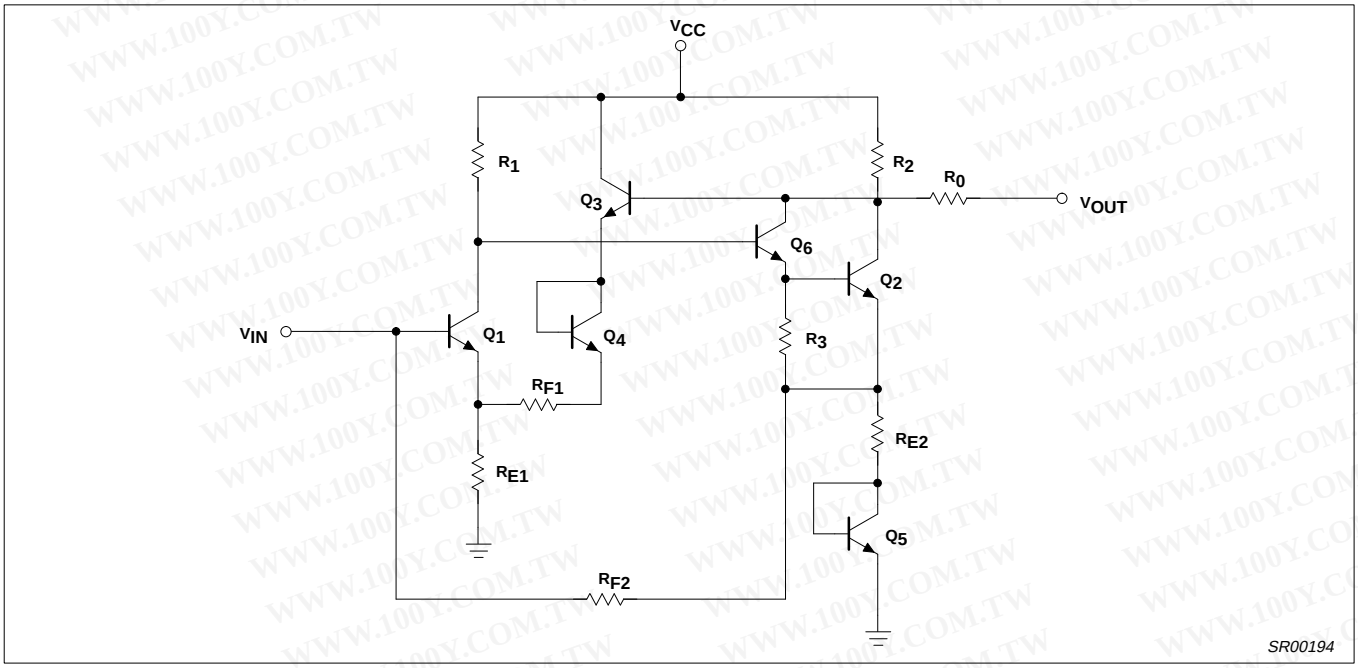



**Figure 2. Equivalent Schematic**

## DC ELECTRICAL CHARACTERISTICS

$V_{CC}$=6V, $Z_S$=$Z_L$=$Z_O$=50Ω and $T_A$=25°C, in all packages, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{CC}$ | Operating supply voltage range | Over temperature | 5 | | 8 | V |
| $I_{CC}$ | Supply current | Over temperature | 19 | 25 | 33 | mA |
| S21 | Insertion gain | f=100MHz, over temperature | 16 | 19 | 22 | dB |
| S11 | Input return loss | f=100MHz | | 25 | | dB |
| | | DC –550MHz | | 12 | | |
| S22 | Output return loss | f=100MHz | | 27 | | dB |
| | | DC –550MHz | | 12 | | |
| S12 | Isolation | f=100MHz | | –25 | | dB |
| | | DC –550MHz | | –18 | | |
| BW | Bandwidth | ±0.5dB | 200 | 350 | | MHz |
| BW | Bandwidth | –3dB | 350 | 550 | | MHz |
| | Noise figure (75Ω) | f=100MHz | | 4.8 | | dB |
| | Noise figure (50Ω) | f=100MHz | | 6.0 | | dB |
| | Saturated output power | f=100MHz | | +7.0 | | dBm |
| | 1dB gain compression | f=100MHz | | +4.0 | | dBm |
| | Third–order intermodulation intercept (output) | f=100MHz | | +17 | | dBm |
| | Second–order intermodulation intercept (output) | f=100MHz | | +24 | | dBm |
| $t_R$ | Rise time | | | 500 | | ps |
| $t_P$ | Propagation delay | | | 500 | | ps |

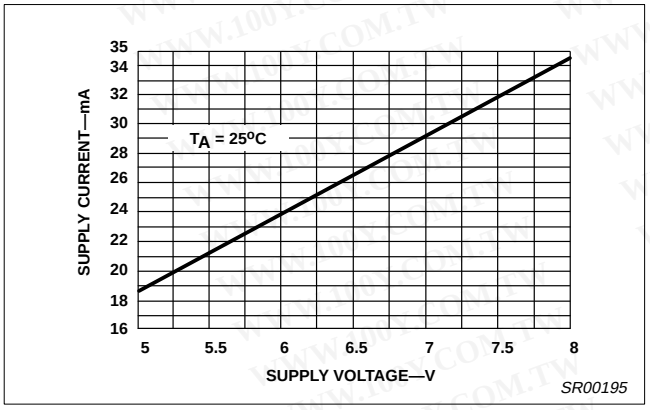



**Figure 3. Supply Current vs Supply Voltage**

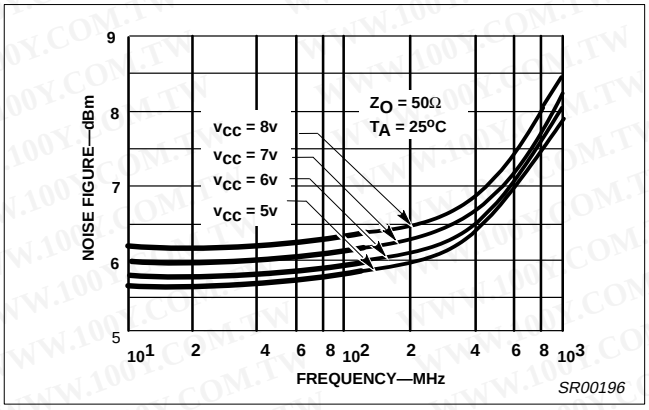



**Figure 4. Noise Figure vs Frequency**

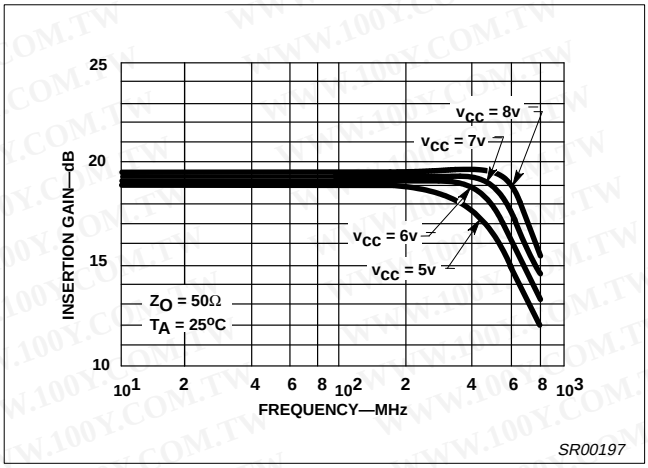



**Figure 5. Insertion Gain vs Frequency ($S_{21}$)**

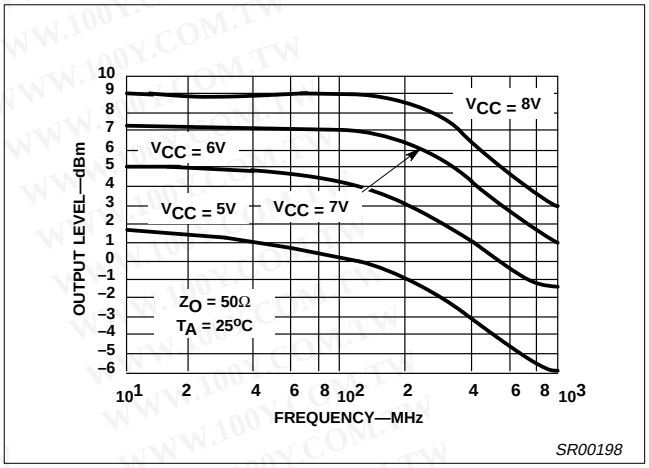



**Figure 8. 1dB Gain Compression vs Frequency**

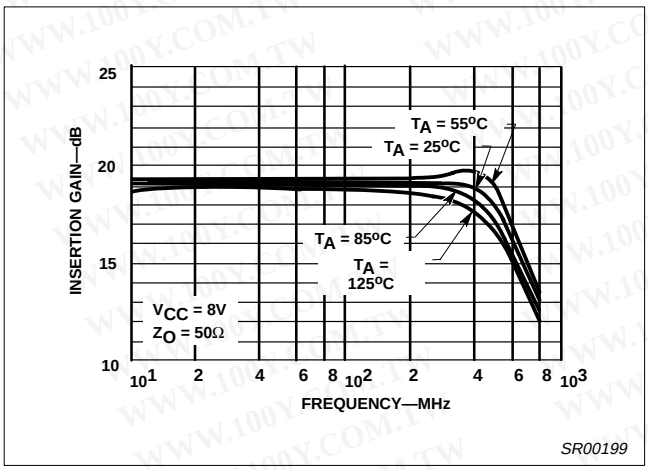



**Figure 6. Insertion Gain vs Frequency ($S_{21}$)**

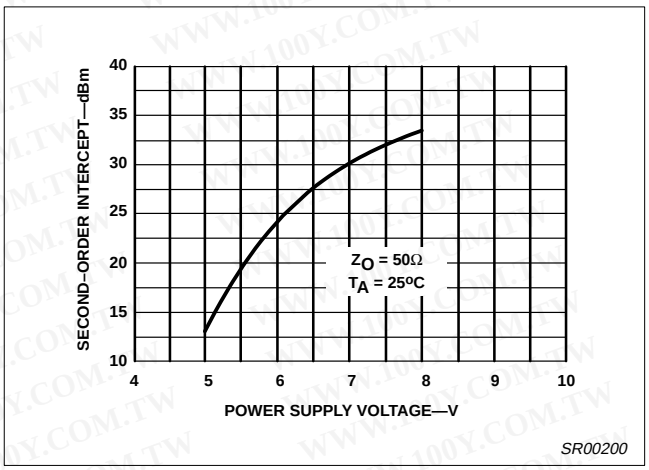



**Figure 9. Second-Order Output Intercept vs Supply Voltage**

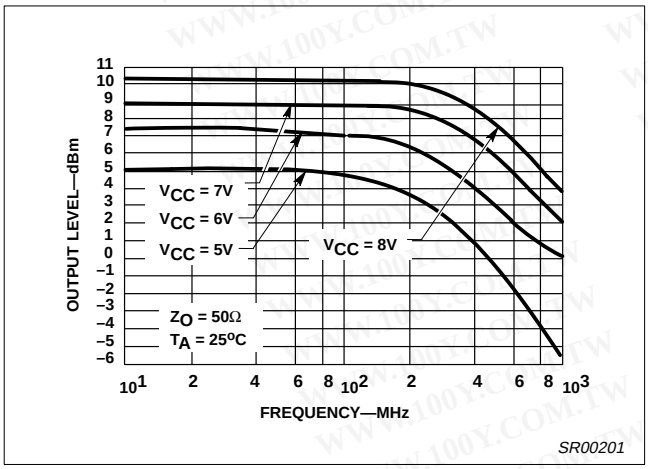



**Figure 7. Saturated Output Power vs Frequency**

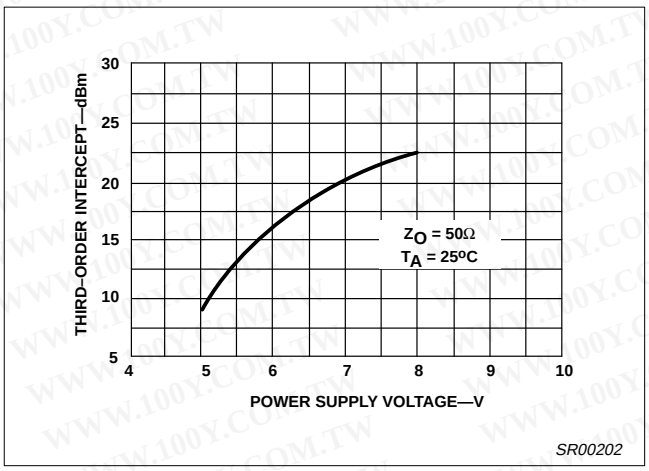



**Figure 10. Third-Order Intercept vs Supply Voltage**

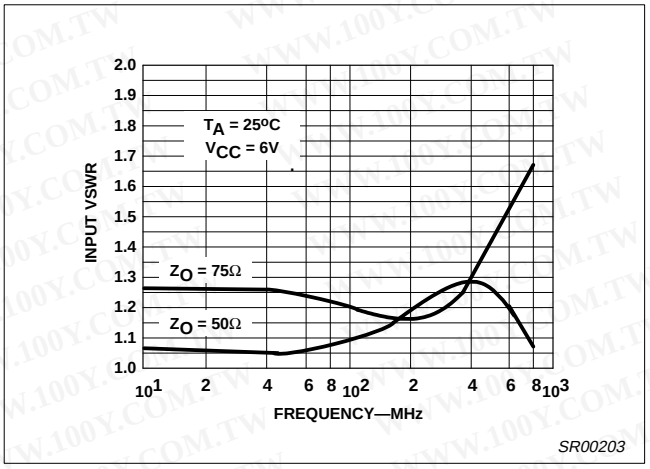



Figure 11. Input VSWR vs Frequency

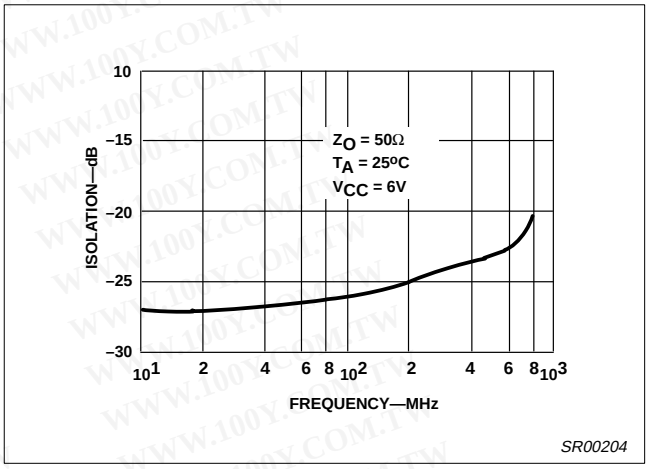



Figure 14. Isolation vs Frequency ($S_{12}$)

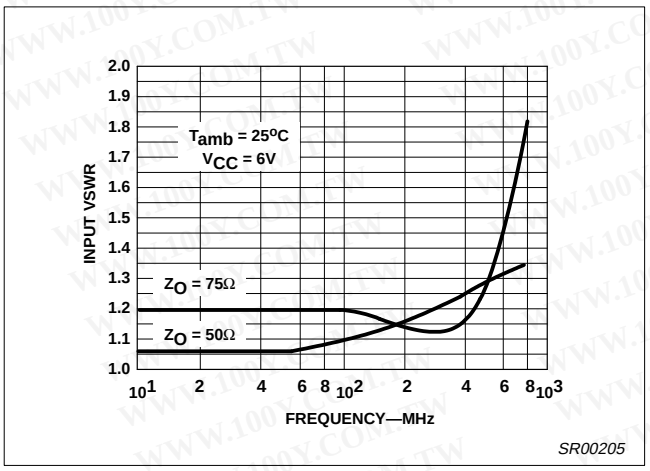



Figure 12. Output VSWR vs Frequency

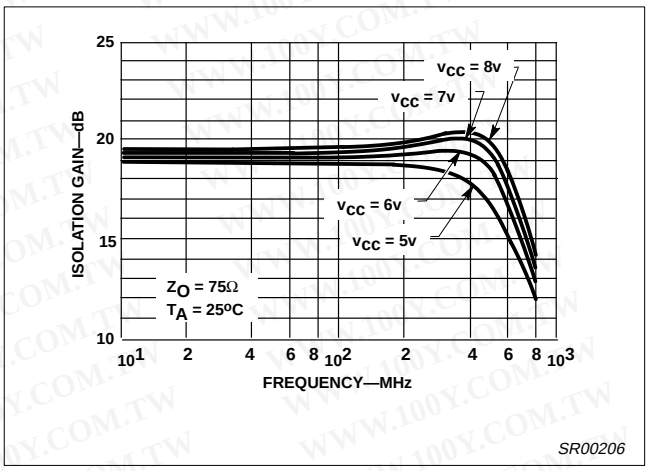



Figure 15. Insertion Gain vs Frequency ($S_{21}$)

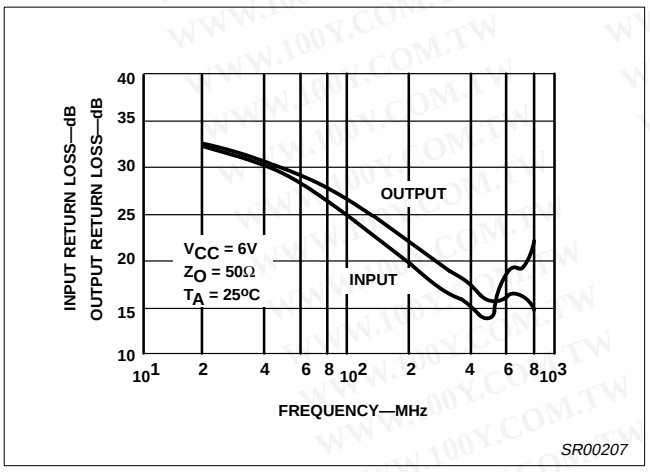



Figure 13. Input ($S_{11}$) and Output ($S_{22}$) Return Loss vs Frequency

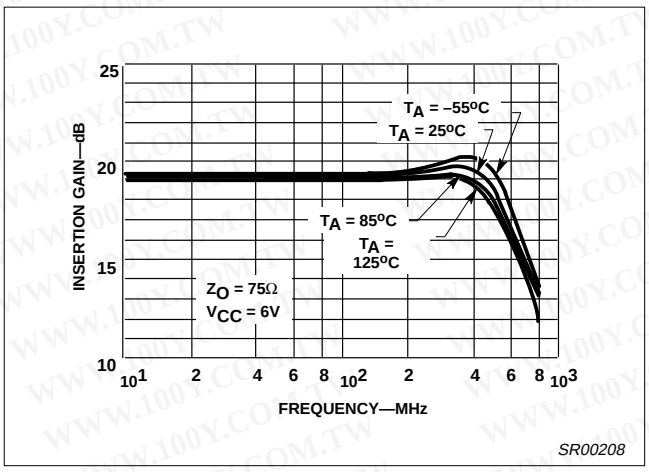



Figure 16. Insertion Gain vs Frequency ($S_{21}$)

## THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 17, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1}) / R_{E1} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to $R_{F2}$ and $R_{E2}$ which aids in producing wide-band terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, $R_{E1}$ and the base resistance of $Q_1$ are kept as low as possible, while $R_{F2}$ is maximized.

The noise figure is given by the following equation:

$$NF = 10\text{Log}\left(1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2qI_{C1}}\right]}{R_O}\right) \text{ dB} \quad (2)$$

where $I_{C1}$=5.5mA, $R_{E1}$=12Ω, $r_b$=130Ω, KT/q=26mV at 25°C and $R_0$=50 for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level $V_{IN}$ can be determined by the equation:

$$V_{IN}=V_{BE1}+(I_{C1}+I_{C3})\ R_{E1} \quad (3)$$

where $R_{E1}$=12Ω, $V_{BE}$=0.8V, $I_{C1}$=5mA and $I_{C3}$=7mA (currents rated at $V_{CC}$=6V).

Under the above conditions, $V_{IN}$ is approximately equal to 1V.

Level shifting is achieved by emitter-follower $Q_3$ and diode $Q_4$, which provide shunt feedback to the emitter of $Q_1$ via $R_{F1}$. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt-feedback loading on the output. The value of $R_{F1}$=140Ω is chosen to give the desired nominal gain. The DC output voltage $V_{OUT}$ can be determined by:

$$V_{OUT}=V_{CC}-(I_{C2}+I_{C6})R2, \quad (4)$$

where $V_{CC}$=6V, $R_2$=225Ω, $I_{C2}$=8mA and $I_{C6}$=5mA.

From here, it can be seen that the output voltage is approximately 3.1V to give relatively equal positive and negative output swings. Diode $Q_5$ is included for bias purposes to allow direct coupling of $R_{F2}$ to the base of $Q_1$. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair ($Q_6$ and $Q_2$) which increases the DC bias voltage on the input stage ($Q_1$) to a more desirable value, and also increases the feedback loop gain. Resistor $R_0$ optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors $L_1$ and $L_2$ are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

## POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (32mA max). For operation at supply voltages other than 6V, see Figure 3 for $I_{CC}$ versus $V_{CC}$ curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat-sinking benefits can be realized by mounting the SO and N package bodies against the PC board plane.

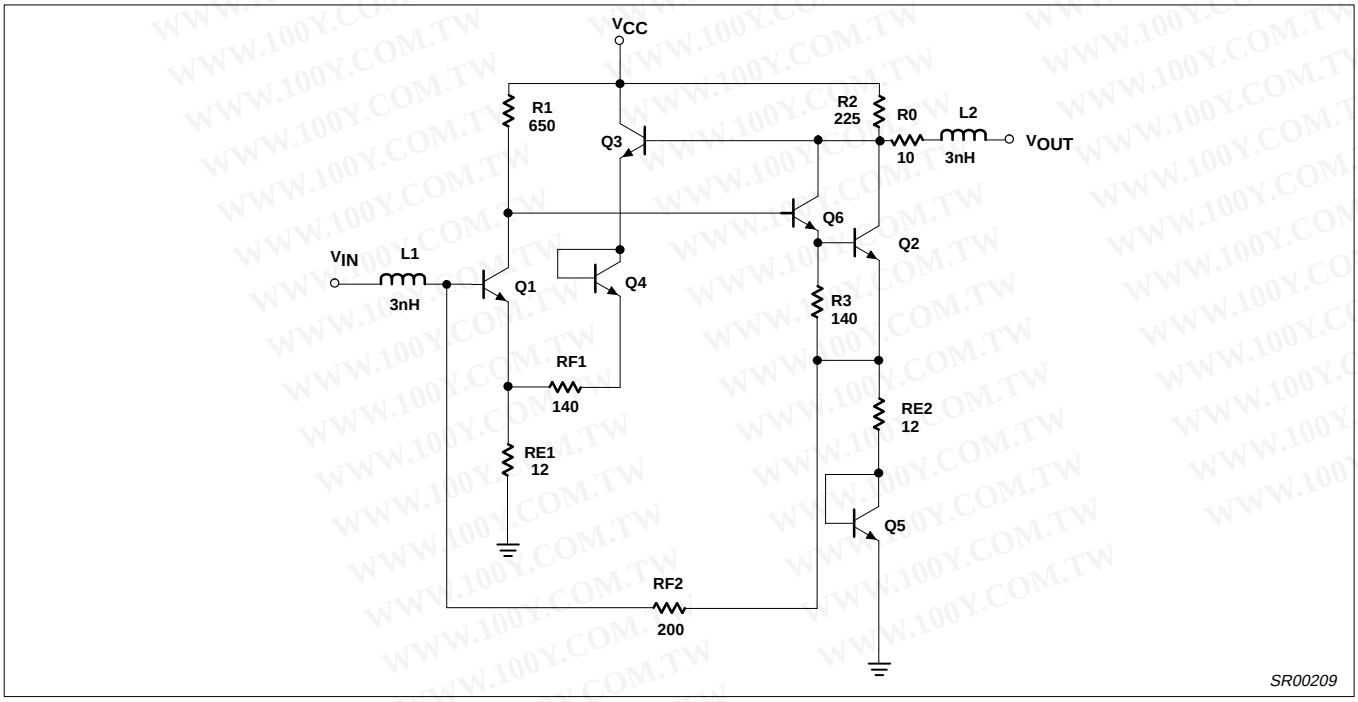



**Figure 17. Schematic Diagram**

## PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5204A to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and $V_{CC}$ pins on the package). The power supply should be decoupled with a capacitor as close to the $V_{CC}$ pins as possible, and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC-coupled. This is because at $V_{CC}$=6V, the input is approximately at 1V while the output is at 3.1V. The output must be decoupled into a low-impedance system, or the DC bias on the output of the amplifier will be loaded down, causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high-frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 18. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

## SCATTERING PARAMETERS

The primary specifications for the NE5204A are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier, and load as well as transmission losses. The parameters for a two-port network are defined in Figure 19.

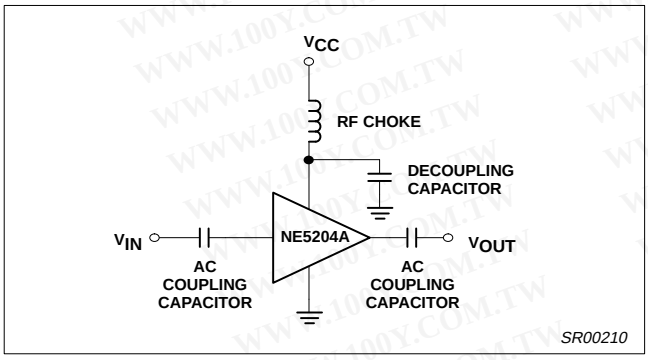
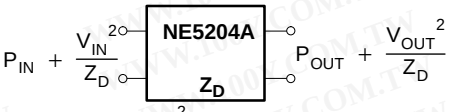



**Figure 18. Circuit Schematic for Coupling and Power Supply Decoupling**

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 20.

Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5204A to other high-frequency amplifiers.
The most important parameter is $S_{21}$. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D=Z_{IN}=Z_{OUT}$ for the NE/SA/SE5204A




$$P_{IN} + \frac{V_{IN}^2}{Z_D} \quad P_{OUT} + \frac{V_{OUT}^2}{Z_D}$$

$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$P_I=V_I{}^2$

$P_I$=Insertion Power Gain

$V_I$=Insertion Voltage Gain

Measured value for the NE/SA/SE5204A = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20\text{dB}$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20\text{dB}$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20\text{dB}$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 21. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

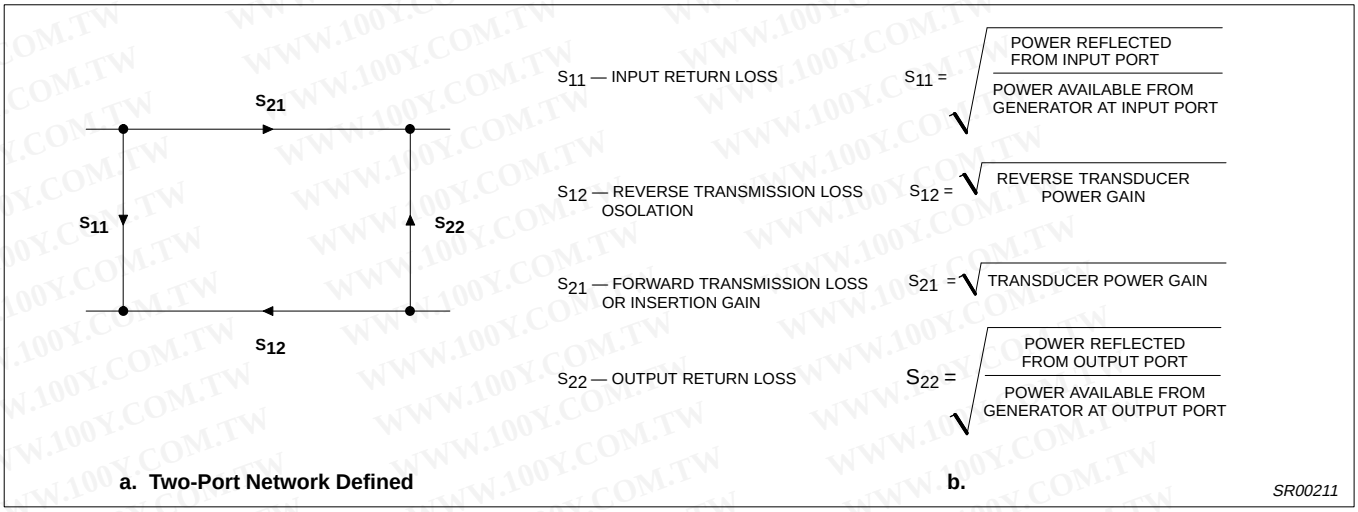

S21
S11
S22
S12
a. Two-Port Network Defined
S11 — INPUT RETURN LOSS
S11 = √ POWER REFLECTED FROM INPUT PORT / POWER AVAILABLE FROM GENERATOR AT INPUT PORT
S12 — REVERSE TRANSMISSION LOSS OSOLATION
S12 = √ REVERSE TRANSDUCER POWER GAIN
S21 — FORWARD TRANSMISSION LOSS OR INSERTION GAIN
S21 = √ TRANSDUCER POWER GAIN
S22 — OUTPUT RETURN LOSS
S22 = √ POWER REFLECTED FROM OUTPUT PORT / POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT
b.
SR00211

**Figure 19.**

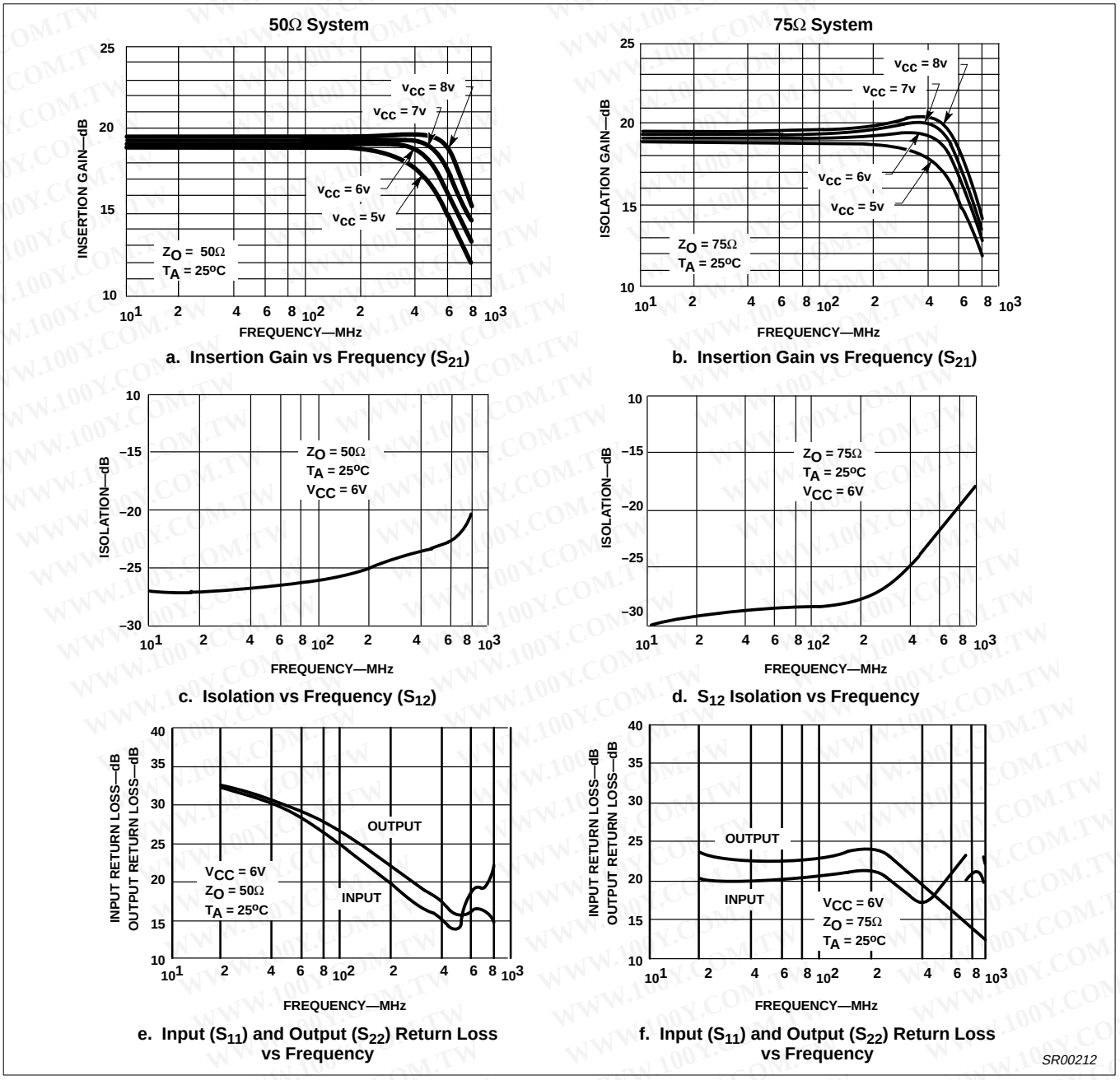



**Figure 20.**

INPUT RETURN LOSS=$S_{11}$dB
$S_{11}$dB=20 Log | $S_{11}$ |

OUTPUT RETURN LOSS=$S_{22}$dB
$S_{22}$dB=20 Log | $S_{22}$ |

INPUT VSWR=≤1.5

OUTPUT VSWR=≤1.5

## 1DB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

## INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and

intermodulation ratio is illustrated in Figure 22, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

$IP_2 = P_{OUT} + IMR_2$

$IP_3 = P_{OUT} + IMR_3/2$

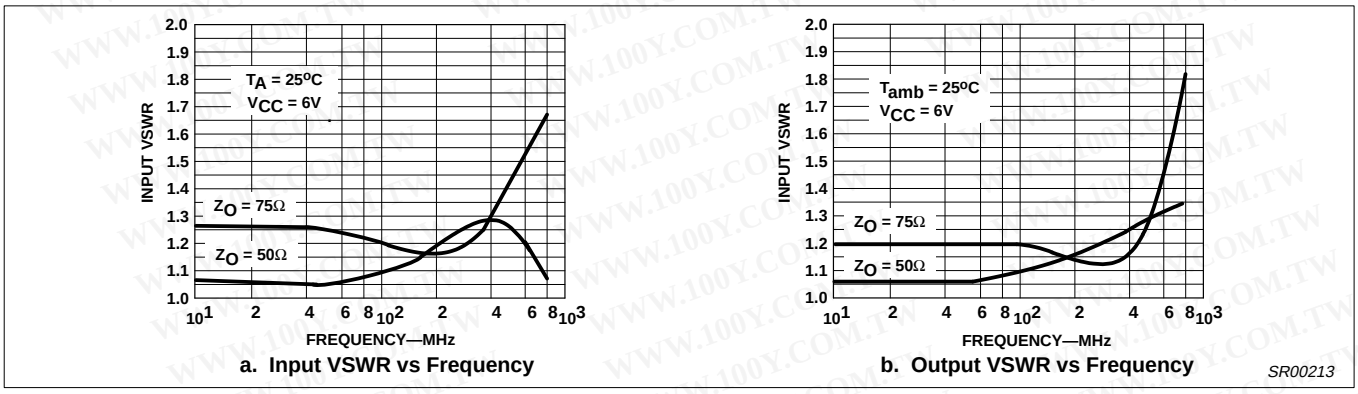
where $P_{OUT}$ is the power level in dBm of each of a pair of equal level fundamental output signals, $IP_2$ and $IP_3$ are the second and third order output intercepts in dBm, and $IMR_2$ and $IMR_3$ are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure $IP_2$ and $IP_3$ at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA5204A we have chosen an output level of –10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.

## ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to High-Frequency Amplifiers by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

“S-Parameter Techniques for Faster, More Accurate Network Design”, HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

“S-Parameter Design”, HP App Note 154, 1972.




a. Input VSWR vs Frequency

b. Output VSWR vs Frequency

**Figure 21. Input/Output VSWR vs Frequency**

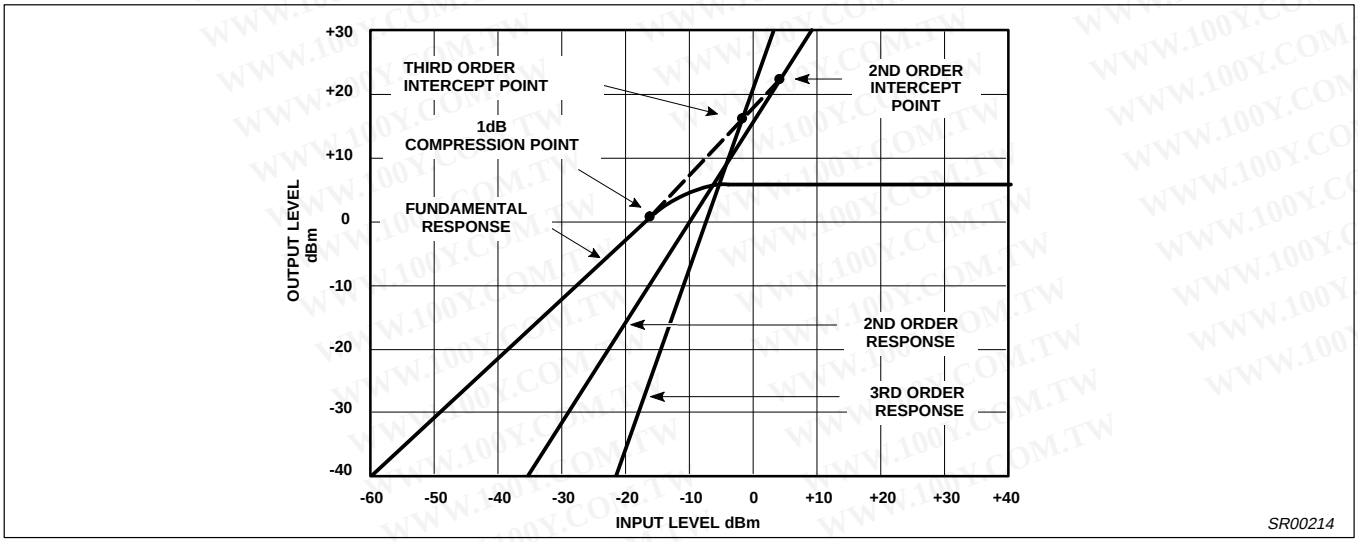
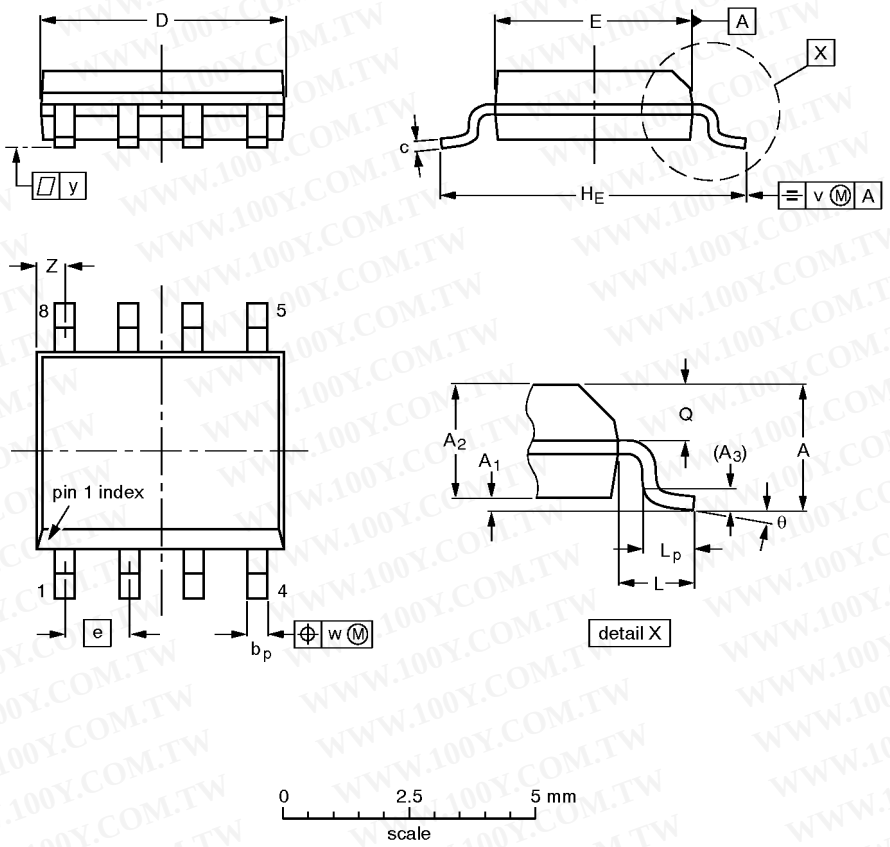



**Figure 22.**

**SO8: plastic small outline package; 8 leads; body width 3.9mm** **SOT96-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

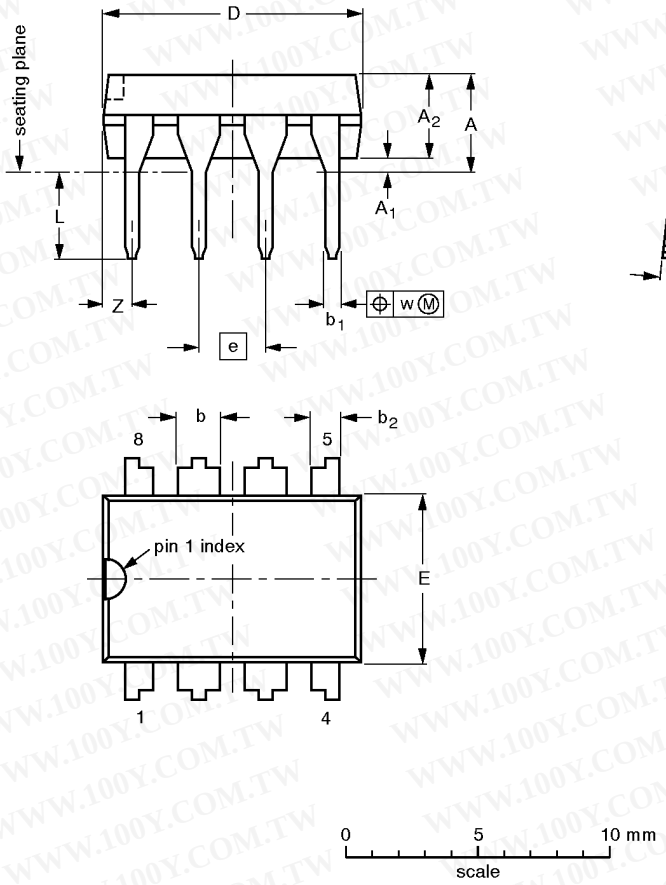
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 5.0<br>4.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | 8°<br>0° |
| inches | 0.069 | 0.0098<br>0.0039 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0098<br>0.0075 | 0.20<br>0.19 | 0.16<br>0.15 | 0.050 | 0.24<br>0.23 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT96-1 | 076E03S | MS-012AA | | | | ~~92-11-17~~<br>95-02-04 |

**DIP8: plastic dual in-line package; 8 leads (300 mil)** **SOT97-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | $b_2$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $e_1$ | L | $M_E$ | $M_H$ | w | $Z^{(1)}$ max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.2 | 0.51 | 3.2 | 1.73<br>1.14 | 0.53<br>0.38 | 1.07<br>0.89 | 0.36<br>0.23 | 9.8<br>9.2 | 6.48<br>6.20 | 2.54 | 7.62 | 3.60<br>3.05 | 8.25<br>7.80 | 10.0<br>8.3 | 0.254 | 1.15 |
| inches | 0.17 | 0.020 | 0.13 | 0.068<br>0.045 | 0.021<br>0.015 | 0.042<br>0.035 | 0.014<br>0.009 | 0.39<br>0.36 | 0.26<br>0.24 | 0.10 | 0.30 | 0.14<br>0.12 | 0.32<br>0.31 | 0.39<br>0.33 | 0.01 | 0.045 |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT97-1 | 050G01 | MO-001AN | | | | ~~92-11-17~~<br>95-02-04 |

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| Data Sheet Identification | Product Status | Definition |
|---|---|---|
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