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RF3194

QUAD-BAND GSM POWER AMP MODULE

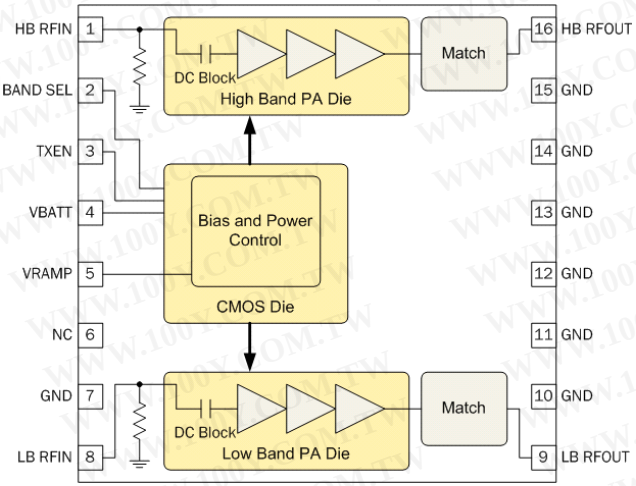
Package: Module, 5.00mmx5.00mmx1.00mm

Features

- Power Margin for Flexible Tuning
- GSM850 Efficiency: 55.5%
- EGSM900 Efficiency: 57%
- DCS1800 Efficiency: 51%
- PCS1900 Efficiency: 53%
- Low Harmonic Power
- 2.6A Current Limiter Reduces Peak Power and Current into VSWR
- Low Switching Spectrum into VSWR
- Industry Standard 5mmx5mm Footprint
- Simple Application Circuitry
- Proven PowerStar® Architecture

Applications

- Battery Powered 2G – 3G Handsets
- GMSK Modulation Transceivers
- Multislot Class 12 Products (4 Transmit Timeslots)



Functional Block Diagram

Product Description

The RF3194 is a high-power, high-efficiency power amplifier module with integrated power control. This device is self-contained with 50Ω input and output terminals. The device is designed for use as the GSM/GPRS power amplifier portion of the transmit chain in 2G and 3G transceivers supporting GSM transmit in the GSM850, EGSM900, DCS, and PCS bands. The RF3194 high performance power amplifier module offers mobile handset designers a compact, easy-to-use, front end component for quick integration into GSM/GPRS, multi-band systems.

Ordering Information

RF3194	Quad-Band GSM Power Amp Module
RF3194SB	Power Amp Module 5-Piece Sample Pack
RF3194PCBA-410	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☑ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☑ Si CMOS	☐ BiFET HBT
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage in Standby Mode	-0.5 to +6.0	V
Supply Voltage in Idle Mode	-0.5 to +6.0	V
Supply Voltage in Operating Mode; Operation time less than 100ms; $V_{RAMP} \leq 1.6V$	-0.5 to +6.0	V
DC Continuous current during burst	2.6	A
Power Control Voltage (V_{RAMP})	-0.5 to 1.8	V
RF Input Power	12	dBm
Duty Cycle at rated power; Period=4.6ms	50	%
Output Load (See Ruggedness Specification)	10:1	VSWR
Operating Temperature	-30 to +85	°C
Storage Temperature	-55 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
General Operating Conditions					
Operating Temperature	-20	25	85	°C	Recommended operating range
V_{BATT} Supply Voltage	3.0	3.6	4.6	V	Recommended operating range
V_{BATT} Supply Current					
Standby		0.1	10	uA	TXEN Low
Operating at Current Limit			2600	mA	
V_{RAMP} Input					Analog control voltage
GMSK Operation	0.2		1.6	V	V_{RAMP} voltage controls saturated power
Impedance	50kΩ		5pF		Worst Case is 50kΩ in parallel with 5pF
TXEN					Logic control voltage
Logic Low Voltage	0	0	0.5	V	
Logic High Voltage	1.3	2.0	3.0	V	
Logic High Current		0.1		uA	
BS					Logic control voltage selects band
Logic Low Voltage	0	0	0.5	V	
Logic High Voltage	1.3	2.0	3.0	V	
Logic High Current		0.1		uA	
RF Input and Output Impedance		50		Ω	Pins 1, 8, 9, 16

Mode	BS (Band Select)	TX_EN (Transmit Enable)	V_{RAMP}
Standby	X	0	X
TXLB	0	1	>0.25
TXHB	1	1	>0.25

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
GSM850 Band					**Unless otherwise stated:** All unused RF ports terminated in 50Ω, Input and Output=50Ω, Temperature=25°C, V_{BATT}=3.6V, Mode=TXLB, GSM timeslots≤2, P_{IN}=3dBm, V_{RAMP}=Max
Operating Frequency	824		849	MHz	
Input Power (P_{IN})	0	3	6	dBm	
Input VSWR			2.5	X:1	P_{OUT}=6.5dBm to Max
Maximum Output Power (Nominal)	34.5	36.4		dBm	P_{IN}=3dBm, Temp=+25°C, V_{BATT}=3.6V
Maximum Output Power (Extreme)	32.5	33.6		dBm	P_{IN}=0dBm, Temp=+85°C, V_{BATT}=3.0V
Power Added Efficiency (Max Power)	48	55.5		%	
Power Added Efficiency (Rated Power)	40	44.5	50	%	P_{OUT}=34.5dBm
Supply Current (Rated Power)	1560	1750	1955	mA	P_{OUT}=34.5dBm
Supply Current (Low Power)		130		mA	P_{OUT}=6.5dBm
Receive Band Noise Power					P_{OUT}≤34.5dBm, Bandwidth=100kHz
869MHz to 894MHz (CEL)		-82	-80	dBm	20MHz noise
1930MHz to 1990 MHz (PCS)		-118	-105	dBm	Out of band noise
Harmonics					P_{OUT}≤34.5dBm
2Fo		-25	-10	dBm	
3Fo		-33	-15	dBm	
4Fo to 12.75GHz		-25	-15	dBm	Typical value of 4Fo
Stability Under Load Mismatch (Spurious Emissions)			-36	dBm	Output Load VSWR=6:1, All phase angles, P_{IN}=0dBm to 6dBm, V_{RAMP}≤V_{RAMP_RP}
Ruggedness Under Load Mismatch	No damage or permanent degradation to device				Output Load VSWR=10:1, All phase angles, Temp=-20°C to +85°C, V_{BATT}=3.0V to 4.6V, V_{RAMP}≤V_{RAMP_RP}
Forward Isolation 1		-45	-30	dBm	Mode=Standby, P_{IN}=Max, V_{RAMP}=Min
Forward Isolation 2		-22	-15	dBm	Mode=TXLB, P_{IN}=Max, V_{RAMP}=Min
Fundamental Cross Coupling		-19	+5	dBm	Measured at HB_RFOUT, Mode=TXLB, V_{RAMP}≤V_{RAMP_RP}
2Fo, 3Fo, Harmonic Cross Coupling		-43	-25	dBm	Measured at HB_RFOUT, Mode=TXLB, V_{RAMP}≤V_{RAMP_RP}

Note: V_{RAMP_RP} is defined as the V_{RAMP} voltage required to achieve 34.5dBm at Output load=50Ω, V_{BATT}=3.6V, Temperature=25°C, P_{IN}=3dBm.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
GSM900 Band					**Unless otherwise stated:** All unused RF ports terminated in 50Ω, Input and Output=50Ω, Temperature=25 °C, V_{BATT}=3.6V, Mode=TXLB, GSM timeslots≤2, P_{IN}=3dBm, V_{RAMP}=Max
Operating Frequency	836		915	MHz	
Input Power (P_{IN})	0	3	6	dBm	
Input VSWR			2.5	X:1	P_{OUT}=6.5dBm to Max
Maximum Output Power (Nominal)	34.5	35.8		dBm	P_{IN}=3dBm, Temp=+25 °C, V_{BATT}=3.6V
Maximum Output Power (Extreme)	32.3	33.0		dBm	P_{IN}=0dBm, Temp=+85 °C, V_{BATT}=3.0V
Power Added Efficiency (Max Power)	50	57		%	
Power Added Efficiency (Rated Power)	43	48.5	56	%	P_{OUT}=34.5dBm
Supply Current (Rated Power)	1400	1610	1800	mA	P_{OUT}=34.5dBm
Supply Current (Low Power)		120		mA	P_{OUT}=6.5dBm
Receive Band Noise Power					P_{OUT}≤34.5dBm, Bandwidth=100kHz
925MHz to 935MHz (EGSM)		-80	-76	dBm	10MHz noise
935MHz to 960MHz (EGSM)		-82	-80	dBm	20MHz noise
1805MHz to 1880MHz (DCS)		-118	-105	dBm	Out of band noise
Harmonics					P_{OUT}≤34.5dBm
2Fo		-18	-10	dBm	
3Fo		-36	-15	dBm	
4Fo to 12.75GHz		-33	-15	dBm	Typical value of 4Fo
Stability Under Load Mismatch (Spurious Emissions)			-36	dBm	Output Load VSWR=6:1, All phase angles, P_{IN}=0dBm to 6dBm, V_{RAMP}≤V_{RAMP_RP}
Ruggedness Under Load Mismatch	No damage or permanent degradation to device				Output Load VSWR=10:1, All phase angles, Temp=-20 °C to +85 °C, V_{BATT}=3.0V to 4.6V, V_{RAMP}≤V_{RAMP_RP}
Forward Isolation 1		-37	-30	dBm	Mode=Standby, P_{IN}=Max, V_{RAMP}=Min
Forward Isolation 2		-22	-15	dBm	Mode=TXLB, P_{IN}=Max, V_{RAMP}=Min
Fundamental Cross Coupling		-10	+5	dBm	Measured at HB_RFOUT, Mode=TXLB, V_{RAMP}≤V_{RAMP_RP}
2Fo, 3Fo, Harmonic Cross Coupling		-34	-25	dBm	Measured at HB_RFOUT, Mode=TXLB, V_{RAMP}≤V_{RAMP_RP}

Note: V_{RAMP_RP} is defined as the V_{RAMP} voltage required to achieve 34.5dBm at Output load=50Ω, V_{BATT}=3.6V, Temperature=25 °C, P_{IN}=3dBm.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
GSM1800 Band					**Unless otherwise stated:** All unused RF ports terminated in 50Ω, Input and Output=50Ω, Temperature=25 °C, V_{BATT}=3.6V, Mode=TXHB, GSM timeslots≤2, P_{IN}=3dBm, V_{RAMP}=Max
Operating Frequency	1710		1785	MHz	
Input Power (P_{IN})	0	3	6	dBm	
Input VSWR			2.5	X:1	P_{OUT}=2.0dBm to Max
Maximum Output Power (Nominal)	32.0	33.4		dBm	P_{IN}=3dBm, Temp=+25 °C, V_{BATT}=3.6V
Maximum Output Power (Extreme)	30.0	30.8		dBm	P_{IN}=0dBm, Temp=+85 °C, V_{BATT}=3.0V
Power Added Efficiency (Max Power)	43	51		%	
Power Added Efficiency (Rated Power)	37.5	43	49	%	P_{OUT}=32.0dBm
Supply Current (Rated Power)	900	1020	1170	mA	P_{OUT}=32.0dBm
Supply Current (Low Power)		120		mA	P_{OUT}=2.0dBm
Receive Band Noise Power					P_{OUT}≤32.0dBm, Bandwidth=100kHz
925MHz to 960MHz (EGSM)		-98	-90	dBm	Out of band noise
1805MHz to 1880MHz (DCS)		-86	-80	dBm	20MHz noise
Harmonics					P_{OUT}≤32.0dBm
2Fo		-38	-10	dBm	
3Fo		-20	-15	dBm	
4Fo to 12.75GHz		-22	-15	dBm	Typical value of 4Fo
Stability Under Load Mismatch (Spurious Emissions)			-36	dBm	Output Load VSWR=6:1, All phase angles, P_{IN}=0dBm to 6dBm, V_{RAMP}≤V_{RAMP_RP}
Ruggedness Under Load Mismatch	No damage or permanent degradation to device				Output Load VSWR=10:1, All phase angles, Temp=-20 °C to +85 °C, V_{BATT}=3.0V to 4.6V, V_{RAMP}≤V_{RAMP_RP}
Forward Isolation 1		-45	-30	dBm	Mode=Standby, P_{IN}=Max, V_{RAMP}=Min
Forward Isolation 2		-24	-15	dBm	Mode=TXLB, P_{IN}=Max, V_{RAMP}=Min

Note: V_{RAMP_RP} is defined as the V_{RAMP} voltage required to achieve 32.0dBm at Output load=50Ω, V_{BATT}=3.6V, Temperature=25 °C, P_{IN}=3dBm.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
GSM1900 Band					**Unless otherwise stated:** All unused RF ports terminated in 50Ω, Input and Output=50Ω, Temperature=25 °C, V_{BATT}=3.6V, Mode=TXHB, GSM timeslots≤2, P_{IN}=3dBm, V_{RAMP}=Max
Operating Frequency	1850		1910	MHz	
Input Power (P_{IN})	0	3	6	dBm	
Input VSWR			2.5	X:1	P_{OUT}=2.0dBm to Max
Maximum Output Power (Nominal)	32.0	32.8		dBm	P_{IN}=3dBm, Temp= +25 °C, V_{BATT}=3.6V
Maximum Output Power (Extreme)	29.5	30.4		dBm	P_{IN}=0dBm, Temp= +85 °C, V_{BATT}=3.0V
Power Added Efficiency (Max Power)	47	53		%	
Power Added Efficiency (Rated Power)	40	46	52	%	P_{OUT}=32.0dBm
Supply Current (Rated Power)	850	950	1100	mA	P_{OUT}=32.0dBm
Supply Current (Low Power)		120		mA	P_{OUT}=2.0dBm
Receive Band Noise Power					P_{OUT}≤32.0dBm, Bandwidth=100kHz
869MHz to 894MHz (EGSM)		-104	-98	dBm	Out of band noise
1930MHz to 1990MHz (DCS)		-88	-80	dBm	20MHz noise
Harmonics					P_{OUT}≤32.0dBm
2Fo		-28	-10	dBm	
3Fo		-25	-15	dBm	
4Fo to 12.75GHz		-20	-10	dBm	Typical value of 4Fo
Stability Under Load Mismatch (Spurious Emissions)			-36	dBm	Output Load VSWR=6:1, All phase angles, P_{IN}=0dBm to 6dBm, V_{RAMP}≤V_{RAMP_RP}
Ruggedness Under Load Mismatch	No damage or permanent degradation to device				Output Load VSWR=10:1, All phase angles, Temp=-20 °C to +85 °C, V_{BATT}=3.0V to 4.6V, V_{RAMP}≤V_{RAMP_RP}
Forward Isolation 1		-32	-27	dBm	Mode=Standby, P_{IN}=Max, V_{RAMP}=Min
Forward Isolation 2		-27	-18	dBm	Mode=TXLB, P_{IN}=Max, V_{RAMP}=Min

Note: V_{RAMP_RP} is defined as the V_{RAMP} voltage required to achieve 32.0dBm at Output load=50Ω, V_{BATT}=3.6V, Temperature=25 °C, P_{IN}=3dBm.

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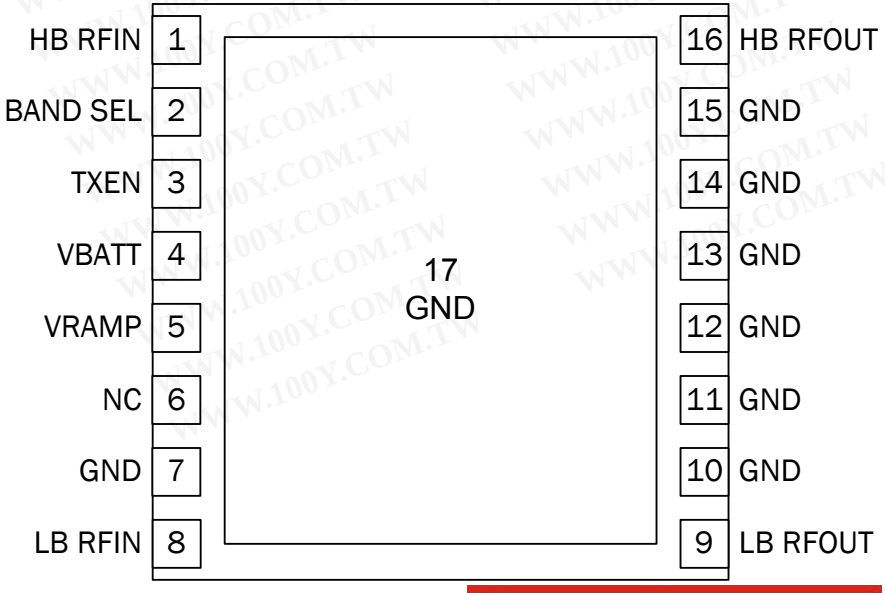
Pin	Function	Description
1	HB_RFIN	RF input to the high band power amplifier. DC blocked inside the module.
2	BS	Digital input enables either the low band or high band amplifier within the module. A logic low selects Low Band (GSM850/EGSM900), a logic high selects High Band (DCS1800/PCS1900). This pin is a high impedance CMOS input with no pull-up or pull-down resistors.
3	TXEN	Digital input enables or disables the internal circuitry. When disabled, the module is in the OFF state, and draws virtually zero current. This pin is a high impedance CMOS input with no pull-up or pull-down resistors.
4	VBATT	Main DC power supply for all circuitry in the module. Traces to this pin will have high current pulses during transmit operation. Proper decoupling and routing to handle this condition should be observed.
5	VRAMP	The voltage on this pin controls the output power by varying the internally regulated collector voltage on the amplifiers. This pin provides an impedance of approximately 60 kΩ.This is a high bandwidth input, so filter considerations for performance must be addressed externally.
6	NC	No connection
7	GND	Ground
8	LB_RFIN	RF input to the low band power amplifier. DC blocked inside the module.
9	LB_RFOUT	RF output from the low band power amplifier. DC blocked inside the module.
10	GND	Ground
11	GND	Ground
12	GND	Ground
13	GND	Ground
14	GND	Ground
15	GND	Ground
16	HB_RFOUT	RF output from the high band power amplifier. DC blocked inside the module.
17	GND	Ground. Main thermal heat sink and electrical ground.

Pin Out

Top Down View



Theory of Operation

Overview

The RF3194 is designed for use as the GSM power amplifier in the transmit section of mobile phones covering the GSM850, EGSM900, DCS1800, and PCS1900MHz frequency bands. The RF3194 is a high power, saturated transmit module containing RFMD's patented PowerStar® Architecture. The module includes a multi function CMOS controller, GaAs HBT power amplifier, and matching circuitry. A single analog voltage controls output power for GSM PCLs and ramping. This analog voltage can be driven from the transceiver DAC to provide very predictable power control, enabling handset manufacturers to achieve simple and efficient phone calibration in production.

Additional Features

Current Limiter

During normal use, a mobile phone antenna will be subjected to a variety of conditions that can affect its designed resonant frequency. This shift in frequency appears as a varying impedance to a power amplifier connected to the antenna. As the impedance presented to the PA varies, so does the output power and current to the power amplifier. If left uncontrolled, power amplifier current can peak at high levels that starve other circuitry, connected to the same supply, of the required voltage to operate. This can result in a reset or shutdown of the mobile phone. The RF3194 contains an active circuit that monitors the current and adjusts the internal power control loop to prevent peak current from going above 2.6A. While this current limiter can limit transmitted power under situations where the antenna is operating at very low efficiency, it is typically more acceptable for users to have a dropped call than a phone reset.

GMSK Operation

GMSK modulation is a constant RF envelope modulation scheme which encodes information in the phase of the signal while amplitude variation is suppressed. Since no information is included in the amplitude of the signal, GMSK transmit is not sensitive to amplitude non-linearity of the power amplifier, allowing it to operate in deep class AB or class C saturation for optimum efficiency. The GMSK power envelope may controlled by any one of a number of power control schemes.

During GMSK transmit RF3194 operates as a traditional PowerStar® module. The basic circuit diagram is shown in Figure 1. The PowerStar® control circuit receives an analog voltage (V_{RAMP}) which sets the amplifier output power. The PowerStar® I architecture is essentially a closed loop method of power control that is invisible to the user. The V_{RAMP} voltage is used as a reference to a high speed linear voltage regulator which supplies the collector voltage to all stages of the amplifier. The base bias is fixed at a point that maintains deep class AB or class C transistor saturation. Because the amplifier remains in saturation at any power level, performance sensitivity to temperature, frequency, voltage and input drive level is essentially eliminated, ensuring robust performance within the ETSI power versus time mask.

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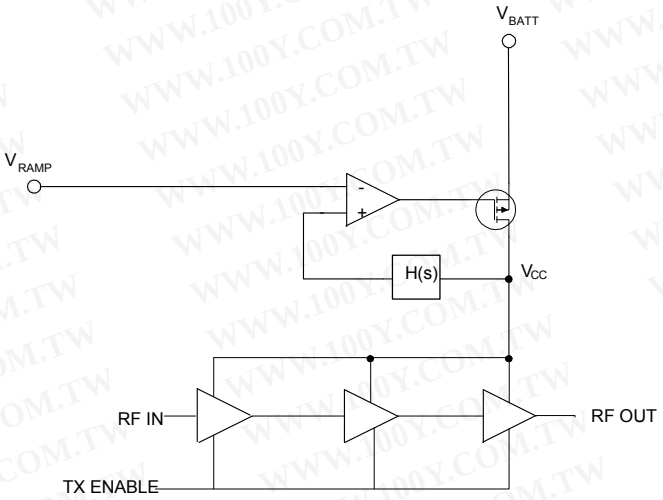


The PowerStar® power control relationship is described in Equation 1 where V_{CC} is the voltage from the linear regulator and the other variables are constants for a given amplifier design and load. The equation shows that load impedance affects output power, but to a lesser degree than V_{CC} supply variations. Since the architecture regulates V_{CC}, the dominant cause of power variation is eliminated. Another important result is that the equation provides a very linear relationship between V_{RAMP} and output power expressed as V_{RMS}.

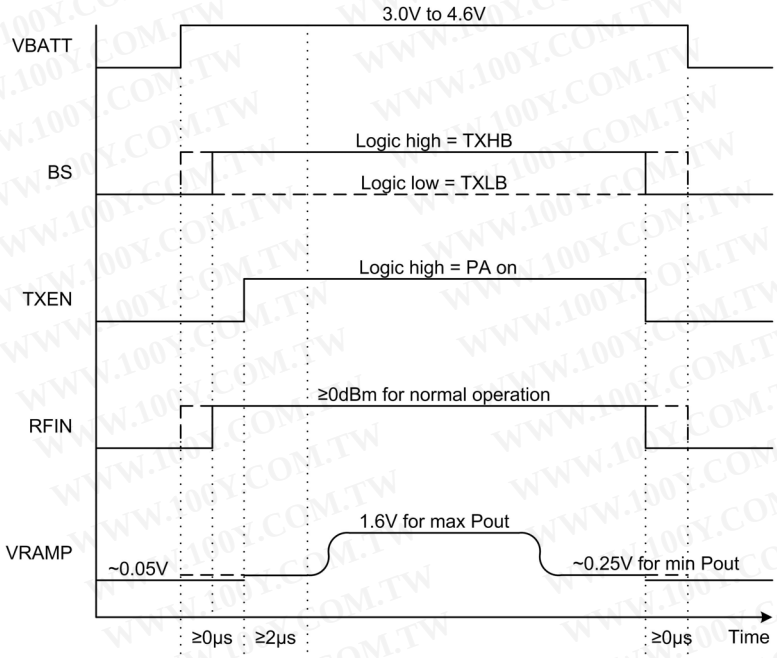
$$P_{OUT}dBm = 10 \cdot \log\left[\frac{(2 \bullet V_{CC} - V_{SAT})^2}{8 \bullet R_{LOAD} \bullet 10^{-3}}\right]$$

Equation 1: Output Power versus Voltage Relationship

The RF signal applied at RFIN of the amplifier must be a constant amplitude signal and should be high enough to saturate the amplifier. The input power range is indicated in the specifications. Power levels below this range will result in reduced maximum output power and the potential for more variation of output power over extreme conditions. Higher input power is unnecessary and will require more current in the circuitry driving the power amplifier. A higher input power may also couple to the output and will increase the minimum output power level.

Power On (Timing) Sequence

In the Power-On Sequence, there are some important set-up times associated with the control signals of the amplifier module. Refer to the logic table for control signal functions. One of the critical relationships is the settling time between TXEN going high and when V_{RAMP} can begin to increase. This time is often referred to as the "pedestal" and is required so that the internal power control loop and bias circuitry can settle after being turned on. The PowerStar® architecture usually requires approximately 1 – 2 µs for proper settling of the power control loop.



Power On Sequence:

1. Apply VBATT
2. Apply BS
3. Apply RFIN
4. Apply VRAMP pedestal value (~0.25V)
5. Apply TXEN
6. Increase VRAMP for desired output power

Steps 2, 3, 4 can occur at the same time.

RFIN can be applied at any time without damage. For good transient response, RFIN must be applied before power ramp begins.

The Power Down Sequence is the reverse order of the Power On Sequence.

Power Ramping

The power ramp waveform must be created such that the output power falls into the ETSI power versus time mask. The ability to ramp the RF output power to meet ETSI switching transient and time mask requirements partially depends upon the predictability of output power versus V_{RAMP} response of the power amplifier. The PowerStar® control loop is very capable of meeting switching transient requirements with the proper raised cosine waveform applied to the V_{RAMP} input. Ramp times between 10 and 14 µs can be optimized to provide excellent switching transients at high power levels. Shorter ramps will have a higher rate of change which will produce higher transients. Longer ramps may have difficulty meeting the time mask. Optimization needs to include all power levels as the time mask requirements change with P_{OUT} levels.

The RF3194 does not include a power control loop saturation detection/correction circuit such as the V_{BATT} tracking circuit found in some PowerStar® modules. If V_{RAMP} is set to a voltage where the FET pass-device in the linear regulator saturates, the response time of the regulated voltage (V_{CC}) slows significantly. Upon ramp-down, the saturated linear regulator does not react immediately, and the output power does not follow the desired ramp-down curve. The result is a discontinuity in the output power ramp and degraded switching transients. To prevent this from happening, V_{RAMP} must be limited as the supply voltage is reduced. By maintaining $V_{RAMP} \leq 0.345 * V_{BATT} + 0.26$, the linear regulator will avoid deep saturation and serious switching transient degradation will be avoided.

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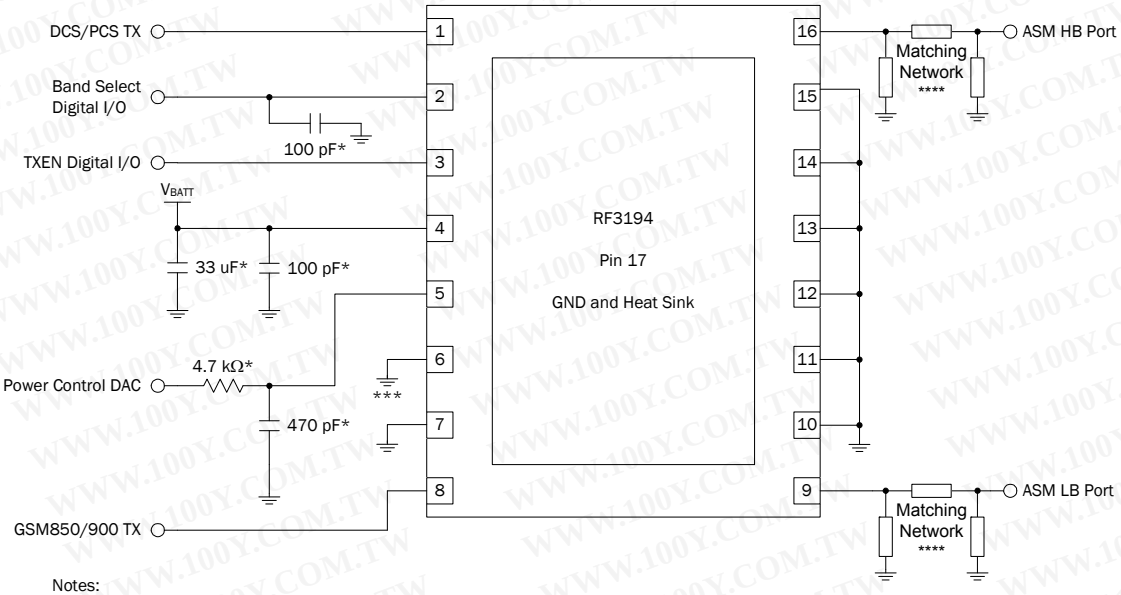
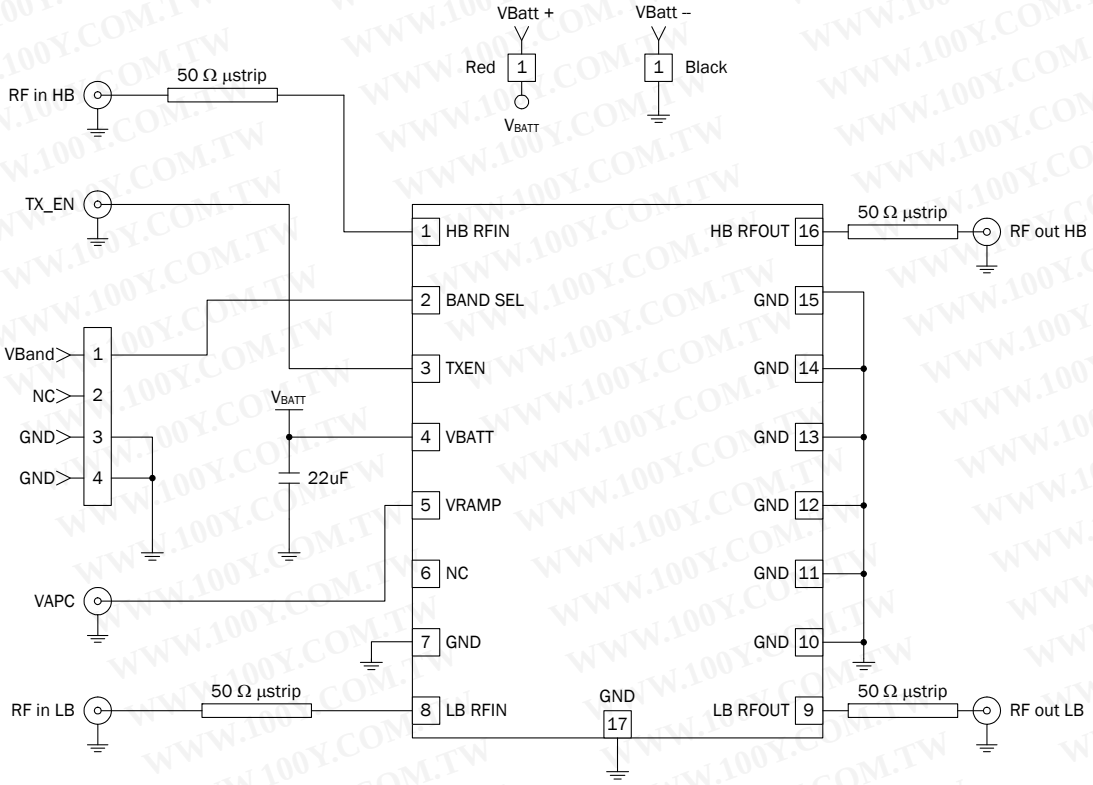
Application Schematic



Notes:
* Suggested values only. Actual requirements will vary with application.
**All RF paths should be designed as 50Ω microstrip or stripline.
***NC pins on this module can be connected to ground.
****π matching network is suggested because it is flexible enough for the tuning needs of most applications. Component values are not given as they are application specific.

Evaluation Board Schematic



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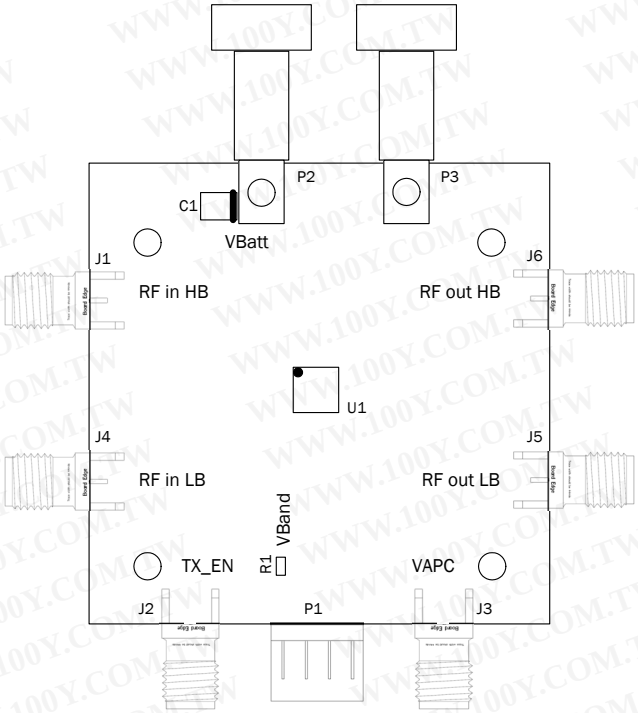
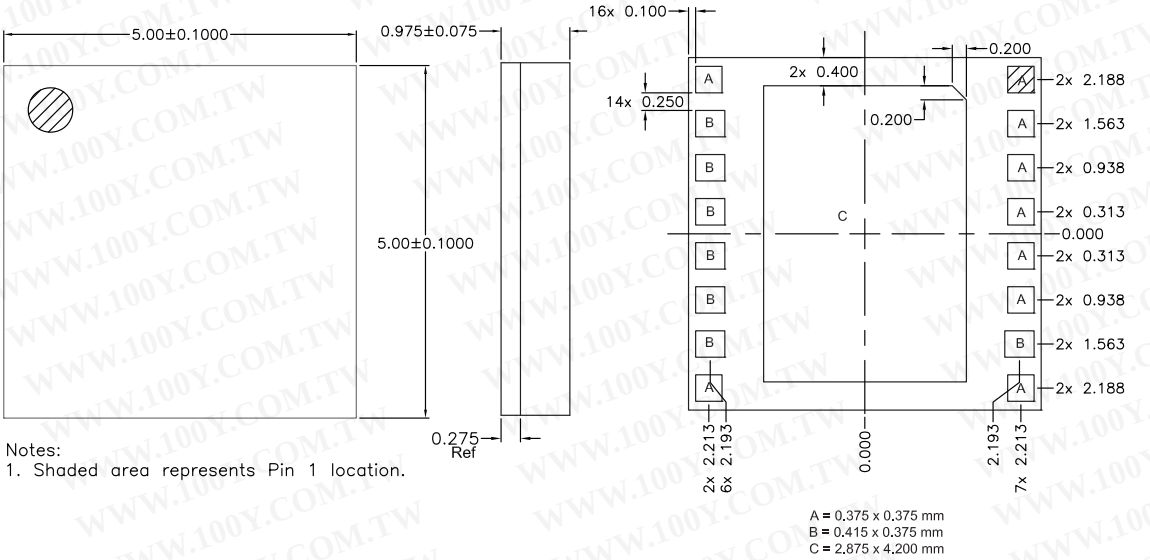
Evaluation Board Layout
Board Size 2.0" x 2.0"

Board Thickness 0.042", Board Material RO4003 Top Layer, FR-4 Core and Bottom Layer

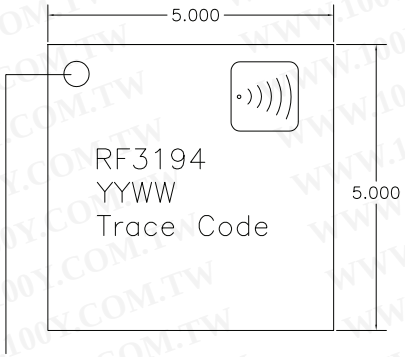


Package Drawing



Notes:
1. Shaded area represents Pin 1 location.

Branding Diagram



Pin 1 Indicator

Date Code
YY = Year
WW = Week

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PCB Design Requirements

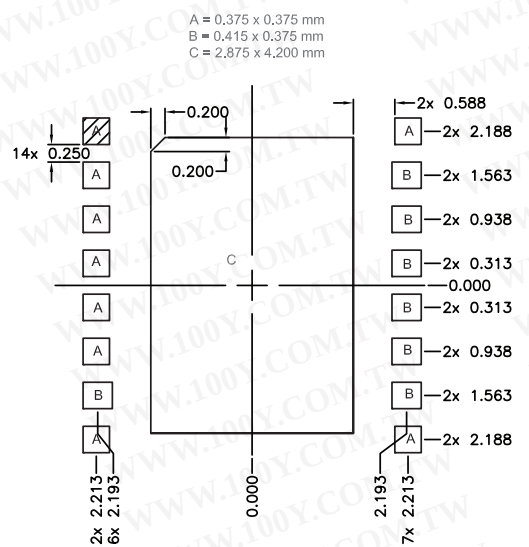
PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 2 to 5 µinch inch gold over 180 µinch nickel.

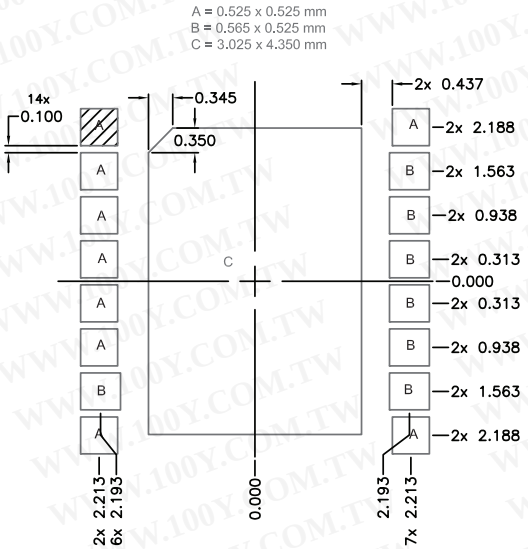
PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land and Solder Mask Pattern



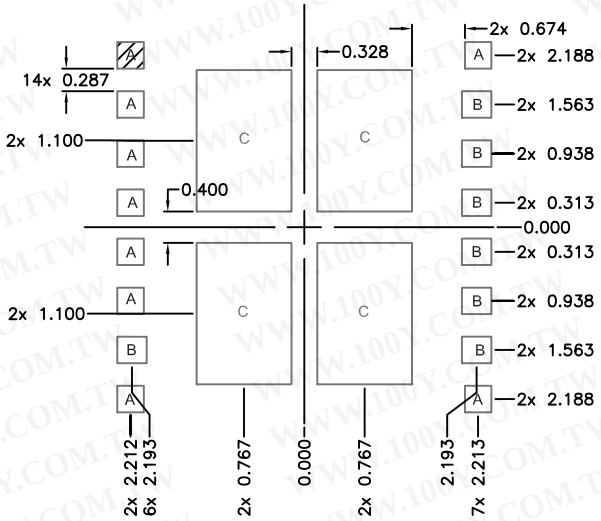
PCB Metal Land Pattern



PCB Solder Mask Pattern

PCB Stencil Pattern

A = 0.338 x 0.338 mm
B = 0.376 x 0.338 mm
C = 1.206 x 1.800 mm



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Tape and Reel

Carrier tape basic dimensions are based on EIA 481. The pocket is designed to hold the part for shipping and loading onto SMT manufacturing equipment, while protecting the body and the solder terminals from damaging stresses. The individual pocket design can vary from vendor to vendor, but width and pitch will be consistent.

Carrier tape is wound or placed onto a shipping reel either 330mm (13 inches) in diameter or 178mm (7 inches) in diameter. The center hub design is large enough to ensure the radius formed by the carrier tape around it does not put unnecessary stress on the parts.

Prior to shipping, moisture sensitive parts (MSL level 2a-5a) are baked and placed into the pockets of the carrier tape. A cover tape is sealed over the top of the entire length of the carrier tape. The reel is sealed in a moisture barrier ESD bag with the appropriate units of desiccant and a humidity indicator card, which is placed in a cardboard shipping box. It is important to note that unused moisture sensitive parts need to be resealed in the moisture barrier bag. If the reels exceed the exposure limit and need to be rebaked, most carrier tape and shipping reels are not rated as bakeable at 125°C. If baking is required, devices may be baked according to section 4, table 4-1, of Joint Industry Standard IPC/JEDEC J-STD-033.

The table below provides information for carrier tape and reels used for shipping the devices described in this document.

Tape and Reel

RFMD Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units per Reel
RF3194TR13	13 (330)	4 (102)	12.9	8	Single	2500
RF3194TR7	7 (178)	2.4 (61)	12.9	8	Single	750