

1.5W MONO FILTER-FREE CLASS-D AUDIO POWER AMPLIFIER DATASHEET

勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-34970699
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

FEATURES

- 1.5 W Into 8 Ω From a 3.7V at THD = 10% (Typ)
- Maximum Battery Life and Minimum Heat
 - 90% at 400 mW
 - 83% at 100 mW
 - 2.4-mA Quiescent Current (Typ)
 - 0.5-uA Shutdown Current
- Only Three External Components
 - Optimized PWM Output Stage Eliminates LC Output Filter
 - Internally Generated 250-KHz Switching Frequency
- Improved PSRR (-70dB at 217-Hz) and wide supply Voltage (3.0 V to 4.2 V)
- Fully Differential Design Reduces RF Rectification
- Improved CMRR Eliminates Two Input

Coupling Capacitors

- Space Saving Package
 - MSOP-8

APPLICATIONS

- Ideal for Wireless or Cellular Handsets and PDAs
- Personal Navigation Devices
- General Portable Audio Devices
- Liner Vibrator Drivers

DESCRIPTION

The SCA2005 is a 1.5-W high efficiency filter-free class-D audio power amplifier in a MSOP-8 package that requires only three external components. A fast start-up time of 4ms with minimal pop makes the SCA2005 ideal for PDA applications.

TYPICAL APPLICATION CIRCUIT

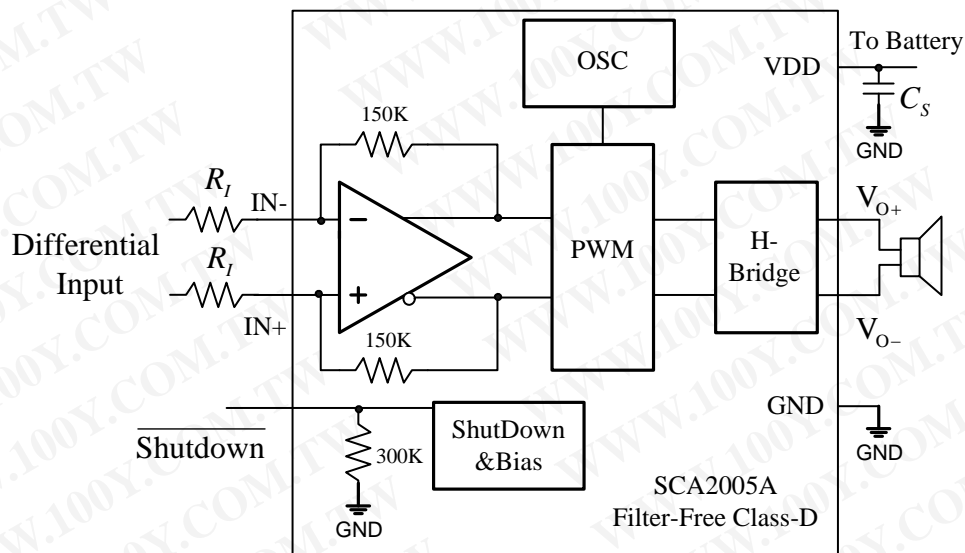


Figure 1. Typical Application Circuit

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PIN CONFIGURATIONS

Part Number	Pin Configurations
SCA2005 MSOP-8	<p style="text-align: center;">TOP VIEW</p>

PIN DESCRIPTION

PIN NAME	MSOP-8	I/O	DESCRIPTION
<u>SHUTDOWN</u>	1	I	Shutdown terminal (active low logic)
NC	2	--	NC
IN+	3	I	Positive differential input
IN-	4	I	Negative differential input
VO+	5	O	Positive BTL output
VDD	6	I	Power supply
GND	7	I	Ground
VO-	8	O	Negative BTL output

FUNCTIONAL BLOCK DIAGRAM

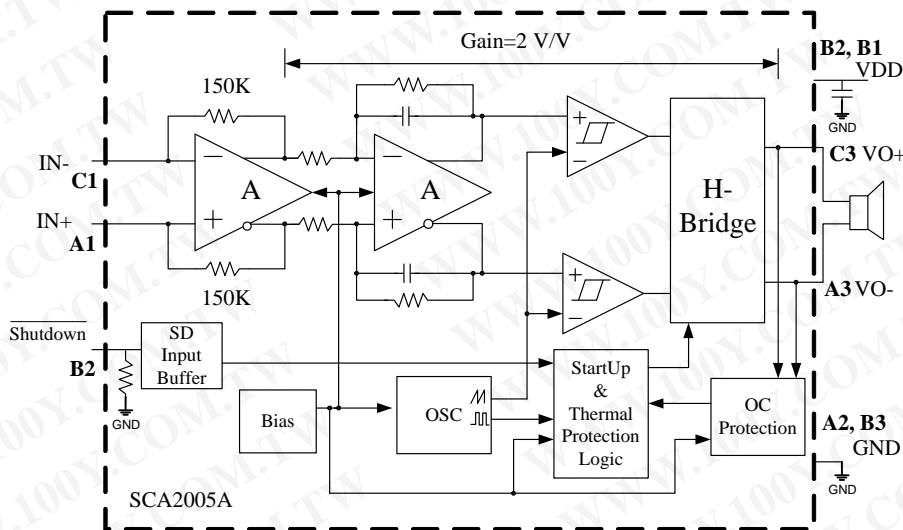


Figure 2. Functional Block Diagram

* Note :

$$\text{Total Gain} = 2 \times \frac{150K\Omega}{R_I}$$

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RECOMMENDED OPERATION CONDITIONS

		MIN	TYP	MAX	UNIT
VDD	Supply Voltage	3.0		4.2	V
VIH	High-level input voltage	Shutdown terminal	1.3	VDD	V
VIL	Low-level input voltage	Shutdown terminal	0	0.35	V
R _i	Input Resistor	2 V/V<Gain< 20 V/V	15	150	KΩ
V _{IC}	Common mode input voltage	VDD=3.0V~4.2V, CMRR<-65dB	0.7	VDD-0.7	V
T _A	Operating free-air temperature	-40		85	°C

ABSOLUTE MAXIMUM RATINGS

	SCA2005
Supply Voltage	4.5 V
Storage Temperature	-65°C to 150°C
ESD Susceptibility (for Human Body Model)	2000V
ESD Susceptibility (for Machine Model)	200V
Junction Temperature	150°C

ELECTRICAL CHARACTERISTICS

T_A=25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OS}		V _I =0V, A _V =2 V/V, VDD=3.0V~4.2V		10		mV
PSRR	Power supply rejection ratio	VDD=3.0V~4.2V		-70		dB
CMRR	Common mode rejection ratio	VDD=3.0V~4.2V, V _{IC} =0.7V to VDD-0.7V		-65		dB
I _{IH}	High-level input current	VDD=4.2 V, V _I =4.5 V			100	uA
I _{IL}	Low-level input current	VDD=4.2V, V _I = - 0.3V			5	uA
I _Q	Quiescent current	VDD=4.2V, no load		3.6		mA
		VDD=3.7V, no load		2.5		
		VDD=3.0 V, no load		2.0		

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I _{SD}	Shut Current	$V_{\text{Shutdown}} = 0.35\text{V}$, VDD = 3.0V to 4.2V	0.2	0.5	uA
r _{DS(on)}	Static drain-source on-state resistor	VDD=4.2 V	350		mΩ
		VDD=3.7 V	450		
		VDD=3.0 V	650		
f _(sw)	Switching frequency	VDD=3.0 V to 4.2 V	250		KHz
Gain			$2 \times \frac{150\text{K}\Omega}{R_i}$		V/V

OPERATING CHARACTERISTICS

T_A=25°C, Gain=2 V/V, R_L=8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P _O	Output Power	THD+N=1%, f=1KHz, R _L =8Ω,	VDD=4.2V	1.24			W
			VDD=3.7 V	0.62			
			VDD=3.0V	0.33			
THD+N	Total harmonic distortion plus noise	VDD=4.2V, Po=1.5W, R _L =8Ω, f=1KHz		0.5%			
			VDD=3.7V, Po=0.5W, R _L =8Ω, f=1KHz	0.2%			
			VDD=3.0V, Po=0.2W, R _L =8Ω, f=1KHz	0.3%			
k _{SVR}	Supply ripple rejection ratio	VDD=3.7 V, Inputs ac-grounded with C _I =2uF	f=217Hz, V _(RIPPLE) =200mV _{pp}	-65			dB
SNR	Signal-to-noise ratio	VDD=3.7V, P _O =1W, R _L =8Ω		86			dB
CMRR	Common mode rejection ratio	VDD=3.7V, V _{IC} =1V _{pp}	f=217Hz	-65			dB
V _n	Output voltage noise	VDD=3.7V, f=20Hz to 20KHz, Inputs ac-grounded with C _I =2uF	No weighting	85			uV _{RMS}
			A weighting	70			
Z _i	Input impedance			150			kΩ
T _{Start}	Startup time from shutdown	VDD=3.7 V		4			ms

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TYPICAL OPERATION CHARACTERISTICS

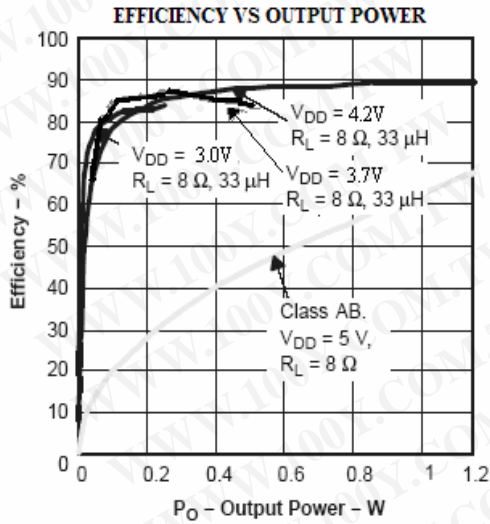


Figure 3

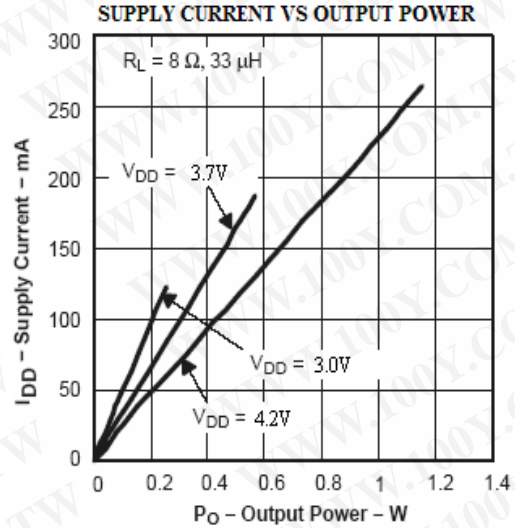


Figure 4

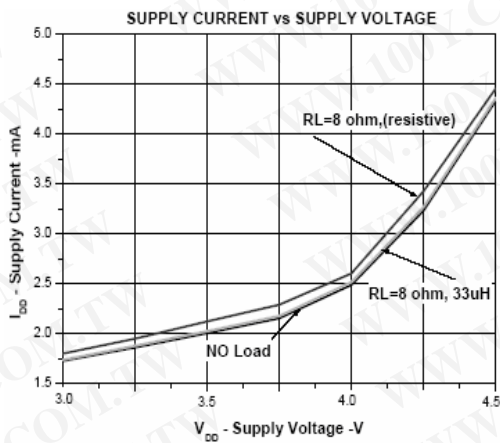


Figure 5

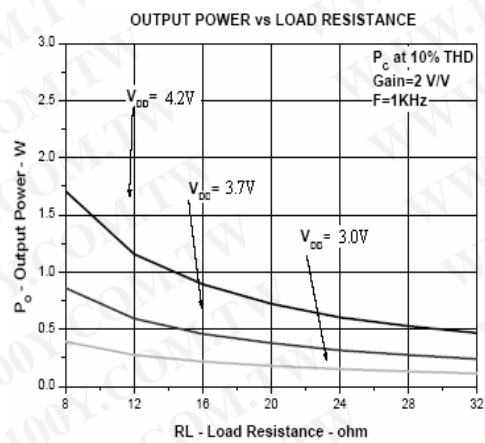


Figure 6

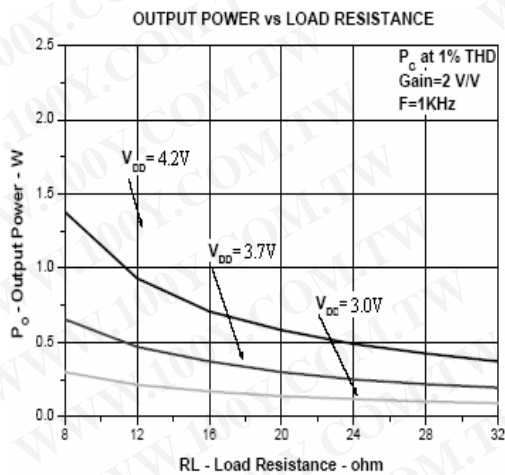


Figure 7

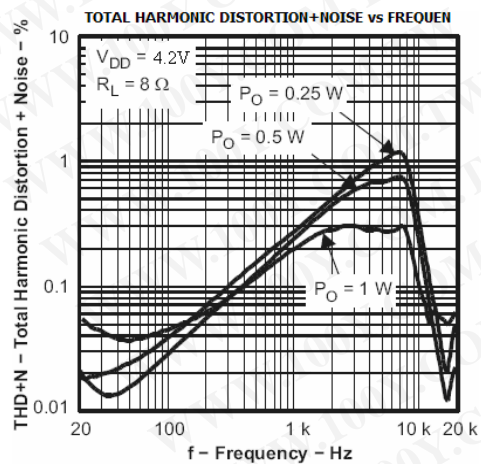


Figure 8

1.5W MONO FILTER-FREE CLASS-D AUDIO POWER AMPLIFIER DATASHEET

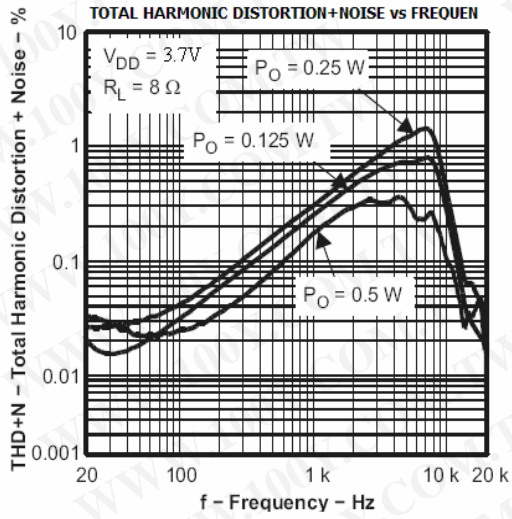


Figure 9

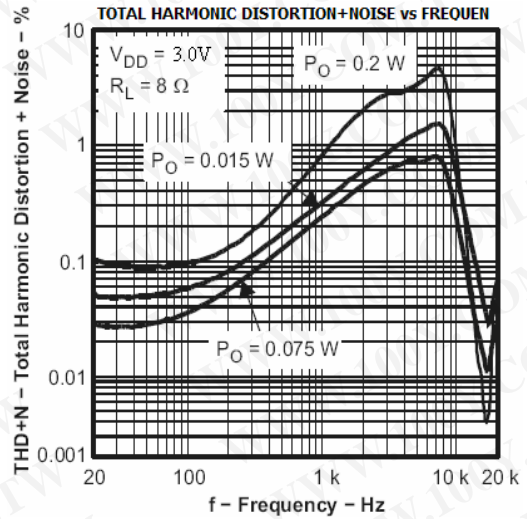


Figure 10

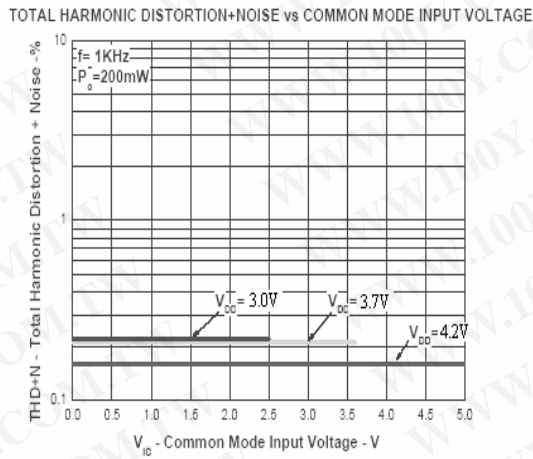


Figure 11

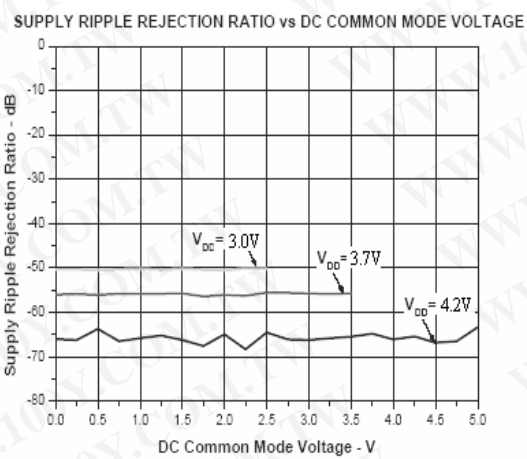


Figure 12

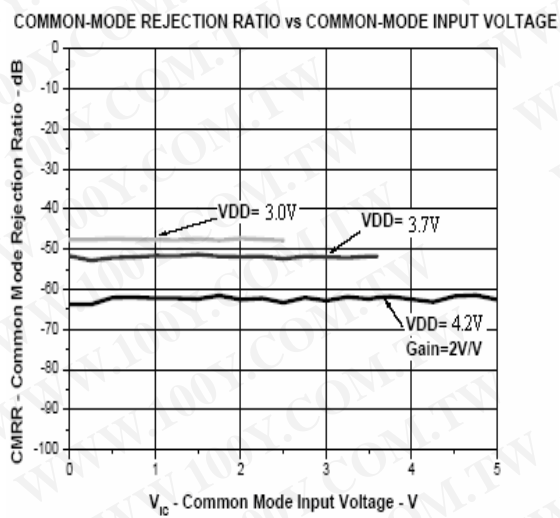


Figure 13

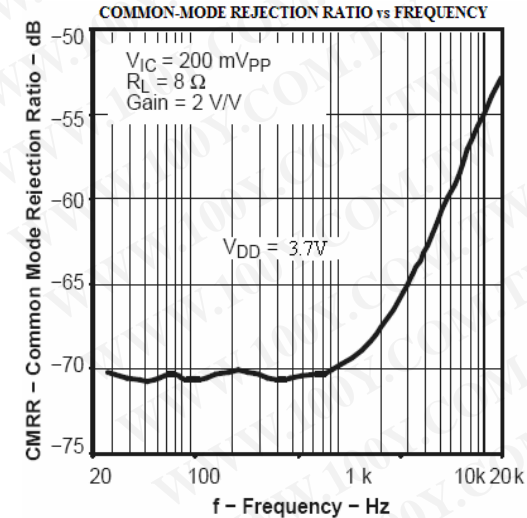


Figure 14

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APPLICATION INFORMATION

全差分放大器

SCA2005 为全差分输入输出放大器，该差分放大器由差模信号放大器及共模信号放大器共同构成，差模信号放大器确保输出差分信号等于差分输入信号与增益的乘积。共模负反馈则确保了输出信号的共模电平与输入信号的共模电平无关，而始终保持在 VDD/2 附近。SCA2005 差分输入典型应用电路参见图 15 与 图 16 所示，另外 SCA2005 允许单端输入应用方式，如图 17 为典型单端应用电路。为获得更好的噪声抑制性能，本产品推荐使用双端差分输入电路方式。

全差分放大器优点

- 无需输入耦合电容
- 更好的射频抑制能力

元器件选择

- 输入电阻 R_I

输入电阻由公式 (1) 用于设置放大器的增益，

$$\text{Gain} = \frac{2 \times 150 \text{K}\Omega}{R_I} (\text{V/V}) \quad (1)$$

该电阻的匹配非常重要，如果失配，CMRR, PSRR 以及谐波抑制能力均会下降。因此建议使用精度好于 1% 的电阻。

- 去耦电容 C_S

为获得高输出效率与低谐波失真，建议选择等效串联电阻(ESR)小的 1uF 电容，并尽可能地贴近芯片 VDD 端放置。

为获得更好的低频噪声滤除效果，可以同时 VDD 端并联 10uF 或更大的电容。

- 输入电容 C_I

如果 SCA2005 为差分输入方式，并且输入信号共模范围在 0.7V 至 VDD-0.7V 之间，则无需输入电容 C_I。反之，需要在输入端串接一个高通滤波电路，该高通滤波电路的下

限截止频率取决于不同的应用领域，并且设计时需要留有一定的裕量。

输入耦合电容的计算公式如式 (2) 所示：

$$C_I = \frac{1}{(2\pi R_I f_c)} \quad (2)$$

其中 f_c 为 RC 串联高通滤波器下限截止频率。一般场合下，C_I 取 1uF 电容即可。

实现输入信号相加

SCA2005 可以较为容易地实现信号相加，并且可以独立设置不同的增益。

- 两路差分信号相加

当需要实现两路差分信号输入时，典型应用电路如图 18 所示，两路增益可以独立设置，其增益分别由式 (3) 与式 (4) 确定，

$$\text{Gain1} = \frac{V_o}{V_{i1}} = \frac{2 \times 150 \text{K}\Omega}{R_{i1}} (\text{V/V}) \quad (3)$$

$$\text{Gain2} = \frac{V_o}{V_{i2}} = \frac{2 \times 150 \text{K}\Omega}{R_{i2}} (\text{V/V}) \quad (4)$$

例如，要求 输入上下两路信号的增益均为 1V/V，则电阻 R_{i1} = R_{i2} = 300KΩ。

- 一路差分与一路单端信号相加

请另行参阅相关文献。

- 一路差分与一路单端信号相加

请另行参阅相关文献。

元器件放置位置

建议所有的片外器件尽可能的靠近 SCA2005。输入电阻在匹配的同时尽可能的靠近 SCA2005 的输入端，以便输入高阻节点受噪声的耦合干扰。为减少电源走线寄生电阻与电感对 D 类功放效率的影响，去耦电容请尽可能靠近芯片 VDD 端放置。

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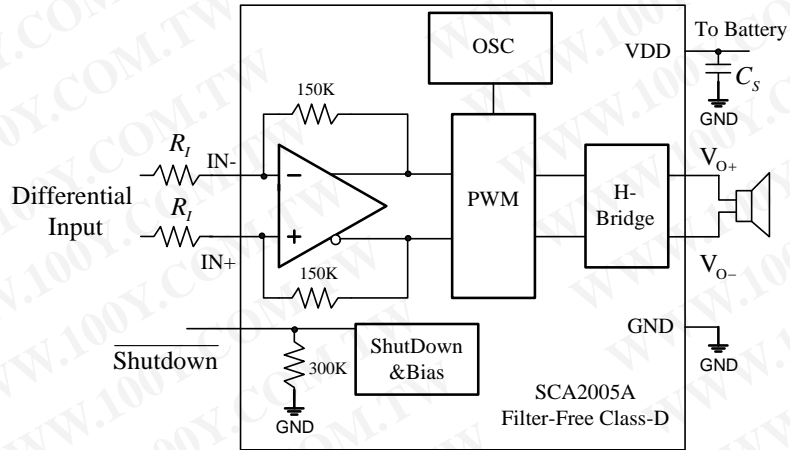


Figure 15. 典型 SCA2005 差分输入应用电路

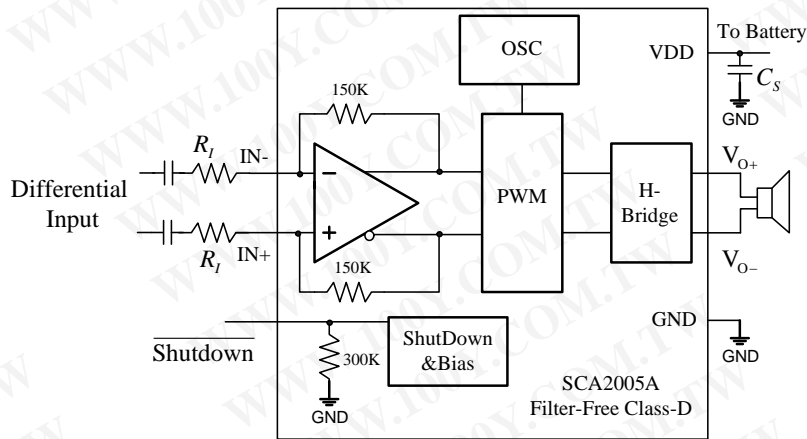


Figure16. 典型 SCA2005 有差分输入电阻电容应用电路

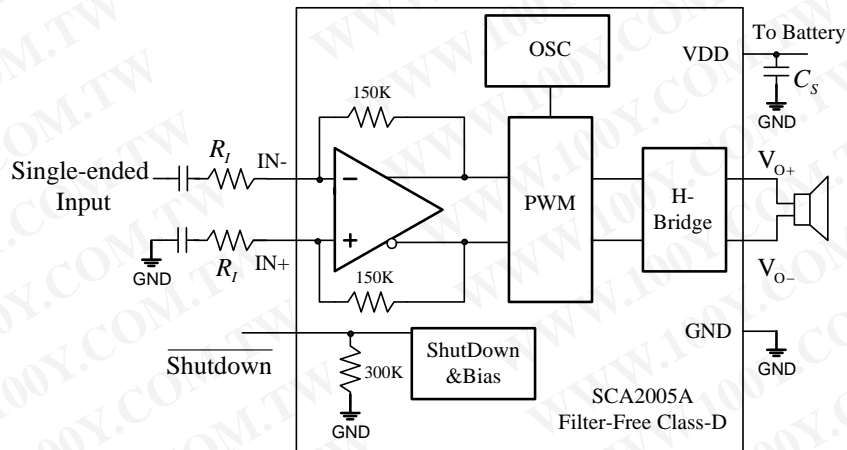


Figure17. SCA2005 单端输入应用电路

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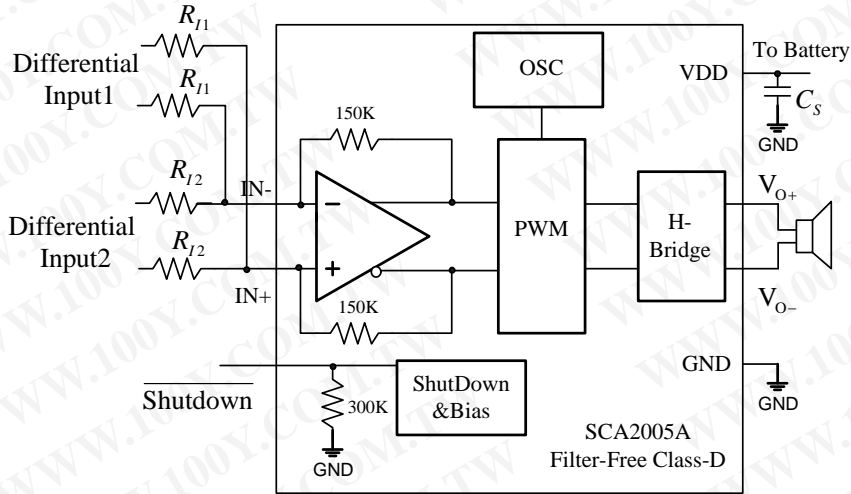


Figure18. SCA2005 典型两路差分信号相加应用电路

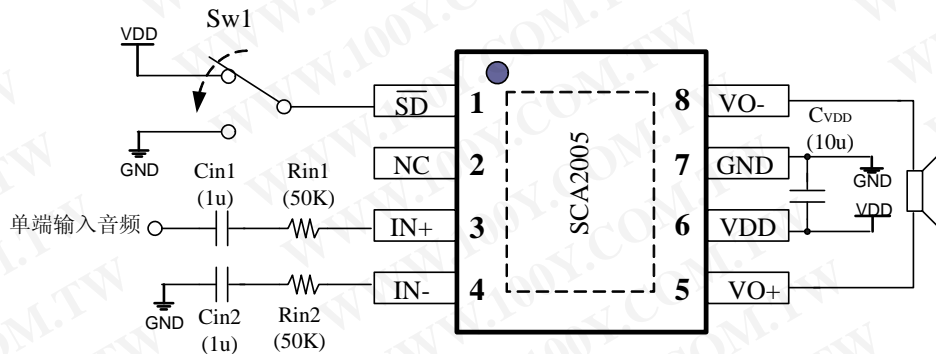
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D 类功放原理图与 PCB 快速设计注意事项

Cin1、Cin2	Rin1、Rin2	电压放大倍数	参考计算公式
1 uF	150K	2 V/V	$A_v \approx 2 \times \frac{150K}{R_{in}}$
	75K	4 V/V	
	50K	6 V/V	
	30K	10 V/V	

一、原理图设计选择

- 1、输入耦合电容 Cin1、Cin2，选择 1uF 即可；
- 2、输入电阻 Rin1、Rin2，根据电压倍数需求参照上表选择；
- 3、去耦电容 1uF，条件允许换用 10uF，效果更佳；
- 4、参考原理图如下图所示。



增益为 6 倍的 SCA2005 应用原理图

二、PCB 设计注意事项与参考

- 1、芯片就近接入电源入口，为避免走线寄生参数影响，电源与地线走线尽可能放宽；
- 2、电源的去耦电容 1uF 越靠近芯片 VDD 端，去除电源噪声效果越好；若条件允许，该电容可增加到 10uF，或者 1~10uF 多个电容并联效果更佳。
- 3、如果音频信号源为差分输入，要求输入电阻电容尽量靠近芯片并注意匹配。
- 4、不用的部分建议铺地线。
- 6、下图为参考设计 PCB 版图，客户应用时输出端短线直接接音箱。
- 7、客户可以根据实际应用需求灵活修改 PCB 版图设计，注意参照以上几点基本设计原则。

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