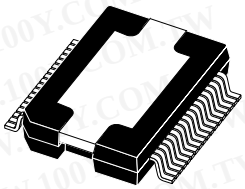
STA510F

44-V, 5.5-A, quad power half bridge

Features

- Minimum input output pulse width distortion
- 150 mW Rdson complementary DMOS output stage
- CMOS compatible logic inputs
- Thermal protection
- thermal warning output
- Under-voltage protection
- No power-on, power- off sequence required



PowerSO36 with exposed pad (or slug) up

Description

STA510F is a monolithic, quad, half-bridge stage in Multipower BCD technology. The device can be used as dual bridge or reconfigured, by connecting CONFIG pin to Vdd pin, as single bridge with double current capability, and as half bridge (binary mode) with half current capability.

The device is particularly designed to make the output stage of a stereo all-digital high efficiency (FFX) amplifier capable of delivering 100 W + 100 W output power into 8-Ω loads with THD = 10% and V_{cc} = 39 V. In single BTL configuration the device can deliver 200 W into a 4-Ω load with THD = 10% and V_{cc} = 39 V.

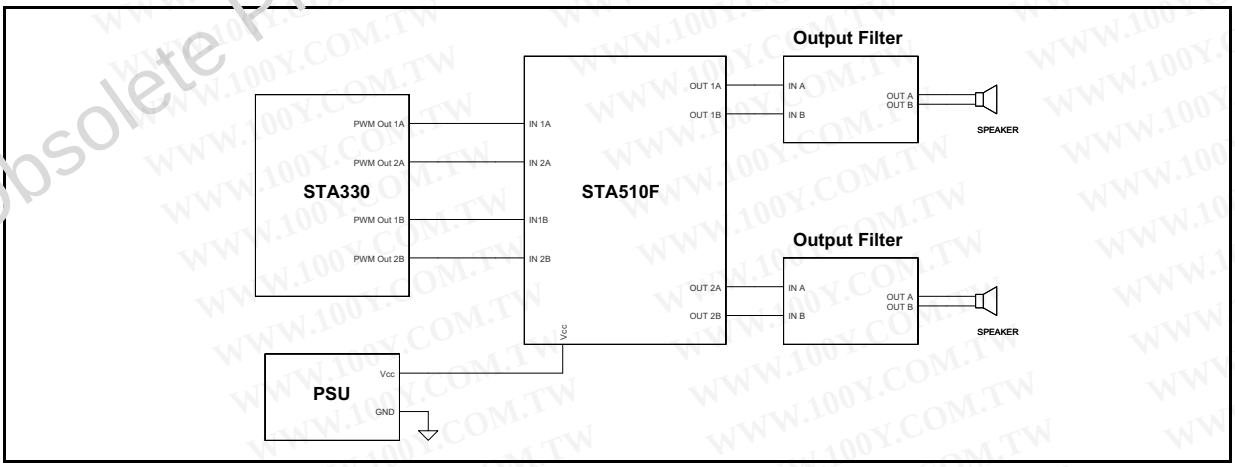
The device is fully compatible with the DDX® driver device.

The input pins have a threshold proportional to V_L pin voltage.

Table 1. Device summary

Order code	Operating Temp. range	Package	Packing
STA510F	0° to 70° C	PowerSO36 (slug up)	Tube

Figure 1. Typical application



1 Pin description

Figure 2. Pin connection (top view)

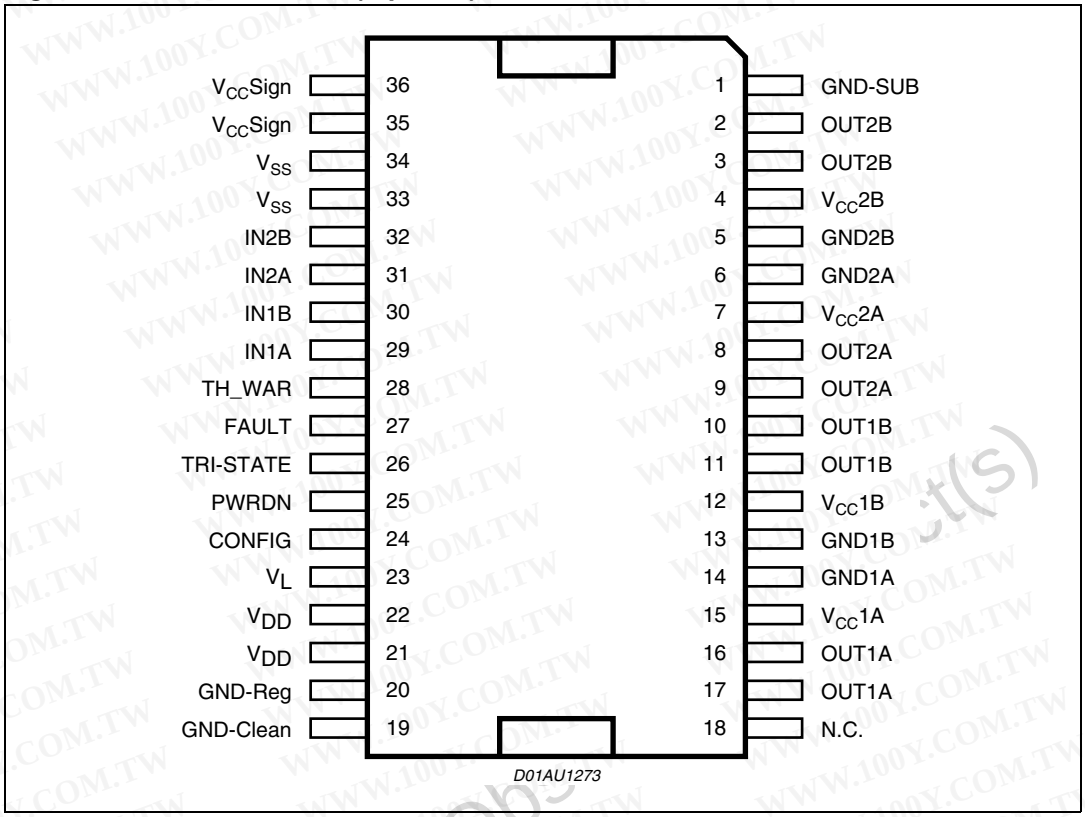


Table 2. Pin list

Pin	Name	Description
1	GND-SUB	Substrate ground
2, 3	OUT2B	Output half bridge 2B
4	Vcc2B	Positive Supply
5	GND2B	Negative Supply
6	GND2A	Negative Supply
7	Vcc2A	Positive Supply
8, 9	OUT2A	Output half bridge 2A
10, 11	OUT1B	Output half bridge 1B
12	Vcc1B	Positive Supply
13	GND1B	Negative Supply
14	GND1A	Negative Supply
15	Vcc1A	Positive Supply
16, 17	OUT1A	Output half bridge 1A

Table 2. Pin list (continued)

Pin	Name	Description
18	NC	Not connected
19	GND-clean	Logical ground
20	GND-Reg	Ground for regulator Vdd
21, 22	Vdd	5V Regulator referred to ground
23	V_L	High logical state setting voltage
24	CONFIG	Configuration
25	PWRDN	Stand-by
26	TRI-STATE	Hi-Z
27	FAULT	Fault pin advisor
28	TH-WAR	Thermal warning advisor
29	IN1A	Input of half bridge 1A
30	IN1B	Input of half bridge 1B
31	IN2A	Input of half bridge 2A
32	IN2B	Input of half bridge 2B
33, 34	Vss	5-V regulator referred to +Vcc
35, 36	VCCSIGN	Signal positive supply

Table 3.

Pin	Logical value	Device status
FAULT (1)	0	Fault detected (short circuit, or thermal)
	1	Normal operation
TRI-STATE	0	All power stages in Hi-Z state
	1	Normal operation
PWRDN	0	Low-power mode
	1	Normal operation
THWAR (1)	0	Temperature of the IC =130° C
	1	Normal operation
CONFIG (2)	0	Normal Operation
	1	OUT1A = OUT1B, OUT2A = OUT2B (IF IN1A = IN1B and IN2A = IN2B)

1. The pin is open collector. To have the high logic value, it needs a pull-up resistor.
2. CONFIG = 1 means connect Pin 24 (CONFIG) to Pins 21, 22 (Vdd).

2 Electrical specifications

2.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage (Pin 4, 7, 12, 15)	44	V
V_{max}	Maximum voltage on pins 23 to 32	5.5	V
ESD	Max ESD on pins (HBM)	±1000	V
T_{op}	Operating temperature range	0 to 70	° C
T_{stg}, T_j	Storage and junction temperature	-40 to 150	° C

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$T_{j\text{-}case}$	Thermal resistance junction to case (thermal pad)		1	2.5	°C/W
T_{jSD}	Thermal shut-down junction temperature		150		° C
T_{warn}	Thermal warning temperature		130		° C
t_{hSD}	Thermal shut-down hysteresis		25		° C

2.3 Electrical specifications

Unless otherwise stated, the results in *Table 6* below are given for the conditions: V_L = 3.3 V, Vcc = 37 V and T = 25° C unless otherwise specified.

Table 6. Electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{dsON}	Power Pchannel/Nchannel MOSFET RdsON	Id = 1 A		150	200	mΩ
I_{dss}	Power Pchannel/Nchannel leakage current				100	µA
g_N	Power Pchannel RdsON matching	Id = 1 A	95			%
g_P	Power Nchannel RdsON matching	Id = 1 A	95			%
Dt_s	Low current dead time (static)	see test circuit *Figure 3*		10	20	ns
Dt_d	High current dead time (dynamic)	L=22µH, C = 470nF, R_L = 8 Ω, Id = 4.5 A, see test circuit *Figure 4*			50	ns

Table 6. Electrical specifications (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{d\ ON}$	Turn-on delay time	Resistive load			100	ns
$t_{d\ OFF}$	Turn-off delay time	Resistive load			100	ns
t_r	Rise time	Resistive load, as *Figure 4*			25	ns
t_f	Fall time	Resistive load, as *Figure 4*			25	ns
V_{CC}	Supply voltage operating voltage		10		40	V
$V_{IN\text{-}High}$	High level input voltage		$V_L/2$ +300 mV			V
$V_{IN\text{-}Low}$	Low level input voltage				$V_L/2$ - 300m V	V
$I_{IN\text{-}H}$	High level input current	Pin voltage = V_L		1		µA
$I_{IN\text{-}L}$	Low level input current	Pin voltage = 0.3V		1		µA
$I_{PWRDN\text{-}H}$	High level PWRDN pin input current	V_L= 3.3V		35		µA
V_{Low}	Low logical state voltage (pins PWRDN, TRISTATE) (see *Table 7*)	V_L = 3.3V			0.8	V
V_{High}	High logical state voltage (pins PWRDN, TRISTATE) (see *Table 7*)	V_L = 3.3V	1.7			V
$I_{VCC\text{-}PWRDN}$	Supply current from Vcc in power down	PWRDN = 0			3	mA
I_{FAULT}	Output current pins FAULT -TH-WARN when FAULT CONDITIONS	Vpin = 3.3V		1		mA
$I_{VCC\text{-}hiz}$	Supply current from Vcc in tri-state	Pin TRI-STATE = 0		22		mA
I_{VCC}	Supply current from Vcc in operation both channel switching)	Input pulse width duty cycle = 50%, switching frequency = 384 kHz, no LC filters;		70		mA
$I_{OUT\text{-}SH}$	Overcurrent protection threshold Isc (short circuit current limit) (note 2)		5.5	7	9	A
V_{UV}	Undervoltage protection threshold			7		V
t_{pw_min}	Output minimum pulse width	No Load	25		40	ns

Table 7. V_{low}, V_{high} threshold variation with V_L

V_L	V_{Low} max	V_{High} min	Unit
2.7	0.7	1.5	V
3.3	0.8	1.7	V
5	0.85	1.85	V

Table 8. Logic truth table

TRI-STATE	INxA	INxB	Q1	Q2	Q3	Q4	Output mode
0	x	x	OFF	OFF	OFF	OFF	Hi-Z
1	0	0	OFF	OFF	ON	ON	DUMP
1	0	1	OFF	ON	ON	OFF	NEGATIVE
1	1	0	ON	OFF	OFF	ON	POSITIVE
1	1	1	ON	ON	OFF	OFF	Not used

Figure 3. Test circuit for low current dead time

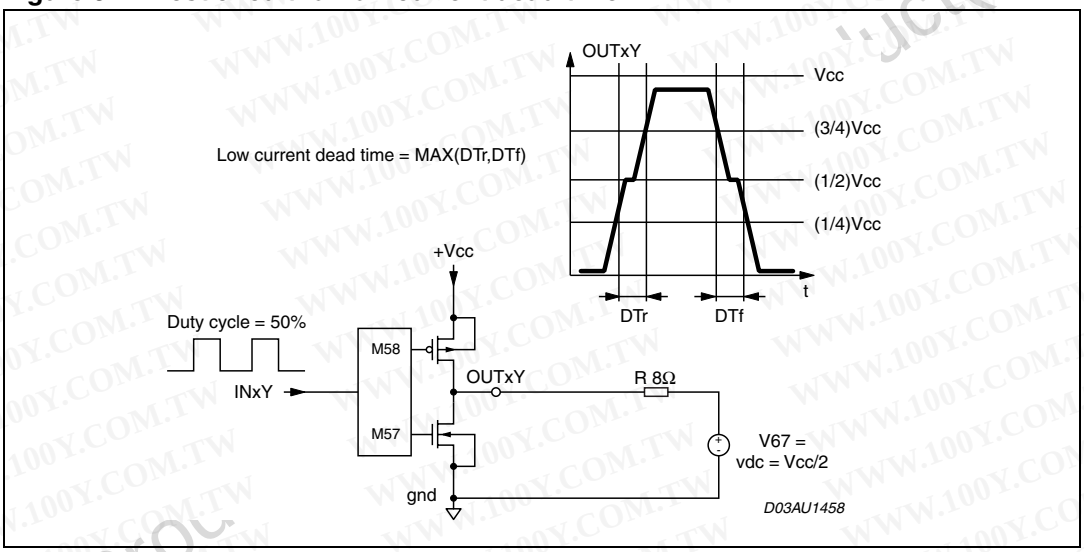


Figure 4. Test circuit for high current dead time

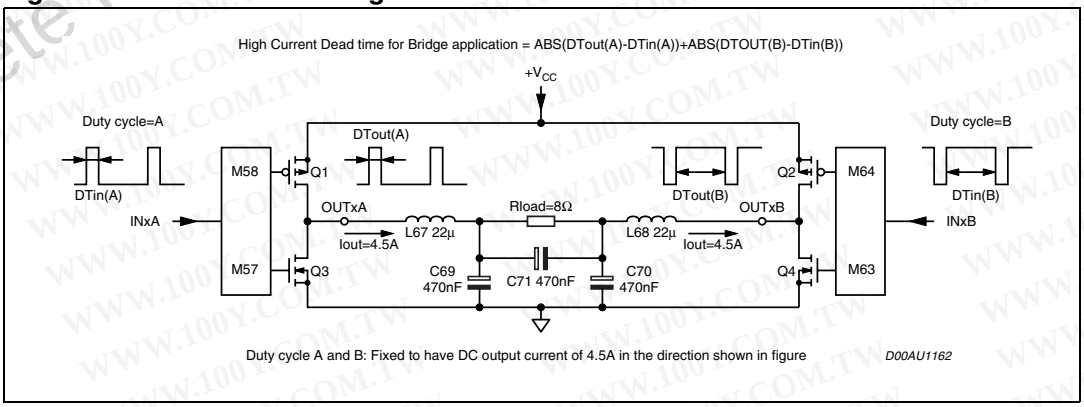


Figure 5. Typical quad half-bridge configuration giving 200 W per channel into 4 Ω speakers, 10% THD, V_{CC} = 39 V

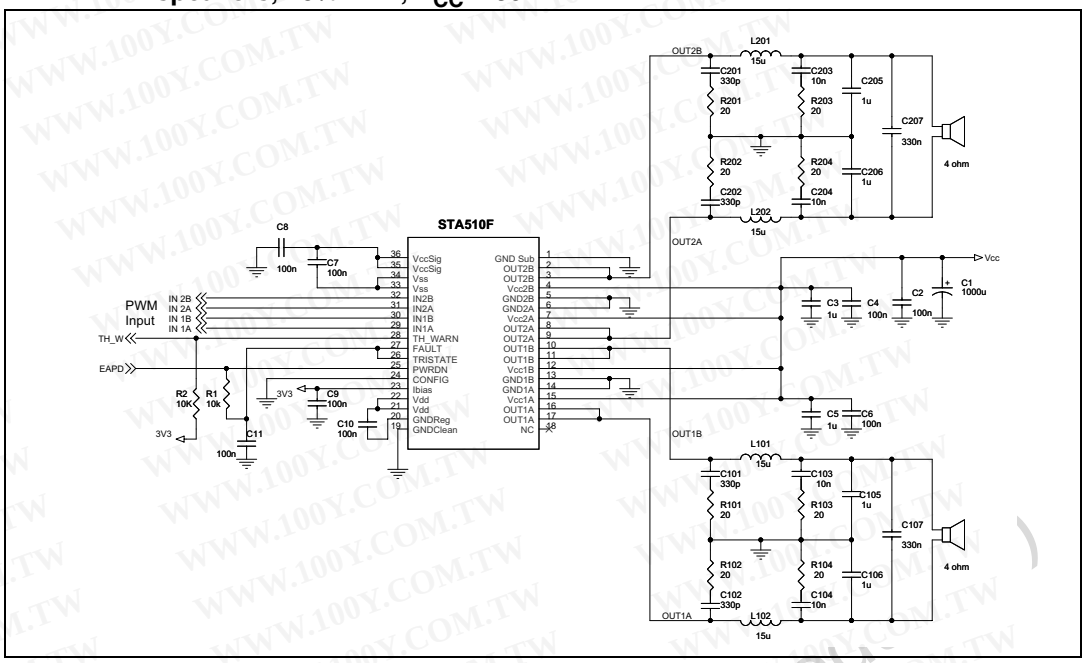
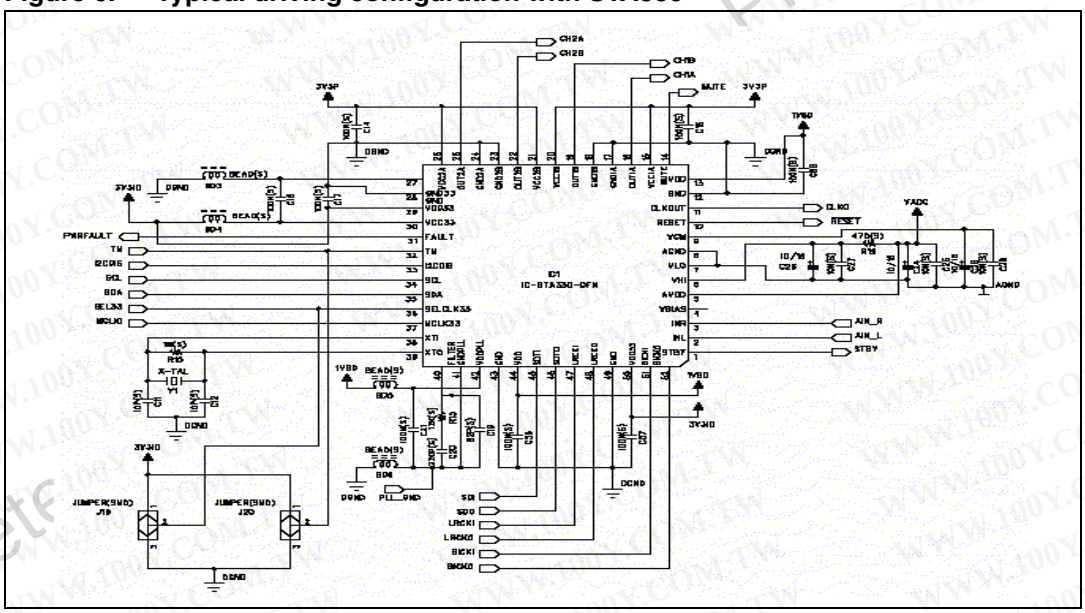


Figure 6. Typical driving configuration with STA330



3 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

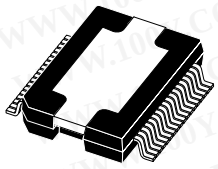
ECOPACK specifications are available at: http://www.st.com.

Figure 7. PowerSO36 package dimensions

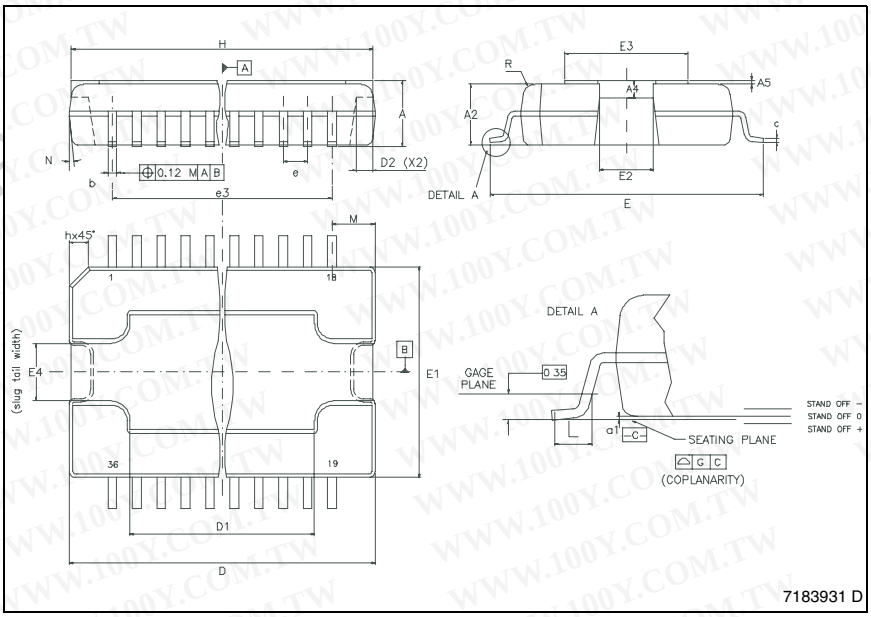
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.25		3.43	0.128		0.135
A2	3.1		3.2	0.122		0.126
A4	0.8		1	0.031		0.039
A5		0.2			0.008	
a1	0.030		-0.040	0.0011		-0.0015
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D	15.8		16	0.622		0.630
D1	9.4		9.8	0.37		0.38
D2		1			0.039	
E	13.9		14.5	0.547		0.57
E1	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
E4	2.9		3.2	0.114		1.259
e		0.65			0.026	
e3		11.05			0.435	
G	0		0.075	0		0.003
H	15.5		15.9	0.61		0.625
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N			10°			10°
s			8°			8°

(1) "D and E1" do not include mold flash or protusions.
Mold flash or protusions shall not exceed 0.15mm (0.006")
(2) No intrusion allowed inwards the leads.

Outline and mechanical data



PowerS036
(exposed pad (slug) up)



4 Trademarks and other acknowledgements

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DDX is a registered trademark of Apogee Technology, Inc.

ECOPACK is a registered trademark of STMicroelectronics.

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
13-Dec-2007	1	Initial release.

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