



TDC7200

SNAS647D - FEBRUARY 2015 - REVISED MARCH 2016

TDC7200 Time-to-Digital Converter for Time-of-Flight Applications in LIDAR, Magnetostrictive and Flow Meters

Features

Resolution: 55 ps

Standard Deviation: 35 ps

Measurement Range:

Mode 1: 12 ns to 500 ns

Mode 2: 250 ns to 8 ms

Low Power Consumption: 0.5 µA (2 SPS)

Supports up to 5 STOP Signals

Autonomous Multi-Cycle Averaging Mode for Low Power Consumption

Supply Voltage: 2 V to 3.6 V

Operating Temperature -40°C to 85°C

SPI Host Interface for Configuration and Register Access

Applications

- Flow Meter: Water Meter, Gas Meter, Heat Meter
- Magnetostrictive Position/Level Sensing
- Time-of-Flight in Drones (LIDAR, SONAR) metering equipment and projectors
- **Heat Cost Allocators**

Description

The TDC7200 is a Time-to-Digital Converter (TDC) for ultrasonic sensing measurement for ultrasonic sensing measurements such as water flow meter, gas flow meter, and heat flow meter. When paired with the TDC1000 (ultracerie and front-end), the TDC7200 can be a part of a complete TI ultrasonic sensing solution that includes the MSP430, power, wireless, and source code.

The Time to Digital Converter (TDC) performs the function of a stopwatch and measures the elapsed time (time-of-flight or TOF) between a START pulse and up to five STOP pulses. The ability to measure from START to multiple STOPs gives users the flexibility to select which STOP pulse yields the best echo performance.

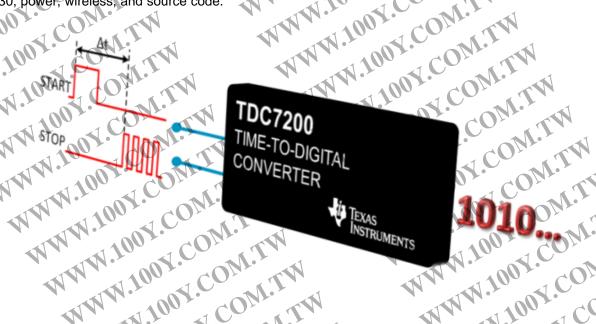
The device has an internal self-calibrated time base which compensates for drift over time and temperature. Self-calibration enables time-to-digital conversion accuracy in the order of picoseconds. This accuracy makes the TDC7200 ideal for flow meter applications, where zero and low flow measurements require high accuracy.

When placed in the Autonomous Multi-Cycle Averaging Mode, the TDC7200 can be optimized for low system power consumption, making it ideal for battery powered flow meters. In this mode, the host can go to sleep to save power, and it can wake up when interrupted by the TDC upon completion of the measurement sequence.

Device Information⁽¹⁾

-6		Dovido imormano	
	PART NUMBER	PACKAGE	BODY SIZE (NOM)
	TDC7200	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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.1 ()	4 Province History	1100 (0)	1100	(0)
	4 Revision History			
		11/1 , 100 , CO ₂ , CA	N 11N 140	$M_{\lambda} \sim Q_{\lambda}$
	Changes from Revision C	(August 2015) to Revision D	N N	Page
90	Added EN = HIGH	1100 (0)		1007 COB
	Added EN = HIGH			/
100	 update equation 			140
	• Changed 3818 TO 318			
400				4, 00)
	10			1
10	Changes from Revision B	(June 2015) to Revision C		Page
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N.		t title From: TDC7200 Time-to-Digital Converter for		(1) (1)
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Changes from Revision B (June 2015) to Revision C Changed the data sheet title From: TDC7200 Time-to-Digital Converter for Water and Gas Flow Sensing, Magnetostrictive Position Sensing, and LIDAR Metering Applications To: TDC7200 Time-to-Digital Converter for Time-of-Flight applications in LIDAR, Magnetostrictive and Flow Meters

Changes from Revision A (March 2015) to Revision B

Changed the data sheet title From: TDC7200 Time-to-Digital Converter for Water, Gas, Heat Flow Metering Applications To: TDC7200 Time-to-Digital Converter for Water and Gas Flow Sensing, Magnetostrictive Position Sensing, and LIDAR Metering Applications......

Changed the Applications list to include: "Magnetostrictive Position Sensing", and "LIDAR Metering"...

Changes from Original (February 2015) to Revision A

Changed From: 1-page Product Preview To: Full data sheet Changed ESD Ratings table......





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N	PART NO.	Utrasonic Sensing Analog Front End for Level	TITLE Concentration Flow and Proximity Ser	psing
4	TEXAS INSTRUMENTS www.ti.com 5 Companion Device PART NO. TDC1000	Surgestille Serioling / Malog F Fork End 101 Estes.	1100 11 CO	iong
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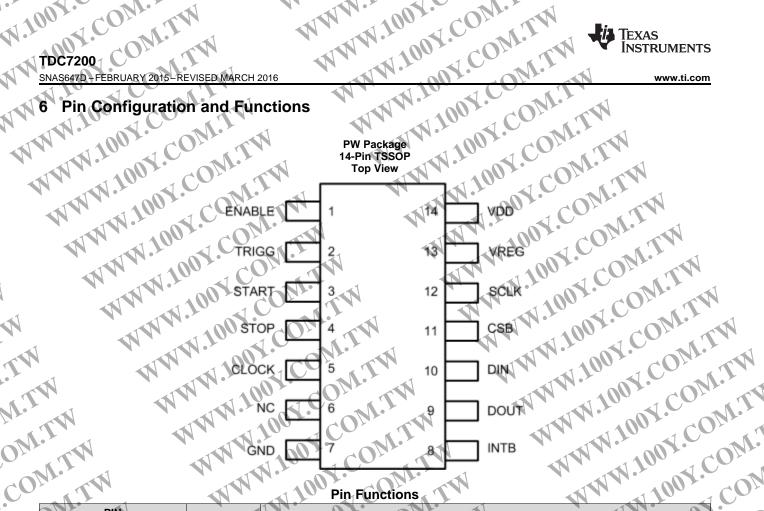
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TDC7200 SNAS647D FFP



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1 (0)		G	100 CON 100 CON 1
10	N. T.		ND TON STATE INTERNATION OF COMMITTEE OF COM
J.Co		M.	DESCRIPTION DOLLAR DOLL
100Å.C	PIN NO.	1/0	20011
100	ENABLE 1	Input	Enable signal to TDC Trigger output signal START signal to TDC
N.1007	TRIGG 2	Output	Trigger output signal
1100	START 3	Input	START signal to TDC STOP signal to TDC Clock input to TDC Not Connected
11.	STOP 4	Input	STOP signal to TDC
TW.LO	CLOCK 5	Input	Clock Input to TDC
N.Y.100	N.C. 6	-	Not Connected Ground
M.	GND 7	Ground	Clock Input to TDC Not Connected Ground Interrupt to MCU, active low (open drain)
NWW.		Output Output	Interrupt to MCU, active low (open drain) SPI Data Output SPI Data Input
	DOUT 9 DIN 10	Input	SPI Data Input
MAN	4 22 2 2	Input	SPI Chip Select, active low
WW	SCLK 12	Input	
	VREG 13	Output	LDO Output terminal for external decoupling cap Supply input
N	100	Power	Supply input
`	100	COL	
4	W. W. W.		N. W. W. T. W. W. T. W. W. T. W. W. T. W.
	1100	CON	LIW WWW.100 LCONTEN
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7 Sp	ecifications	MANN TOOK CONTIN
	bsolute Maximum Ratings	WW. 100X. COM. TW
$T_A = 25^{\circ}$	\dot{C} , \dot{V} DD = 3.3 \dot{V} , \dot{G} ND = 0 \dot{V} (unless otherwise	ise noted). (1)(2)(3)
	1100 (0)	MIN MAX UNIT
V_{DD}	Supply voltage	-0.3 3.9 V
V_{l}	Terminal input voltage	-0.3 V _{DD} +0.3 V
V_{DIFF_IN}	Voltage differential between any two input te	terminals 3.9 V
$V_{IN_GND_}$	v Voltage differential between any input termin	inal and GND or VDD 3.9 V
DD		
I _I -	Input current at any pin	-5, 5 mA
T_A	Ambient temperature	-40 125 °C
T _{stg}	Storage temperature	-65 150 °C

W.Ioux.

7.2 ESD Ratings

			1100	CO . T			VALUE	UNIT	
	N. N.		Human-body model	(HBM), per ANSI/E	ESDA/JEDEC JS-00	1 ⁽¹⁾	±1000	1.	
1 C	V _(ESD) Ele	ectrostatic discharge	4 110		DEC specification JE		1	V	Dr. 4
		1	C101 ⁽²⁾	(0311.), ps	opomicanion cz	.0022	±250		
₄₁ ((1) JEDEC	document JEP155 states th	at 500-V HBM allow	vs safé manufacturi	ng with a standard F	SD control proc	999	00	
10%		document JEP157 states the							
00	1 CO . 1			11 CO		-		100	1 (0)
00.	7.3 Reco	ommended Operati	ing Condition	S	ON.		NIV.	4.	
700	$T_A = 25^{\circ}C$	VDD = 3.3V, GND = 0V	(unless otherwise	noted). 1			N	11100	41 C
40	0, 20%			.00	MIN	NOM	MAX	UNIT	
21	1 /			1110				- 1	

JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

00 7	40			.00	10/1	MIN NO	MAX	UNIT	00%
W.10	V _{DD}	Supply voltage	The state of the s	1		2	3.6		100
400	V ₁	Terminal voltage		100,	CO	0	VDD	4	1003.
TIN . Le	Vill	Voltage input high		No.	0.7	× VDD	3.6		1.10
7	VIII	Voltage input low		1100	, C	0	0.3 × VDD	- 7	100
	F _{CALIB_CLK}	Frequency (Reference/C	Calibration Clock)	111	.03	1 (1)	8 16		W
	DUTY _{CLOCK}	Input clock duty cycle		(1)	<u> </u>	50%	6		1 10
		MENTS: Measurement M	Mode 1 ⁽¹⁾		.00	dON.			NN
N	T1STARTSTOP_Min	Minimum Time between	Start and Stop Sign	al	700	1 12		ns	
	T1 _{STOPSTOP_Min}	Minimum Time between	2 Stop Signals		100	67		ns	
	T1 _{STARTSTOP_Max}	Maximum time bet. Star	t and Stop Signal	1	11.5	01.	500	ns	10
	T1 _{STOPSTOP_Max}	Maximum time bet. Star	t and last Stop Signa	al	-11	10	500	ns	NIN .
	TIMING REQUIRE	MENTS: Measurement 2	(1)		1111	007.	.01	į.	
	T2 _{STARTSTOP_Min}	Minimum Time between	Start and Stop Signa	al	2>	kt _{CLOCK}	CO	S	
	T2 _{STOPSTOP_Min}	Minimum Time between	2 Stop Signals		2>	kt _{CLOCK}	COM	S	
_	T2 _{STARTSTOP_Max}	Maximum time bet. Star	t and Stop Signal			N.I	(2 ¹⁶ -2)×t _{CLOCK}	s	
_	T2 _{STOPSTOP_Max}	Maximum. time bet. Star		al		100	(2 ¹⁶ -2)×t _{CLOCK}	S	
	TIMING REQUIRE	MENTS: ENABLE INPUT			11	TW.	al.	1.	
	T _{REN}	Rise Time for Enable Si	gnal (20%-80%)			1 to 10		ns	
	T _{FEN}	Fall Time for Enable Sig	nal (20%-80%)	N		1 to 10	0	ns	N
(1) Specified by de	esign.	Co	4	*	N	700 T C		
		141, 100,	COM				1007.	OIN	
		N. IN. LO	1.00	1		N	N.L		
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		N.	.007.	Mr.	N		WW.	ov.co	M.
			100	U' , 1	7	.4			

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(3) All voltages are with respect to ground, unless otherwise specified. OY.COM.TW

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TAN	SNAS647D - FEBRUARY 2015-REVISED MARCH 2016	.007.	www.ti.com
<i>M</i> ,	Recommended Operating Conditions (continued)	1.10	
	Recommended Operating Conditions (continued)	100 CON TAN	
	$T_A = 25^{\circ}\text{C}$, VDD = 3.3V, GND = 0V (unless otherwise noted).	W. Fare and a	
<	1100 100 1100	MIN NOM MAX	UNIT
	TIMING REQUIREMENTS: START, STOP, CLOCK	W. O. O. O.	
	T _{RST} , T _{FST} Maximum rise, fall time for START, STOP signals (20%-80%)	NW. LUCK CONT. T	ns
	T _{RXCLK} , T _{FXCLK} Maximum rise, fall time for external CLOCK (20%-80%)	1 CO 1	ns
	TIMING REQUIREMENTS: TRIGG	100 CON	
(T _{TRIGSTART} Time from TRIG to START	5	ns
1	TEMPERATURE	100, 00	
1	T _A Ambient temperature	-40 85.	°C
	T _J Junction temperature	40 85	°C
- 1			

7.4 Thermal Information

	7.4	Thermal Information		1100	100
		NW.	THERMAL METRIC(1)	TDC7200 PW [TSSOP]	UNIT
OW.	TW		THERMAL METRIC	14 PINS	ON CONTRACTOR
	$R_{\theta_{i}}$	A Junction-to-ambie	nt thermal resistance	134.9	
CO_{λ}	R_{θ}	_{C(top)} Junction-to-case	top) thermal resistance	63	100 , 407, 44
	$R_{\theta_{s}}$	B Junction-to-board	thermal resistance	76.8	°C/W
41 C	Ψυτ	Junction-to-top ch	aracterization parameter	12.4	1 1000
	Ψјε	Junction-to-board	characterization parameter	76.2	4. 001.
-1	θ_{JA}	Package thermal	impedance	113	130° CO'
00 2.	(1)	For more information about tra	ditional and new thermal metrics, see the IC Packa	age Thermal Metrics application rep	ort, SPRA953.
00		N. V	M. M. ON		W. Landy.
700	1 C		WW 31 100 11 CO		NA TITON I CO
40	0.	COMM	100 · CO		
	4		W. W. To a Co		W . W . 100
14.	100,	CONSTAN	1001.	ON	1007.
IN.	70	Y. O. M.	W. W. W.		W. W. TO

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7.5 Electrical Characteristics

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W.	7.5 Ele	ectrical Charac	teristics		M. M. M.	ON!			
M	A 1			unless otherwise noted).	100	1 CO			
	N	PARAMETER		TEST CON	DITIONS	MIN	TYP M	AX UNIT	
	TDC CHA	RACTERISTICS		. 1	111.	04.	1		
<	LSB	Resolution	O.	Single shot measurement	110	0, (0)	55	ps	
· ·	T _{ACC-2}	Accuracy (Mode 2)	(1)	CLOCK = 8 MHz		001.	28	1 ps	
	T _{STD-2}	Standard Deviation	(Mode 2)	Measured time = 100 μs		100 1 C	50	ps	
		N , Ω	40	Measured time = 1 µs		1007.	35	ps	
×1	OUTPUT	CHARACTERISTICS	: TRIGG, II	NTB, DOUT		1.1			
	V _{OH}	Output voltage high	0 >	Isource = -2 mA		2.31	2.95	V	
	V _{OL}	Output voltage low		Isink = 2 mA		N. I	0.35 0.	99 V	1
	INPUT CH	IARACTERISTICS: I	ENABLÉ, S	TART, STOP, CLOCK, DIN	I, CSB,SCLK	4, 100	CO		4
·	C _{in}	Input capacitance (2	2)				3	pF	
	POWER C	CONSUMPTION (see	Measurem	nent Mode 1 and Measure	ment Mode 2)		1 ()), " (
N. C.	I _{sh}	Shutdown current	4	EN = LOW			0.3	2 μΑ	
	I_{QA}	Quiescent Current A	4 1 1	EN = HIGH; TDC running		W. W.	1.35	mA	
Oh	I _{QB}	Quiescent Current E	3	EN = HIGH; TDC OFF, Clo			71	μA	
dom.	loc	Quiescent Current (EN = HIGH; measurement communication only	stopped, SPI	W.	87	μА	Mil
COM	I_{QD}	Quiescent Current [EN = HIGH, TDC OFF, cou communication	unter stopped, no	W.	50	1 μΑ	OM.T.
1.00	(1) Accura	acvis defined as the	systematic	error in the output signal; the	ne error of the device exc	cluding noise.	1.77	, <u> </u>	
00	(2) Specif	fied by design.		100,	OB	3		1002.	COL
	7 6 Tim	mina Boquirom	onto	M.M.			N. TIN.	The off	
1 (7.6 Tin	ning Requirem	ents	1400	COLL	MAL	NOM MA	X UNIT	1000
003.						MIN	NOM MA	UNII	11.0

MMM Jun 1.

-			A.111					<u> </u>	A
	(1) Accuracy is de	fined as the systematic err	or in the output sig	gnal; the error of	the device exclud	ling noise.	W.IV	-01.	
	(2) Specified by de	esign.	1100	1 CO 1			NIN 31	00	COR
ام	7.6 Timing R	equirements	144.		N. T.			00	
			1711.10	4.0	1	MIN	NOM MAX	UNIT	4.0
4	TIMING REQUIRE	MENTS: START, STOP IN	PUTS, CLOCK	00,	Dr. Ch	1		10	O, CC
	PW _{START}	Pulse width for Start Signa				10		ns	
y	PW _{STOP}			100	COX	10		ns	100
Ω	SERIAL INTERFA	CE TIMING CHARACTERI	STICS (VDD = 3.	3 V, f _{SCLK} = 20	MHz) (See <mark>Figure</mark>	1)			007.
,	f _{SCLK}	SCLK Frequency		1100	1 CO' N		20	MHz	1.100
4	40	SCLK period	111	400	i.	50		ns	00
. >	t_2	SCLK High Time		N. Lu	4.0	16	1	ns	W.10
. 4	t ₃ (V)	SCLK Low Time	-1	N	10 - 40	16	4	ns	10
N	t ₄	DIN setup time				4	<u>~1</u>	ns	TW.LO
·	t ₅₁	DIN hold time	4	NN T	100	4		ns	11
	t ₆	CSB fall to SCLK rise				6		ns	· IN.
1	t ₇	Last SCLK rising edge to	CSB rising edge		1100	6		ns	
.1	T 8	Minimum pause time (CSI	3 high)		14. 100	40		ns	
N	tg	Clk fall to DOUT bus trans	ition	N.	N.Tu	10	12	ns	
	11 12 12 12 12 12 12 12 12 12 12 12 12 1	7.6 Timing R TIMING REQUIRED PWSTART PWSTOP SERIAL INTERFACE	7.6 Timing Requirements TIMING REQUIREMENTS: START, STOP IN PWSTOP Pulse width for Start Signal PWSTOP Pulse width for Stop Signal SERIAL INTERFACE TIMING CHARACTERI fSCLK SCLK Frequency to SCLK period to SCLK High Time to SCLK Low Time to DIN setup time to DIN hold time to Last SCLK rising edge to to to the setup time (CSE)	7.6 Timing Requirements TIMING REQUIREMENTS: START, STOP INPUTS, CLOCK PW _{START} Pulse width for Start Signal PW _{STOP} Pulse width for Stop Signal SERIAL INTERFACE TIMING CHARACTERISTICS (VDD = 3. f _{SCLK} SCLK Frequency t SCLK period t SCLK High Time t SCLK Low Time t DIN setup time	7.6 Timing Requirements TIMING REQUIREMENTS: START, STOP INPUTS, CLOCK PW_START Pulse width for Start Signal PW_STOP Pulse width for Stop Signal SERIAL INTERFACE TIMING CHARACTERISTICS (VDD = 3.3 V, f_SCLK = 20 f_SCLK SCLK Frequency t, SCLK period t_2 SCLK High Time t_3 SCLK Low Time t_4 DIN setup time t_5 DIN hold time t_6 CSB fall to SCLK rise t_7 Last SCLK rising edge to CSB rising edge t_8 Minimum pause time (CSB high)	7.6 Timing Requirements TIMING REQUIREMENTS: START, STOP INPUTS, CLOCK PWSTART Pulse width for Start Signal PWSTOP Pulse width for Stop Signal SERIAL INTERFACE TIMING CHARACTERISTICS (VDD = 3.3 V, fSCLK = 20 MHz) (See Figure fSCLK SCLK Frequency t1 SCLK period t2 SCLK High Time t3 SCLK Low Time t4 DIN setup time t5 DIN hold time t6 CSB fall to SCLK rise t7 Last SCLK rising edge to CSB rising edge t8 Minimum pause time (CSB high)	TIMING REQUIREMENTS: START, STOP INPUTS, CLOCK	7.6 Timing Requirements MIN NOM MAX TIMING REQUIREMENTS: START, STOP INPUTS, CLOCK	7.6 Timing Requirements Min Nom Max Unit

Switching Characteristics

tg	9 Clk fall to DOUT bus transition 12 ns	W.
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7	.7 Switching Characteristics	
Τ,	A = 25°C , VDD = 3.3 V, GND = 0 V (unless otherwise noted).	-
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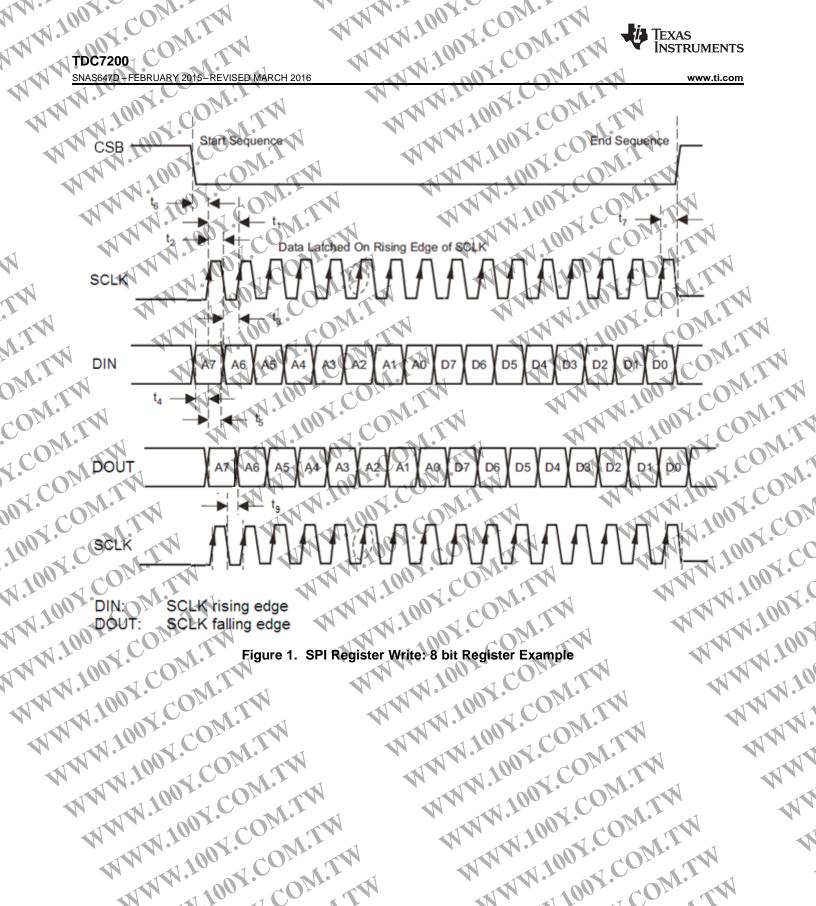
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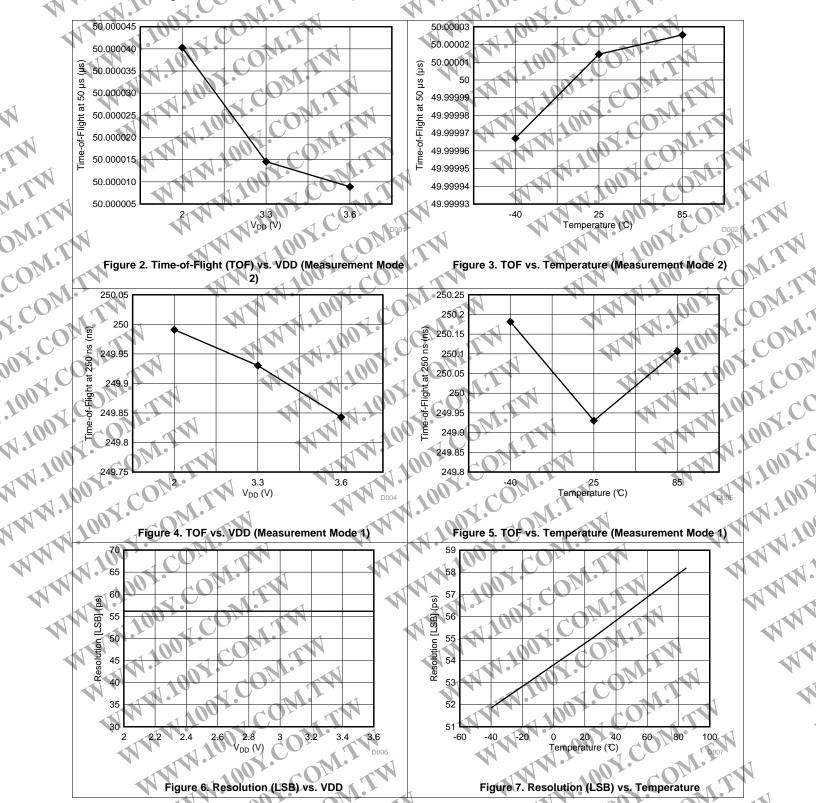
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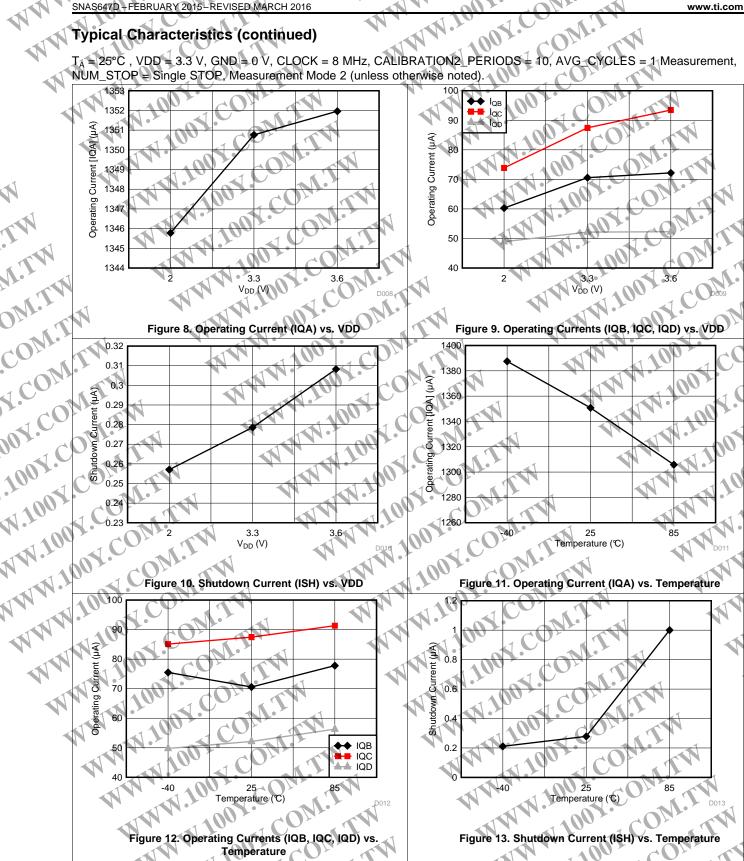
 $T_A=25^{\circ}\text{C}\text{ , VDD} \neq 3.3\text{ V, GND} = 0\text{ V, CLOCK} = 8\text{ MHz, CALIBRATION2} \text{ PERIODS} \neq 10\text{, AVG_CYCLES} = 1\text{ Measurement, NUM_STOP} = \text{Single STOP, Measurement Mode 2 (unless otherwise noted)}.$

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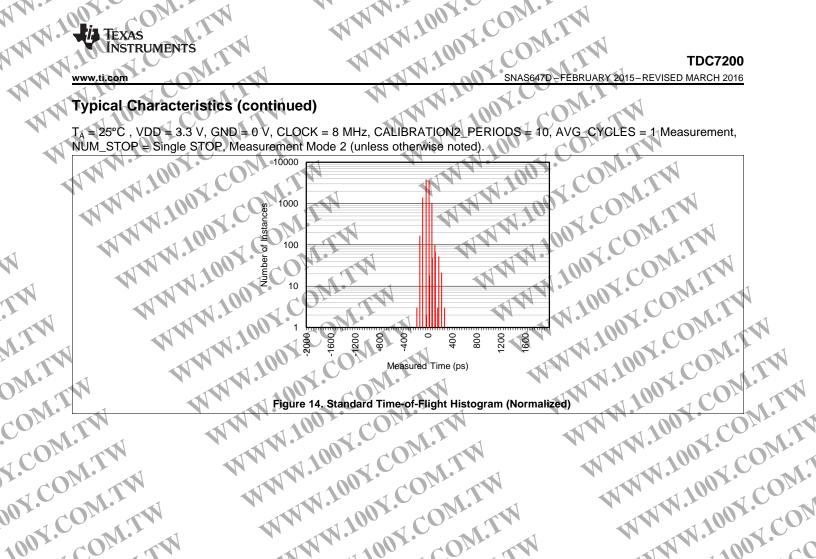
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TEXAS **INSTRUMENTS**

TDC7200 SNAS647D FF-

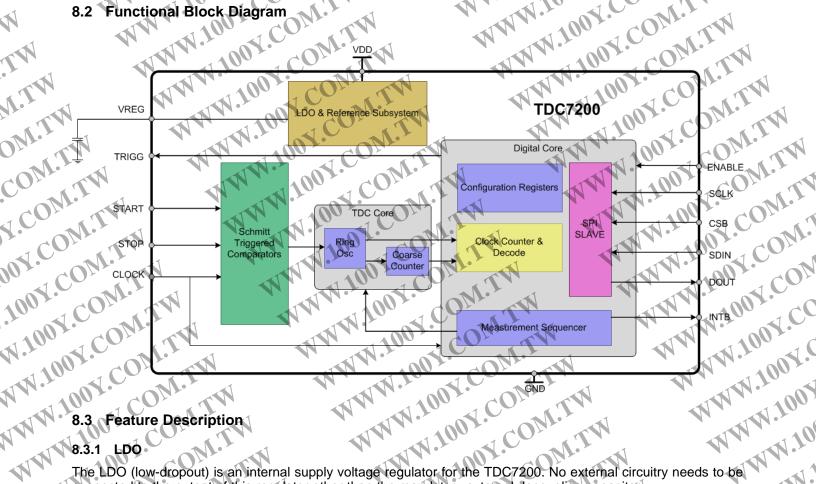
WW.100Y.C 8 Detailed Description
8.1 Overview
The TDC7200 is a stopwatch IC used to measure time between a single event (edge on START pin) and multiple subsequent events (edge on STOP pin). An event from a START pulse to a STOP pulse is also known as timeof-flight, or TOF for short. The device has an internal time base that is used to measure time with accuracy in the order of picoseconds. This accuracy makes the TDC7200 ideal for application such as flow meter, where zero and low flow measurements require high accuracy in the picoseconds range.

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Functional Block Diagram



NW 8.3.1 connected to the output of this regulator other than the mandatory external decoupling capacitor.

Recommendations for the decoupling capacitor parameters:

- Type: ceramic
- Capacitance: 0.4 µF–2.7 µF (1 µF typical). If using a capacitor value outside the recommended range, the WW.100Y.COM.T WWW.100Y.COM part may malfunction and can be damaged. WWW.100Y.COM.TW WWW.100Y.COM.TW
- ESR: 100 mΩ (max)

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YW.100Y.T Feature Description (continued)

8.3.2 CLOCK

TDC7200 needs an external reference clock connected to the CLOCK pin. The external CLOCK is used to calibrate the internal time base accurately and therefore the material time base accurately and the material time base accurate the material time base accur calibrate the internal time base accurately and therefore, the measurement accuracy is heavily dependent on the external CLOCK accuracy. This reference clock is also used by all digital circuits inside the device; thus, CLOCK has to be available and stable at all times when the device is enabled (ENABLE = HIGH).

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Figure 15 shows the typical effect of the external CLOCK frequency on the measurement uncertainty. With a reference clock of 1MHz, the standard deviation of a set of measurement results is approximately 243ps. As the reference clock frequency is increased, the standard deviation (or measurement uncertainty) reduces. Therefore, using a reference clock of 16MHz is recommended for optimal performance. W.100Y.COM.T

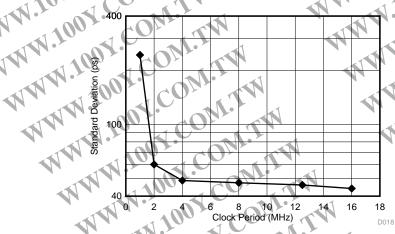


Figure 15. Standard Deviation vs. CLOCK

.100Y.COM.TW 8.3.3 Counters

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WW.100Y.COM Time measurements by the TDC7200 rely on two counters: the Coarse Counter and the Clock Counter. The Coarse Counter counts the number of times the ring oscillator (the TDC7200's core time measurements) wraps, which is used to generate the results in the TIME 1 to TIME 1.

The Clock Counter counts the number of integer clock cycles between START and STOP events and is used in Measurement Mode 2 only. The results for the Clock Counter are displayed in the CLOCK_COUNT1 CLOCK_COUNT5 registers.

8.3.3.2 Coarse and Clock Counters Overflow

Once the coarse counter value has reached the corresponding value of the Coarse Counter Overflow registers, then its interrupt bit will be set to 1. In other words, if (TIMEn / 63) ≥ COARSE_CNTR_OVF, then COARSE_CNTR_OVF_INT = 1 (this interrupt bit is located in the INT_STATUS register). COARSE_CNTR_OVF = (COARSE_CNTR_OVF_H x 2⁸ + COARSE_CNTR_OVF_L), and TIMEn refers to the TIME1 to TIME6 registers.

Similarly, once the clock counter value has reached the corresponding value of the Clock Counter Overflow registers, then its interrupt bit will be set to 1. In other words, if GLOCK_COUNTn > CLOCK_CNTR_OVF, then CLOCK_CNTR_OVF_INT = 1 (this interrupt bit is located in the INT_STATUS register). CLOCK_CNTR_OVF = (CLOCK CNTR_OVF_H x 28 + CLOCK_CNTR_OVF_L), and CLOCK_COUNTn refers to the CLOCK_COUNT1 to CLOCK COUNT5 registers.

W.100Y.COM.T As soon as there is an overflow detected, the running measurement will be terminated immediately. Instr VWW.1001 M.M.M.100,

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TDC7200 SNAS647D+FEF

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Feature Description (continued)

8.3.3.3 Clock Counter STOP Mask

The value in the Clock Counter STOP Mask registers define the end of the mask window. The Clock Counter STOP Mask value will be referred to as CLOCK CNTR STOP MASK = (OLOCK CNTR STOP MASK = 28) STOP Mask value will be referred to as CLOCK_CNTR_STOP_MASK = (CLOCK_CNTR_STOP_MASK_H x 28 + CLOCK_CNTR_STOP_MASK_L).

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The Clock Counter is started by the first rising edge of the external CLOCK after the START signal (see Figure 18). All STOP signals occurring before the value set by the CLOCK_CNTR_STOP_MASK registers will be ignored. This feature can be used to help suppress wrong or unwanted STOP trigger signals.

For example, assume the following values:

- The first time-of-flight (TOF1), which is defined as the time measurement from the START to the 1st STOP = 19 us.
- The second time-of-flight (TOF2), which is defined as the time measurement from the START to the 2nd STOP = 119 µs.
- CLOCK = 8 MHz

In this example, the TDC7200 will provide a CLOCK_COUNT1 of approximately 152 (19 µs / t_{CLOCK}), and CLOCK_COUNT2 of approximately 952 (119 µs / t_{CLOCK}). If the user sets CLOCK ONTE CTOCK CLOCK_COUNT2 of approximately 952 (119 µs / t_{CLOCK}). If the user sets CLOCK_CNTR_STOP_MASK anywhere between 152 and 952, then the 1st STOP will be ignored and 2nd STOP will be measured.

The Clock Counter Overflow value (CLOCK_CNTR_OVF_H x 2⁸ + CLOCK_CNTR_OVF_L) should always be higher than the Clock Counter STOP Mask value (CLOCK_CNTR_STOP_MASK_H x 2⁸ + CLOCK_CNTR_STOP_MASK_L). Otherwise, the Clock Counter Overflow Interrunt will be set before the force. CLOCK CNTR_STOP_MASK_L). Otherwise, the Clock Counter Overflow Interrupt will be set before the STOP mask time expires, and the measurement will be halted.

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The ENABLE pin is used as a reset to all digital circuits in the TDC7200. Therefore, it is essential that the ENABLE pin sees a positive edge after the device has powered up. It is also important to ensure that the no transients (glitches, etc.) on the ENABLE pin; such alitches could oox.co WWW.100Y.COM

Device Functional Modes

8.4.1 Calibration
The time The time measurements performed by the TDC7200 are based on an internal time base which is represented as the LSB value of the TIME1 to TIME6 results registers. The typical LSB value can be seen in *Electrical Characteristics*. However, the actual value of the LSB can vorte date. (temperature, systematic noise, etc.). This variation can introduce significant error into the measurement result. There is also an offset error in the measurement due to certain internal delays in the device.

In order to compensate for these errors and to calculate the actual LSB value, calibration needs to be performed. The TDC7200 calibration consists of two measurement cycles of the external CLOCK. The first is a measurement of a single clock cycle period of the external clock; the second measurement is for the number of external CLOCK periods set by the CALIBRATION2_PERDIOS in the CONFIG2 register. The results from the calibration measurements are stored in the CALIBRATION1 and CALIBRATION2 registers.

The two-point calibration is used to determine the actual LSB in real time in order to convert the TIME1 to TIME6 results from number of delays to a real time-of-flight (TOF) number. As discussed in the next sections, the WWW.100Y.COM. WWW.100X.CO WWW.100Y.COM.TW calibrations will be used for calculating time-of-flight (TOF) in measurement modes 1 and 2. WWW.100Y.COM.T

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Device Functional Modes (continued)

8.4.2 Measurement Modes

8.4.2.1 Measurement Mode 1

JAN 100Y COM. In measurement mode 1 as shown in Figure 16, the TDC7200 performs the entire counting from START to the last STOP using its internal ring oscillator plus coarse counter. This method is recommended for measuring shorter time durations of < 500 ns. Using measurement mode 1 for measuring time > 500 ns decreases accuracy of the measurement (as shown in Figure 17), and is not recommended.

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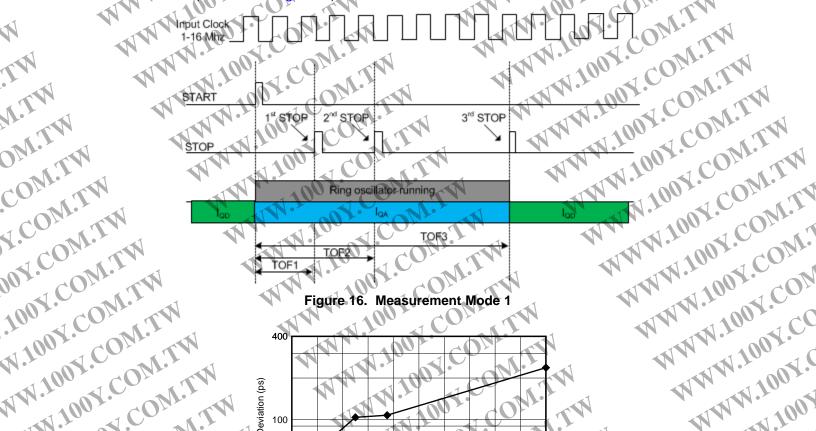
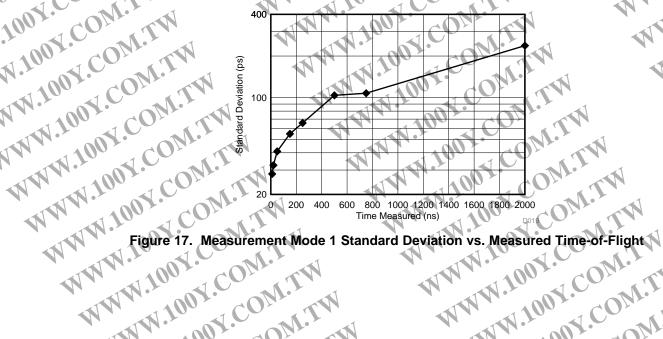


Figure 16. Measurement Mode 1



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where

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- TOF_n [sec] = time-of-flight measurement from the START to the n^th STOP

CALIBRATION2 [count] = TDC count for first calibration cycle

CALIBRATION2 [count] = TDC count for second calibration cycle

CALIBRATION2 PERIODS = setting for the second calibration cycle; located in register CONFIG2

(1)

, assume the time-of-flight between the START to the 1st STOP is desired. and the elements obtained:

TION2 = 21121 (decimal)

TION2 PET COM.TW For example, assume the time-of-flight between the START to the 1st STOP is desired, and the following readouts were obtained:

• CALIBRATION2 = 21121 (decimal)

• CALIBRATION4 2011 W.100Y.COM.TV W.100Y.COM.

- CALIBRATION2 PERIODS = 10
- 007.CO CLOCK = 8MHz

Therefore, the calculation for time-of-flight is:

- calcount = (21121 2110) / (10 1) = 2112.33normLSB = $(1/8MHz) / (2112.33) = 5.917 \times 10^{-11}$ TOF1 = $(4175)(5.917 \times 10^{-11}) = 247.5$

calCount = (21121 - 2110) / (10 - 1) = 2112.33normLSB = $(1/8\text{MHz}) / (2112.33) = 5.917 \times 10^{-11}$ TOF1 = $(4175)(5.917 \times 10^{-11}) = 247.061 \text{ ns}$ WW.100Y.C 8.4.2.2 Measurement Mode 2
In measurement mode 1
total mos In measurement mode 2, the internal ring oscillator of the TDC7200 is used only to count fractional parts of the total measured time. As shown in Figure 18, the internal ring oscillator starts counting from when it receives the START signal until the first rising edge of the CLOCK. Then, the internal ring oscillator switches of the Clock counter starts counting the clock cycles of th internal ring oscillator again starts counting from the STOP signal until the next rising edge of the CLOCK. W.1007.COM.

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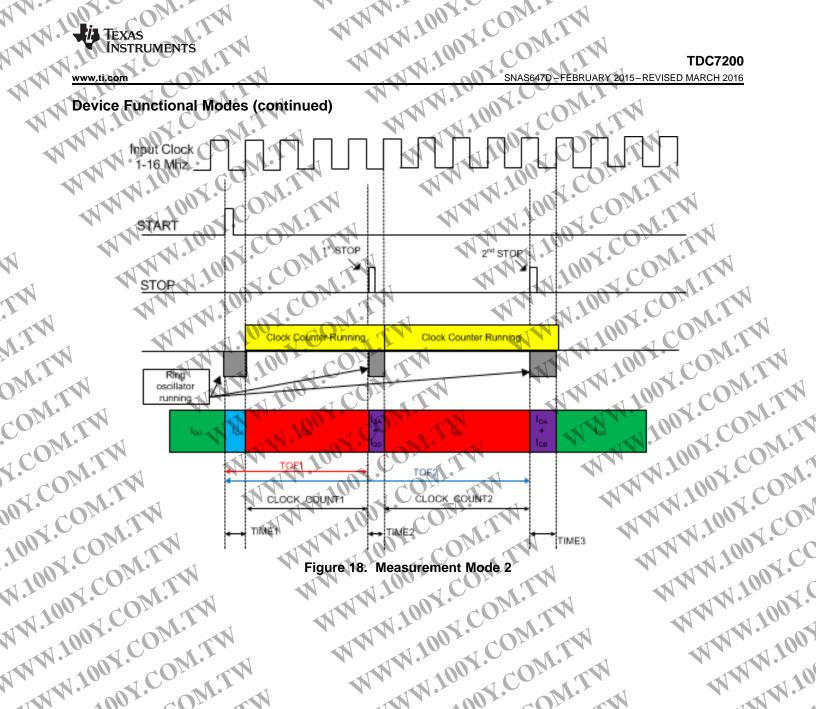
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Device Functional Modes (continued)

8.4.2.2.1 Calculating Time-of-Flight (TOF) (Measurement Mode 2)

The time-of-flight (TOF) between the START to the nth STOP can be calculated using Equation 2:

TOF_n = normLSB(TIME1=TIME_{n+1})+ (CLOCK_COUNT_n)(CLOCKperiod)

normLSB =
$$\frac{(CLOCKperiod)}{(CalCount)}$$

calCount =
$$\frac{CALIBRATION2-CALIBRATION1}{(CALIBRATION2-PERIODS)-1}$$

where

• TOF_n [sec] = time-of-flight measurement from the START to the nth STOP

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-griv measurement from the START to the nth STOP

 TIME1 = time 1 measurement given by the TDC7200 register address 0x10

 TIME_(n+1) = (n+1) time measurement, where n = 1 to 5 (TIME2 to TIME6 registers)

 normLSB [sec] = normalized LSB value from calibration

 CLOCK_COUNT_n = nth clock count, where n = 1 to 5 (CLOCK_COUNT_CLOCK_CLOCK_COUNT_CLOCK_CLOCK_COUNT_CLOCK_CLOCK_COUNT_CLOCK_CL

- normLSB [sec] = normalized LSB value from calibration

 CLOCK_COUNT₀ = nth clock count, where n = 1 to 5 (CLOCK_COUNT1 to CLOCK_COUNT5)

 CLOCKperiod [sec] = external CLOCK period

 CALIBRATION1 [count] = TDC count for first calibration cycle

 CALIBRATION2 [count] = TDC count for second collibrations W. 100 Y. CO. M. T. W.

CALIBRATION2 [count] = TDC count for first calibration cycle

CALIBRATION2_PERIODS = setting for the second calibration; located in register CONFIG2

, assume the time-of-flight between the START to the 1st STOP is decision to the obtained:

TION2 = 23133 (decimal)

TION1 = 2315 (1) CALIBRATION2_PERIODS = setting for the second calibration; located in register CONFIG2

For example, assume the time-of-flight between the START to the 1st STOP is desired, and the following readouts were obtained:

CALIBRATION2 = 23133 (decimal)

CALIBRATION1 = 2315 (decimal)

CALIBRATION2_PERIODS = 10

CLOCK = 8MHz

TIME1 = 2147 (decimal) N.COM.TW or example, assume t readouts were obtained:

• CALIBRATION? MMM.100X.COM

TOF1 = (TIME1)(normLSB) + (CLOCK_COUNT1)(CLOCKperiod) – (TIME2)(normLSB)
TOF1 =
$$(2147)(5.40*10^{-11})$$
 + $(318)(1/8MHz)$ – $(201)(5.40*10^{-11})$
TOF1 = 39.855μ s

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Device Functional Modes (continued)

8.4.3 Timeout

For one STOP, the TDC performs the measurement by counting from the START signal to the STOP signal. If no STOP signal is received, either the Clock Counter or Coarse Counter will overflow and will generate an interrupt (see Coarse and Clock Counters Overflow). If no START signal is received, the timer waits indefinitely for a START signal to arrive.

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For multiple STOPs, the TDC performs the measurement by counting from the START signal to the last STOP signal. All earlier STOP signals are captured and stored into the corresponding Measurement Results registers (TIME1 to TIME6, CLOCK_COUNT1 to CLOCK_COUNT5, CALIBRATION1, CALIBRATION2). The minimum time required between two consecutive STOP signals is defined in the Recommended Operating Conditions table. The device can be programmed to measure up to 5 STOP signals by setting the NUM_STOP bits in the CONFIG2 register.

8.4.4 Multi-Cycle Averaging

In the Multi-Cycle Averaging Mode, the TDC7200 will perform a series of measurements on its own and will only send an interrupt to the MCU (for example, MSP430, C2000, etc) for wake up after the series has been completed. While waiting, the MCU can remain in sleep mode during the whole cycle (as shown in Figure 19).

Multi-Cycle Averaging Mode Setup and Conditions:

- The number of averaging cycles should be selected (1 to 128). This is done by programming the AVG CYCLES bit in the CONFIG2 register.
- The results of all measurements are reported in the Measurement Results registers (TIME1 to TIME6, CLOCK_COUNT1 to CLOCK_COUNT5, CALIBRATION1, CALIBRATION2 registers). The CLOCK_COUNTn registers should be right shifted by the log2(AVG_CYCLES) before calculating the time-of-flight (TOF). For example, if using the multi-cycle averaging mode, Equation 2 should be rewritten as: TOFn = normLSB [TIME1 - TIME(n+1)] + [CLOCK_COUNTn >> log 2 (AVG_CYCLES)] x [CLOCKperiod]
- Following each average cycle, the TDC generates either a trigger event on the TRIGG pin after the calibration measurement to commence a new measurement or an interrupt on the INTB pin, indicating that the averaging sequence has completed.

This mode allows multiple measurements without MCU interaction, thus optimizing power consumption for the overall system.

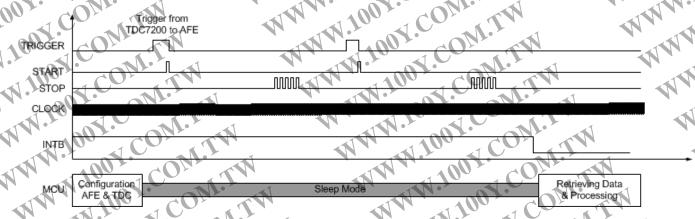


Figure 19. Multi-Cycle Averaging Mode Example with 2 Averaging Cycles and 5 STOP Signals

START and STOP Edge Polarity

In order to achieve the highest measurement accuracy, having the same edge polarity for the START and STOP input signals is highly recommended. Otherwise, slightly different propagation delays due to symmetry shift between the rising and falling edge configuration will impact the measurement accuracy.

For highest measurement accuracy in measurement mode 2, it's strongly recommended to choose for the START and STOP signal the "rising edge". This is done by setting the START_EDGE and STOP_EDGE bits in the CONFIG1 register to 0.

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Device Functional Modes (continued)

8.4.6 Measurement Sequence

The TDC7200 is a stopwatch IC that measures time between a START and multiple STOP events. The measurement sequence of the TDC7200 is as follows:

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- 1. After powering up the device, the EN pin needs to be low. There is one low to high transition required while VDD is supplied for correct initialization of the device.
 - MCU software requests a new measurement to be initiated via the SPI™ interface.
 - 3. After the start new measurement bit START_MEAS has been set in the CONFIG1 register, the TDC7200 generates a trigger signal on the TRIGG pin, which is typically used by the corresponding ultrasonic analogfront-end (such as the TDC1000) as start trigger for a measurement (for example, transmit signal for the ultrasonic burst)
 - 4. Immediately after sending the trigger, the TDC7200 enables the START pin and waits to receive the START pulse edge
 - After receiving a START, the TDC resets the TRIGG pin
- 6. The Clock counter is started after the next rising edge of the external clock signal (Measurement Mode 2) Counter STOP Mask registers (CLOCK_CNTR_STOP_MASK_H) CLOCK_CNTR_STOP MASK_L) determine the length of the STOP mask window.
- After reaching the Clock Counter STOP Mask value, the STOP pin waits to receive a single or multiple STOP trigger signal from the analog-front-end (for example, detected echo signal of the ultrasonic burst signal)
- After the last STOP trigger has been received, the TDC will signal to the MCU via interrupt (INTB pin) that there are new measurement results waiting in the registers. START, STOP and TRIGG pin are disabled (in Multi-Cycle Averaging Mode, the TDC will start the next cycle automatically by generating a new TRIGG signal). Note: INTB must be utilized to determine TDC measurement completion; polling the INT_STATUS register to determine measurement completion is NOT recommended as it will interfere with the TDC measurement.
- After the results are retrieved, the MCU can then start a new measurement with the same register settings. This is done by just setting the START measurement bit via SPI. It is not required to drive the ENABLE pin low between measurements.
- The ENABLE pin can be taken low, if the time duration between measurements is long, and it is desired to put the TDC7200 in its lowest power state. However, upon taking ENABLE high again, the device will come up with its default register settings and will beed to be seeffered visited. up with its default register settings and will need to be configured via SPI.

8.4.7 Wait Times for TDC7200 Startup

The required wait time following the rising edge of the ENABLE pin of the TDC7200 is defined by three key times, as shown in Figure 20. All three times relate to the startup of the TDC7200's internal LDO, which is power gated when the device is disabled for optimal power consumption. The first parameter, T1_{SPI_RDY}, is the time after which the SPI interface is accessible. The second (T2_{LDO SET1}) parameter and third (T3_{LDO SET2}) parameter are related to the performance of a measurement made while the internal LDO is settling. The LDO supplies the TDC7200's time measurement device, and a change in voltage on its supply during a measurement translates directly to an inaccuracy. It is therefore recommended to wait until the LDO is settled before time measurement. begins.

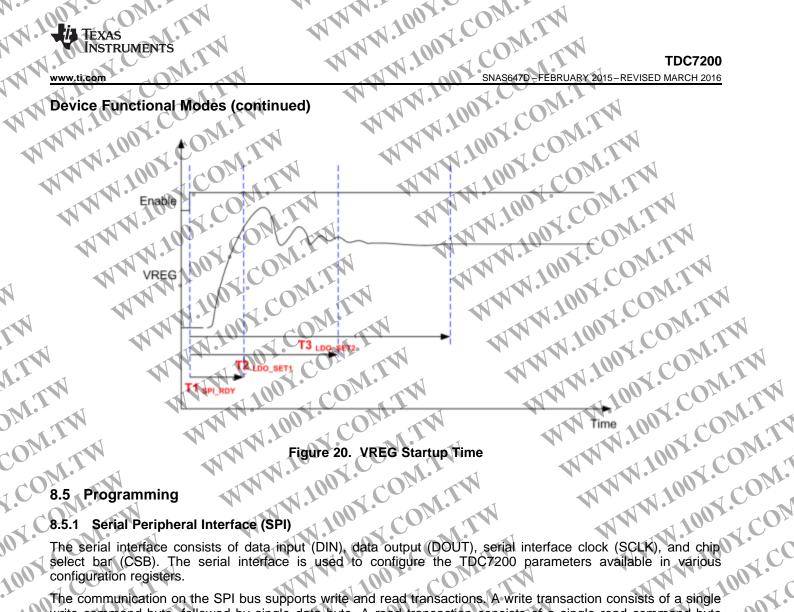
The first time period relating to the measurement accuracy is $T2_{LDO_SET1}$, the LDO settling time 1. This is the time after which the LDO has settled to within 0.3% of its final value. A 0.3% error translates to a worst case time error (due to the LDO settling) of 0.3% x t_{CLOCK} , which is 375ps in the case of an 8MHz reference clock, or 187.5ps if a 16MHz clock is used. Finally, the time T3_{LDO SET2} is the time after which the LDO has settled to its final value. For best performance, it is recommended that a time measurement is not started before T3_{IDO SET2} to allow the LDO to fully settle. Typical times for $T1_{SPI_RDY}$ is 100 μ s, for $T2_{LDO_SET1}$ is 300 μ s, and for $T3_{LDO_SET2}$ is 1.5 ms.

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WWW.100Y.COM.TV 8.5.1 Serial Peripheral Interface (SPI)

The serial interface consists of data input (DIN), data output (DOUT), serial interface clock (SCLK), and chip select bar (CSB). The serial interface is used to configure the TDC7200 parameters available in various configuration registers.

The communication on the SPI bus supports write and an inferior of the serial interface is used to configure the TDC7200 parameters available in various configuration on the SPI bus supports write and an inferior of the serial interface is used to configure the TDC7200 parameters available in various configuration on the SPI bus supports write and an inferior of the serial interface is used to configure the TDC7200 parameters available in various configuration on the SPI bus supports write and an inferior of the serial interface is used to configure the TDC7200 parameters available in various configuration on the SPI bus supports write and an inferior of the serial interface is used to configure the TDC7200 parameters available in various configuration on the SPI bus supports write and an inferior of the serial interface is used to configure the TDC7200 parameters available in various configuration.

The communication on the SPI bus supports write and read transactions. A write transaction consists of a single write command byte, followed by single data byte. A read transaction consists of a single read command byte followed by 8 or 24 SCLK cycles. The write and read command bytes consist of a 1-bit read or write instruction, and a 6-bit register address. Figure 21 shows the SPI protocol for a transaction involving one byte of data (read or write). WWW.100Y.COM.TW WWW.100Y.COM.T

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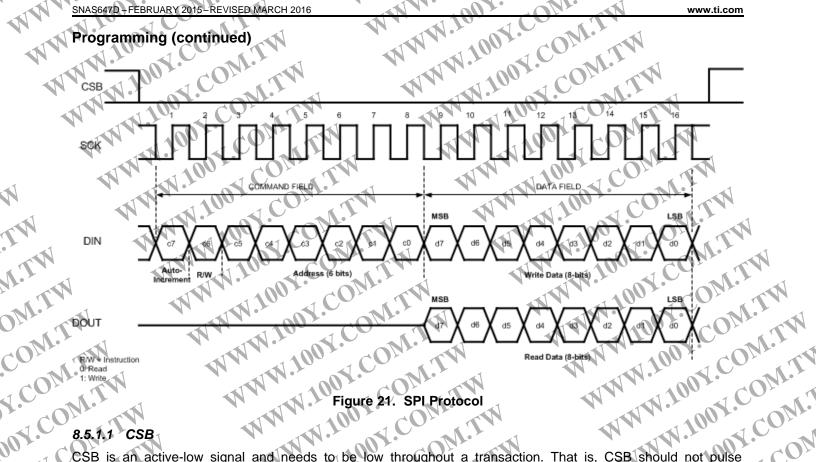
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TDC7200 SNAS647D - FF Programming (continued)



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OOX.COM. 8.5.1.1 CSB

CSB is an active-low signal and needs to be low throughout a transaction. That is, CSB should not pulse between the command byte and the data byte of a single transaction.

De-asserting CSB always terminates an ongoing transaction, even if it is not yet complete. Re-asserting CSB will always bring the device into a state ready for the next transaction, regardless of the termination status of a previous transaction.

SPI clock can idle high or low. It is recommended to keep SCLK as clean as possible to prevent glitches from corrupting the SPI frame.

8.5.1.3 DIN N. 100

8.5.1.3 DIN 8.5.1.3 DIN

Data In (DIN) is driven by the SPI master by sending the command and the data byte to configure the TDC7200.

8.5.1.4 DOUT

Data Out (DOUT) is driven by the TDC7200 when the SPI master initiates a read transaction. When the TDC7200 is not being read out, the DOUT pin is in high impedance mode and is undriven. WW.100Y.COM.TW WWW.100Y.COM.T WWW.100Y.C

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YW.100Y.T Programming (continued)

8.5.1.5 Register Read/Write

Access to the internal registers can be done through the serial interface formed by pins CSB (Chip Select - active low), SCI K (serial interface clock). DIN (data input), and DOLIT (data input). low), SCLK (serial interface clock), DIN (data input), and DOUT (data out).

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Serial shift of bits into the device is enabled when CSB is low. Serial data DIN is latched (MSB received first, LSB received last) at every rising edge of SCLK when CSB is active (low). The serial data is loaded into the register with the last data bit SCLK rising edge when CSB is low. In the case that the word length exceeds the register size, the excess bits are ignored. The interface can work with SCLK frequency from 20MHz down to very low speeds (a few Hertz) and even with a non-50% duty-cycle SCLK. Address and Control: Auto Increment Mode selection bit, Read/Write bit, Address 6 bits

Data: 8 bit or 24 bit

~ 1	low speeds (a	a few Hertz) and even w	rith a non-50% duty-o	cycle SCLK.			
	The SPI trans	saction is divided in two	main portions:		N 1 100	COM	TW
- N	 Address a 	nd Control: Auto Increm	nent Mode selection l	oit, Read/Write	bit, Address 6 b	its	1.
J.	• Data: 8 bi	or 24 bit			111	0, 1 CO,	
	When writing	to a register with unuse	d bits, these should	be set to 0.		100%	DIV. TV
	(1.00	(\$\) 1 (47 40)	W.	10	
		130, 400	Address and Co	ntrol (A7 - A0)			
	A7	A6 A5	A4	A3	A2	A1 1	A0
ON	Auto Increment	RW	in T.Com	Register Ad	dress	100	COR
COL	0: OFF 1: ON	Read = 0 Write = 1	100, 1COp.	00 h up to	3Fh	1100	COD
COM	1.01	wite = 1	1007.00				107.
1.00	8.5.1.6 Aut	o Increment Mode	N. To W.Co	TX.		1.11.7	S. W.
	When the Au	to Increment Mode is O	FF only the register	indicated by th	e Register Add	ress will be acc	cessed all

8.5.1.6 Auto Increment Mode

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When the Auto Increment Mode is OFF, only the register indicated by the Register Address will be accessed, all .100Y.C Address is accessed first, then without interruption, subsequent registers are accessed.

The Auto Increment Mode can be either used to access the configuration (CONFIG1 and CONFIG2) and status (INT_STATUS) registers, or for the Measurement Results registers (TIME1 to TIME6, CLOCK COUNTS CALIBRATIONS). As both registers. W.100Y.CC (INT_STATUS) registers, or for the Measurement Results registers (TIME1 to TIME6, CLOCK_COUNT1 to CLOCK_COUNT5, CALIBRATION1, CALIBRATION2). As both register block use registers with different length, it's not possible to access all registers of the device within one single access cycle. WWW.100Y.C NWW.1007.CON ...ces WWW.100Y.COM.TW WWW.100Y.COM.TW

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TDC7200 SNAS647D+FEP-8.6

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8.6.1 Register Initialization

After power up (VDD supplied, ENABLE Pin low to high transition) the internal registers are initialized with the default value. Disabling the part by pulling ENABLE pin to GND will set the device into total shutdown. As the internal LDO is turned off settings in the register will be lost. The device initializes the registers with default values with the next enable (ENABLE pin to VDD).

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Table 1. Register Summary

	values with the next e	enable (ENABLE pin to VDD).	100	COL	
	W. TWW. IC	Table 1	. Register Summary	OY.COM.T	
N	REGISTER ADDRESS	REGISTER NAME	REGISTER DESCRIPTION	SIZE (BITS)	RESET VALUE
· <1	00h	CONFIG1	Configuration Register 1	8	00h
	01h	CONFIG2	Configuration Register 2	8 00	40h
1	02h	INT_STATUS	Interrupt Status Register	8	00h
	03h	INT_MASK	Interrupt Mask Register	1 8	07h
A.TW	04h	COARSE_CNTR_OVF_H	Coarse Counter Overflow Value High	8	FFh
OM.TV	05h	COARSE_CNTR_OVF ₊ L	Coarse Counter Overflow Value Low	8	FFh
) Live	06h	CLOCK_CNTR_OVF_H	CLOCK Counter Overflow Value High	8	FFh
	07h	CLOCK_CNTR_OVF_L	CLOCK Counter Overflow Value Low	8	1 FEh
40 h	08h	CLOCK_CNTR_STOP_MASK_H	CLOCK Counter STOP Mask High	8	00h
I.COM	09h	CLOCK_CNTR_STOP_MASK_L	CLOCK Counter STOP Mask Low	8	00h
1	10h	TIME1	Measured Time 1	24	00_0000h
10	11h	CLOCK_COUNT1	CLOCK Counter Value	24	00_0000h
100	12h	TIME2	Measured Time 2	24	00_0000h
Joy.co	13h	CLOCK_COUNT2	CLOCK Counter Value	24	00_0000h
100 A . C.	14h	TIME3	Measured Time 3	24	00_0000h
100	15h	CLOCK_COUNT3	CLOCK Counter Value	24	00_000h
100	16h	TIME4	Measured Time 4	24	00_0000h
N.100Y	17h	CLOCK_COUNT4	CLOCK Counter Value	24	00_000h
100	18h	TIME5	Measured Time 5	24	00_0000h
11.10	19h	CLOCK_COUNT5	CLOCK Counter Value	24	00_0000h
	1Ah	TIME6	Measured Time 6	24	00_0000h 00_0000h
TN.	1Bh	CALIBRATION1	Calibration 1, 1 CLOCK Period	24	00_0000h
	100 1Ch	CALIBRATION2	Calibration 2, 2/10/20/40 CLOCK Periods	24	00_0000h
		N. ST	NAMA TO TO TO		
	11 100 at CO		MM 1 1001 CO		WW.
	1007	ON.	1003.	MI.	
M.	IN. TO		W. W. Joseph C.		
	M. 100,	COM	100	COMM	
N	M.1007.CO		M.M.M. 100 X .CO.		N
<	W.1007.1007. WW.1007.007.	COM.TW	M.M.M. 100 X .C.	COM.TW	
	W. VO	Y. COM. TW	N. W.	Y. ON.	
	1 10°		1100	CU	N'

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WW.100Y.COM. 8.6.2 CONFIG1: Configuration Register 1 R/W (address = 00h) [reset = 0h]

Figure 22. Configuration Register 1

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7	16	5	4	3	2.1	0
FORCE_CAL	PARITY_EN	TRIGG_EDGE	STOP_EDGE	START_EDGE	MEAS_MODE	START_MEAS
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h 1 R/W-0	h R/W-0h

	R/W-0h	7-	R/W-0h		W-0h R/W-0h R/W-0h R/W-0h
I	LEGEND: F	R/W = Read/Write; R = F	Read only; -r	= value aft	er reset
_		M. OOX.	Table 2. (Configura	ation Register 1 Field Descriptions
	Bit	Field	Туре	Reset	Description
	7	FORCE_CAL	R/W	0	0: Calibration is not performed after interrupted measurement (for example, due to counter overflow or missing STOP signal)
N		WW.	7	W.	Calibration is always performed at the end (for example, after a counter)
-1		My, Min	C	0,	overflow)
	6	PARITY_EN	RW	00 X	0: Parity bit for Measurement Result Registers* disabled (Parity Bit always 0)
		M.	1007		1. Parity bit for Measurement Result Registers enabled (Even Parity)
	.1		1.100	J.CO	*The Measurement Results registers are the TIME1 to TIME6, CLOCK_COUNT1 to CLOCK_COUNT5, CALIBRATION1, CALIBRATION2
	N		R/W	7	registers.
W.	5	TRIGG_EDGE	RW		0: TRIGG is output as a Rising edge signal
, ,		STOP_EDGE	R/W	0 41	1: TRIGG is output as a Falling edge signal
ON	4	STOP_EDGE \	1000	1003	Measurement is stopped on Rising edge of STOP signal Measurement is stopped on Falling edge of STOP signal
	3	START_EDGE	R/W	0	
				1100	Measurement is started on Rising edge of START signal Measurement is started on Falling edge of START signal
. ~	[2:1]	MEAS_MODE	R/W	00h	00: Measurement Mode 1 (for expected time-of-flight < 500 ns).
N.	OM		W.	W.	01: Measurement Mode 2 (recommended)
1	0 1	STADT MEAS	R/W	0	10, 11) Reserved for future functionality
100%	COL	START_MEAS	K/VV		Start New Measurement: This bit is cleared when Measurement is Completed.
70	1.0	1	*	N T	0: No effect
1100	11 C			NN	1: Start New Measurement. Writing a 1 will clear all bits in the Interrupt Status Register and Start the measurement (by generating an TRIGG signal) and will
N.100	oy.C	ON			reset the content of all Measurement Results registers (TIME1 to TIME6,
1	-01.		<	N	CLOCK_COUNT1 to CLOCK_COUNT5, CALIBRATION1, CALIBRATION2) to 0.
1	N.100	M.CO.M.T.		·	MAN TITON TON TAN
MA	000	COM	N		NAMA TOOK CONTIN
1	N.L	100 X COM	1		
NY	11.1	21 CO	T		MAN, 21700, COL, LAN
1	N. A.	1002. 401			TANNA 1007. CONT. TAN
M.	MIN	. It and . Co		. 1	M. M. M. Com. M.
1	My,	N.100A'CON	OM.		MANN TOOX CONTIN
		1007.	OM	TW	MAN TON TON THE
		-1 T		1	

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TDC7200 SNAS647D-FEBRUARY 2015-REVISED MARCH 201	TEXAS INSTRUMENTS www.ti.com
8.6.3 CONFIG2: Configuration Regis	ster 2 R/W (address = 01h) [reset = 40h] igure 23. Configuration Register 2
7 6 5 CALIBRATION2 PERIODS	4 3 2 1 0 AVG_CYCLES NUM_STOP
R/W-0h R/W-1h R/W-0h	
LEGEND; R/W = Read/Write; R = Read only; -n Table 3. C	= value after reset Configuration Register 2 Field Descriptions

	R/W-0h	R/W-1h	R/W-0h R/M	V-0h R/W-0h R/W-0h R/W-0h
	LEGEND: R	/W = Read/Write; R = Re	ead only; -n = value after	reset
		W. 1	able 3. Configurati	ion Register 2 Field Descriptions
.1	Bit	Field	Type Reset	Description
N	[7:6]	CALIBRATION2_PERIODS	R/W On the state of the state o	00: Calibration 2 - measuring 2 CLOCK periods 01: Calibration 2 - measuring 10 CLOCK periods 10: Calibration 2 - measuring 20 CLOCK periods 11: Calibration 2 - measuring 40 CLOCK periods
. N		ODS	Y. O. M.	01: Calibration 2 - measuring 10 CLOCK periods
TW		WW 31100	41 00	10; Calibration 2 - measuring 20 CLOCK periods
M.TW	[5:3]	ODS AVG_CYCLES	PAN OOH	
	[5.5]	AVG_CTCLES	DR/W JOHN	000: 1 Measurement Cycle only (no Multi-Cycle Averaging Mode)
		NW	100 x CO2	010: 4 Measurement Cycles
OM.T		N	RW 00H	011: 8 Measurement Cycles
			N.100 J.C.	400 40 Marshard Coules
COM		WW	100,	10; Calibration 2 - measuring 10 CLOCK periods 10; Calibration 2 - measuring 20 CLOCK periods 11: Calibration 2 - measuring 40 CLOCK periods 000: 1 Measurement Cycle only (no Multi-Cycle Averaging Mode) 001: 2 Measurement Cycles 010: 4 Measurement Cycles 011: 8 Measurement Cycles 100: 16 Measurement Cycles 101: 32 Measurement Cycles 110: 64 Measurement Cycles
Z.COM	1.		R/W N OOh	
J.CO.	[2:0]	NUM_STOP	2011	111: 128 Measurement Cycles 000: Single Stop 001: Two Stops 010: Three Stops 011: Four Stops 100: Five Stops 101, 110, 111: No Effect. Single Stop
), (R/W 00h	001: Two Stops
W.			11.10	001: Two Stops 010: Three Stops
JO .	CO. "		WW 3110	011: Four Stops
* UD »	40/2			001: Two Stops 010: Three Stops 011: Four Stops 100: Five Stops 101, 110, 111: No Effect. Single Stop
.70	1			101, 110, 111: No Επετι. Single Stop
A 1	7 3 1 1		ANN .	
M.	07.	M. W		W. OUX. ONL. THE WAY.
	S. C.			1N.100 1.CO 1.111
N	TOON.COM	T.COM.TW		001: Two Stops 010: Three Stops 101: Four Stops 100: Five Stops 101, 110, 111: No Effect. Single Stop
N	· You Y.	LCOM.TW		M. M
N.	N.100	CU		MAN, 100A, COW, LAN MAN, 10
	00	COM	N	MAN. 1001. COM. LA
	1		*	

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8.6.4 INT STATUS: Interrupt Status Register (address = 02h) [reset = 00h]	
Figure 24. Interrupt Status Register	
Figure 24. Interrupt Status Register	
7 6 5 4 3 2	0
Reserve Reserve Reserve MEAS_COMPLET MEAS_STARTED_FL_CLOCK_CNT_COARSE_CNTR_ N	IEW_MEAS_
d d d E_FLAG AG R_ OVF_INT	INT
OVENT	
R/W-0h R/W-0h R/W-0h R/W-0h R/W-0h R/W-0h	R/W-0h

			VV-UII	R/W-UII	R/VV-OII R/VV-OII
	LEGEND: R	/W = Read/Write; R = Read of			WW. OOX. CON.
~ 1	W.	Table	e 4. Interrupt St	atus Regi	ster Field Descriptions
N	Bit	Field	Туре	Reset	ster Field Descriptions Description
TW	7	Reserved	R/W	0h	N. M. Park
	6	Reserved	R/W	0h	NY 1100 1 CO' TY
	5	Reserved	R/W	0h	, Maria Contraction
M.TW	4	MEAS_COMPLETE_FLAG	RW CON	0h	Writing a 1 will clear the status 0: Measurement has not completed 1: Measurement has completed (same information as
		110	JOJ. CON		0: Measurement has not completed
OM.TW	N		100 RWCC		1: Measurement has completed (same information as NEW_MEAS_INT) Writing a 1 will clear the status 0: Measurement has not status
COM:L	3	MEAS_STARTED_FLAG CLOCK_CNTR_OVF_INT	R/W	0h	Writing a 1 will clear the status 0: Measurement has not started 1: Measurement has started (START signal received) Requires writing a 1 to clear interrupt status 0: No overflow detected
COR			1100	Oz	0: Measurement has not started
			N. O.		1: Measurement has started (START signal received)
N.COM	2	CLOCK_CNTR_OVF_INT	R/W	0h	Requires writing a 1 to clear interrupt status
0		N	1400	c0	0: No overflow detected
	OM.T			17.0	Writing a 1 will clear the status 0: Measurement has not started 1: Measurement has started (START signal received) Requires writing a 1 to clear interrupt status 0: No overflow detected 1: Clock overflow detected, running measurement will be stopped immediately Requires writing a 1 to clear interrupt status 0: No overflow detected 1: Coarse overflow detected running measurement will be
C	1	COARSE_CNTR_OVF_INT	R/W	0h _1 C	Requires writing a 1 to clear interrupt status
100,2	COM.			Oh	0: No overflow detected
M.100X	1.60		W.	You Y	1. Codies Cramen describe, running medicarement that so
W.100	10	NEW_MEAS_INT	R/W	0h	Requires writing a 1 to clear interrupt status 0: Interrupt not detected 1: Interrupt detected — New Measurement has been completed
1100				1101	0: Interrupt not detected
N. 100				M.	1: Interrupt detected - New Measurement has been completed
1	. T			113	100
NAM.	100,1.	COMM			1. Interrupt detected – New Measurement has been completed
W.	· To				in of continuity
	1 100	TO THE		MIN.	1100, CON LIN
	14.	07. COM.	N		W.100Y.COM.TW
W.	TW.I	COM.TW COM.TW OV.COM.TW	×1	M.	Tamerupi delecied - New Measurement has been completed.
	N	COM.TW			M. 100 A. COM. LAN MANN. 10 M. 100 A. COM. LAN MANN. 10 M. 100 A. COM. LAN MANN. 10
	WN.	My Coll			N.M. 100X. COM. L.M.
<		1100		4	AN TOUR CO' THE

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TDC7200 SNAS647D+FFF MAN 100X COM ooy.com.TW 8.6.5 INT MASK: Interrupt Mask Register R/W (address ± 03h) [reset = 07h]

Figure 25. Interrupt Mask Register

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	7	16	5	4	3	2.1		0
. 4	Reserve	Reserve	Reserve	Reserve	Reserve	CLOCK_CNTR	COARSE_CNT	_
V					1	_OVF_MASK	_OVF_MASK	_MASK
	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5. Interrupt Mask Register Field Descriptions

			<u> </u>	
N	Bit	Field	Reset	Description
N	7	Reserve	0 1	
	6	Reserve R/W	0	
	5	Reserve R/W	0	
	4	Reserve R/W	0	My Alibert Co. Ville
Nac CAN	3	Reserve R/W	0	
	2	CLOCK_CNTR_OVF_MASK R/W	1	0: CLOCK Counter Overflow Interrupt disabled
On L		1100	77	CLOCK Counter Overflow Interrupt enabled
aOM.	1	COARSE_CNTR_OVF_MASK R/W	1	0: Coarse Counter Overflow Interrupt disabled
CO		11 110		1. Coarse Counter Overflow Interrupt enabled
CON	0	NEW_MEAS_MASK R/W	1,000	0: New Measurement Interrupt disabled
				1: New Measurement Interrupt enabled
1100	Λ diaable	d interrupt will be longer be vibible or	tho dovice	e pin (INTB). The interrupt bit in the INT_STATUS
107.	register wi	Il still be active.	i me devid	e pin (into). The intenupt bit in the int status
11 C	TOGISTET WI	in aun de deuve.	1 (O. CO.
.007.	8.6.6 CO	ARSE_CNTR_OVF_H: Coarse Count	er Overflo	w High Value Register (address = 04h) [reset =
			A 112	

ooy.co? register will still be active. 8.6.6 COARSE_CNTR_OVF_H: Coarse Counter Overflow High Value Register (address = 04h) [reset = FFh]

Figure 26. Coarse Counter Overflow WWW.looy.co.

100,	8.6.6 COARSE_CNTR_	OVF_H: Coarse C	ounter Overflow	w High Value Regi	ister (address =	04h) [reset =	-10
30	FFh]		W. Tu		.1	W. 100	$_{1}C$
1100,	CONTAN	Figure 26. Coar	rse Counter Ov	erflow Value_H Re	egister	100	. (
M.	7.0	- E	211	2	1	01	N.
11.10	100	3	COARSE CNTR	OVF1H		10	10
	R/W-1h R/W-1h	R/W-1h	1	R/W-1h R/W-	1h R/W-1h	R/W-1h	00
	LEGEND: R/W = Read/Write;	R = Read only; -n = valu	ie after reset			N N	In
	100° CON			100, 400			.40
	Table	6. Coarse Counter	r Overflow Valu	e_H Register Field	d Descriptions	W.	N.L
	Rit Field	Tyr	no Poset	Description		- 1 N	7

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Table 6. Coarse Counter Overflow Value_H Register Field Descriptions

(• -	LEGEND:	R/W = Read	d/Write; R = Read only; -n	i = value afte	r reset		110.2
	100.	$\alpha(0)$				100 CON CON	130
S	. 10	1.0	Table 6. Coarse Co	unter Ove	erflow Val	ue_H Register Field Descriptions	M. M.T.
	Bit	Field		Туре	Reset	Description	
N	7-0	COARSE	_CNTR_OVF_H	R/W	FFh	Coarse Counter Overflow Value, upper 8 Bit	
4.	11.7	41	Co			100	
A1	N	100,	COMM		-1	My 1001. COM	
N	· IN	.70	1.0	41			
	IN	1100	CON 1			TAN TOOL COM	
		M.	W.			W. T. W. T. C. W. T.	
	MAN	11	10 CO			MM, 1100, 100, 12	
	7	MN.	any.	· N		M. O. O.	
	<1°						

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on com.Tw 8.6.7 COARSE_CNTR_OVF_L: Coarse Counter Overflow Low Value Register (address = 05h) [reset = FFh]

Figure 27. Coarse Counter Overflow Value L Register

MMM Jun x.

١.								
	A A	6	5	4	3	2	1	0
		1 C		COARSE_C	NTR_OVF_L	41		
	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; n = value after reset

Table 7. Coarse Counter Overflow Value_L Register Field Descriptions

Bit	Field	.007.		Type	Reset	Description
7-0	COARSE_C	NTR_OVF_L		R/W	FFh	Coarse Counter Overflow Value, lower 8 Bit
		100 7	CC	N. P.		Note: Don't set COARSE_CNTR_OVF_L to 1.

8.6.8 CLOCK_CNTR_OVF_H: Clock Counter Overflow High Register (address = 06h) [reset = FFh]

Figure 28. CLOCK Counter Overflow Value_H Register

	Figure 28. CLOCK Counter Overflow Valu	a H Pagistar
	rigule 20? CLOCK Counter Overnow valu	e_II Register
7	6 5 4 3	2 1 0
	CLOCK_CNTR_OVF_H	100, 60,
R/W-1h	R/W-1h R/W-1h R/W-1h	R/W-1h R/W-1h R/W-1h
LEGEND: R/V	V = Read/Write; R = Read only; -n = value after reset	1100,100
	N. O. O. O. O.	
1 Co	Table 8. CLOCK Counter Overflow Value_H Regist	er Field Descriptions
Bit	ield Type Reset Description	1007

() N	LEGEND: R/	/W = Read/Write;	R = Read only; -n	⇒ value after	reset			1 100
				00%		1.		4.
J.Co.		Table	8. CLOCK Co	unter Ove	rflow Va	lue_H Register Fie	eld Descriptions	-N.100 -1 C
0	Bit	Field		Туре	Reset	Description		100,
	7-0	CLOCK_CNTR_C	OVF_H	R/W	FFh	CLOCK Counter Over	rflow Value, upper 8 E	Bit
00	OF 1		N IN	110	0	10 h	<u> </u>	1100,
201	8.6.9 CLC	OCK_CNTR_C	VF_L: Clock	Counter C	verflow	Low Register (add	lress = 07h) [res	et = FFh]
100	CO		Figuro 20	CLOCKIC	ounter C	verflow Value_L R	logistor :	110°
003	NO.	1.	Figure 29.	CLUCK	ounter C	vernow value_L R	egistei	N. T. W.

			11/1.		•	4.			
J.CO.		Table 8. CL	OCK Counter Ov	erflow Valu	ue_H Register	Field Descri	ptions	100 1 C	Or V
CC	Bit Fiel	ld	Туре	Reset	Description			100	COM
ay.	7-0 CLC	OCK_CNTR_OVF_H	R/W	FFh	CLOCK Counter	Overflow Value,	upper 8 Bit	N.J.	
00				30 - 1 C	Or any			1100	1 COR
100	8.6.9 CLOCI	K_CNTR_OVF_L	: Clock Counter	Overflow L	ow Register ((address = 07	'h)	FFh]	1.
70		Fig	ure 29. CLOCK (Counter Ov	erflow Value	L Register		1, 10,	C
1100	109	6	5	41 100	30	2	1 4	0	00, 1
M.			Cl	LOCK_CNTR	OVF_L				OOY.
- N.10	R/W-1h	R/W-1h	R/W-1h R/N	W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	100
N	LEGEND: R/W =	Read/Write; R = Rea	ad only; -n = value afte	r reset	001. CC	Mr. WA			100
	T. C.	Toble 0. Ol	OCK Counter Ov	anglater Val	us I Baristar	Field Deseri	milana	N	W.I.
	1		OCK Counter Ov		100-	rieid Descri	puons		110
	Bit Fiel	ld	Туре	Reset	Description		1		ATN.

Table 9. CLOCK Counter Overflow Value L Register Field Descriptions

170	R/W-1h	R/W-1h	R/W-1h	R/W	-1h-1	R/W-1h R/W-1h	R/W-1h	R/W-1h	1 100
1	LEGEND: R/W =	Read/Write; R =	Read only; -n = valu	ie after	reset	007.			W. OU
(1)	100		4	W.	1	1 CO 1		W.	11.100
	100,1	Table 9.	CLOCK Counte	r Ove	rflow Val	ue_L Register Field	Descriptions		
	Bit Field	d	Ty	эе 🖷	Reset	Description	1	N	J. W.J.
di.	7-0 CLC	OCK_CNTR_OVF	L R/	٧	FFh	CLOCK Counter Overflow	Value, lower 8 Bit		
	11.002		N	•	4	11.	ONL.		W.
M.	- N. 100	1 CO			M	1 100 cl C	O' The		W
1	W VOI	0_{J}			-1	W. 1007.	COM	N	
M	TW.LO				N	IN. IV		-1	W.
	NIN 11	00,	Die			100	COA		
	W.	007.		1		W. To ac	N. OW.		
	WW.	1.100				WW W.10	1 00		
		1007	dON.	N.			007. 001	T.	
		170							

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TDC7200 SNAS647D+FEP-VW.100Y.CU. ooy.coM.TW 8.6.10 CLOCK_CNTR_STOP_MASK_H: CLOCK Counter STOP Mask High Value Register (address = 08h) [reset = 00h]

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Figure 30. CLOCK Counter STOP Mask_H Register

	X X	6	5	4	3	(2)	1	0
4		27 (CLOCK_CNTR	_STOP_MASK_H	100		
	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. CLOCK Counter STOP Mask_H Register Field Descriptions

Bit Field	1.	Туре	Reset	Description	007.	ON.	N.
7-0 CLOCK_CNTR_STO	P_MASK_H	R/W	0	CLOCK Counter STOP M	lask, upper 8 Bit		LA.

8.6.11 CLOCK_CNTR_STOP_MASK_L: CLOCK Counter STOP Mask Low Value Register (address = 09h) Figure 31. CLOCK Counter STOP Mask_L Register

		F:	N OOK O	CTOD Maste	1 30	.1	
N. AN		Figure 31. C	LUCK Count	er STOP Mask_	L Register		
7	6	1 5 1		2	2	<1 A	1 (0)
		3	CLOCK CNTR	STOP MASK I	2	00	
R/W-0h	R/W-0h	R/W-0h	1 R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
	W = Read/Write; R =	Read only; -n = va			1411 211	N	0, 0
	W.				N	N.J.	
CONTAIN	Table 1	. CLOCK Co	unter STOP M	ask_L Register	Field Descrip	tions	100,20
Bit	Field	Т	ype Reset	Description		N TIN	
7.0	CLOCK CNTP STOE	MASKI	DAW 0	CLOCK Count	or STOP Mack Joy	or 9 Bit	1100

R/W-0h R/W-0h R/W-0h R/W-0h R/W-0h R/W-0h	R/W-0h	R/W-0h	
LEGEND: R/W = Read/Write; R = Read only; -n = value after reset	111	0_{2} 0_{2}	
	N. W.Y.		
Table 11. CLOCK Counter STOP Mask_L Register Field Desc	criptions	100° CC	
Bit Field Type Reset Description	TIN.		ON.
7-0 CLOCK_CNTR_STOP_MASK_L R/W 0 CLOCK Counter STOP Mask,	, lower 8 Bit	1100	
		1007	CON
8.6.12 TIME1: Time 1 Register (address: 10h) [reset = 00_0000h]	W.	1.10°	
Figure 32. TIME1 Register		13, 100,	CC
			1.0
23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	5 4 3	2 1 0	0 >

Figure 32. TIME1 Register

										4 8 8 9	
100	7-0	CLOCK_CNTR_	_STOP_MAS	SK_L R/W	0.1 C	CLOCK Counter S	TOP Mask, lo	ower 8 Bit		U	CO
10.1. ~	Olyman				0.	ON. W				.007	
	8.6.12 TI	ME1: Time 1	Register	(address: 10h)	[reset = 0	00_000h]	4		11.	1.10	41 CO
100,2	COL			Figure	32 TIME	1 Register	N			200	7.
				119010	02. IIIVIL	Thegister	1		11,	11.10	
1100	23	22 21 20	19 18 1	17 16 15 14	13 12	11 10 9 8	7 6	5 4	3 2	1 0	00 -
W.	Parity Bit		1	Measurement Res	ult: 23 bit inte	eger value (Bit 22: M	SB, Bit 0: LS	B)	11.		
110	R-0 / F	R-0 R-0 R-0	R-0 R-0 R	1-0 R-0 R-0 R-0	R-0 R-0	R-0 R-0 R-0 R-0	R-0 R-0	R-0 R-0	R-0 R-0	R-0 R-0	100,
TIN .	LEGEND: R	/W = Read/Write	; R = Read o	only; -n = value afte	r reset	-01		1			1.1
11		10°			N 11	00					1100
M.	00%	ON.		Table 12. TIME	1 Registe	r Field Descripti	ions				M.x
	Bit	Field	3	Туре	Reset	Description	0, 1			N	110
	23	Parity Bit		R	0	Parity Bit	101				

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Table 12. TIME1 Register Field Descriptions

1U'	R-0	R-0 R-0 R-0 R-0 R-0	0 R-0 R-0 R-0 R-0	R-0 R-0	R-0	. 4 (10)
To.	LEGEND: F	R-0	ead only; -n = value after	r reset	R-0	N.1007
411	00	CON		1		, 100,
M.	00%		Table 12. TIME	1 Register	Field Descriptions	IN.
	Bit	Field	Type	Reset	Description 1	1 10
MA	23	Parity Bit	R	0	Parity Bit	
-1	23	Measurement Result: 23	B bit integer R	0	Measurement Result	1
IN		Measurement Result: 23 value (Bit 22: MSB, Bit 0): LSB)		TOWN COMPANY	
			- 7		MM.1007.COM.TM	11
	1	100, 1 CO.		₹ N	W. 1100, COR. LA	
		100 1. CON.	M.		WWW.100X.COM.TW	
4	MAN	11.100 1 CO		4	MAN TO STOOM TON	
		1007	ON. W		TAN TOO TOOM	
	M.	W. N. J.			MMM 1001. COMILIA	
	W	N 100 x	COM		TW 1003 CONTRA	
		M.1007.CO.	CONTA	~ I	MMM.100X.COM.LM	1
	41	MM. 1007	CONT	L	1007. COM. TW	

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M.M. 100 A. C.O.M. 8.6.13 CLOCK_COUNT1: Clock Count Register (address: 11h) [reset = 00_0000h] Figure 33 CLOCK C

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23	22	<i>)</i> 71	20	/19	18	17	16	15	14	13	12	11	10	19	8	7	6	5	4	3	2	1	0
Parity B	it	100	1	4		*							C	LOCK	_co	JNT1	Resu	lt \	7.		1		
R-0	R	0 R-0	R-01	R-0 ◀	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. CLOCK_COUNT1 Register Field Descriptions

1		~		
Bit	Field	Type	Reset	Description
23	Parity Bit	Ŕ	0	Parity Bit
22-16	Not Used	R	0	These bits will be used in Multi-Cycle Averaging Mode in order to allow higher averaging results.
15-0	CLOCK_COUNT1 Measurement Result	R	0	CLOCK_COUNT1 Measurement Result

TIME2: Time 2 Register (address: 12h) [reset = 00_0000h]

Figure 34. TIME2 Register

	15-0	CLOCK_	COUNT1 Me	easurement /	R	0	CLOCK	_COUN	IT1 Mea	asureme	nt Result	121				
		Result		001.						111		12.		12.		
				100					1		130	∠ 1	Co.	. ()		
NEW	8.6.14	TIME2: T	ime 2 Re	gister (addre	ess: 12h)	[reset =	00_000	0h]			14.	00	40	Mr.	M	
	-1			1.70	Figure :	MIT NO	E2 Bogi	ctor				100	10	_ [4
Ober	N			100	rigure .	34. × 1 IIVI	LZ Negi	SIGI			1	00	7.	10 K		N
	23	22 21	20 19	18 17 16	15 14	13 12	11 10	9	8	7 6	5	4 3	2 1 1	0		
COR	Parity Bit			Measur	ement Resu	lt: 23 bit ir	teger valu	e (Bit 22	2: MSB,	Bit 0: L	SB)	`	10 2	_<0	The same of	
No.	R-0	R-0 R-0	R-0 R-0	R-0 R-0 R-0	R-0 R-0	R-0 R-0	R-0 R-0	R-0	R-0 F	R-0 R-0	R-0 F	R-0 R-0	R-0 R	0 R-0		
COR	LEGEND:	R/W = Rea	d/Write; R =	Read only; -n =	value after i	reset		N				14.	100		Olas	
1.0		~ 1		· N.				.41			14.		. 1	W.		
1,00				Table 1	4. TIME2	Registe	er Field	Descri	iption	S		M.	10	10 .	COE	
	Bit	Field			Туре	Reset	Descri	otion	N				M.	200		N
	22 4	Parity Rit			P = 1	0	Parity F	it.	4			3177	.4 '	100	- 0	J > .

Table 14. TIME2 Register Field Descriptions

-	_ /	- IX O _ X \	10 10 10 10 10	, , , , , , , , , , , , , , , , , , , ,	11.0	TO ROTE ROTE	A ILO INDIATO I		
. (Oh	LEGEND: F	R/W = Read/Write; R = Re	ad only; -n = value afte	er reset			00, 00	N. P.
		1.		TIN.	1.0		M. M.		-N.
) · ∡1	CO			Table 14. TIME	2 Registe	r Field Descriptions		1100	$O_{N_{i}}$
10,	•	Bit	Field	Туре	Reset	Description		4. 003	AO.
	4.0	23	Parity Bit	R	0	Parity Bit		1 100	Co.
100		22-0	Measurement Result	R	00	Measurement Result		100	· aC
. 1					.10			T. N. I.	1.0
.11	00 ,	8.6.15 C	LOCK_COUNT2: CI	ock Count Regis	ter (addre	ss: 13h)	00h]	11 100	
$M \cdot $		1.0	M. V	Figure 35.	CLOCK C	OUNT2 Register		No. Le	any.
. 1	100		J' (1)	35					n_{α}
	1.	23	22 21 20 19 18	17 16 15 14	13 12	11 10 9 8 7 6	5 4 3	2 1 0	
	- 41	De la Principia de	~			OLDOVE COUNTS			. (7)

8.6.15 CLOCK_COUNT2: Clock Count Register (address: 13h) [reset = 00_0000h]

Figure 35. CLOCK_COUNT2 Register

8.6.15 CLOC	K_COUNT2: Clock Co	ount Register (address: 13	h) [reset = 00_0000h]		1007.
W. TOON. COM	F	Figure 35. CLOCK_COUNT	2 Register		Y.YouY.
23 22	21 20 19 18 17	16 15 14 13 12 11	0 9 8 7 6 5	4 3 2 1	0
Parity Bit R-0 R-0	R-0 R-0 R-0 R-0 F	R-0 R-0 R-0 R-0 R-0 R	CLOCK_COUNT2 -0 R-0 R-0 R-0 R-0 R	R-0 R-0 R-0 R	-0
LEGEND: R/W =	Read/Write; R = Read only;	-n = value after reset	CONT		W , 10
WW 100 1	Table 15.	CLOCK_COUNT2 Register	Field Descriptions		WW
Die Char		Type Beest Dees	dination (Continuity		

Table 15. CLOCK_COUNT2 Register Field Descriptions

>	R-0 F	2-0 P-0 P-0	P-0 P-0 P-0 P-0	P-0 P-0	P-0 P-0	R-0	
L		7 1 2 7	A TOTAL CONTRACTOR OF THE PARTY			14-0 14-0 14-0 14-0 14-0 14-0 14-0 14-0	. 0
1	LEGEND: R	/W = Read/Write	e; R = Read only; -n =	value after	reset	100	10
	00.	7. OB					10
	1 100	-1 CO	Table 15. CL	OCK_CC	DUNT2 Re	gister Field Descriptions	-11A
11	Dit O	Hadd (- 1		$\cdot M \cdot$
7	-17	Field	1	Туре	Reset	Description	'
	23	Parity bit	-1	R	0	Parity Bit	
1	22-16	Not Used	Ober	R	0	These bits will be used in Multi-Cycle Averaging Mode in order	W.
4				.1		to allow higher averaging results.	
	15-0	CLOCK_COUN	IT2 result	R	0	CLOCK_COUNT2 result	1
				.1	•		N.
		N. 1005	1001 COM			MANN TOOX COM LAN	`
			41 U			1 0	
			U. July			The contract of the contract o	
	N	1 10	A TOO A COL			MANN:100X.COM:LA	
					N.		
			(00 CO)			100, 60, 41	
		1111			~ 1		
			100, 40				
					-1		
		NAMA	A:100 A:CO	OM		MMM.100A.COM.LM	
			1170				



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8.6.16 TIME3: Time 3 Register (address	14h) [reset = 00 gure 36. TIME3	1100	N.TW	
23 22 21 20 19 18 17 16 1	14 13 12 11	10 9 8 7 6	5 4 3 2 1	0
Parity Bit Measureme	nt Result: 23 bit intege	r value (Bit 22: MSB, Bit 0: LS	SBI	
R-0	R-0 R-0 R-0 R-	0 R-0 R-0 R-0 R-0	R-0 R-0 R-0 R-0 R-0) R-0
LEGEND; R/W = Read/Write; R = Read only; -n =-val	e after reset	100	COMMEN	

K-0 K-0 K-0 K-0 K-0 K-0 K-0	7 K-0 K-0	K-0 K-0	K-0									
LEGEND; R/W = Read/Write; R = Read only; -n	= value after	reset	1001. COM									
Table 16. TIME3 Register Field Descriptions												
Bit Field	Type	Reset	Description									
23 Parity bit	R	0	Parity Bit									
22-0 Measurement result	R	0	Measurement Result									

8.6.17 CLOCK_COUNT3: Clock Count Registers (address: 15h) [reset = 00_0000h]

Figure 37. CLOCK_COUNT3 Count Register

<u> </u>	22-0	Measurement	result	R	0 1	Measurem	ent Result	N.L.	41.0		1
			100	40 h			-11	. 1	00,	017	N
	8.6.17	CLOCK_COU	NT3: Clock (Count Regis	ters (addr	ess: 15h)	[reset =	00_0000	h]		
			1100 Fic	ure 37. CL	OCK COL	INT3 Cour	nt Redis	tor	100	COR	
M. XI	[7	N.	Juic 37. OL		1	it ivedia	101	1.5	·	
	23	22 21 20	19 18 17	16 15 1	4 13 12	11 10	9 8	7 6	5 4 3	2 1 0	
	Parity Bit	t					CLOCK_0	COUNT3	N.		
0' 1	R-0	R-0 R-0 R-0	R-0 R-0 R-0	R-0 R-0 R-	0 R-0 R-0	R-0 R-0 I	R-0 R-0	R-0 R-0	R-0 R-0 R-	0 R-0 R-0 R-0	
· OD	LEGEND	: R/W = Read/Writ	e; R = Read only	/; -n = value aft	er reset						
CO	1.4.			100	CO	C. A.			41	100), (J
			Table 17	. CLOCK_C	COUNT3 R	egister Fie	eld Desc	riptions	W.	1007.	ON.
1.00	Bit	Field	W.	Туре	Reset	Description	n	-	W.	V.100	
	- 00			2.0		5					

	- C	R-0	R-0 R-0 R-0	R-0 R-0 F	R-0 R-0 R-0 R-	0√R-0 I	R-0 R-0 R-0 R-0 R	-0 R-0 R-0 R-0	0 R ₇ 0 R-0	' R-0 R-0 R-0	0	
C C	Mr.	LEGEND: F	R/W = Read/Writ	te; R = Read	only; -n = value aft	er reset			W.	004.0	OW.	
	101	N. P. W.		Table	17. CLOCK_C	OUNT	Register Field De	escriptions	MIN.	100 X.C	a ON	1.1
4.		Bit	Field	111,	Туре	Reset	Description					~ ()
	. 6	23	Parity bit		R	0	Parity bit			100		17.
00		22-16	Not Used		R	0.	These bits will be to allow higher av	used in Multi-Cyc eraging results.	le Averaging	Mode in order	1.0	MO.
		15-0	CLOCK_COU	NT3 Result	R	0	CLOCK_COUNT	3 Result	di.	T.N.L.	1.	
10		1 602				100	CON			11	n_{r}	CC
•	00	8.6.18	IME4: Time	4 Registe	r (address: 16	h) [rese	t = 00_0000h]			- TW-2		
N.	100	oy.Co.	MIT	N	Figur	e 38. T	IME4 Register		~	WW	700	1.0
	134	23	22 21 20	19 18	17 16 15 14	1 13 1	12 11 10 9	8 7 6 5	4 3	2 1 0	1 (0)	0
N	14.	Parity Bit	ON		Measurement Re	sult: 23 b	it integer value (Bit 22:	MSB, Bit 0: LSB)			11.	00
7	1	R-0_1	R-0 R-0 R-0	R-0 R-0 F	R-0 R-0 R-0 R-	0 R-0 J	R+0 R-0 R-0 R-0 R	-0 R-0 R-0 R-	0 R-0 R-0	R-0 R-0 R-0) 411	100
		LEGEND E	NV - Read/Writ	P R - Read	only: -n - value aft	or rocot	N 01.		1		-1 N .	-

8.6.18 TIME4: Time 4 Register (address: 16h) [reset = 00_0000h] Figure 38. TIME4 Register 23	15-0 CLOCK_COUNT3 Result R 0 CLOCK_COUNT3 Result	M. M. To
Figure 38. TIME4 Register 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 Parity Bit	100, CO. LA	100, 00
23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	8.6.18	W. F. CO.
Parity Bit Measurement Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB) R-0	Figure 38. TIME4 Register	WW.100 X.
R-0	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5	4 3 2 1 0
LEGEND: R/W = Read/Write; R = Read only; -n = value after reset Table 18. TIME4 Register Field Descriptions	Parity Bit Measurement Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)	7
Table 18. TIME4 Register Field Descriptions	R-0	0 R-0 R-0 R-0 R-0
	LEGEND: R/W = Read/Write; R = Read only; -n = value after reset	N
Bit Field Type Reset Description	Table 18. TIME4 Register Field Descriptions	
	Bit Field Type Reset Description	

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Table 18. TIME4 Register Field Descriptions

\mathcal{F}	11 02			11 0	11 0 11 0	to hother he he he he he he	21
Ī	LEGEND: R	R/W = Read/V	/rite; R = Read only; -n =	value after	reset	ON ON	N. O.
1	10	1.00				The st Co. Williams	1130
	100	40	Table 1	8. TIME4	Register	Field Descriptions	TAN TO
1	Bit	Field	-N- 1	Туре	Reset	Description	
1	23	Parity bit	Or TW	R	0	1100, COLTA	
	22-0	Measureme	nt result	R	0	Measurement result	
		100	CO		N	100, 17	AN IN
		00	· CON .	N		TAN TON TON	
1	1	1.70	1.00	.1	~	N AND A CO	
		101				1M 100 1 COM	
	44.		W.	. 1		W. IN. IO OX. CO ON. I	
		N 11	00 , CO_{2}			100 CON TW	
					1	TIN . TO THE STATE OF THE STATE	
	<		100 × 100			MAN 100 CON LAN	

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MM.1007.COM. 8.6.19 CLOCK_COUNT4: Clock Count Register (address: 17h) [reset = 00_0000h]

Figure 39. CLOCK_COUNT4 Count Register

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	23	13	22 21	20	19	18	17	16	15	14	13	12	11	10	19	8	7	6	5	4	3	2	1	0
Į	Parity B	it	40	0.2.	. <		*								CLC	OCK_	COUN	T4		7.		1		
	R-0	R	-0 R-	0 R-(0 R-0	R-0◀	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0						

LEGEND; R/W = Read/Write; R = Read only; -n = value after reset

Table 19. CLOCK_COUNT4 Register Field Descriptions

			~		
	Bit	Field	Туре	Reset	Description
	23	Parity bit	Ŕ	0	Parity bit
	22-16	Not Used	R	0	These bits will be used in Multi-Cycle Averaging Mode in order to allow higher averaging results,
ŀ	45.0	STORY COUNTY OF II) × (1	0	
	15-0	CLOCK_COUNT4 Result	R	90	CLOCK_COUNT4 Result

TIME5: Time 5 Register (address: 18h) [reset = 00_0000h]

Figure 40. TIME5 Register

						U .	0 0				
	15-0	CLOCK_COUNT	Γ4 Result	R 0	CL	OCK_COUNT	4 Result	11.10			
			100	COL			TIN .	100	901		
1	8.6.20	TIME5: Time 5	Register (add	ress: 18h) [r	eset = 00_	_0000h]	di.	TW.10	4.0		<1
	.1	WW	100	Figure 40	. TIME5 F	Register	W	N 110	O TO		
Obra	23	22 21 20	19 18 17 16	15 14 1	3 12 11	10 9	8 7	6 5 4	3 2	1 0	CN
	Parity Bit		Meas	urement Result:	23 bit integer	value (Bit 22:	MSB, Bit	0: LSB)			
CO	R-0	R-0 R-0 R-0 I	R-0 R-0 R-0 R-	0 R-0 R-0 R	-0 R-0 R-0	R-0 R-0 F	R-0 R-0	R-0 R-0 R-0	R-0 R-0 R	-0 R-0	
	LEGEND:	R/W = Read/Write	; R = Read only; -n	= value after res	set				1.2		
1 CO	L. A.		AN -1	100	30,			A TOWN	1100	100	
7.	Mr.	N	Table	20. TIME5 R	egister Fi	eld Descri _l	otions		M.	07.	O.
	Bit	Field	M	Type R	eset De	escription	.4		1.17	,	
700 x	23	Parity bit		R . 0	Pa	rity Bit				00	

Table 20. TIME5 Register Field Descriptions

•		LEGENE	: R/W = Re	ead/Write; R =	Read on	ly; -n = '	value after	reset		1			N_{\bullet}	100		
.1	10,			<	M.	-11	00	. ())			N	1	100	0) ×
	<u>م</u>	W.	N		Ţ	able 2	0. TIME:	5 Regi	ster Fie	eld Description	ons		JW	00		ON.
		Bit	Field		W.		Туре	Reset	De	scription		11		N. 100		
00		23	Parity b	oit	4 1	11	R	0	Pai	rity Bit			N I	40	10.	
	N.	22-0	Measu	ement result		\ \ \ \	R	0	Me	asurement result	×1					1.0
10	0	COE					-1	100	10	Or W				N	100	·
•	003	8.6.21	CLOCK	_COUNT5:	Clock	Count	Regist	er (ad	dress: 1	19h) [reset =	00_0000h	1]			• *	
N.	100	N.C.			Fi	gure 4	II. CLO	CK_C	OUNT5	Count Regis	ster		<	MA	W.1	
	110	23	22 21	20 19	18 17	16 -	15 14	131	12 11	10 9 8	7 6	5 4	3	2 1	0	100
	4.	Parity Bi	t				-41	111	00	CLOCK	COUNT5	1		7	1	
4	1	R-0	R-0 R-0	R-0 R-0	R-0 R-0) R-0	R-0 R-0	R-0	R+0 R-0	R-0 R-0 R-0	R-0 R-0	R-0 R-0	R-0	R-0 R-0	R-0	1100
_		LECEND	DAM D	ad/Mita. D	Jan an		value ofter	و المحمدة				~ 1			-1	

8.6.21 CLOCK_COUNT5: Clock Count Register (address: 19h) [reset = 00_0000h] Figure 41. CLOCK_COUNT5 Count Register 23	-01.0	22-0 Measu	rement result	R	0	Measurement re	sult			N.Y	1.0
Figure 41. CLOCK_COUNT5 Count Register 23	100	CONT			1100	CON				1100	- CC
23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 Parity Bit R-0	· any	8.6.21 CLOCK	_COUNT5: Clo	ock Count Re	egister (addr	ess: 19h) [reset	= 00_0000h]			1110	
Parity Bit CLOCK_COUNT5 R-0 R-0	W.100	Y.Co. M.		Figure 41.	CLOCK_CO	UNT5 Count Re	gister		MA	. W.1	30.
R-0	11 100	23 22 21	1 20 19 18	17 16 15	14 13 12	11 10 9	8 7 6	5 4	3 2	1 0	100
LEGEND: R/W = Read/Write; R = Read only; -n = value after reset Table 21. CLOCK_COUNT5 Register Field Descriptions	NN	Parity Bit			N.	CLO	CK_COUNT5				003
Table 21. CLOCK_COUNT5 Register Field Descriptions	13	R-0 R-0 R-	0 R-0 R-0 R-0	R-0 R-0 R-0	R-0 R-0 R-0	0 R-0 R-0 R-0 F	R-0 R-0 R-0 R	-0 R-0	R-0 R-0	R-0 R-0	1100
		LEGEND: R/W = Re	ead/Write; R = Rea	d only; -n = valu	e after reset	.007.	ON	N			14.
	N	70		.1	W.	1.10				M.	11.10
Bit Field Type Reset Description		100 1	Tab	le 21. CLOCI	K_COUNT5 F	Register Field D	escriptions	N		1	
	W.	Bit Field		Тур	e Reset	Description	I. M		1		TW.

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Table 21. CLOCK_COUNT5 Register Field Descriptions

≫L	11 0	10 110 110	tto ito ito ito	11 0 11 0	11 0 11 0	RO RO RO RO RO RO RO RO RO	
	LEGEND: R	/W = Read/Write	e; R = Read only; -n =	value after	reset	TON COMP.	1.
1	To	1.0					N.J.
_	100	COR	Table 21. CL	OCK_CO	UNT5 Re	gister Field Descriptions	
1	Bit	Field		Туре	Reset	Description	N.
N	23	Parity bit	7.	R	0	Parity bit	W.
4	22-16	Not Used	W. W	R	0	These bits will be used in Multi-Cycle Averaging Mode in order	
1		Si 201/ 21/1		_		to allow higher averaging results.	
L	15-0	CLOCK_COUN	T5 Result	R	0	CLOCK_COUNT5 Result	1
		v.100	CO		4	NA NATURAL CONTRACTOR	N
		100	COM			TAN TOOK COME	
	111,	W.L	J. Comment	1		W. M. Joseph Co. M. T. M.	
		10				TAN TOO TO COLUMN	
		TW.Le	N1		.1	W. T. W. T. C. C. T.	
		1	rooxicon			TAN TOO TON	
					. 1	W. TW. T. C.	
		WW.	100 A . CO.	Jy 1		M.M.M. 1007. COM. I.M.	

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TDC7200 CONTIN	TEXAS INSTRUMENTS
SNAS647D - FEBRUARY 2015 - REVISED MARCH 2016	6 www.ti.com
8.6.22 TIME6: Time 6 Register (addr	ress: 1Ah) [reset = 00_0000h] Figure 42. TIME6 Register
23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Parity Bit Measu	rement Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)
R-0 R-0 R-0 R-0 R-0 R-0 R-0 R-0	0 R-0 R-0 R-0 R-0 R-0 R-0 R-0 R-0 R-0 R-
LEGEND; R/W = Read/Write; R = Read only; -n :	= value after reset

THE RESIDENCE TO THE RESIDENCE TO THE RESIDENCE	RO RO RO RO RO RO RO RO
LEGEND; R/W = Read/Write; R = Read only; -n = value after reset	1001. CONT.
Table 22. TIME6 Register	Field Descriptions
Bit Field Type Reset	Description
23 Parity bit R 0	Parity Bit
22-0 Measurement result R 0	Measurement result

8.6.23 CALIBRATION1: Calibration 1 Register (address: 1Bh) [reset = 00_0000h]

Figure 43. CALIBRATION1 Register

8.6.23 CALIBRATION1: Calibration 1 Register (address: 1Bh) [reset = 00_0000h] Figure 43. CALIBRATION1 Register 23	-1	22-0	Measurem	ent result	1.0	R 0	Mea	surement re	esult			1
Figure 43. CALIBRATION1 Register 23				1100	CC			.4		100	Or al	N
23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 Parity Bit R-0		8.6.23	CALIBRAT	JON1: Cali	ibration 1	Register (ad	dress: 1B	າ) [rese	t = 00_000	0h]		<u>~1</u>
Párity Bit CÁLIBRATION1 R-0	1.TW		WY	W.1	Fig	ure 43. CAL	IBRATION	1 Regist	ter	W.100	CON	
R-0		23	22 21	20 19 18	17 16	15 14 13	12 11	10 9	8 7 6	5 5 4 3	2 1 0	
LEGEND: R/W = Read/Write; R = Read only; -n = value after reset Table 23. CALIBRATION1 Register Field Descriptions		Parity Bit			• •		CALIBRATION	DN1		ATN.		
Table 23. CALIBRATION1 Register Field Descriptions		R-0	R-0 R-0 F	R-0 R-0 R-0	0 R-0 R-0	R-0 R-0 R-0	R-0 R-0	R-0 R-0	R-0 R-0 R-	-0 R-0 R-0 R-	0 R-0 R-0 R-0	
	COM	LEGEND:	: R/W = Read/	Write; R = Re	ead only; -n =	value after rese		N			004.00	Min
	COM		I .	Ta	able 23. C	ALIBRATION	11 Registe	Field D	escription	s	LOON.	OM
Bit Field Type Reset Description	1.00	Bit	Field	N		Type Res	et Desc	ription		N	1.10	

		R-0	R-0 R-0	R-0 R-0	R-0 R-0	R-0 R-0	R-0 R-0	R-0 R	-0 R-0 R-0	<u>) R-0</u>	R-0 R-0	R-0 R-0	R-0 I	R-0 R-0	R-0		1
	Mr.	LEGEND:	R/W = Rea	nd/Write; R :	= Read only	y; -n = value	after reset	M.				M.			70	1.	4
C) ′	LA			N 3	100	.1 CU	* * *	LA.			M.	1 10	1	CO_{\flat}		
	ON,				Table 2	23. CALIB	RATION	1 Regi	ster Field	Descr	iptions		N.	OOY.	,	W.	*
1.		Bit	Field	4		Туре	Res	et l	Description	1	4		M.	10	1.0		
) "	CO	23	Parity Bl	t		R	JU 0		Parity Bit	N			14.	100		40 D	>
0		22-0	CALIBRA	ATION1		R	0		Calibration 1	Result: 2	23 bit integ	er value (l	Bit 22: N	ISB, Bit 0:			J
20	.1 (D>	CAL				100,	10	LSB)	114			IN	1	20	- CC	7
				TIONS	0 111 41		20			. 45	1		1	IN	200		
10	-1	8.6.24	CALIBRA	AHON2: (Calibrati	on 2 Regi	ster (ad	dress:	1Ch) [res	set = 0	u_0000h)]	N	-1	100	1	V
• ′	007	· ~ ~ ~	Me	N	,	Figure 4	14. CAL	IBRAT	ION2 Regi	ister	N			N		W.	
N.	In.	1 22	22 21	20.<119	18 17	16 15	14 13	12 -1	1 10 0		7 6	E 1	2	2 1		3 ℃	
4,	100	Dority Dit		20 19	10 17	10' 15	14 13	CALIDO	ATIONS	0	100	<u> </u>	<u> </u>	2	U ·	.00	r.

100,	90/2		N		Figure 44.	CALIBR	ATION2 R	egister	N				00,
M. I	23	22 21	20 19	18 17	16 15 1	13 12	11 10	9 8	7 6	5 4	3 2	1 0	V
1100	Parity Bit	J			N	CAL	JBRATION2	OF	111		- 1	1	1100
NN.	R-0 I	R-0 R-0	R-0 R-0	R-0 R-0	R-0 R-0 R-	0 R-0 R-0	R-0 R-0	R-0 R-0	R-0 R-0	R-0 R-0	R-0 R-0	R-0 R-0	4.2
1	LEGEND: R	R/W = Read	d/Write; R =	Read only	y; -n = value aft	er reset	100	Co					100
	100%.	~O]		N			00	30	Nr.	N.			11.
N	70	1.00		Table 2	4. CALIBRA	TION2 R	egister Fie	ld Descr	iptions			M.	11.1
	Bit	Field ~	$O_{\Sigma_{i}}$	TN	Туре	Reset	Descripti	on	Ozz	CN			M

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Write: R = Read only; -n = value after reset Table 24. CALIBRATION2 Register Field Descriptions

-			-7		
	Bit	Field	Туре	Reset	Description
41	23	Parity Bit	R	0	Parity Bit
1	22-0	CALIBRATION2	R	0	Calibration 2 Result: 23 bit integer value (Bit 22: MSB, Bit 0:
	111.				LSB)
	1	100			W. 1100, CO. LM
4.			1.		W. ON.
<		1110 11 CO		4	My 1100 1CO, CI
		100	JUL TO		AN W. OOK. ONL.
	M.	1 C			My Allow I Co. The
	` .1	1,100,1	COM.		
		N. I		A	
		14, 100,	COL	N	1001. COM. LA
				*	

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Application and Implementation

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NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality

Application Information

In the Time Of Flight (TOF) method, the upstream flight time as well as the downstream flight time is measured. The difference between the Downstream and Upstream values is proportional to the flow.

The microcontroller (MCU) configures the TDC and AFE and issues a measurement start command to the TDC via the SPI interface. The TDC sends a TRIGGER pulse to the AFE which is set up to actuate one of the transducers and transmit a START signal to the TDC which starts its counter(s). The echo pulse will travel through the AFE and arrive to the TDC as the STOP signal. The counter will be stopped and after performing calibration, the counter value is reported as VAL.

W.100Y.COM.TW Depending on system implementation, the above procedure is repeated for the same direction or opposite direction. direction. W.100Y.COM.TV

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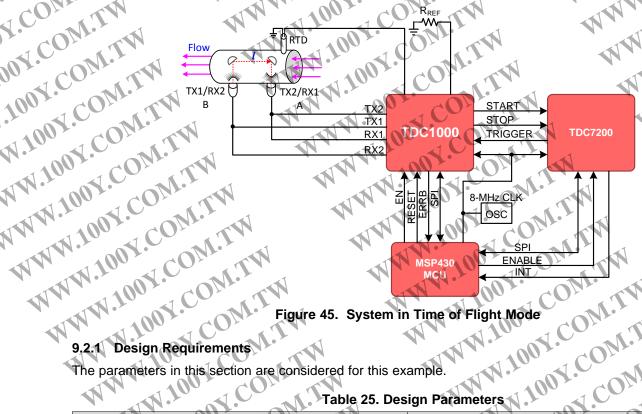


Figure 45. System in Time of Flight Mode

Figure 45. Systemin	n Time of Flight Mode
9.2.1 Design Requirements	MAN TOOX CON TAN
The parameters in this section are considered for this ex	ample.
Table 25. Des	ign Parameters
DESIGN PARAMETER	EXAMPLE VALUE
Pipe diameter	15 mm
Distance between transducers	60 mm
Minimum flow rate	0.015 m³/h
Accuracy at minimum flow rate	5%

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The design of flow-meters requires a thorough technical assessment of the system where the device will be used. The following is a list of areas to consider:

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- Minimum and maximum flow rate at maximum allowable error in the system
- Transitional flow rate
- Accuracy of the meter within prescribed limits per applicable standards

 Pressure in the system
- Operating temperature range

The appropriate ultrasonic sensor and the proper electronics for interfacing to the sensor are determined based on the system requirements. The following is a list of specifications applicable to the senor/assembly used in the system:

- **Excitation frequency**
- Excitation source voltage
- Pipe diameter
- Distance between the transducers (or reflectors)

9.2.2 Detailed Design Procedure

The following subsections describe the detailed design procedure for a flow meter application.

Flow Meter Regulations and Accuracy

If the flow meter is intended for residential applications, it must be designed to meet the required standards. For example, per the INTERNATIONAL ORGANIZATION OF LEGAL METROLOGY (OIML), the metrological requirements of water meters are defined by the values of Q1 Q2 Q3 and Q4 which are designed as the control of th requirements of water meters are defined by the values of Q1, Q2, Q3 and Q4, which are described in Table 26.

FLOW-RATE ZONE DESCRIPTION Lowest flow rate at which the meter is to operate within the maximum permissible errors. Flow rate between the permanent flow rate and the minimum flow rate that divides the flow rate range into two zones, the upper flow rate zone and the lower flow rate zone, each characterized by its own maximum permissible errors. Highest flow rate within the rated operating condition at which the meter is to operate within the maximum permissible errors. Highest flow rate at which the meter is to operate for a short period of time within the maximum permissible errors, while maintaining its metrological performance when it is subsequently operating within the rated operating conditions.

Table 26. Flow-rate Zones per OIML

A water meter is designated by the numerical value of Q3 in m³/h and the ratio Q3/Q1. The value of Q3 and the ratio of Q3/Q1 are selected from the lists provided in the OIML standards.

Water meters have to be designed and manufactured such that their errors do not exceed the maximum permissible errors (MPE) defined in the standards. For example, in OIML standards, water meters need to be designated as either accuracy class 1 or accuracy class 2, according to the requirements.

For class 1 water meters, the maximum permissible error in the upper flow rate zone ($Q2 \le Q \le Q4$) is ±1%, for temperatures from 0.1°C to 30°C, and ±2% for temperatures greater than 30°C. The maximum permissible error for the lower flow-rate zone (Q1 \leq Q \leq Q2) is \pm 3%, regardless of the temperature range.

For class 2 water meters, the maximum permissible error for the upper flow rate zone (Q2 \leq Q4) is \pm 2%, for temperatures from 0.1°C to 30°C, and ±3% for temperatures greater than 30°C. The maximum permissible error for the lower flow rate zone (Q1 \leq Q < Q2) is \pm 5% regardless of the temperature range.

The flow meter accuracy specified in the standards dictates the required accuracy in the electronics used for driving the ultrasonic transducers, circuits in the receiver path, and time measurement sub circuits. The stringent accuracy required at lower flow rates would require a very low noise signal chain in the transmitter and receiver circuits used in ultrasonic flow meters, as well as the ability to measure picosecond time intervals

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9.2.2.2 Transmit Time in Ultrasonic Flow Meters

9.2.2.2 Transmit Time in Ultrasonic Flow Meters

Transit-time ultrasonic flow meters works based on the principle that sound waves in a moving fluid travel faster in the direction of flow (downstream), and slower in the opposite direction of flow (upstream).

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The system requires at least two transducers. The first transducer operates as a transmitter during the upstream cycle and as a receiver during the downstream cycle, and the second transducer operates as a receiver during the upstream cycle and as a transmitter during the downstream cycle. An ultrasonic flow meter operates by alternating transmit and receive cycles between the pair of transducers and accurately measuring the time-offlight both directions.

In this example, the upstream TOF is defined as:

$$t_{BA} = \frac{l}{(c-v)}$$

where

- I is the path length between the two transducers in meters (m)
- c is the speed of sound in water in meters per second (m/s)
- v is the velocity of the water in the pipe in meters per second (m/s)

In this example, the downstream TOF is defined as:

$$t_{AB} = \frac{l}{(c+v)}$$

- / is the path length between the two transducers in meters (m)
- c is the speed of sound in water in meters per second (m/s)
- W.100Y.COM.TV M.M. TOLOY COM. v is the velocity of the water in the pipe in meters per second (m/s)

ON Twhere where $\Delta TOF = t_{BA}$ The difference of TOF is defined as:

$$\Delta TOF = t_{PA} - t_{AP}$$

After the difference in time-of-flight (Δ TOF) is calculated, the water velocity inside the pipe can be related to the Δ TOF using the following equation: $v = \frac{\Delta TOF \times c^2}{c^2}$ ΔTOF using the following equation:

$$v = \frac{\Delta TOF \times c^2}{2 \times l}$$
where
$$c \text{ is the}$$

$$l \text{ is the}$$

- c is the speed of sound in water in meters per second (m/s
- I is the path length between the two transducers in meters (m) ass flow rate can be calculated as ("

Finally, the mass flow rate can be calculated as follows: $0 = \nu \times n \times 4$

$$0 - k \times n \times 4$$

where

△TOF Accuracy Requirement Calculation

A is the flow-meter constant
wis the velocity of the water in the pipe in meters per second (m/s)

A is the cross-section area of the pipe in meters-squared (m²)

F Accuracy Requirement Calculate

minimum nents in Table 25, the ΔTQF accuracy Based on the minimum mass flow requirement and accuracy requirements in Table needed can be calculated as follows:

Convert the mass flow rate to m³/s:



$$Q = (0.015 \, m^3/h) \left(\frac{1 \, h}{3600 \, s} \right) = 4.167 x 10^{-6} \, m^3/s$$

Calculate the flow velocity assuming k = 1:

$$v = \frac{Q}{kA} = \frac{4.167 \times 10^{-6} \text{ m}^3/\text{s}}{\pi \left(\frac{0.015 \text{ m}}{2}\right)^2} = 0.0236 \text{ m/s}$$

3. Calculate the ΔTOF for the given speed of sound. In this example, a speed of sound c=14 assumed: $\Delta TOF = \frac{2 \times l \times v}{c^2} = \frac{(2)(0.06 \, m)(0.0236 \, m/s)}{1.153}$

$$\Delta TOF = \frac{2 \times l \times v}{c^2} = \frac{(2)(0.06 \, m)(0.0236 \, m/s)}{1400 \, m/s^2} = 1.445 \, ns$$

4. The requirement of 5% accuracy for minimum flow will result in a ΔTOF accuracy of:

$$\Delta TOF_{error} = (0.05)(1.445 \text{ ns}) = 72.25 \text{ ps}$$

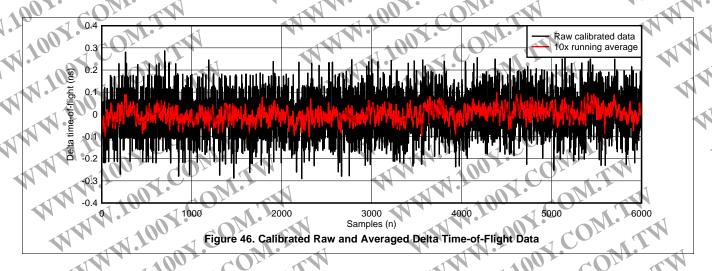
For this reason, this system requires a high accuracy timer/stopwatch that can measure the lower flow rate state.

The TDC1000 ultrasonic analog-front-end is used to drive the transmitter, amplify and filter the received signal and conditioning the echo for START and STOP pulse generation. The TDC7200 ps-accurate timer is used to measure the time interval between the rising edge of the START pulse and the rising edge of the STOP pulse produced by the TDC1000.

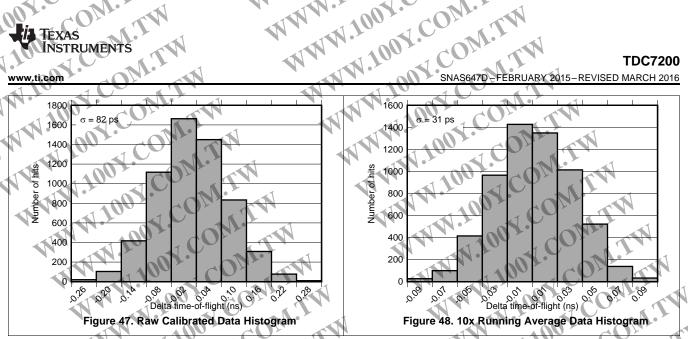
The microcontroller should first configure the TDC7200 and the TDC1000 for the measurement. When the microcontroller issues a start command to the TDC7200 via the SPI interface, the TDC7200 sends a trigger pulse to the TRIGGER pin of the TDC1000. When the TDC1000 drives the transmit transducer, a synchronous START pulse is produced on the START pin, which commands the TDC7200 to start its counters. When a valid echo pulse is received on the receive transducer, the TDC1000 generates a STOP pulse on the STOP pin, which commands the TDC7200 to stop its counters. This procedure is repeated for the upstream and downstream cycles.

A temperature measurement can be performed and the result can be used to correct for temperature dependency of the speed of sound.

Figure 46, Figure 47, and Figure 48 show data and histograms created with data collected under a zero flow condition at room temperature. A simple offset calibration has been applied, where the overall average figure data is subtracted from the data. condition at room temperature. A simple offset calibration has been applied, where the overall average of the







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9.3 Post Filtering Recommendations

For application such as flow meters where conversion results are accumulated over a long period of time, post filtering is not required. However, for applications where a specific action is taken based on individual conversion results, post filtering is recommended. One advantage of post filtering is to remove the conversion results that are outside of the normal distribution.

One such post filtering method commonly applied by an MCU is the Median Filter Method. The median of a finite number of conversion results can be found by arranging all the conversions from the lowest value to the highest value, and picking the middle one. For example, a conversion result of {50, 51, 49, 40, 51} can be rearranged from lowest to highest {40, 49, 50, 51, 51}, and the median value after applying the Median Filter Method is 50

CLOCK Recommendations

A stable, known reference clock is crucial to the ability to measure time, regardless of the time measuring device. Two parameters of a clock source primarily affect the ability to measure time: accuracy and jitter. The following subsections will discuss recommendations for the CLOCK in order to increase accuracy and reduce jitter.

9.4.1 CLOCK Accuracy

CLOCK sources are typically specified with an accuracy value as the clock period is not exactly equal to the nominal value specified. For example, an 8 MHz clock reference may have a 20 ppm accuracy. The true value of the clock period therefore has an error of ±20ppm, and the real frequency is in the range 7.99984 MHz to $8.00016 \text{ MHz} [8 \text{ MHz} \pm (8 \text{ MHz}) \times (20/10^6)].$

If the clock accuracy is at this boundary, but the reference time used to calculate the time of flight relates to the nominal 8 MHz clock period, then the time measured will be affected by this error. For example, if the time period measured is 50 μs, and the 8MHz reference clock has +50ppm of error in frequency, but the time measured refers to the 125 ns period (1/8 MHz), then the 50 µs time period will have an error of 50µs x 50/1000000 = 2.5

In summary, a clock inaccuracy translates proportionally to a time measurement error.

9.4.2 CLOCK Jitter

Clock jitter introduces uncertainty into a time measurement, rather than inaccuracy. As shown in Figure 49, the jitter accumulates on each clock cycle so the uncertainty associated to a time measurement is a function of the clock jitter and the number of clock cycles measured.

Clock_Jitter_Uncertainty = $(\sqrt{n}) \times (\theta_{JITTER})$, where n is the number of clock cycles counted, and θ_{JITTER} is the cycle-to-cycle jitter of the clock.1

For example, if the time measured is 50 μ s using an 8 MHz reference clock, n = 50 μ s/(1/8 MHz) = 400 clock cycles. If the RMS cycle-to-cycle jitter, $\theta_{JITTER} = 10$ ps, then the RMS uncertainty introduced in a single measurement is in the order of (\forall n) x (θ _{JITTER}) = 200 ps.

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TDC7200 SNAS647D+FEP **CLOCK Recommendations (continued)**

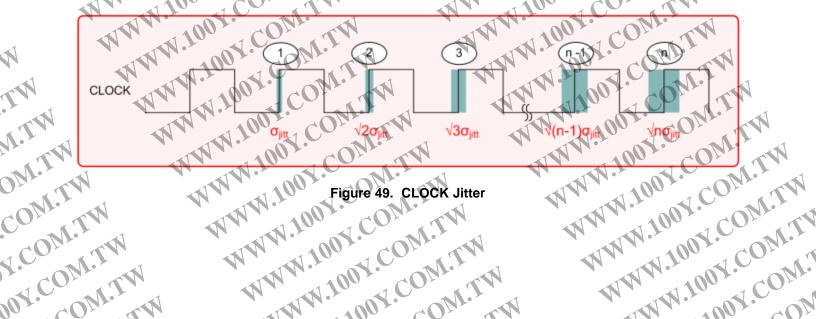
JOM.T CLOCK Recommendations (continued)

Because the effect of jitter is random, averaging or accumulating time results reduces the effect of the uncertainty introduced. If the time is measured m times and the result is averaged, then the uncertainty is reduced to: Clock_Jitter_Uncertainty = $(\sqrt{n}) \times (\theta_{JITTER}) / (\sqrt{m})$.

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For example, if 64 averages are performed in the example above, then the jitter-related uncertainty is reduced to 25 ps RMS.



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10 Power Supply Recommendations

The analog circuitry of the TDC7200 is designed to operate from an input voltage supply range between 2 V and 3.6 V. It is recommended to place a 100 nF ceramic bypass capacitar to ground as alocal and a second control of the secon 3.6 V. It is recommended to place a 100 nF ceramic bypass capacitor to ground as close as possible to the VDD pins. In addition, an electrolytic or tantalum capacitor with value greater than 1 µF is recommended. The bulk capacitor does not need to be in close vicinity with the TDC7200 and could be close to the voltage source terminals or at the output of the voltage regulators powering the TDC7200.

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Layout Guidelines

- In a 4-layer board design, the recommended layer stack order from top to bottom is: signal, ground, power
- Bypass capacitors should be placed in close proximity to the VDD pin.
- Bypass capacitors should be placed in close proximity to the VDD pin.

 The length of the START and STOP traces from the TDC7200 to the stopwatch/MCU should be matched to snort/direct as possible to minimize parasitic capacitance on the PCB.

 Route the SPI signal traces close together. Place a series resistor at the source of DOUT (close to the TDC7200) and series resistors at the sources of DIN, SCLK, and CSB (close to the master MCU).
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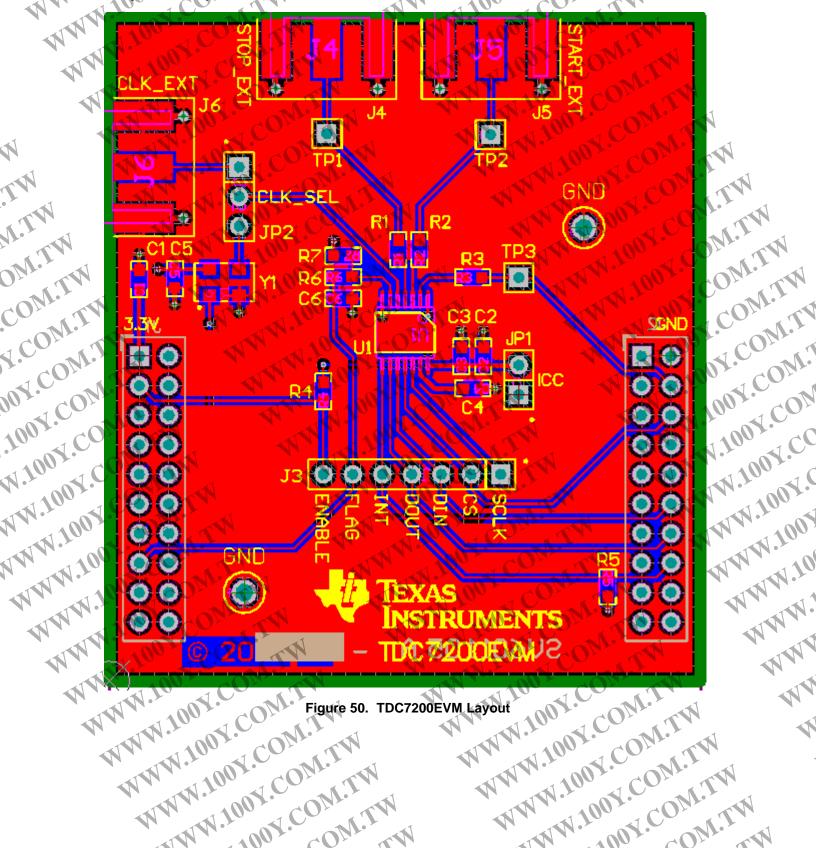
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Device and Documentation Support

Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

W.100Y.COM.TW Concentration, Flow & Proving TDC1000 : Ultrasonic Sensing Analog Front End for Level, Applications. Proximity Sensing Applications.

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12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Causian



W.100Y.COM.TV These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates. WWW.loox.com during storage or handling to prevent electrostatic damage to the MOS gates. MM.1007.CC

SLYZ022 — TI Glossary. This glossary lie

This glossary lists and explains terms, acronyms, and definitions.

WWW.100Y.C The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation. WW.100Y.COM.TW

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PACKAGE OPTION ADDENDUM

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PACKAGING INFORMATION

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	PACKAGING INFORMATION	MMM. 100%. COM. TW	MANN TOOL COM LAN	
U	Orderable Device Status	Package Type Package Pins Package Eco Plan	Lead/Ball Finish MSL Peak Temp Op Temp (°C) Device Marking	Samples
	(1)	Drawing Qty (2)	(6) (3)	
	TDC7200PW ACTIVE	TSSOP PW 14 90 Green (RoH		Samples
		& no Sb/Br)		
1	TDC7200PWR ACTIVE	TSSOP PW 14 2000 Green (RoH		Samples
1		& no Sb/Br		ountpies

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LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

DBSOLETE: TI has discontinued the production of the device.

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Corporation and additional product content details:

The Pb-Free/Green conversion plan has not been defined. information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. WWW.100Y.COM.TW Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homographics to be a special participation of the companion of the compani in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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- -" will appear on a device. If a line is indented then it is a continuation.

 Vine. Lead/Ball Finish values may wre-

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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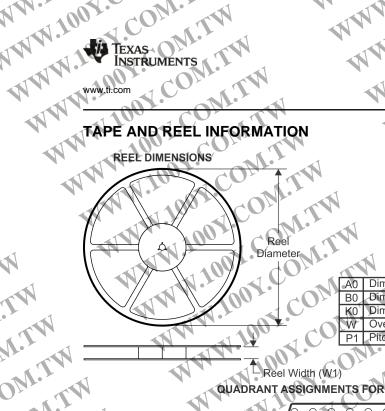
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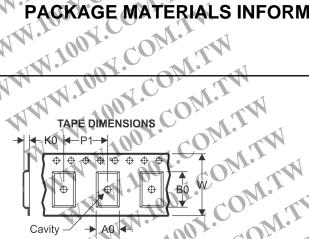
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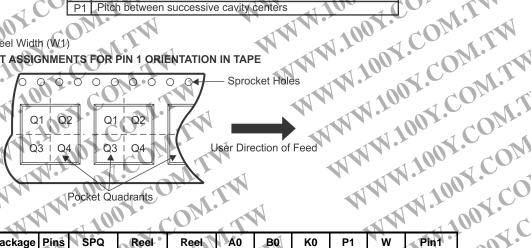
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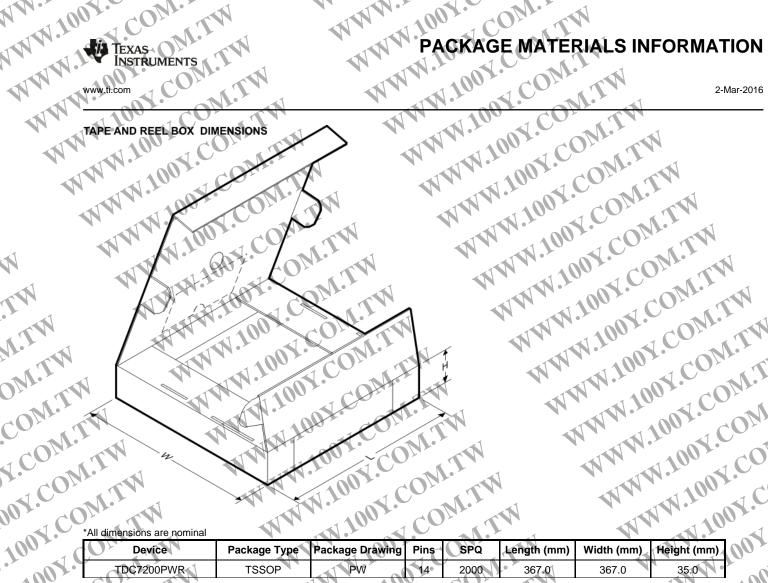
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NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.

B. This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

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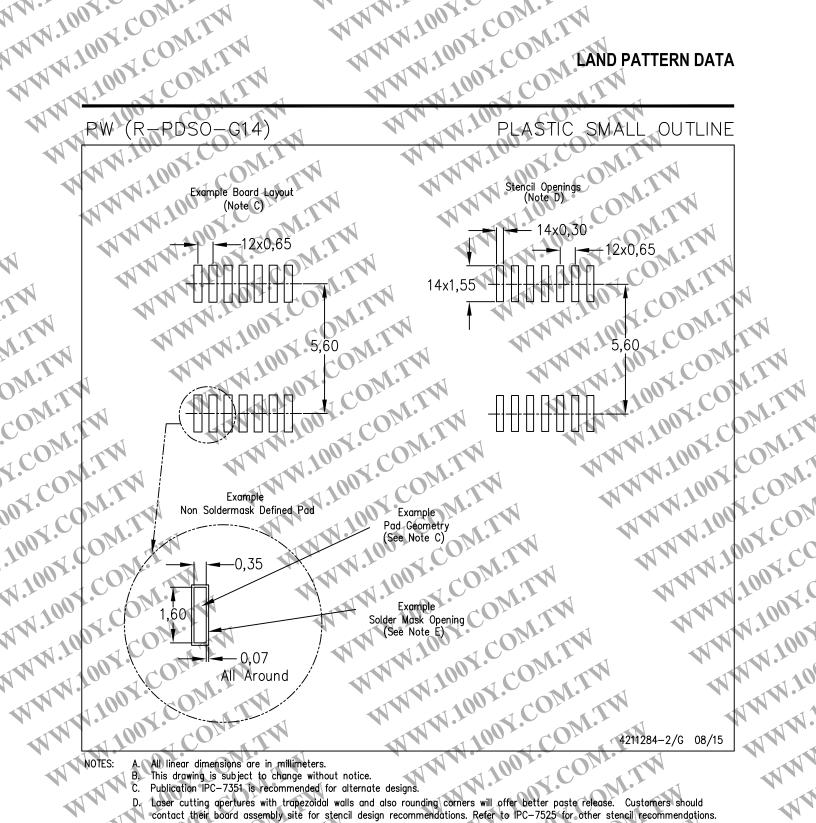
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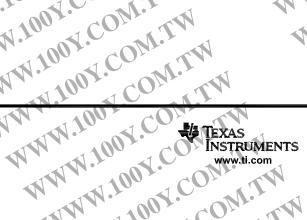
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- This drawing is subject to change without notice.
 Publication IPC-7351 is recommended for alternate designs.

 Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- WWW.100Y.COM. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads. MWW.100Y.COM. WWW.100Y. WWW.100Y W.100Y.COM.TW



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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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