TDC7200 Time-to-Digital Converter for Time-of-Flight Applications in LIDAR, Magnetostrictive and Flow Meters

1 Features

- Resolution: 55 ps
- Standard Deviation: 35 ps
- Measurement Range:
  - Mode 1: 12 ns to 500 ns
  - Mode 2: 250 ns to 8 ms
- Low Power Consumption: 0.5 µA (2 SPS)
- Supports up to 5 STOP Signals
- Autonomous Multi-Cycle Averaging Mode for Low Power Consumption
- Supply Voltage: 2 V to 3.6 V
- Operating Temperature –40°C to 85°C
- SPI Host Interface for Configuration and Register Access

2 Applications

- Flow Meter: Water Meter, Gas Meter, Heat Meter
- Magnetostrictive Position/Level Sensing
- Time-of-Flight in Drones (LIDAR, SONAR), metering equipment and projectors
- Heat Cost Allocators

3 Description

The TDC7200 is a Time-to-Digital Converter (TDC) for ultrasonic sensing measurements such as water flow meter, gas flow meter, and heat flow meter. When paired with the TDC1000 (ultrasonic analog-front-end), the TDC7200 can be a part of a complete TI ultrasonic sensing solution that includes the MSP430, power, wireless, and source code.

The Time to Digital Converter (TDC) performs the function of a stopwatch and measures the elapsed time (time-of-flight or TOF) between a START pulse and up to five STOP pulses. The ability to measure from START to multiple STOPs gives users the flexibility to select which STOP pulse yields the best echo performance.

The device has an internal self-calibrated time base which compensates for drift over time and temperature. Self-calibration enables time-to-digital conversion accuracy in the order of picoseconds. This accuracy makes the TDC7200 ideal for flow meter applications, where zero and low flow measurements require high accuracy.

When placed in the Autonomous Multi-Cycle Averaging Mode, the TDC7200 can be optimized for low system power consumption, making it ideal for battery powered flow meters. In this mode, the host can go to sleep to save power, and it can wake up when interrupted by the TDC upon completion of the measurement sequence.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TDC7200	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Revision History

Changes from Revision C (August 2015) to Revision D — **Page**

- Added EN = HIGH ... 7
- update equation ... 14
- Changed 3818 TO 318 ... 18

Changes from Revision B (June 2015) to Revision C — **Page**

- Changed the data sheet title From: *TDC7200 Time-to-Digital Converter for Water and Gas Flow Sensing, Magnetostrictive Position Sensing, and LIDAR Metering Applications* To: *TDC7200 Time-to-Digital Converter for Time-of-Flight applications in LIDAR, Magnetostrictive and Flow Meters* ... 1

Changes from Revision A (March 2015) to Revision B — **Page**

- Changed the data sheet title From: *TDC7200 Time-to-Digital Converter for Water, Gas, Heat Flow Metering Applications* To: *TDC7200 Time-to-Digital Converter for Water and Gas Flow Sensing, Magnetostrictive Position Sensing, and LIDAR Metering Applications* ... 1
- Changed the *Applications* list to include: "Magnetostrictive Position Sensing", and "LIDAR Metering" ... 1

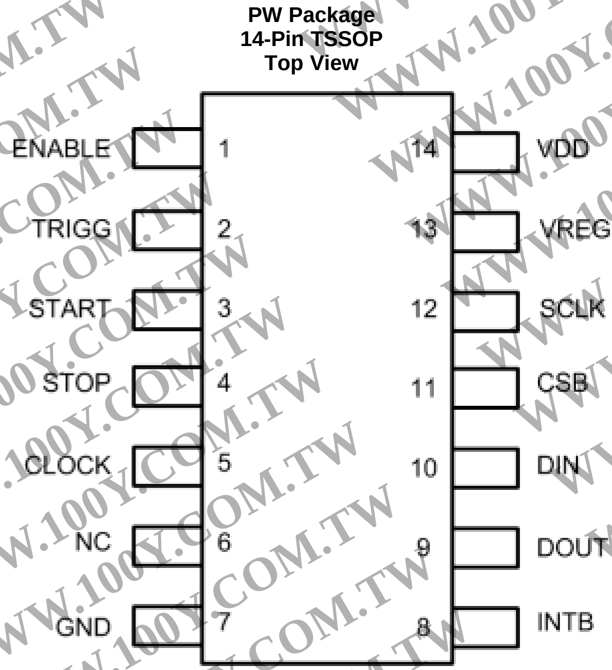
Changes from Original (February 2015) to Revision A — **Page**

- Changed From: 1-page Product Preview To: Full data sheet ... 1
- Changed ESD Ratings table ... 5

5 Companion Device

PART NO.	TITLE
TDC1000	Ultrasonic Sensing Analog Front End for Level, Concentration, Flow and Proximity Sensing

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ENABLE	1	Input	Enable signal to TDC
TRIGG	2	Output	Trigger output signal
START	3	Input	START signal to TDC
STOP	4	Input	STOP signal to TDC
CLOCK	5	Input	Clock Input to TDC
N.C.	6	–	Not Connected
GND	7	Ground	Ground
INTB	8	Output	Interrupt to MCU, active low (open drain)
DOUT	9	Output	SPI Data Output
DIN	10	Input	SPI Data Input
CSB	11	Input	SPI Chip Select, active low
SCLK	12	Input	SPI clock
VREG	13	Output	LDO Output terminal for external decoupling cap
VDD	14	Power	Supply input

7 Specifications

7.1 Absolute Maximum Ratings

T_A = 25°C , VDD = 3.3V, GND = 0V (unless otherwise noted).[(1)(2)(3)]

		MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.3	3.9	V
V_I	Terminal input voltage	–0.3	V_{DD}+0.3	V
V_{DIFF_IN}	|Voltage differential| between any two input terminals		3.9	V
$V_{IN\_GND\_VDD}$	|Voltage differential| between any input terminal and GND or VDD		3.9	V
I_I	Input current at any pin	–5	5	mA
T_A	Ambient temperature	-40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

T_A = 25°C , VDD = 3.3V, GND = 0V (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	2		3.6	V
V_I	Terminal voltage	0		VDD	V
V_{IH}	Voltage input high	0.7 × VDD		3.6	V
V_{IL}	Voltage input low	0		0.3 × VDD	V
F_{CALIB_CLK}	Frequency (Reference/Calibration Clock)	1 [(1)]	8	16	MHz
$DUTY_{CLOCK}$	Input clock duty cycle		50%		
TIMING REQUIREMENTS: Measurement Mode 1 [(1)]					
$T1_{STARTSTOP\_Min}$	Minimum Time between Start and Stop Signal	12			ns
$T1_{STOPSTOP\_Min}$	Minimum Time between 2 Stop Signals	67			ns
$T1_{STARTSTOP\_Max}$	Maximum time bet. Start and Stop Signal			500	ns
$T1_{STOPSTOP\_Max}$	Maximum time bet. Start and last Stop Signal			500	ns
TIMING REQUIREMENTS: Measurement 2 [(1)]					
$T2_{STARTSTOP\_Min}$	Minimum Time between Start and Stop Signal	$2 \times t_{CLOCK}$			s
$T2_{STOPSTOP\_Min}$	Minimum Time between 2 Stop Signals	$2 \times t_{CLOCK}$			s
$T2_{STARTSTOP\_Max}$	Maximum time bet. Start and Stop Signal			$(2^{16}-2) \times t_{CLOCK}$	s
$T2_{STOPSTOP\_Max}$	Maximum. time bet. Start and last Stop Signal			$(2^{16}-2) \times t_{CLOCK}$	s
TIMING REQUIREMENTS: ENABLE INPUT					
T_{REN}	Rise Time for Enable Signal (20%-80%)		1 to 100		ns
T_{FEN}	Fall Time for Enable Signal (20%-80%)		1 to 100		ns

(1) Specified by design.

Recommended Operating Conditions (continued)

T_A = 25°C , VDD = 3.3V, GND = 0V (unless otherwise noted).

		MIN	NOM	MAX	UNIT
TIMING REQUIREMENTS: START, STOP, CLOCK					
T_{RST}, T_{FST}	Maximum rise, fall time for START, STOP signals (20%-80%)		1		ns
T_{RXCLK}, T_{FXCLK}	Maximum rise, fall time for external CLOCK (20%-80%)		1		ns
TIMING REQUIREMENTS: TRIGG					
$T_{TRIGSTART}$	Time from TRIG to START		5		ns
TEMPERATURE					
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature	–40		85	°C

7.4 Thermal Information

THERMAL METRIC[(1)]		TDC7200 PW [TSSOP] 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63	
$R_{\theta JB}$	Junction-to-board thermal resistance	76.8	
ψ_{JT}	Junction-to-top characterization parameter	12.4	
ψ_{JB}	Junction-to-board characterization parameter	76.2	
θ_{JA}	Package thermal impedance	113	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_A = 25°C , VDD = 3.3 V, GND = 0 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TDC CHARACTERISTICS						
LSB	Resolution	Single shot measurement		55		ps
T_{ACC-2}	Accuracy (Mode 2) [1]	CLOCK = 8 MHz		28		ps
T_{STD-2}	Standard Deviation (Mode 2)	Measured time = 100 µs		50		ps
		Measured time = 1 µs		35		ps
OUTPUT CHARACTERISTICS: TRIGG, INTB, DOUT						
V_{OH}	Output voltage high	Isource = -2 mA	2.31	2.95		V
V_{OL}	Output voltage low	Isink = 2 mA		0.35	0.99	V
INPUT CHARACTERISTICS: ENABLE, START, STOP, CLOCK, DIN, CSB,SCLK						
C_{in}	Input capacitance [2]			3		pF
POWER CONSUMPTION (see Measurement Mode 1 and Measurement Mode 2)						
I_{sh}	Shutdown current	EN = LOW		0.3	2	µA
I_{QA}	Quiescent Current A	EN = HIGH; TDC running		1.35		mA
I_{QB}	Quiescent Current B	EN = HIGH; TDC OFF, Clock Counter running		71		µA
I_{QC}	Quiescent Current C	EN = HIGH; measurement stopped, SPI communication only		87		µA
I_{QD}	Quiescent Current D	EN = HIGH, TDC OFF, counter stopped, no communication		50		µA

(1) Accuracy is defined as the systematic error in the output signal; the error of the device excluding noise.
(2) Specified by design.

7.6 Timing Requirements

		MIN	NOM	MAX	UNIT
TIMING REQUIREMENTS: START, STOP INPUTS, CLOCK					
PW_{START}	Pulse width for Start Signal	10			ns
PW_{STOP}	Pulse width for Stop Signal	10			ns
SERIAL INTERFACE TIMING CHARACTERISTICS (VDD = 3.3 V, f_{SCLK} = 20 MHz) (See Figure 1)					
f_{SCLK}	SCLK Frequency			20	MHz
t_1	SCLK period	50			ns
t_2	SCLK High Time	16			ns
t_3	SCLK Low Time	16			ns
t_4	DIN setup time	4			ns
t_5	DIN hold time	4			ns
t_6	CSB fall to SCLK rise	6			ns
t_7	Last SCLK rising edge to CSB rising edge	6			ns
t_8	Minimum pause time (CSB high)	40			ns
t_9	Clk fall to DOUT bus transition			12	ns

7.7 Switching Characteristics

T_A = 25°C , VDD = 3.3 V, GND = 0 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
WAKE UP TIME						
T_{WAKEUP_PERIOD}	Time to be ready for Measurement	LSB within 0.3% of settled value		300		µs

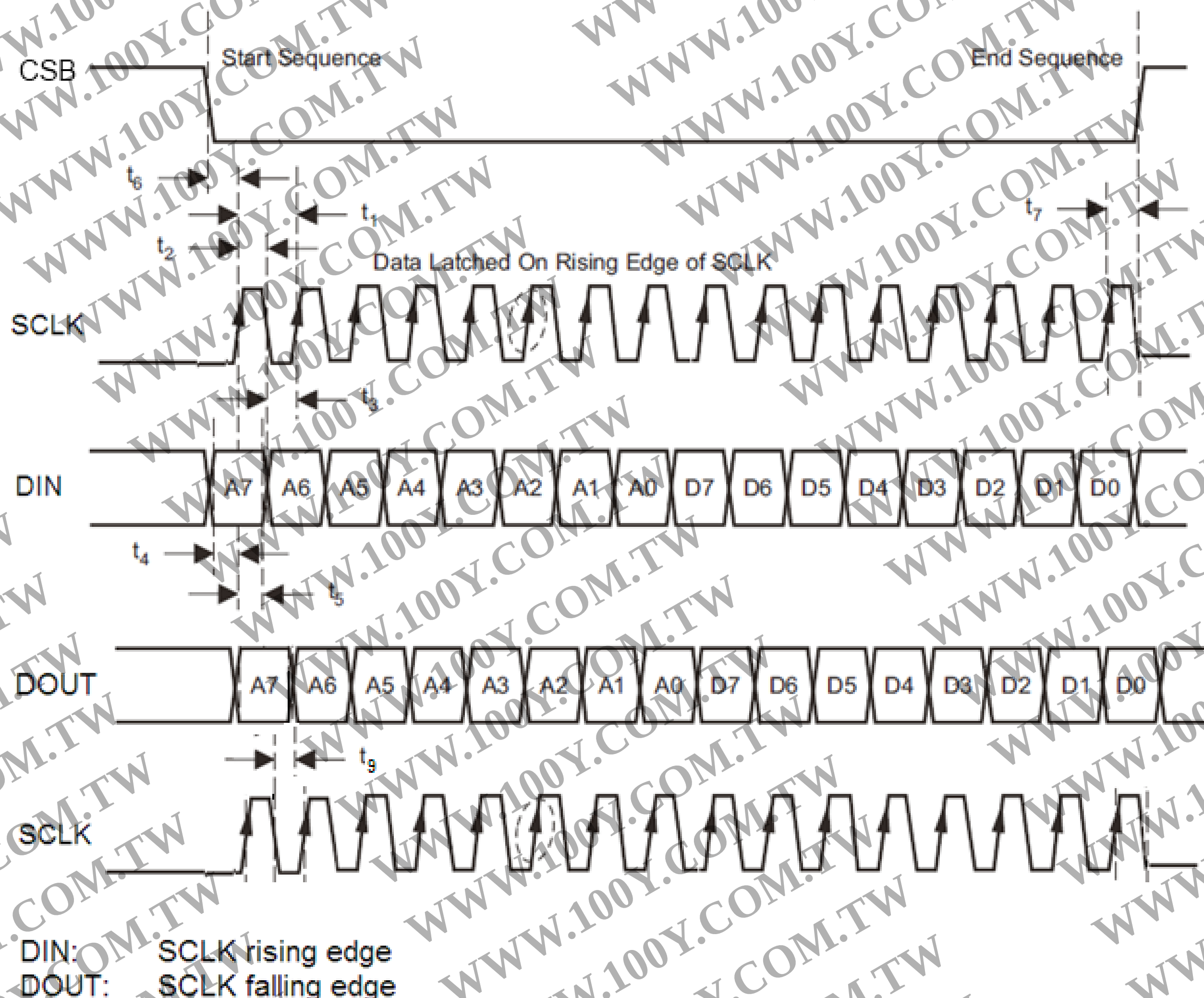


Figure 1. SPI Register Write: 8 bit Register Example

7.8 Typical Characteristics

T_A = 25°C , VDD = 3.3 V, GND = 0 V, CLOCK = 8 MHz, CALIBRATION2_PERIODS = 10, AVG_CYCLES = 1 Measurement, NUM_STOP = Single STOP, Measurement Mode 2 (unless otherwise noted).

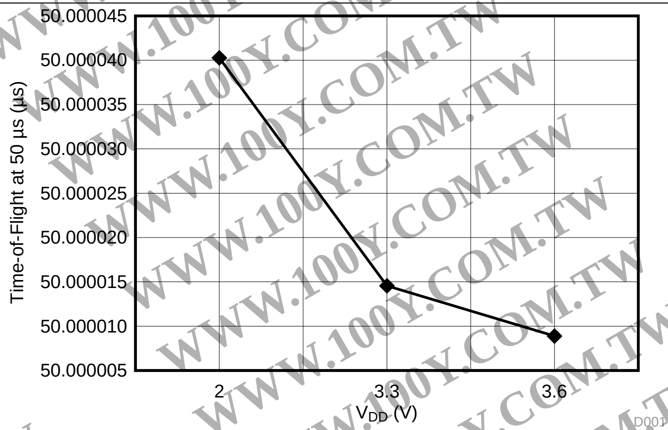


Figure 2. Time-of-Flight (TOF) vs. VDD (Measurement Mode 2)

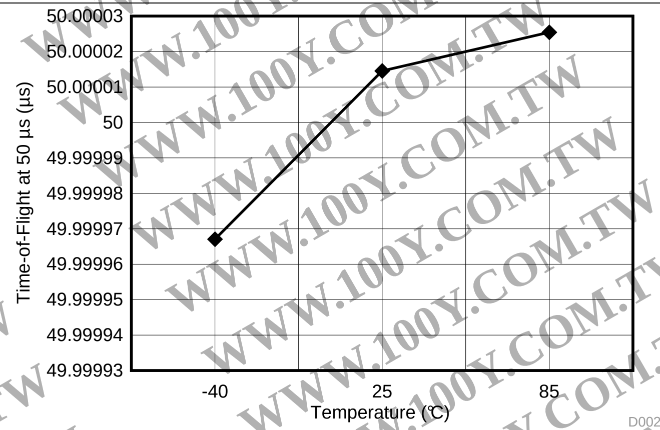


Figure 3. TOF vs. Temperature (Measurement Mode 2)

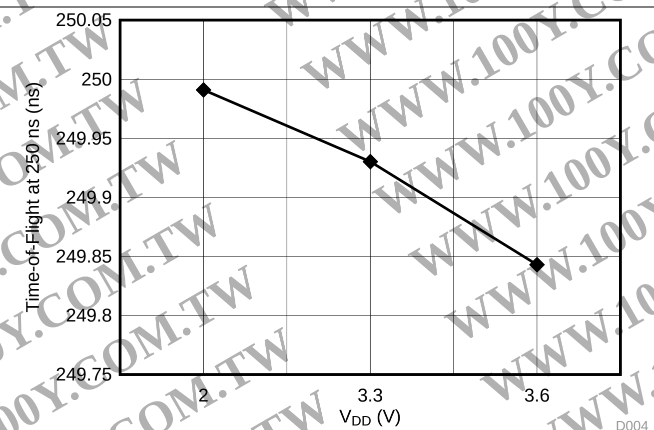


Figure 4. TOF vs. VDD (Measurement Mode 1)

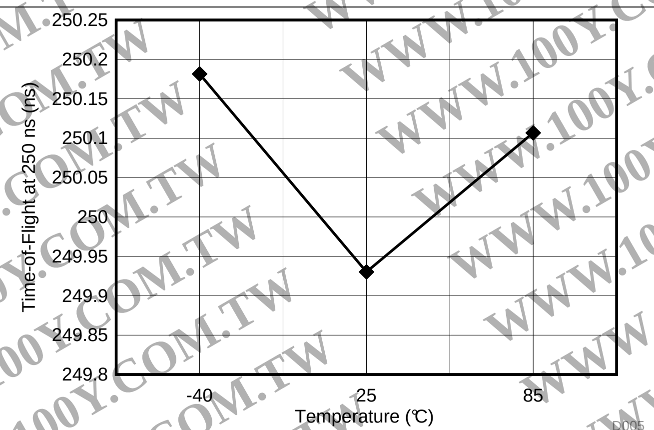


Figure 5. TOF vs. Temperature (Measurement Mode 1)

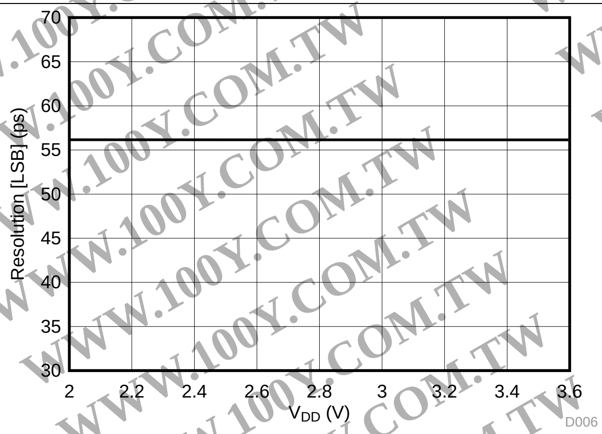


Figure 6. Resolution (LSB) vs. VDD

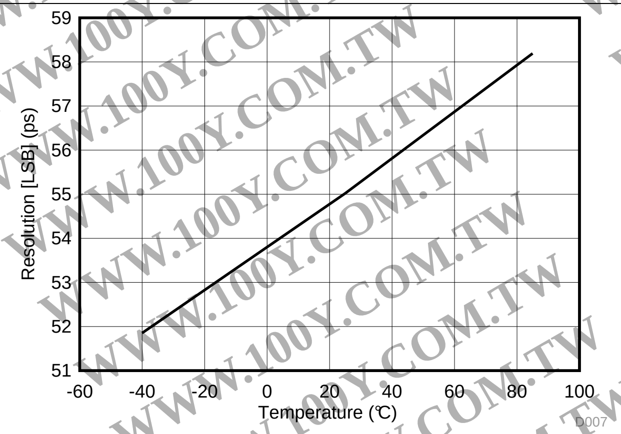


Figure 7. Resolution (LSB) vs. Temperature

Typical Characteristics (continued)

T_A = 25°C , VDD = 3.3 V, GND = 0 V, CLOCK = 8 MHz, CALIBRATION2_PERIODS = 10, AVG_CYCLES = 1 Measurement, NUM_STOP = Single STOP, Measurement Mode 2 (unless otherwise noted).

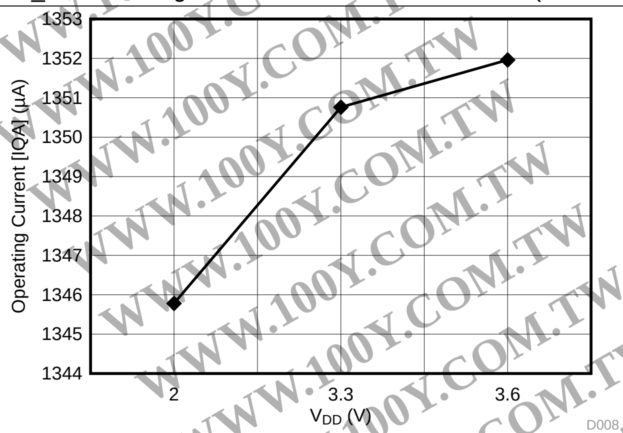


Figure 8. Operating Current (IQA) vs. VDD

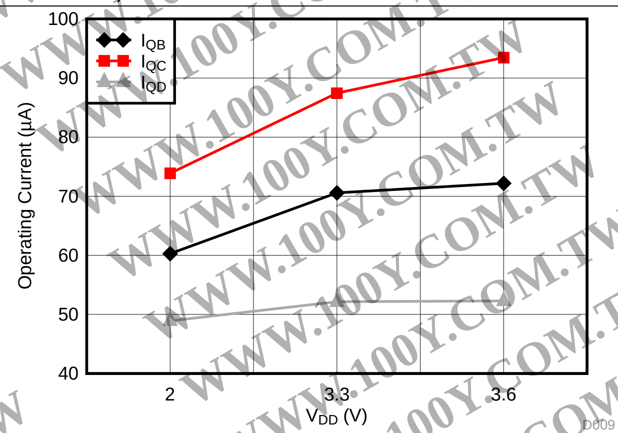


Figure 9. Operating Currents (IQB, IQC, IQD) vs. VDD

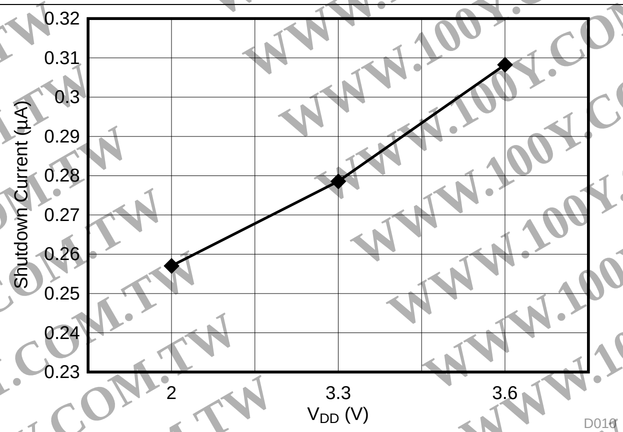


Figure 10. Shutdown Current (ISH) vs. VDD

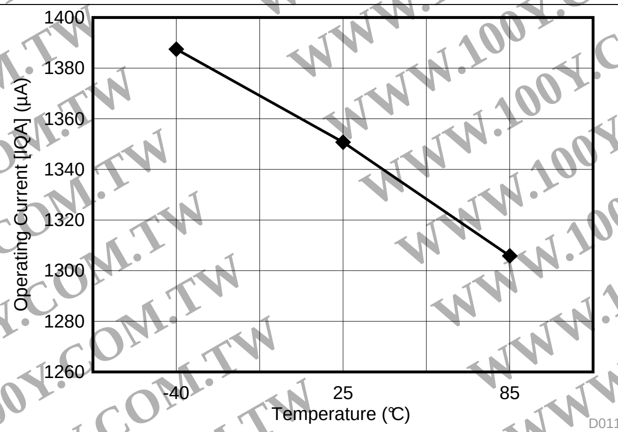


Figure 11. Operating Current (IQA) vs. Temperature

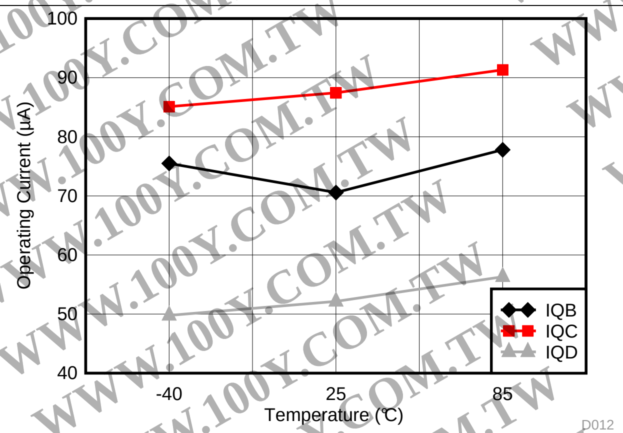


Figure 12. Operating Currents (IQB, IQC, IQD) vs. Temperature

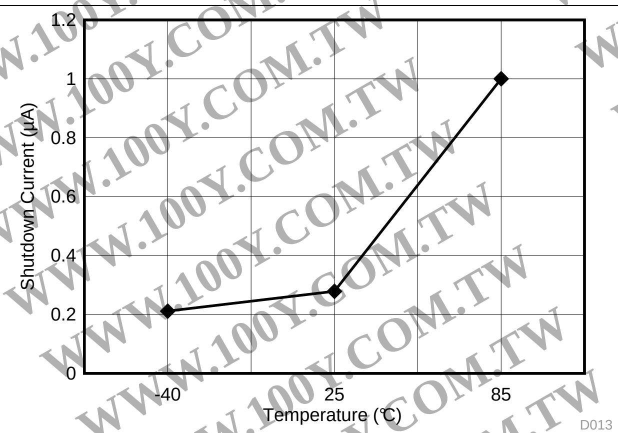


Figure 13. Shutdown Current (ISH) vs. Temperature

Typical Characteristics (continued)

T_A = 25°C , VDD = 3.3 V, GND = 0 V, CLOCK = 8 MHz, CALIBRATION2_PERIODS = 10, AVG_CYCLES = 1 Measurement, NUM_STOP = Single STOP, Measurement Mode 2 (unless otherwise noted).

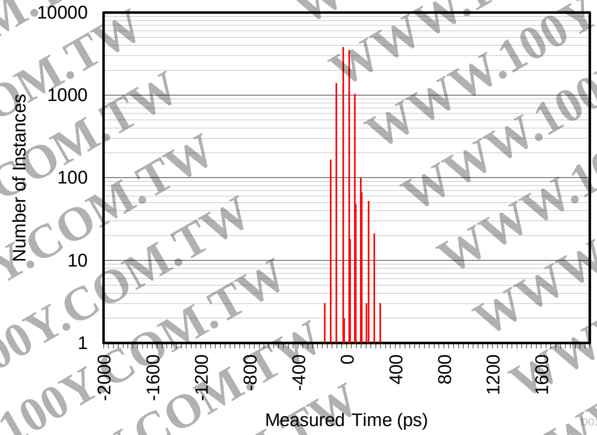


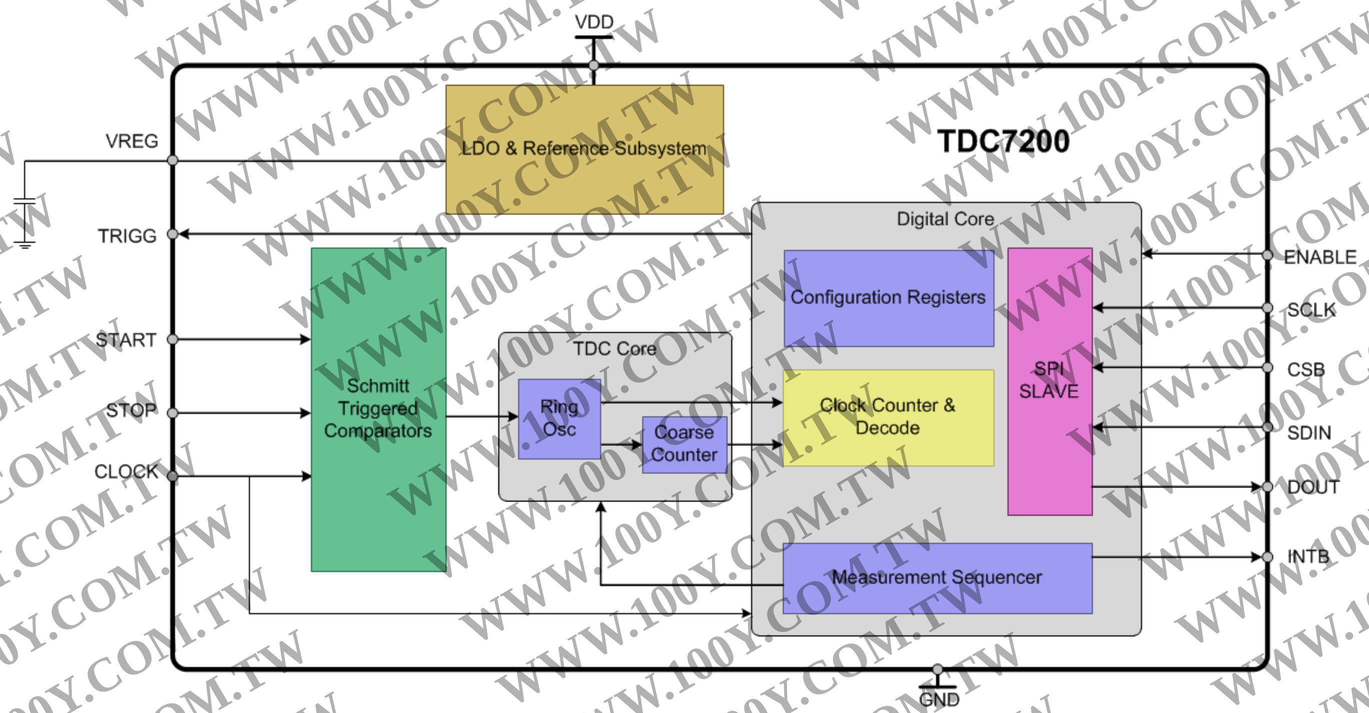
Figure 14. Standard Time-of-Flight Histogram (Normalized)

8 Detailed Description

8.1 Overview

The TDC7200 is a stopwatch IC used to measure time between a single event (edge on START pin) and multiple subsequent events (edge on STOP pin). An event from a START pulse to a STOP pulse is also known as time-of-flight, or TOF for short. The device has an internal time base that is used to measure time with accuracy in the order of picoseconds. This accuracy makes the TDC7200 ideal for application such as flow meter, where zero and low flow measurements require high accuracy in the picoseconds range.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 LDO

The LDO (low-dropout) is an internal supply voltage regulator for the TDC7200. No external circuitry needs to be connected to the output of this regulator other than the mandatory external decoupling capacitor.

Recommendations for the decoupling capacitor parameters:

- Type: ceramic
- Capacitance: 0.4 µF–2.7 µF (1 µF typical). If using a capacitor value outside the recommended range, the part may malfunction and can be damaged.
- ESR: 100 mΩ (max)

Feature Description (continued)

8.3.2 CLOCK

TDC7200 needs an external reference clock connected to the CLOCK pin. The external CLOCK is used to calibrate the internal time base accurately and therefore, the measurement accuracy is heavily dependent on the external CLOCK accuracy. This reference clock is also used by all digital circuits inside the device; thus, CLOCK has to be available and stable at all times when the device is enabled (ENABLE = HIGH).

Figure 15 shows the typical effect of the external CLOCK frequency on the measurement uncertainty. With a reference clock of 1MHz, the standard deviation of a set of measurement results is approximately 243ps. As the reference clock frequency is increased, the standard deviation (or measurement uncertainty) reduces. Therefore, using a reference clock of 16MHz is recommended for optimal performance.

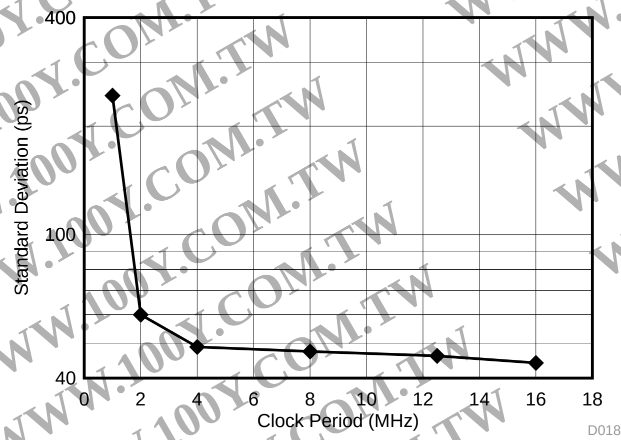


Figure 15. Standard Deviation vs. CLOCK

8.3.3 Counters

8.3.3.1 Coarse and Clock Counters Description

Time measurements by the TDC7200 rely on two counters: the Coarse Counter and the Clock Counter. The Coarse Counter counts the number of times the ring oscillator (the TDC7200's core time measurement mechanism) wraps, which is used to generate the results in the TIME1 to TIME6 registers.

The Clock Counter counts the number of integer clock cycles between START and STOP events and is used in *Measurement Mode 2* only. The results for the Clock Counter are displayed in the CLOCK_COUNT1 to CLOCK_COUNT5 registers.

8.3.3.2 Coarse and Clock Counters Overflow

Once the coarse counter value has reached the corresponding value of the Coarse Counter Overflow registers, then its interrupt bit will be set to 1. In other words, if (TIMEn / 63) ≥ COARSE_CNTR_OVF, then COARSE_CNTR_OVF_INT = 1 (this interrupt bit is located in the INT_STATUS register). COARSE_CNTR_OVF = (COARSE_CNTR_OVF_H x 2^8 + COARSE_CNTR_OVF_L), and TIMEn refers to the TIME1 to TIME6 registers.

Similarly, once the clock counter value has reached the corresponding value of the Clock Counter Overflow registers, then its interrupt bit will be set to 1. In other words, if CLOCK_COUNTn > CLOCK_CNTR_OVF, then CLOCK_CNTR_OVF_INT = 1 (this interrupt bit is located in the INT_STATUS register). CLOCK_CNTR_OVF = (CLOCK_CNTR_OVF_H x 2^8 + CLOCK_CNTR_OVF_L), and CLOCK_COUNTn refers to the CLOCK_COUNT1 to CLOCK_COUNT5 registers.

As soon as there is an overflow detected, the running measurement will be terminated immediately.

Feature Description (continued)

8.3.3.3 Clock Counter STOP Mask

The value in the Clock Counter STOP Mask registers define the end of the mask window. The Clock Counter STOP Mask value will be referred to as CLOCK_CNTR_STOP_MASK = (CLOCK_CNTR_STOP_MASK_H x 2^8 + CLOCK_CNTR_STOP_MASK_L).

The Clock Counter is started by the first rising edge of the external CLOCK after the START signal (see Figure 18). All STOP signals occurring before the value set by the CLOCK_CNTR_STOP_MASK registers will be ignored. This feature can be used to help suppress wrong or unwanted STOP trigger signals.

For example, assume the following values:
- The first time-of-flight (TOF1), which is defined as the time measurement from the START to the 1st STOP = 19 µs.
- The second time-of-flight (TOF2), which is defined as the time measurement from the START to the 2nd STOP = 119 µs.
- CLOCK = 8 MHz

In this example, the TDC7200 will provide a CLOCK_COUNT1 of approximately 152 (19 µs / t_{CLOCK}), and CLOCK_COUNT2 of approximately 952 (119 µs / t_{CLOCK}). If the user sets CLOCK_CNTR_STOP_MASK anywhere between 152 and 952, then the 1st STOP will be ignored and 2nd STOP will be measured.

The Clock Counter Overflow value (CLOCK_CNTR_OVF_H x 2^8 + CLOCK_CNTR_OVF_L) should always be higher than the Clock Counter STOP Mask value (CLOCK_CNTR_STOP_MASK_H x 2^8 + CLOCK_CNTR_STOP_MASK_L). Otherwise, the Clock Counter Overflow Interrupt will be set before the STOP mask time expires, and the measurement will be halted.

8.3.3.4 ENABLE

The ENABLE pin is used as a reset to all digital circuits in the TDC7200. Therefore, it is essential that the ENABLE pin sees a positive edge after the device has powered up. It is also important to ensure that there are no transients (glitches, etc.) on the ENABLE pin; such glitches could cause the device to RESET.

8.4 Device Functional Modes

8.4.1 Calibration

The time measurements performed by the TDC7200 are based on an internal time base which is represented as the LSB value of the TIME1 to TIME6 results registers. The typical LSB value can be seen in *Electrical Characteristics*. However, the actual value of the LSB can vary depending on environmental variables (temperature, systematic noise, etc.). This variation can introduce significant error into the measurement result. There is also an offset error in the measurement due to certain internal delays in the device.

In order to compensate for these errors and to calculate the actual LSB value, calibration needs to be performed. The TDC7200 calibration consists of two measurement cycles of the external CLOCK. The first is a measurement of a single clock cycle period of the external clock; the second measurement is for the number of external CLOCK periods set by the CALIBRATION2_PERDIOS in the CONFIG2 register. The results from the calibration measurements are stored in the CALIBRATION1 and CALIBRATION2 registers.

The two-point calibration is used to determine the actual LSB in real time in order to convert the TIME1 to TIME6 results from number of delays to a real time-of-flight (TOF) number. As discussed in the next sections, the calibrations will be used for calculating time-of-flight (TOF) in measurement modes 1 and 2.

Device Functional Modes (continued)

8.4.2 Measurement Modes

8.4.2.1 Measurement Mode 1

In measurement mode 1 as shown in Figure 16, the TDC7200 performs the entire counting from START to the last STOP using its internal ring oscillator plus coarse counter. This method is recommended for measuring shorter time durations of **< 500 ns**. Using measurement mode 1 for measuring time > 500ns decreases accuracy of the measurement (as shown in Figure 17), **and is not recommended.**

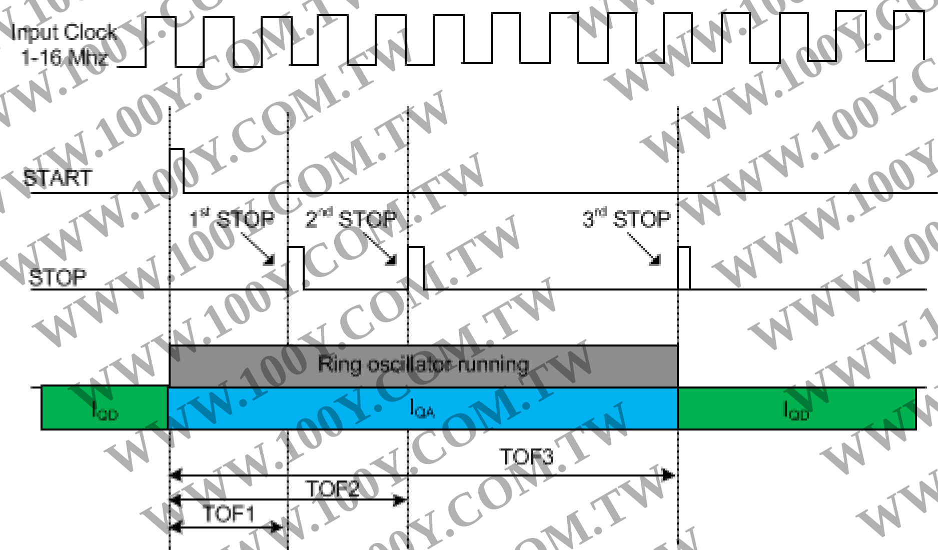


Figure 16. Measurement Mode 1

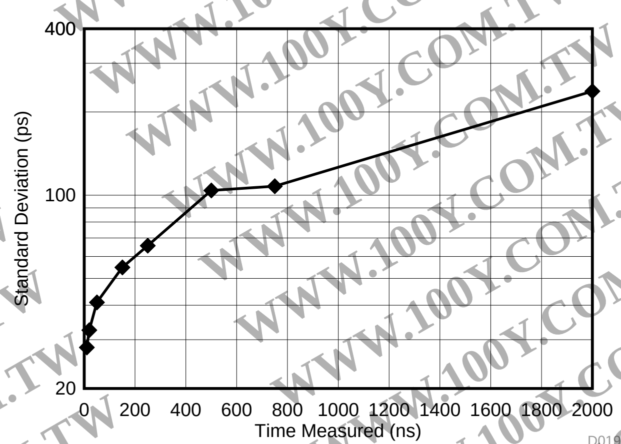


Figure 17. Measurement Mode 1 Standard Deviation vs. Measured Time-of-Flight

Device Functional Modes (continued)

8.4.2.1.1 Calculating Time-of-Flight (Measurement Mode 1)

For measurement mode 1, the time-of-flight (TOF) between the START to the n^{th} STOP can be calculated using Equation 1:

$$TOF_n = (TIME_n)(normLSB)$$

$$normLSB = \frac{(CLOCKperiod)}{(calCount)}$$

$$calCount = \frac{CALIBRATION2 - CALIBRATION1}{(CALIBRATION2\_PERIODS) - 1}$$

where

- TOF_n [sec] = time-of-flight measurement from the START to the n^{th} STOP
- $TIME_n$ = n^{th} TIME measurement given by the TIME1 to TIME6 registers
- normLSB [sec] = normalized LSB value from calibration
- CLOCKperiod [sec] = external CLOCK period
- CALIBRATION1 [count] = TDC count for first calibration cycle
- CALIBRATION2 [count] = TDC count for second calibration cycle
- CALIBRATION2_PERIODS = setting for the second calibration cycle; located in register CONFIG2 (1)

For example, assume the time-of-flight between the START to the 1^{st} STOP is desired, and the following readouts were obtained:

- CALIBRATION2 = 21121 (decimal)
- CALIBRATION1 = 2110 (decimal)
- CALIBRATION2_PERIODS = 10
- CLOCK = 8MHz
- TIME1 = 4175 (decimal)

Therefore, the calculation for time-of-flight is:

- calCount = (21121 – 2110) / (10 – 1) = 2112.33
- normLSB = (1/8MHz) / (2112.33) = 5.917×10^{-11}
- TOF1 = (4175)(5.917×10^{-11}) = 247.061 ns

8.4.2.2 Measurement Mode 2

In measurement mode 2, the internal ring oscillator of the TDC7200 is used only to count fractional parts of the total measured time. As shown in Figure 18, the internal ring oscillator starts counting from when it receives the START signal until the first rising edge of the CLOCK. Then, the internal ring oscillator switches off, and the Clock counter starts counting the clock cycles of the external CLOCK input until a STOP pulse is received. The internal ring oscillator again starts counting from the STOP signal until the next rising edge of the CLOCK.

Device Functional Modes (continued)

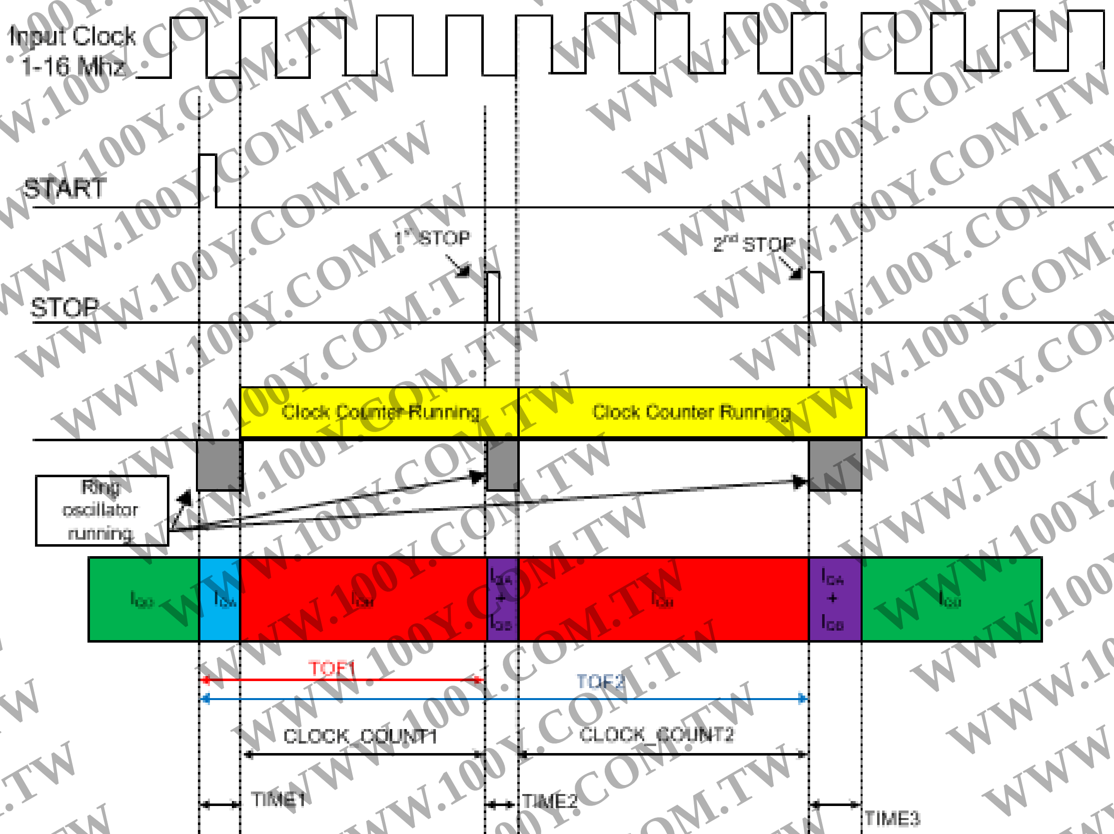


Figure 18. Measurement Mode 2

Device Functional Modes (continued)

8.4.2.2.1 Calculating Time-of-Flight (TOF) (Measurement Mode 2)

The time-of-flight (TOF) between the START to the n^{th} STOP can be calculated using Equation 2:

$$TOF_n = normLSB(TIME1 - TIME_{n+1}) + (CLOCK\_COUNT_n)(CLOCKperiod)$$

$$normLSB = \frac{(CLOCKperiod)}{(calCount)}$$

$$calCount = \frac{CALIBRATION2 - CALIBRATION1}{(CALIBRATION2\_PERIODS) - 1}$$

where

- TOF_n [sec] = time-of-flight measurement from the START to the n^{th} STOP
- TIME1 = time 1 measurement given by the TDC7200 register address 0x10
- $TIME_{(n+1)}$ = (n+1) time measurement, where n = 1 to 5 (TIME2 to TIME6 registers)
- normLSB [sec] = normalized LSB value from calibration
- $CLOCK\_COUNT_n$ = nth clock count, where n = 1 to 5 (CLOCK_COUNT1 to CLOCK_COUNT5)
- CLOCKperiod [sec] = external CLOCK period
- CALIBRATION1 [count] = TDC count for first calibration cycle
- CALIBRATION2 [count] = TDC count for second calibration cycle
- CALIBRATION2_PERIODS = setting for the second calibration; located in register CONFIG2 (2)

For example, assume the time-of-flight between the START to the 1^{st} STOP is desired, and the following readouts were obtained:

- CALIBRATION2 = 23133 (decimal)
- CALIBRATION1 = 2315 (decimal)
- CALIBRATION2_PERIODS = 10
- CLOCK = 8MHz
- TIME1 = 2147 (decimal)
- TIME2 = 201 (decimal)
- CLOCK_COUNT1 = 318 (decimal)

Therefore, the calculation for time-of-flight is:

$$calCount = \frac{CALIBRATION2 - CALIBRATION1}{(CALIBRATION2\_PERIODS) - 1} = \frac{(23133 - 2315)}{(10 - 1)} = 2313.11$$

$$normLSB = \frac{(CLOCKperiod)}{(calCount)} = \frac{(1/8MHz)}{2313.11} = 5.40 * 10^{-11}$$

$$TOF1 = (TIME1)(normLSB) + (CLOCK\_COUNT1)(CLOCKperiod) - (TIME2)(normLSB)$$

$$TOF1 = (2147)\left(5.40 * 10^{-11}\right) + (318)(1/8MHz) - (201)(5.40 * 10^{-11})$$

$$TOF1 = 39.855\mu s \tag{3}$$

Device Functional Modes (continued)

8.4.3 Timeout

For one STOP, the TDC performs the measurement by counting from the START signal to the STOP signal. If no STOP signal is received, either the Clock Counter or Coarse Counter will overflow and will generate an interrupt (see *Coarse and Clock Counters Overflow*). If no START signal is received, the timer waits indefinitely for a START signal to arrive.

For multiple STOPs, the TDC performs the measurement by counting from the START signal to the last STOP signal. All earlier STOP signals are captured and stored into the corresponding Measurement Results registers (TIME1 to TIME6, CLOCK_COUNT1 to CLOCK_COUNT5, CALIBRATION1, CALIBRATION2). The minimum time required between two consecutive STOP signals is defined in the *Recommended Operating Conditions* table. The device can be programmed to measure up to 5 STOP signals by setting the NUM_STOP bits in the CONFIG2 register.

8.4.4 Multi-Cycle Averaging

In the Multi-Cycle Averaging Mode, the TDC7200 will perform a series of measurements on its own and will only send an interrupt to the MCU (for example, MSP430, C2000, etc) for wake up after the series has been completed. While waiting, the MCU can remain in sleep mode during the whole cycle (as shown in Figure 19).

Multi-Cycle Averaging Mode Setup and Conditions:

- The number of averaging cycles should be selected (1 to 128). This is done by programming the AVG_CYCLES bit in the CONFIG2 register.
- The results of all measurements are reported in the Measurement Results registers (TIME1 to TIME6, CLOCK_COUNT1 to CLOCK_COUNT5, CALIBRATION1, CALIBRATION2 registers). The CLOCK_COUNTn registers should be right shifted by the log2(AVG_CYCLES) before calculating the time-of-flight (TOF). For example, if using the multi-cycle averaging mode, Equation 2 should be rewritten as: TOFn = normLSB [TIME1 - TIME(n+1)] + [CLOCK_COUNTn >> log 2 (AVG_CYCLES)] x [CLOCKperiod]
- Following each average cycle, the TDC generates either a trigger event on the TRIGG pin after the calibration measurement to commence a new measurement or an interrupt on the INTB pin, indicating that the averaging sequence has completed.

This mode allows multiple measurements without MCU interaction, thus optimizing power consumption for the overall system.

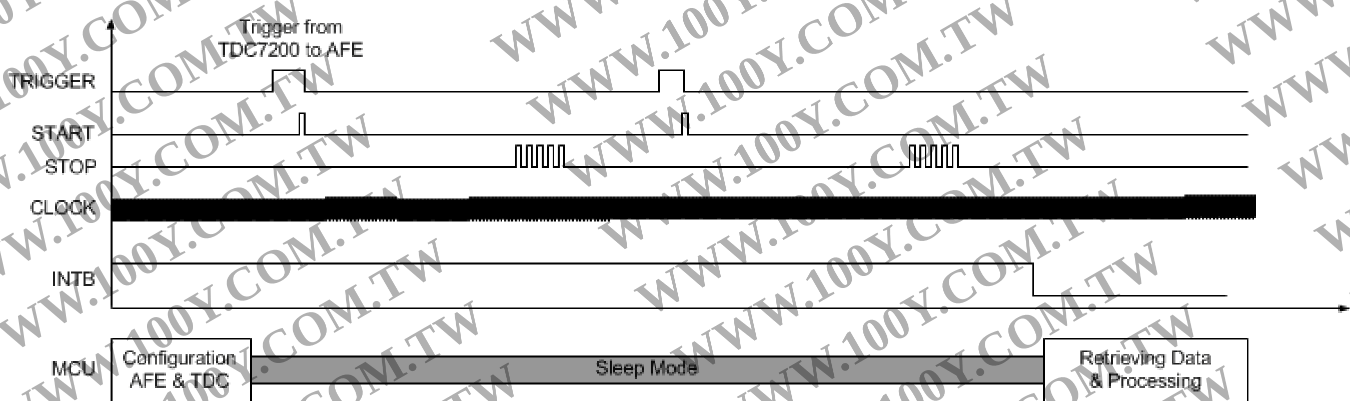


Figure 19. Multi-Cycle Averaging Mode Example with 2 Averaging Cycles and 5 STOP Signals

8.4.5 START and STOP Edge Polarity

In order to achieve the highest measurement accuracy, having the same edge polarity for the START and STOP input signals is highly recommended. Otherwise, slightly different propagation delays due to symmetry shift between the rising and falling edge configuration will impact the measurement accuracy.

For highest measurement accuracy in measurement mode 2, it's strongly recommended to choose for the START and STOP signal the “rising edge”. This is done by setting the START_EDGE and STOP_EDGE bits in the CONFIG1 register to 0.

Device Functional Modes (continued)

8.4.6 Measurement Sequence

The TDC7200 is a stopwatch IC that measures time between a START and multiple STOP events. The measurement sequence of the TDC7200 is as follows:

1. After powering up the device, the EN pin needs to be low. There is one low to high transition required while VDD is supplied for correct initialization of the device.
2. MCU software requests a new measurement to be initiated via the SPI™ interface.
3. After the start new measurement bit START_MEAS has been set in the CONFIG1 register, the TDC7200 generates a trigger signal on the TRIGG pin, which is typically used by the corresponding ultrasonic analog-front-end (such as the TDC1000) as start trigger for a measurement (for example, transmit signal for the ultrasonic burst)
4. Immediately after sending the trigger, the TDC7200 enables the START pin and waits to receive the START pulse edge
5. After receiving a START, the TDC resets the TRIGG pin
6. The Clock counter is started after the next rising edge of the external clock signal (Measurement Mode 2). The Clock Counter STOP Mask registers (CLOCK_CNTR_STOP_MASK_H and CLOCK_CNTR_STOP_MASK_L) determine the length of the STOP mask window.
7. After reaching the Clock Counter STOP Mask value, the STOP pin waits to receive a single or multiple STOP trigger signal from the analog-front-end (for example, detected echo signal of the ultrasonic burst signal)
8. After the last STOP trigger has been received, the TDC will signal to the MCU via interrupt (INTB pin) that there are new measurement results waiting in the registers. START, STOP and TRIGG pin are disabled (in Multi-Cycle Averaging Mode, the TDC will start the next cycle automatically by generating a new TRIGG signal). Note: INTB must be utilized to determine TDC measurement completion; polling the INT_STATUS register to determine measurement completion is NOT recommended as it will interfere with the TDC measurement.
9. After the results are retrieved, the MCU can then start a new measurement with the same register settings. This is done by just setting the START measurement bit via SPI. It is not required to drive the ENABLE pin low between measurements.
10. The ENABLE pin can be taken low, if the time duration between measurements is long, and it is desired to put the TDC7200 in its lowest power state. However, upon taking ENABLE high again, the device will come up with its default register settings and will need to be configured via SPI.

8.4.7 Wait Times for TDC7200 Startup

The required wait time following the rising edge of the ENABLE pin of the TDC7200 is defined by three key times, as shown in Figure 20. All three times relate to the startup of the TDC7200's internal LDO, which is power gated when the device is disabled for optimal power consumption. The first parameter, $T1_{SPI\_RDY}$, is the time after which the SPI interface is accessible. The second ($T2_{LDO\_SET1}$) parameter and third ($T3_{LDO\_SET2}$) parameter are related to the performance of a measurement made while the internal LDO is settling. The LDO supplies the TDC7200's time measurement device, and a change in voltage on its supply during a measurement translates directly to an inaccuracy. It is therefore recommended to wait until the LDO is settled before time measurement begins.

The first time period relating to the measurement accuracy is $T2_{LDO\_SET1}$, the LDO settling time 1. This is the time after which the LDO has settled to within 0.3% of its final value. A 0.3% error translates to a worst case time error (due to the LDO settling) of 0.3% x t_{CLOCK}, which is 375ps in the case of an 8MHz reference clock, or 187.5ps if a 16MHz clock is used. Finally, the time $T3_{LDO\_SET2}$ is the time after which the LDO has settled to its final value. For best performance, it is recommended that a time measurement is not started before $T3_{LDO\_SET2}$ to allow the LDO to fully settle. Typical times for $T1_{SPI\_RDY}$ is 100 µs, for $T2_{LDO\_SET1}$ is 300 µs, and for $T3_{LDO\_SET2}$ is 1.5 ms.

Device Functional Modes (continued)

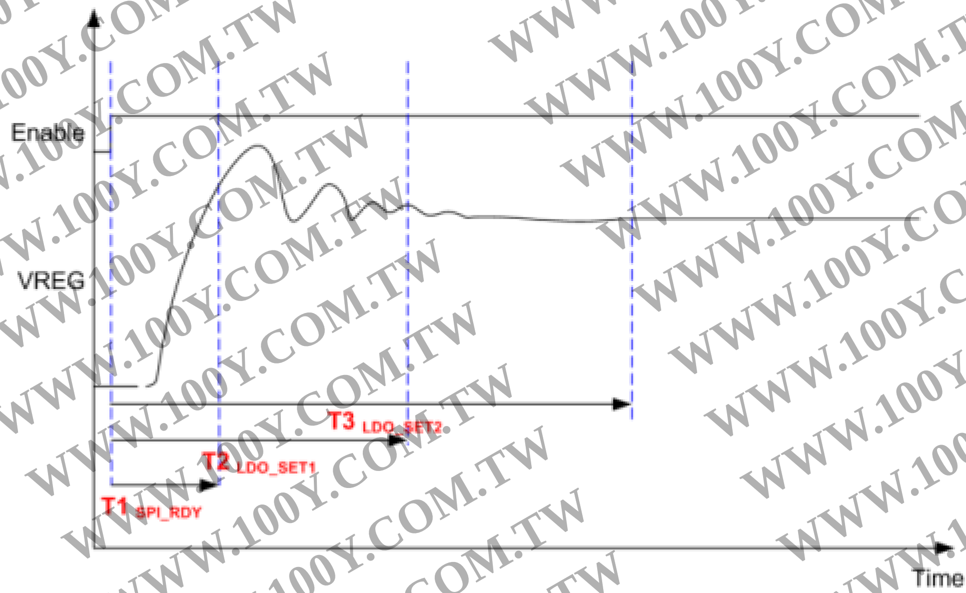


Figure 20. VREG Startup Time

8.5 Programming

8.5.1 Serial Peripheral Interface (SPI)

The serial interface consists of data input (DIN), data output (DOUT), serial interface clock (SCLK), and chip select bar (CSB). The serial interface is used to configure the TDC7200 parameters available in various configuration registers.

The communication on the SPI bus supports write and read transactions. A write transaction consists of a single write command byte, followed by single data byte. A read transaction consists of a single read command byte followed by 8 or 24 SCLK cycles. The write and read command bytes consist of a 1-bit auto-increment bit, a 1-bit read or write instruction, and a 6-bit register address. Figure 21 shows the SPI protocol for a transaction involving one byte of data (read or write).

Programming (continued)

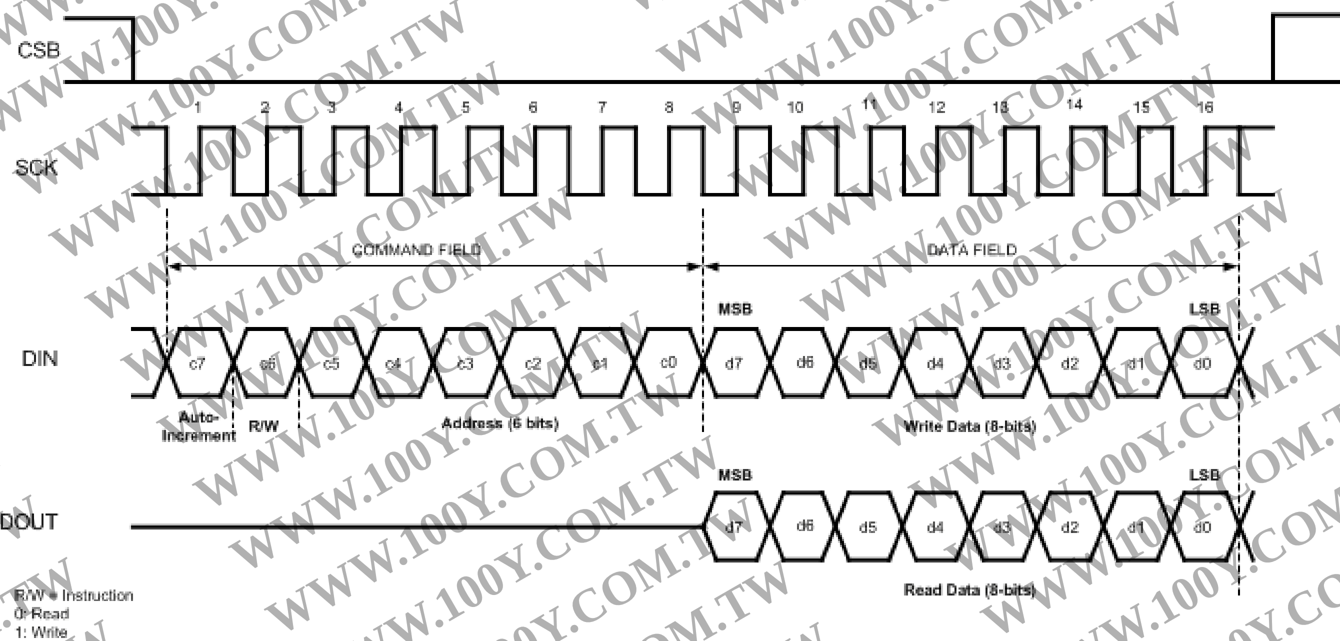


Figure 21. SPI Protocol

8.5.1.1 CSB

CSB is an active-low signal and needs to be low throughout a transaction. That is, CSB should not pulse between the command byte and the data byte of a single transaction.

De-asserting CSB always terminates an ongoing transaction, even if it is not yet complete. Re-asserting CSB will always bring the device into a state ready for the next transaction, regardless of the termination status of a previous transaction.

8.5.1.2 SCLK

SPI clock can idle high or low. It is recommended to keep SCLK as clean as possible to prevent glitches from corrupting the SPI frame.

8.5.1.3 DIN

Data In (DIN) is driven by the SPI master by sending the command and the data byte to configure the TDC7200.

8.5.1.4 DOUT

Data Out (DOUT) is driven by the TDC7200 when the SPI master initiates a read transaction. When the TDC7200 is not being read out, the DOUT pin is in high impedance mode and is undriven.

Programming (continued)

8.5.1.5 Register Read/Write

Access to the internal registers can be done through the serial interface formed by pins CSB (Chip Select - active low), SCLK (serial interface clock), DIN (data input), and DOUT (data out).

Serial shift of bits into the device is enabled when CSB is low. Serial data DIN is latched (MSB received first, LSB received last) at every rising edge of SCLK when CSB is active (low). The serial data is loaded into the register with the last data bit SCLK rising edge when CSB is low. In the case that the word length exceeds the register size, the excess bits are ignored. The interface can work with SCLK frequency from 20MHz down to very low speeds (a few Hertz) and even with a non-50% duty-cycle SCLK.

The SPI transaction is divided in two main portions:

- Address and Control: Auto Increment Mode selection bit, Read/Write bit, Address 6 bits
- Data: 8 bit or 24 bit

When writing to a register with unused bits, these should be set to 0.

Address and Control (A7 - A0)							
A7	A6	A5	A4	A3	A2	A1	A0
Auto Increment	RW	Register Address					
0: OFF 1: ON	Read = 0 Write = 1	00 h up to 3Fh					

8.5.1.6 Auto Increment Mode

When the Auto Increment Mode is OFF, only the register indicated by the Register Address will be accessed, all cycles beyond the register length will be ignored. When the Auto Increment is ON, the register of the Register Address is accessed first, then without interruption, subsequent registers are accessed.

The Auto Increment Mode can be either used to access the configuration (CONFIG1 and CONFIG2) and status (INT_STATUS) registers, or for the Measurement Results registers (TIME1 to TIME6, CLOCK_COUNT1 to CLOCK_COUNT5, CALIBRATION1, CALIBRATION2). As both register block use registers with different length, it's not possible to access all registers of the device within one single access cycle.

8.6 Register Maps

8.6.1 Register Initialization

After power up (VDD supplied, ENABLE Pin low to high transition) the internal registers are initialized with the default value. Disabling the part by pulling ENABLE pin to GND will set the device into total shutdown. As the internal LDO is turned off settings in the register will be lost. The device initializes the registers with default values with the next enable (ENABLE pin to VDD).

Table 1. Register Summary

REGISTER ADDRESS	REGISTER NAME	REGISTER DESCRIPTION	SIZE (BITS)	RESET VALUE
00h	CONFIG1	Configuration Register 1	8	00h
01h	CONFIG2	Configuration Register 2	8	40h
02h	INT_STATUS	Interrupt Status Register	8	00h
03h	INT_MASK	Interrupt Mask Register	8	07h
04h	COARSE_CNTR_OVF_H	Coarse Counter Overflow Value High	8	FFh
05h	COARSE_CNTR_OVF_L	Coarse Counter Overflow Value Low	8	FFh
06h	CLOCK_CNTR_OVF_H	CLOCK Counter Overflow Value High	8	FFh
07h	CLOCK_CNTR_OVF_L	CLOCK Counter Overflow Value Low	8	FFh
08h	CLOCK_CNTR_STOP_MASK_H	CLOCK Counter STOP Mask High	8	00h
09h	CLOCK_CNTR_STOP_MASK_L	CLOCK Counter STOP Mask Low	8	00h
10h	TIME1	Measured Time 1	24	00_0000h
11h	CLOCK_COUNT1	CLOCK Counter Value	24	00_0000h
12h	TIME2	Measured Time 2	24	00_0000h
13h	CLOCK_COUNT2	CLOCK Counter Value	24	00_0000h
14h	TIME3	Measured Time 3	24	00_0000h
15h	CLOCK_COUNT3	CLOCK Counter Value	24	00_0000h
16h	TIME4	Measured Time 4	24	00_0000h
17h	CLOCK_COUNT4	CLOCK Counter Value	24	00_0000h
18h	TIME5	Measured Time 5	24	00_0000h
19h	CLOCK_COUNT5	CLOCK Counter Value	24	00_0000h
1Ah	TIME6	Measured Time 6	24	00_0000h
1Bh	CALIBRATION1	Calibration 1, 1 CLOCK Period	24	00_0000h
1Ch	CALIBRATION2	Calibration 2, 2/10/20/40 CLOCK Periods	24	00_0000h

8.6.2 CONFIG1: Configuration Register 1 R/W (address = 00h) [reset = 0h]

Figure 22. Configuration Register 1

7	6	5	4	3	2	1	0
FORCE_CAL	PARITY_EN	TRIGG_EDGE	STOP_EDGE	START_EDGE	MEAS_MODE		START_MEAS
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 2. Configuration Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	FORCE_CAL	R/W	0	0: Calibration is not performed after interrupted measurement (for example, due to counter overflow or missing STOP signal) 1: Calibration is always performed at the end (for example, after a counter overflow)
6	PARITY_EN	R/W	0	0: Parity bit for Measurement Result Registers* disabled (Parity Bit always 0) 1: Parity bit for Measurement Result Registers enabled (Even Parity) *The Measurement Results registers are the TIME1 to TIME6, CLOCK_COUNT1 to CLOCK_COUNT5, CALIBRATION1, CALIBRATION2 registers.
5	TRIGG_EDGE	R/W	0	0: TRIGG is output as a Rising edge signal 1: TRIGG is output as a Falling edge signal
4	STOP_EDGE	R/W	0	0: Measurement is stopped on Rising edge of STOP signal 1: Measurement is stopped on Falling edge of STOP signal
3	START_EDGE	R/W	0	0: Measurement is started on Rising edge of START signal 1: Measurement is started on Falling edge of START signal
[2:1]	MEAS_MODE	R/W	00h	00: Measurement Mode 1 (for expected time-of-flight < 500 ns). 01: Measurement Mode 2 (recommended) 10, 11: Reserved for future functionality
0	START_MEAS	R/W	0	Start New Measurement: This bit is cleared when Measurement is Completed. 0: No effect 1: Start New Measurement. Writing a 1 will clear all bits in the Interrupt Status Register and Start the measurement (by generating an TRIGG signal) and will reset the content of all Measurement Results registers (TIME1 to TIME6, CLOCK_COUNT1 to CLOCK_COUNT5, CALIBRATION1, CALIBRATION2) to 0.

8.6.3 CONFIG2: Configuration Register 2 R/W (address = 01h) [reset = 40h]

Figure 23. Configuration Register 2

7	6	5	4	3	2	1	0
CALIBRATION2_PERIODS		AVG_CYCLES			NUM_STOP		
R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3. Configuration Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
[7:6]	CALIBRATION2_PERIODS	R/W	01h	00: Calibration 2 - measuring 2 CLOCK periods 01: Calibration 2 - measuring 10 CLOCK periods 10: Calibration 2 - measuring 20 CLOCK periods 11: Calibration 2 - measuring 40 CLOCK periods
[5:3]	AVG_CYCLES	R/W	00h	000: 1 Measurement Cycle only (no Multi-Cycle Averaging Mode) 001: 2 Measurement Cycles 010: 4 Measurement Cycles 011: 8 Measurement Cycles 100: 16 Measurement Cycles 101: 32 Measurement Cycles 110: 64 Measurement Cycles 111: 128 Measurement Cycles
[2:0]	NUM_STOP	R/W	00h	000: Single Stop 001: Two Stops 010: Three Stops 011: Four Stops 100: Five Stops 101, 110, 111: No Effect. Single Stop

8.6.4 INT_STATUS: Interrupt Status Register (address = 02h) [reset = 00h]

Figure 24. Interrupt Status Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	MEAS_COMPLETE_FLAG	MEAS_STARTED_FLAG	CLOCK_CNTR_OVF_INT	COARSE_CNTR_OVF_INT	NEW_MEAS_INT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 4. Interrupt Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0h	
6	Reserved	R/W	0h	
5	Reserved	R/W	0h	
4	MEAS_COMPLETE_FLAG	R/W	0h	Writing a 1 will clear the status 0: Measurement has not completed 1: Measurement has completed (same information as NEW_MEAS_INT)
3	MEAS_STARTED_FLAG	R/W	0h	Writing a 1 will clear the status 0: Measurement has not started 1: Measurement has started (START signal received)
2	CLOCK_CNTR_OVF_INT	R/W	0h	Requires writing a 1 to clear interrupt status 0: No overflow detected 1: Clock overflow detected, running measurement will be stopped immediately
1	COARSE_CNTR_OVF_INT	R/W	0h	Requires writing a 1 to clear interrupt status 0: No overflow detected 1: Coarse overflow detected, running measurement will be stopped immediately
0	NEW_MEAS_INT	R/W	0h	Requires writing a 1 to clear interrupt status 0: Interrupt not detected 1: Interrupt detected – New Measurement has been completed

8.6.5 INT_MASK: Interrupt Mask Register R/W (address = 03h) [reset = 07h]

Figure 25. Interrupt Mask Register

7	6	5	4	3	2	1	0
Reserve	Reserve	Reserve	Reserve	Reserve	CLOCK_CNTR_OVF_MASK	COARSE_CNTR_OVF_MASK	NEW_MEAS_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5. Interrupt Mask Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserve	R/W	0	
6	Reserve	R/W	0	
5	Reserve	R/W	0	
4	Reserve	R/W	0	
3	Reserve	R/W	0	
2	CLOCK_CNTR_OVF_MASK	R/W	1	0: CLOCK Counter Overflow Interrupt disabled 1: CLOCK Counter Overflow Interrupt enabled
1	COARSE_CNTR_OVF_MASK	R/W	1	0: Coarse Counter Overflow Interrupt disabled 1: Coarse Counter Overflow Interrupt enabled
0	NEW_MEAS_MASK	R/W	1	0: New Measurement Interrupt disabled 1: New Measurement Interrupt enabled

A disabled interrupt will no longer be visible on the device pin (INTB). The interrupt bit in the INT_STATUS register will still be active.

8.6.6 COARSE_CNTR_OVF_H: Coarse Counter Overflow High Value Register (address = 04h) [reset = FFh]

Figure 26. Coarse Counter Overflow Value_H Register

7	6	5	4	3	2	1	0
COARSE_CNTR_OVF_H							
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. Coarse Counter Overflow Value_H Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	COARSE_CNTR_OVF_H	R/W	FFh	Coarse Counter Overflow Value, upper 8 Bit

8.6.7 COARSE_CNTR_OVF_L: Coarse Counter Overflow Low Value Register (address = 05h) [reset = FFh]

Figure 27. Coarse Counter Overflow Value_L Register

7	6	5	4	3	2	1	0
COARSE_CNTR_OVF_L							
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. Coarse Counter Overflow Value_L Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	COARSE_CNTR_OVF_L	R/W	FFh	Coarse Counter Overflow Value, lower 8 Bit Note: Don't set COARSE_CNTR_OVF_L to 1.

8.6.8 CLOCK_CNTR_OVF_H: Clock Counter Overflow High Register (address = 06h) [reset = FFh]

Figure 28. CLOCK Counter Overflow Value_H Register

7	6	5	4	3	2	1	0
CLOCK_CNTR_OVF_H							
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. CLOCK Counter Overflow Value_H Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK_CNTR_OVF_H	R/W	FFh	CLOCK Counter Overflow Value, upper 8 Bit

8.6.9 CLOCK_CNTR_OVF_L: Clock Counter Overflow Low Register (address = 07h) [reset = FFh]

Figure 29. CLOCK Counter Overflow Value_L Register

7	6	5	4	3	2	1	0
CLOCK_CNTR_OVF_L							
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. CLOCK Counter Overflow Value_L Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK_CNTR_OVF_L	R/W	FFh	CLOCK Counter Overflow Value, lower 8 Bit

8.6.10 CLOCK_CNTR_STOP_MASK_H: CLOCK Counter STOP Mask High Value Register (address = 08h) [reset = 00h]

Figure 30. CLOCK Counter STOP Mask_H Register

7	6	5	4	3	2	1	0
CLOCK_CNTR_STOP_MASK_H							
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. CLOCK Counter STOP Mask_H Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK_CNTR_STOP_MASK_H	R/W	0	CLOCK Counter STOP Mask, upper 8 Bit

8.6.11 CLOCK_CNTR_STOP_MASK_L: CLOCK Counter STOP Mask Low Value Register (address = 09h) [reset = 00h]

Figure 31. CLOCK Counter STOP Mask_L Register

7	6	5	4	3	2	1	0
CLOCK_CNTR_STOP_MASK_L							
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. CLOCK Counter STOP Mask_L Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK_CNTR_STOP_MASK_L	R/W	0	CLOCK Counter STOP Mask, lower 8 Bit

8.6.12 TIME1: Time 1 Register (address: 10h) [reset = 00_0000h]

Figure 32. TIME1 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	Measurement Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. TIME1 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity Bit	R	0	Parity Bit
22-0	Measurement Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)	R	0	Measurement Result

8.6.13 CLOCK_COUNT1: Clock Count Register (address: 11h) [reset = 00_0000h]

Figure 33. CLOCK Count Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit								CLOCK_COUNT1 Result															
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. CLOCK_COUNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity Bit	R	0	Parity Bit
22-16	Not Used	R	0	These bits will be used in Multi-Cycle Averaging Mode in order to allow higher averaging results.
15-0	CLOCK_COUNT1 Measurement Result	R	0	CLOCK_COUNT1 Measurement Result

8.6.14 TIME2: Time 2 Register (address: 12h) [reset = 00_0000h]

Figure 34. TIME2 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	Measurement Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. TIME2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity Bit	R	0	Parity Bit
22-0	Measurement Result	R	0	Measurement Result

8.6.15 CLOCK_COUNT2: Clock Count Register (address: 13h) [reset = 00_0000h]

Figure 35. CLOCK_COUNT2 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit								CLOCK_COUNT2															
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. CLOCK_COUNT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity bit	R	0	Parity Bit
22-16	Not Used	R	0	These bits will be used in Multi-Cycle Averaging Mode in order to allow higher averaging results.
15-0	CLOCK_COUNT2 result	R	0	CLOCK_COUNT2 result

8.6.16 TIME3: Time 3 Register (address: 14h) [reset = 00_0000h]

Figure 36. TIME3 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	Measurement Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. TIME3 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity bit	R	0	Parity Bit
22-0	Measurement result	R	0	Measurement Result

8.6.17 CLOCK_COUNT3: Clock Count Registers (address: 15h) [reset = 00_0000h]

Figure 37. CLOCK_COUNT3 Count Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit								CLOCK_COUNT3															
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. CLOCK_COUNT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity bit	R	0	Parity bit
22-16	Not Used	R	0	These bits will be used in Multi-Cycle Averaging Mode in order to allow higher averaging results.
15-0	CLOCK_COUNT3 Result	R	0	CLOCK_COUNT3 Result

8.6.18 TIME4: Time 4 Register (address: 16h) [reset = 00_0000h]

Figure 38. TIME4 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	Measurement Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. TIME4 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity bit	R	0	
22-0	Measurement result	R	0	Measurement result

8.6.19 CLOCK_COUNT4: Clock Count Register (address: 17h) [reset = 00_0000h]

Figure 39. CLOCK_COUNT4 Count Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit								CLOCK_COUNT4															
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. CLOCK_COUNT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity bit	R	0	Parity bit
22-16	Not Used	R	0	These bits will be used in Multi-Cycle Averaging Mode in order to allow higher averaging results.
15-0	CLOCK_COUNT4 Result	R	0	CLOCK_COUNT4 Result

8.6.20 TIME5: Time 5 Register (address: 18h) [reset = 00_0000h]

Figure 40. TIME5 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	Measurement Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. TIME5 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity bit	R	0	Parity Bit
22-0	Measurement result	R	0	Measurement result

8.6.21 CLOCK_COUNT5: Clock Count Register (address: 19h) [reset = 00_0000h]

Figure 41. CLOCK_COUNT5 Count Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit								CLOCK_COUNT5															
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. CLOCK_COUNT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity bit	R	0	Parity bit
22-16	Not Used	R	0	These bits will be used in Multi-Cycle Averaging Mode in order to allow higher averaging results.
15-0	CLOCK_COUNT5 Result	R	0	CLOCK_COUNT5 Result

8.6.22 TIME6: Time 6 Register (address: 1Ah) [reset = 00_0000h]

Figure 42. TIME6 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	Measurement Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. TIME6 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity bit	R	0	Parity Bit
22-0	Measurement result	R	0	Measurement result

8.6.23 CALIBRATION1: Calibration 1 Register (address: 1Bh) [reset = 00_0000h]

Figure 43. CALIBRATION1 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	CALIBRATION1																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. CALIBRATION1 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity BIt	R	0	Parity Bit
22-0	CALIBRATION1	R	0	Calibration 1 Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)

8.6.24 CALIBRATION2: Calibration 2 Register (address: 1Ch) [reset = 00_0000h]

Figure 44. CALIBRATION2 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	CALIBRATION2																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. CALIBRATION2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity BIt	R	0	Parity Bit
22-0	CALIBRATION2	R	0	Calibration 2 Result: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

In the Time Of Flight (TOF) method, the upstream flight time as well as the downstream flight time is measured. The difference between the Downstream and Upstream values is proportional to the flow.

The microcontroller (MCU) configures the TDC and AFE and issues a measurement start command to the TDC via the SPI interface. The TDC sends a TRIGGER pulse to the AFE which is set up to actuate one of the transducers and transmit a START signal to the TDC which starts its counter(s). The echo pulse will travel through the AFE and arrive to the TDC as the STOP signal. The counter will be stopped and after performing calibration, the counter value is reported as VAL.

Depending on system implementation, the above procedure is repeated for the same direction or opposite direction.

9.2 Typical Application

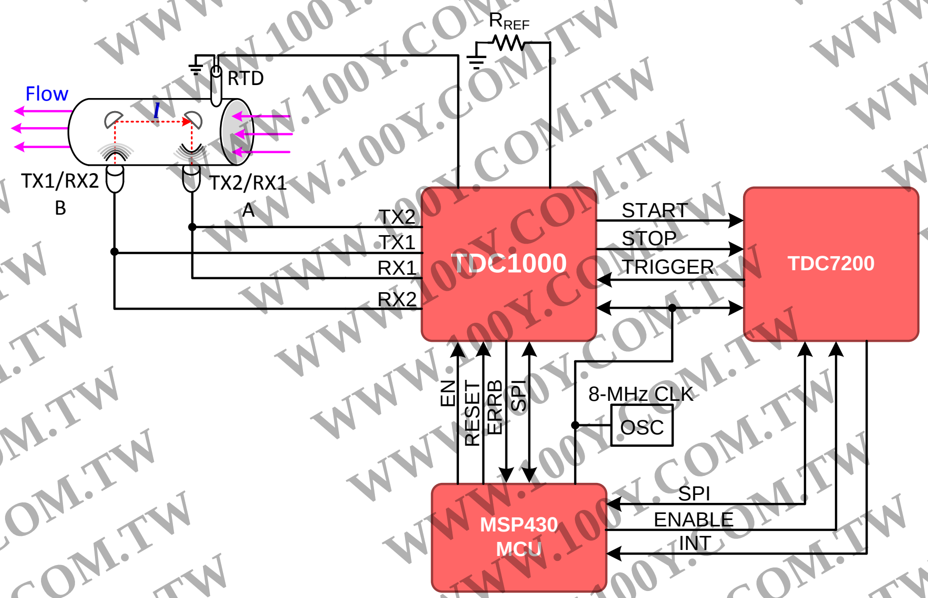


Figure 45. System in Time of Flight Mode

9.2.1 Design Requirements

The parameters in this section are considered for this example.

Table 25. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Pipe diameter	15 mm
Distance between transducers	60 mm
Minimum flow rate	0.015 m^3/h
Accuracy at minimum flow rate	5%

The design of flow-meters requires a thorough technical assessment of the system where the device will be used. The following is a list of areas to consider:

- Minimum and maximum flow rate at maximum allowable error in the system
- Transitional flow rate
- Instantaneous and total quantity pumped over time
- Accuracy of the meter within prescribed limits per applicable standards
- Pressure in the system
- Operating temperature range

The appropriate ultrasonic sensor and the proper electronics for interfacing to the sensor are determined based on the system requirements. The following is a list of specifications applicable to the senor/assembly used in the system:

- Excitation frequency
- Excitation source voltage
- Pipe diameter
- Distance between the transducers (or reflectors)

9.2.2 Detailed Design Procedure

The following subsections describe the detailed design procedure for a flow meter application.

9.2.2.1 Flow Meter Regulations and Accuracy

If the flow meter is intended for residential applications, it must be designed to meet the required standards. For example, per the INTERNATIONAL ORGANIZATION OF LEGAL METROLOGY (OIML), the metrological requirements of water meters are defined by the values of Q1, Q2, Q3 and Q4, which are described in Table 26.

Table 26. Flow-rate Zones per OIML

FLOW-RATE ZONE	DESCRIPTION
Q1	Lowest flow rate at which the meter is to operate within the maximum permissible errors.
Q2	Flow rate between the permanent flow rate and the minimum flow rate that divides the flow rate range into two zones, the upper flow rate zone and the lower flow rate zone, each characterized by its own maximum permissible errors.
Q3	Highest flow rate within the rated operating condition at which the meter is to operate within the maximum permissible errors.
Q4	Highest flow rate at which the meter is to operate for a short period of time within the maximum permissible errors, while maintaining its metrological performance when it is subsequently operating within the rated operating conditions.

A water meter is designated by the numerical value of Q3 in m^3/h and the ratio Q3/Q1. The value of Q3 and the ratio of Q3/Q1 are selected from the lists provided in the OIML standards.

Water meters have to be designed and manufactured such that their errors do not exceed the maximum permissible errors (MPE) defined in the standards. For example, in OIML standards, water meters need to be designated as either accuracy class 1 or accuracy class 2, according to the requirements.

For class 1 water meters, the maximum permissible error in the upper flow rate zone ($Q2 \leq Q \leq Q4$) is ±1%, for temperatures from 0.1°C to 30°C, and ±2% for temperatures greater than 30°C. The maximum permissible error for the lower flow-rate zone ($Q1 \leq Q < Q2$) is ±3%, regardless of the temperature range.

For class 2 water meters, the maximum permissible error for the upper flow rate zone ($Q2 \leq Q \leq Q4$) is ±2%, for temperatures from 0.1°C to 30°C, and ±3% for temperatures greater than 30°C. The maximum permissible error for the lower flow rate zone ($Q1 \leq Q < Q2$) is ±5% regardless of the temperature range.

The flow meter accuracy specified in the standards dictates the required accuracy in the electronics used for driving the ultrasonic transducers, circuits in the receiver path, and time measurement sub circuits. The stringent accuracy required at lower flow rates would require a very low noise signal chain in the transmitter and receiver circuits used in ultrasonic flow meters, as well as the ability to measure picosecond time intervals.

9.2.2.2 Transmit Time in Ultrasonic Flow Meters

Transit-time ultrasonic flow meters works based on the principle that sound waves in a moving fluid travel faster in the direction of flow (downstream), and slower in the opposite direction of flow (upstream).

The system requires at least two transducers. The first transducer operates as a transmitter during the upstream cycle and as a receiver during the downstream cycle, and the second transducer operates as a receiver during the upstream cycle and as a transmitter during the downstream cycle. An ultrasonic flow meter operates by alternating transmit and receive cycles between the pair of transducers and accurately measuring the time-of-flight both directions.

In this example, the upstream TOF is defined as:

$$t_{BA} = \frac{l}{(c - v)}$$

where
- l is the path length between the two transducers in meters (m)
- c is the speed of sound in water in meters per second (m/s)
- v is the velocity of the water in the pipe in meters per second (m/s) (4)

In this example, the downstream TOF is defined as:

$$t_{AB} = \frac{l}{(c + v)}$$

where
- l is the path length between the two transducers in meters (m)
- c is the speed of sound in water in meters per second (m/s)
- v is the velocity of the water in the pipe in meters per second (m/s) (5)

The difference of TOF is defined as:

$$\Delta TOF = t_{BA} - t_{AB}$$

where
- t_{BA} is the upstream TOF from transducer B to transducer A in seconds (s)
- t_{AB} is the downstream TOF from transducer A to transducer B in seconds (s) (6)

After the difference in time-of-flight (ΔTOF) is calculated, the water velocity inside the pipe can be related to the ΔTOF using the following equation:

$$v = \frac{\Delta TOF \times c^2}{2 \times l}$$

where
- c is the speed of sound in water in meters per second (m/s)
- l is the path length between the two transducers in meters (m) (7)

Finally, the mass flow rate can be calculated as follows:

$$Q = k \times v \times A$$

where
- k is the flow-meter constant
- v is the velocity of the water in the pipe in meters per second (m/s)
- A is the cross-section area of the pipe in meters-squared (m^2) (8)

9.2.2.3 ΔTOF Accuracy Requirement Calculation

Based on the minimum mass flow requirement and accuracy requirements in Table 25, the ΔTOF accuracy needed can be calculated as follows:

1. Convert the mass flow rate to m^3/s:

$$Q = (0.015\ m^3/h)\left(\frac{1\ h}{3600\ s}\right) = 4.167x10^{-6}\ m^3/s$$

2. Calculate the flow velocity assuming k = 1:

$$v = \frac{Q}{kA} = \frac{4.167x10^{-6}\ m^3/s}{\pi\left(\frac{0.015\ m}{2}\right)^2} = 0.0236\ m/s$$

3. Calculate the ΔTOF for the given speed of sound. In this example, a speed of sound c = 1400 m/s is assumed:

$$\Delta TOF = \frac{2 \times l \times v}{c^2} = \frac{(2)(0.06\ m)(0.0236\ m/s)}{1400\ m/s^2} = 1.445\ ns$$

4. The requirement of 5% accuracy for minimum flow will result in a ΔTOF accuracy of:

$$\Delta TOF_{error} = (0.05)(1.445\ ns) = 72.25\ ps$$

For this reason, this system requires a high accuracy timer/stopwatch that can measure the lower flow rate state.

The TDC1000 ultrasonic analog-front-end is used to drive the transmitter, amplify and filter the received signal and conditioning the echo for START and STOP pulse generation. The TDC7200 ps-accurate timer is used to measure the time interval between the rising edge of the START pulse and the rising edge of the STOP pulse produced by the TDC1000.

The microcontroller should first configure the TDC7200 and the TDC1000 for the measurement. When the microcontroller issues a start command to the TDC7200 via the SPI interface, the TDC7200 sends a trigger pulse to the TRIGGER pin of the TDC1000. When the TDC1000 drives the transmit transducer, a synchronous START pulse is produced on the START pin, which commands the TDC7200 to start its counters. When a valid echo pulse is received on the receive transducer, the TDC1000 generates a STOP pulse on the STOP pin, which commands the TDC7200 to stop its counters. This procedure is repeated for the upstream and downstream cycles.

A temperature measurement can be performed and the result can be used to correct for temperature dependency of the speed of sound.

9.2.3 Application Curves

Figure 46 , Figure 47, and Figure 48 show data and histograms created with data collected under a zero flow condition at room temperature. A simple offset calibration has been applied, where the overall average of the data is subtracted from the data.

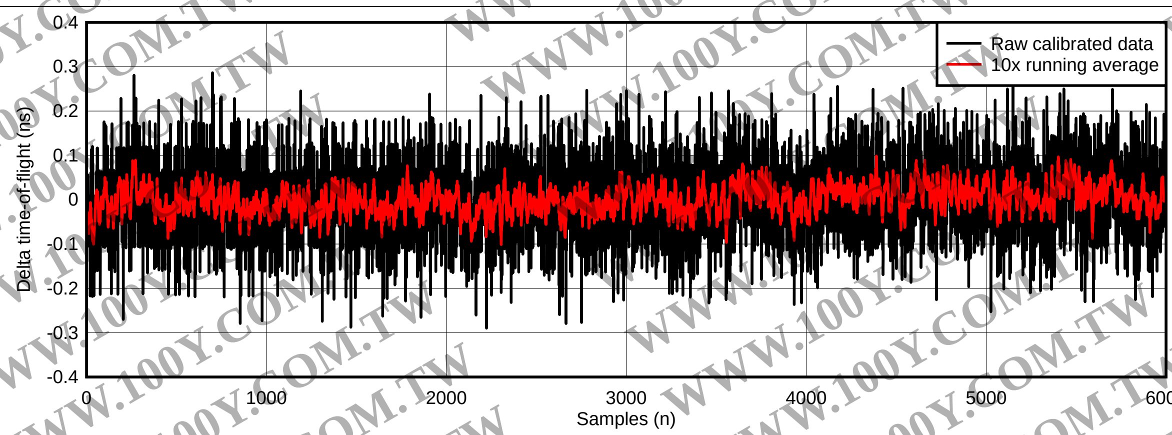


Figure 46. Calibrated Raw and Averaged Delta Time-of-Flight Data

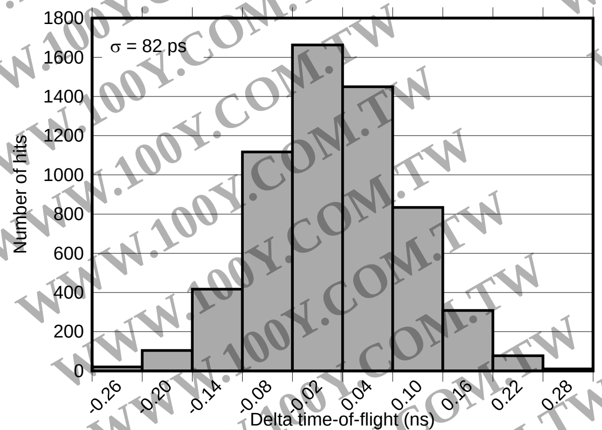


Figure 47. Raw Calibrated Data Histogram

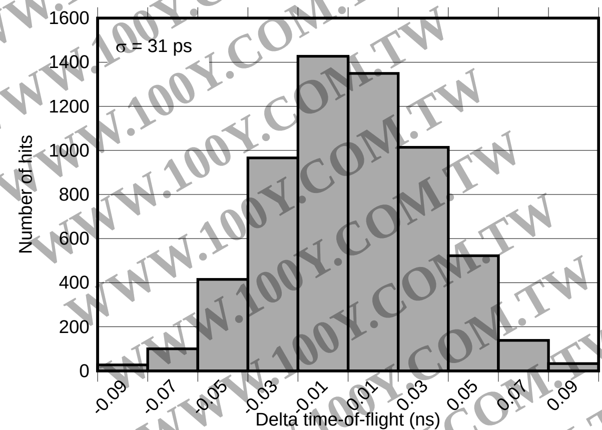


Figure 48. 10x Running Average Data Histogram

9.3 Post Filtering Recommendations

For application such as flow meters where conversion results are accumulated over a long period of time, post filtering is not required. However, for applications where a specific action is taken based on individual conversion results, post filtering is recommended. One advantage of post filtering is to remove the conversion results that are outside of the normal distribution.

One such post filtering method commonly applied by an MCU is the Median Filter Method. The median of a finite number of conversion results can be found by arranging all the conversions from the lowest value to the highest value, and picking the middle one. For example, a conversion result of {50, 51, 49, 40, 51} can be rearranged from lowest to highest {40, 49, 50, 51, 51}, and the median value after applying the Median Filter Method is 50.

9.4 CLOCK Recommendations

A stable, known reference clock is crucial to the ability to measure time, regardless of the time measuring device. Two parameters of a clock source primarily affect the ability to measure time: accuracy and jitter. The following subsections will discuss recommendations for the CLOCK in order to increase accuracy and reduce jitter.

9.4.1 CLOCK Accuracy

CLOCK sources are typically specified with an accuracy value as the clock period is not exactly equal to the nominal value specified. For example, an 8 MHz clock reference may have a 20 ppm accuracy. The true value of the clock period therefore has an error of ±20ppm, and the real frequency is in the range 7.99984 MHz to 8.00016 MHz [8 MHz ± (8 MHz) x $(20/10^6)$].

If the clock accuracy is at this boundary, but the reference time used to calculate the time of flight relates to the nominal 8 MHz clock period, then the time measured will be affected by this error. For example, if the time period measured is 50 µs, and the 8MHz reference clock has +50ppm of error in frequency, but the time measured refers to the 125 ns period (1/8 MHz), then the 50 µs time period will have an error of 50µs x 50/1000000 = 2.5 ns.

In summary, a clock inaccuracy translates proportionally to a time measurement error.

9.4.2 CLOCK Jitter

Clock jitter introduces uncertainty into a time measurement, rather than inaccuracy. As shown in Figure 49, the jitter accumulates on each clock cycle so the uncertainty associated to a time measurement is a function of the clock jitter and the number of clock cycles measured.

Clock_Jitter_Uncertainty = (√n) x (θ_{JITTER}), where n is the number of clock cycles counted, and θ_{JITTER} is the cycle-to-cycle jitter of the clock.

For example, if the time measured is 50 µs using an 8 MHz reference clock, n = 50 µs/(1/8 MHz) = 400 clock cycles. If the RMS cycle-to-cycle jitter, θ_{JITTER} = 10 ps, then the RMS uncertainty introduced in a single measurement is in the order of (√n) x (θ_{JITTER}) = 200 ps.

CLOCK Recommendations (continued)

Because the effect of jitter is random, averaging or accumulating time results reduces the effect of the uncertainty introduced. If the time is measured m times and the result is averaged, then the uncertainty is reduced to: Clock_Jitter_Uncertainty = (√n) x (θ_{JITTER}) / (√m).

For example, if 64 averages are performed in the example above, then the jitter-related uncertainty is reduced to 25 ps RMS.

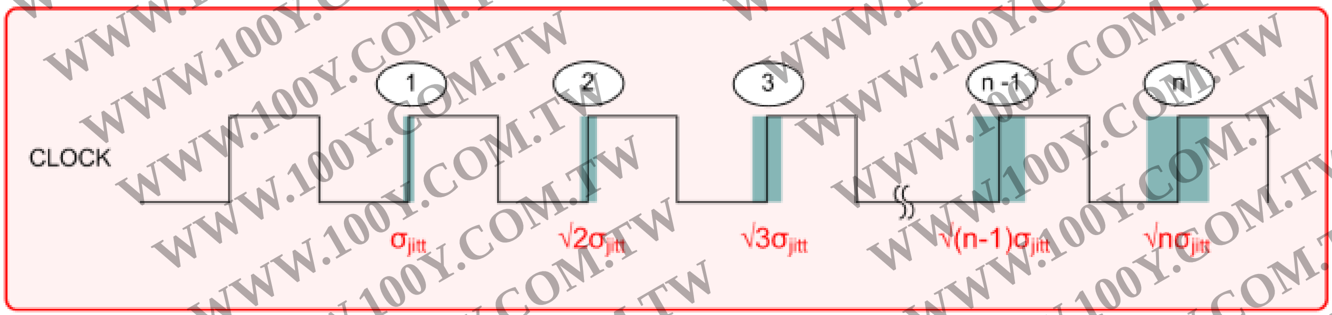


Figure 49. CLOCK Jitter

10 Power Supply Recommendations

The analog circuitry of the TDC7200 is designed to operate from an input voltage supply range between 2 V and 3.6 V. It is recommended to place a 100 nF ceramic bypass capacitor to ground as close as possible to the VDD pins. In addition, an electrolytic or tantalum capacitor with value greater than 1 µF is recommended. The bulk capacitor does not need to be in close vicinity with the TDC7200 and could be close to the voltage source terminals or at the output of the voltage regulators powering the TDC7200.

11 Layout

11.1 Layout Guidelines

- In a 4-layer board design, the recommended layer stack order from top to bottom is: signal, ground, power and signal.
- Bypass capacitors should be placed in close proximity to the VDD pin.
- The length of the START and STOP traces from the TDC7200 to the stopwatch/MCU should be matched to prevent uneven signal delays. Also, avoid unnecessary via-holes on these traces and keep the routing as short/direct as possible to minimize parasitic capacitance on the PCB.
- Route the SPI signal traces close together. Place a series resistor at the source of DOUT (close to the TDC7200) and series resistors at the sources of DIN, SCLK, and CSB (close to the master MCU).

11.2 Layout Example

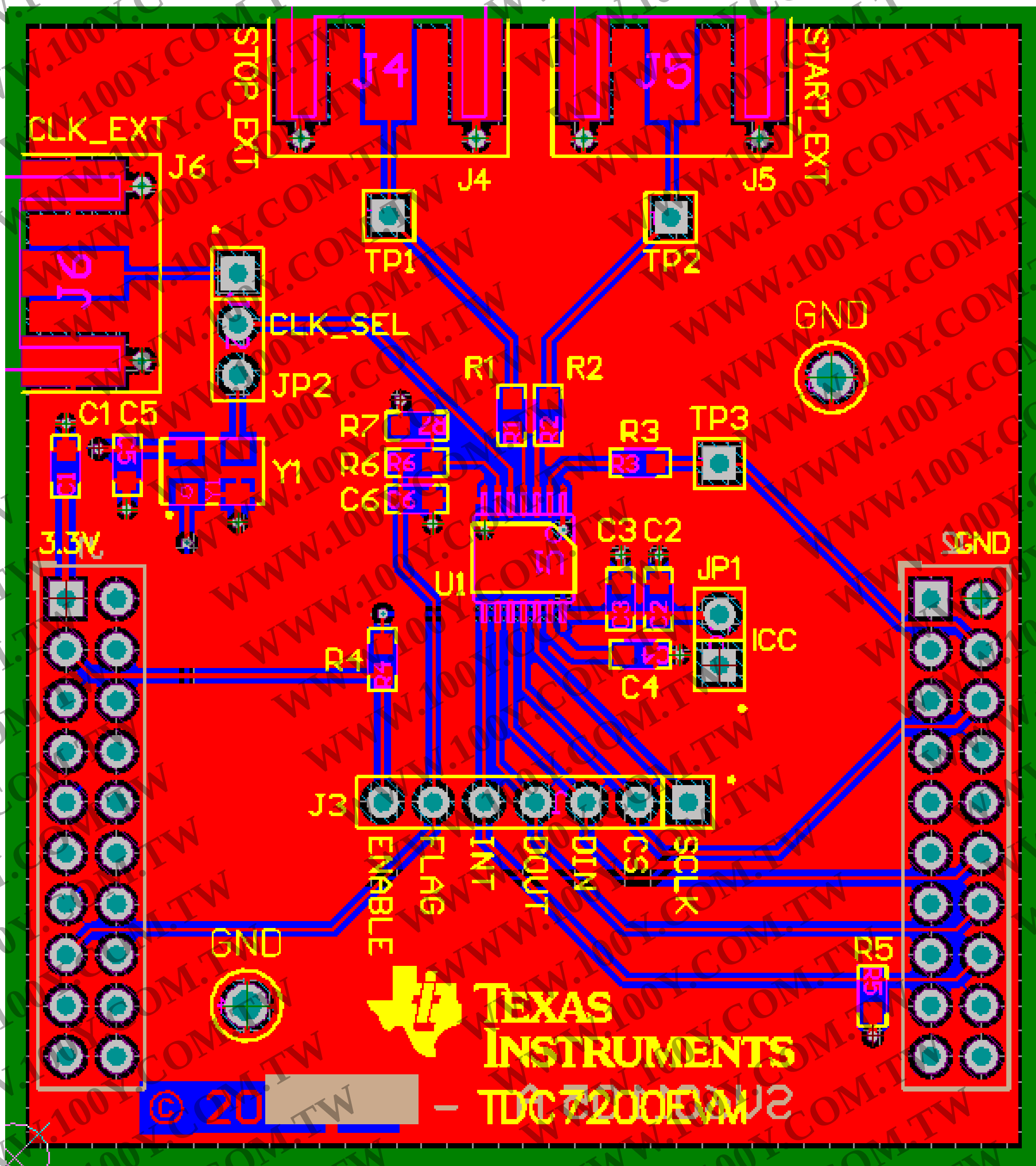


Figure 50. TDC7200EVM Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- TDC1000 : Ultrasonic Sensing Analog Front End for Level, Concentration, Flow & Proximity Sensing Applications.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
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12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TDC7200PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	T7200	Samples
TDC7200PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	T7200	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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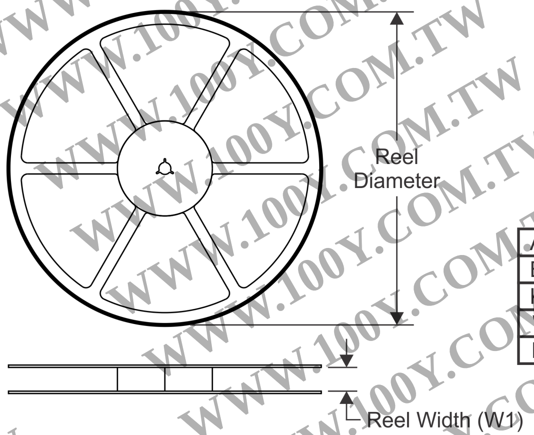
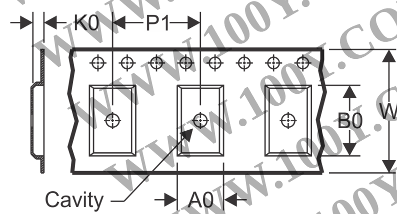
TAPE AND REEL INFORMATION

REEL DIMENSIONS

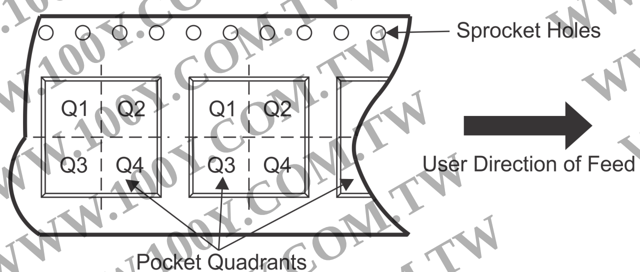


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

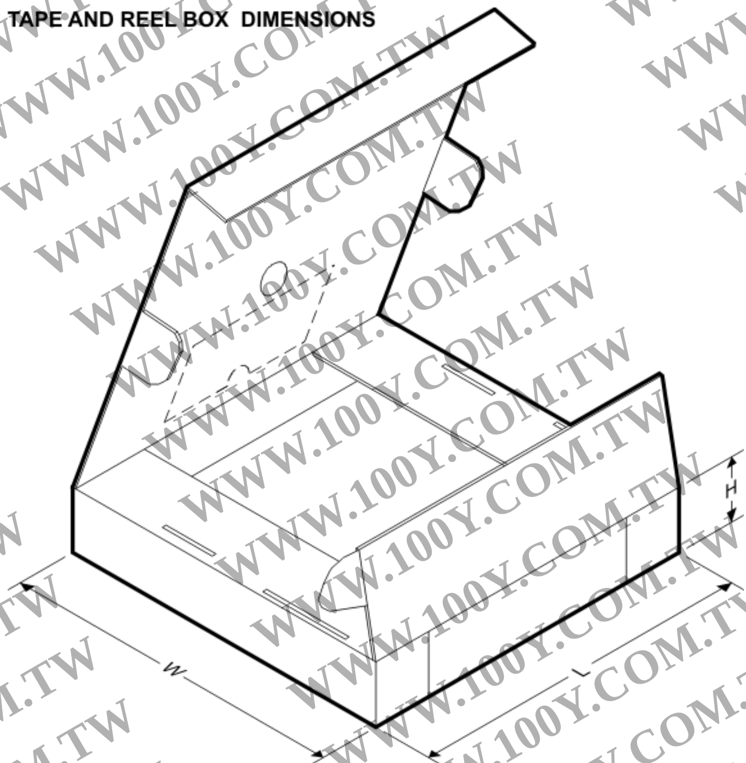
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TDC7200PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

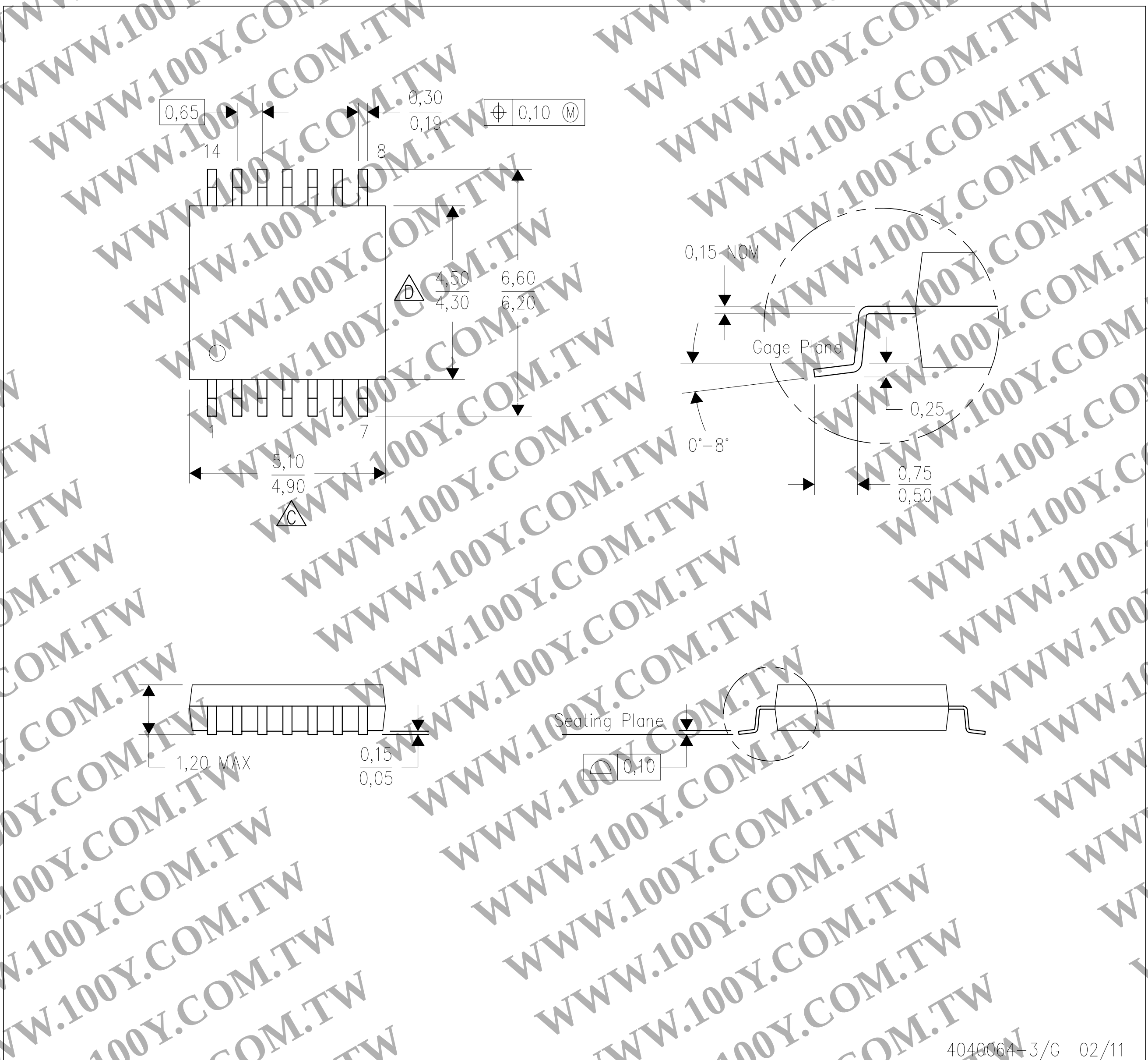
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

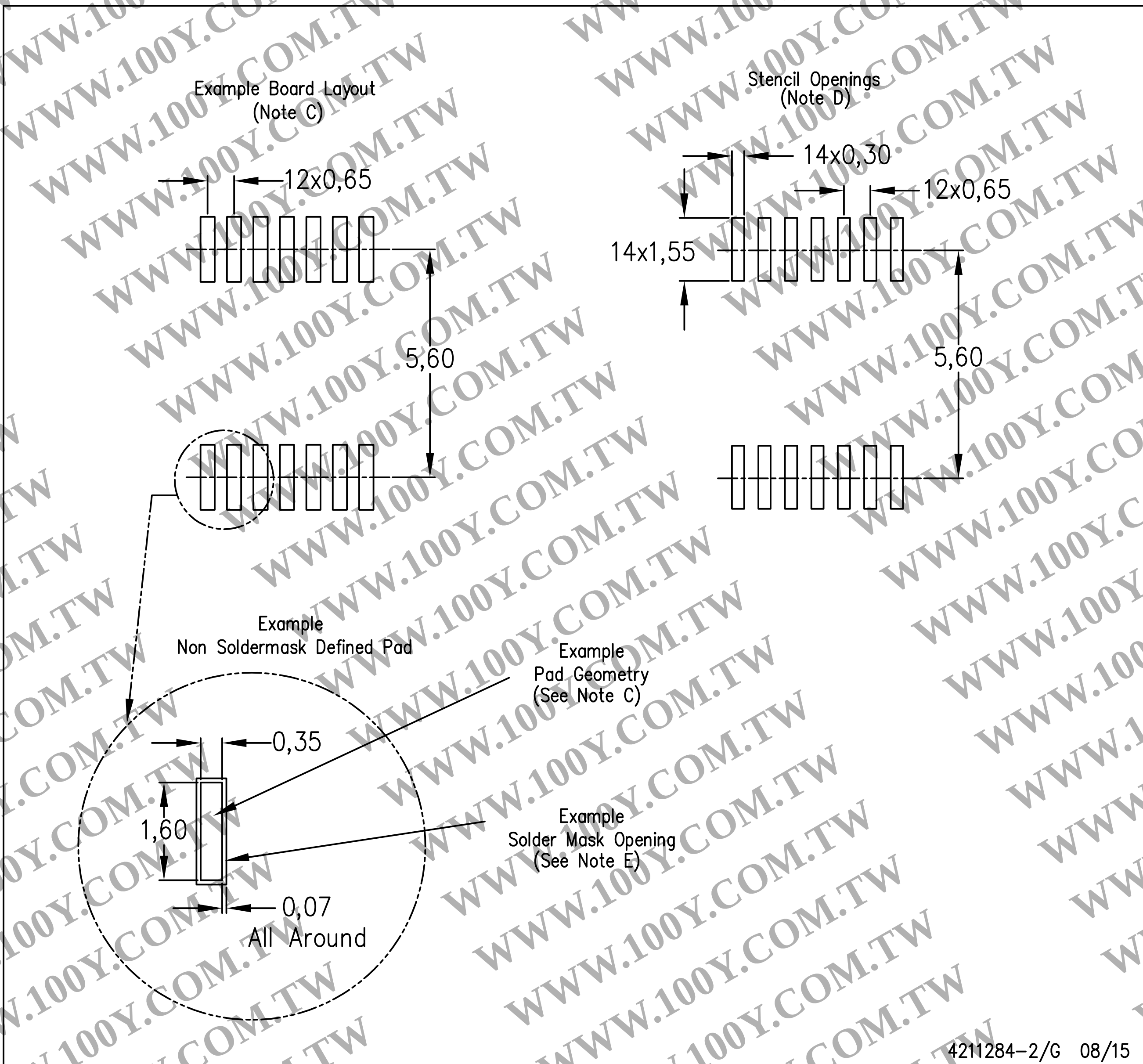
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TDC7200PWR	TSSOP	PW	14	2000	367.0	367.0	35.0

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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