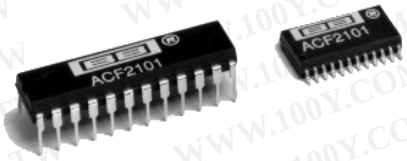
BURR-BROWN®



ACF2101

Low Noise, Dual SWITCHED INTEGRATOR

FEATURES

- INCLUDES INTEGRATION CAPACITOR, RESET AND HOLD SWITCHES, AND OUTPUT MULTIPLEXER
- LOW NOISE: 10μVrms
- LOW CHARGE TRANSFER: 0.1pC
- WIDE DYNAMIC RANGE: 120dB
- LOW BIAS CURRENT: 100fA

APPLICATIONS

- CURRENT TO VOLTAGE CONVERSION
- PHOTODIODE INTEGRATOR
- CURRENT MEASUREMENT
- CHARGE MEASUREMENT
- CT SCANNER FRONT END
- MEDICAL, SCIENTIFIC, AND INDUSTRIAL INSTRUMENTATION

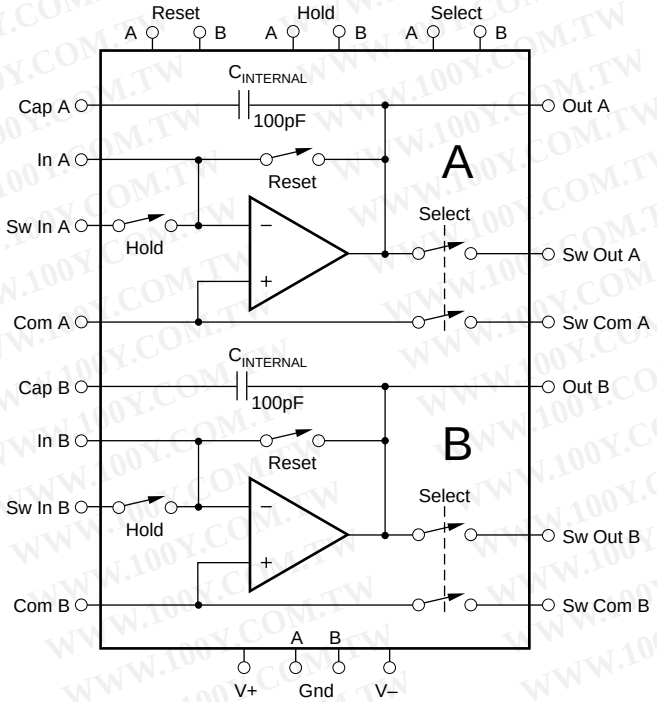
DESCRIPTION

The ACF2101 is a dual switched integrator for precision applications. Each channel can convert an input current to an output voltage by integration, using either an internal or external capacitor. Included on the chip are precision 100pF integration capacitors, hold and reset switches, and output multiplexers.

As a complete circuit on a single chip, the ACF2101 eliminates many of the problems commonly encountered in discrete designs, such as leakage current errors and noise pickup. The integrating approach can provide lower noise than conventional transimpedance amplifier designs and also eliminates the need for high performance, high value feedback resistors.

The extremely low bias current and low noise of the ACF2101's ***Difet®*** amplifiers, along with active laser trimming of both offset and drift, assure precision current to voltage conversion.

Although designed for +5V, –15V supplies, the ACF2101 can be operated on supplies up to ±18VDC. It is available in both 24-pin plastic DIP and SOIC packages.



Difet® Burr-Brown Corp.

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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V+ = +5V, V– = –15V, Internal $C_{INTEGRATION}$ = $C_{INTERNAL}$ = 100pF, unless otherwise noted.

PARAMETER	CONDITIONS	ACF2101BP, BU MIN	ACF2101BP, BU TYP	ACF2101BP, BU MAX	UNITS
ANALOG INPUT					
INPUT RANGE					
Input Current Range					
Switched Input (Sw In A, Sw In B)				±100	µA
Direct Input (In A, In B)				±100	µA
INPUT IMPEDANCE					
Switched Input					
Hold Switch OFF			1000		GΩ
Hold Switch ON			1.5		kΩ
Direct Input			Virtual Ground		
HOLD SWITCH VOLTAGE					
Hold Switch Withstand Voltage	Hold Switch OFF	–10		+0.5	V
OFFSET VOLTAGE					
Input Offset Voltage			±0.5	±2	mV
Average Drift			±1	±5	µV/°C
DIGITAL INPUTS					
Logic Family	TTL Compatible				
V_{IH} (Logic 1 = Switch OFF)		2		5.5	V
V_{IL} (Logic 0 = Switch ON)		–0.5		0.8	V
I_{IH}	V_{IH} = +5V		2		µA
I_{IL}	V_{IL} = 0V		0		µA
Switching Speed (All Switches)					
Switch ON			200		ns
Switch OFF			200		ns
TRANSFER CHARACTERISTICS					
TRANSFER FUNCTION			$V_{OUT} = -\frac{1}{C_{INTEGRATION}}\int I_{IN}dt$		V
DYNAMIC CHARACTERISTICS					
Integrate Mode					
Slew Rate		1	3		V/µs
Reset Mode					
Slew Rate			3		V/µs
Settling Time to 0.01%FSR[1]	10V Step		5	10	µs
Overload Recovery	Positive or Negative		5		µs
Output Multiplexer (Select Switches)					
Settling Time to 0.01%FSR	C_{LOAD} < 1000pF		6.5		µs
Settling Time to 0.01%FSR	C_{LOAD} < 100pF		2		µs
INTEGRATION CAPACITOR ($C_{INTERNAL}$)					
Internal Capacitor					
Value			100		pF
Accuracy			0.5	2	%
Temperature Coefficient		–50	–25	0	ppm/°C
Memory			30	100	ppm of FSR
RESET SWITCH					
Impedance					
Reset OFF			1000		GΩ
Reset ON			1.5		kΩ
MODES OF OPERATION					
Switch	Hold / Reset				
Integrate Mode	ON / OFF				
Hold Mode	OFF / OFF				
Reset Mode	ON/OFF / ON				
(Logic 1 = OFF, Logic 0 = ON)					

SPECIFICATIONS (CONT)

At T_A = +25°C, V+ = +5V, V– = –15V, Internal $C_{INTEGRATION} = C_{INTERNAL}$ = 100pF, unless otherwise noted.

PARAMETER	CONDITIONS	ACF2101BP, BU MIN	ACF2101BP, BU TYP	ACF2101BP, BU MAX	UNITS
OUTPUT					
Voltage Output Range (All Outputs)		–10	–13.5, +1.0	+0.5	V
Current Output, Direct Output (Out A, Out B)		±5			mA
Short Circuit Current					
Direct Output			±25		mA
Switched Output (Sw Out A, Sw Out B)		±2	±8		mA
Select Switch Withstand Voltage					
Switched Output		–10		+0.5	V
Switched Common (Sw Com A, Sw Com B)		–0.5		+0.5	V
Output Impedance					
Direct Output			0.1		Ω
Switched Output					
Select Switch ON			250 || 5		Ω || pF
Select Switch OFF			1000 || 4		GΩ || pF
Leakage Current	Select Switch OFF		10	100	pA
Load Capacitance Stability					
Direct Output			500		pF
Switched Output			Any		pF
OUTPUT ACCURACY					
Nonlinearity			±0.005	±0.01	%FSR
Channel Separation			–80		dB
Op Amp Bias Current					
Value			100	1000	fA
Temperature Coefficient			Doubles Each +10°C		
Hold Mode Droop			1	10	nV/µs
Integrate Mode Droop			1	10	nV/µs
Voltage Offset[2]					
Value			3		mV
Temperature Coefficient			5		µV/°C
Power Supply Rejection	V_S = +4.5V to +18V, –10V to –18V	80	100		dB
OUTPUT NOISE					
Total Output Noise[3]	BW = 0.1Hz to 10Hz		2		µVrms
Integrate Mode[4]	BW = 0.1Hz to 250kHz		$10(1 + C_{IN}/C_{INTEGRATION})$		µVrms
Hold Mode	BW = 0.1Hz to 250kHz		10		µVrms
Reset Mode	BW = 0.1Hz to 250kHz		10		µVrms
CHARGE TRANSFER ERRORS[5]					
Reset to Integrate Mode[6]					
Charge Transfer			0.1	0.5	pC
Charge Transfer TC			0.2		fC/°C
Charge Offset Error			1	5	mV
Charge Offset TC			2		µV/°C
Integrate to Hold Mode	C_{IN} > 50pF				
Charge Transfer			0.2	1	pC
Charge Transfer TC			0.4		fC/°C
Charge Offset Error			2	10	mV
Charge Offset TC			4		µV/°C
Hold to Integrate Mode	C_{IN} > 50pF				
Charge Transfer			0.2	1	pC
Charge Transfer TC			0.4		fC/°C
Charge Offset Error			2	10	mV
Charge Offset TC			4		µV/°C
POWER SUPPLY					
Specified Operating Voltage			+5, –15		V
Operating Voltage Range					
Positive Supply		+4.5		+18	V
Negative Supply		–10		–18	V
Current					
Positive Supply	For Dual		12	15	mA
Negative Supply	For Dual		3.5	5.2	mA
TEMPERATURE RANGE					
Specification		–40		+85	°C
Operation		–40		+125	°C
Storage		–40		+125	°C
Thermal Resistance (both packages)	Junction to Ambient		100		°C/W

NOTES: (1) FSR is Full Scale Range = 10V (0 to –10V). (2) Includes offset errors from all modes of operation. (3) Total noise is rms total of noise for the modes of operation used. (4) C_{IN} = capacitance of sensor connected to ACF2101 input; $C_{INTERGRATION}$ = integration capacitance = $C_{INTERNAL} + C_{EXTERNAL}$. (5) Errors created when the internal switches are driven from one mode to another. (6) The charge transfer is 0.1pC; for an integration capacitance of 100pF, the resultant charge offset voltage error is 1mV.

ABSOLUTE MAXIMUM RATINGS

Supply	±18V
Input Current	±5mA
Output Short Circuit Duration	Continuous to Ground
Power Dissipation	500mW
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE/ORDERING INFORMATION

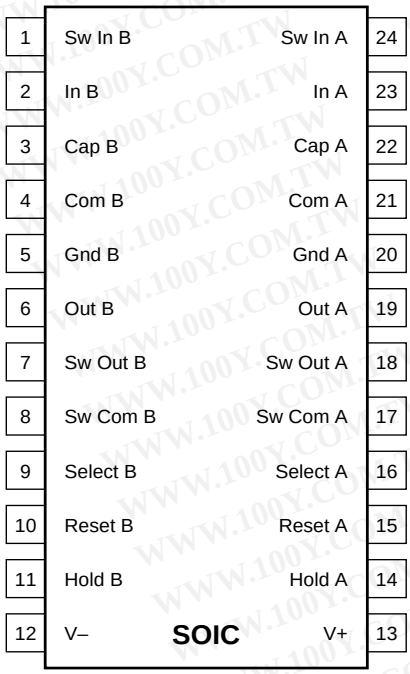
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
ACF2101BP	24-Pin Plastic DIP	243	–40°C to +85°C
ACF2101BU	24-Pin Plastic SOIC	239	–40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN CONFIGURATION

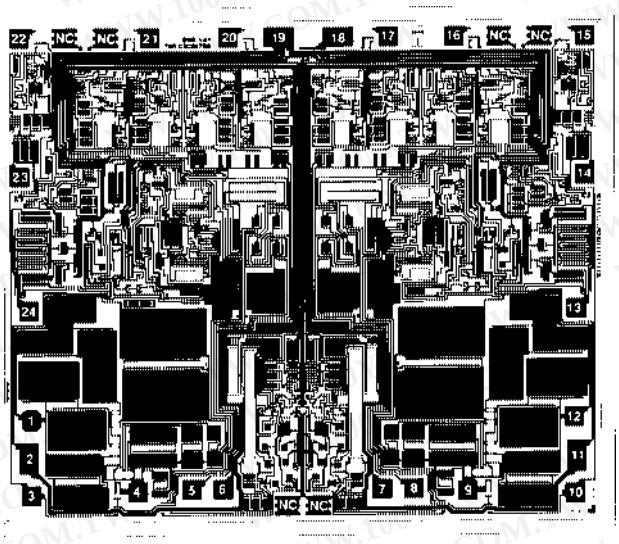
DIP and SOIC package have different pinouts.

TOP VIEW **ACF2101BU**



TOP VIEW **ACF2101BP**

DICE INFORMATION



ACF2101 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	A Out	13	B Switch-Out
2	A Ground	14	B Switch-Common
3	A Common	15	B Select
4	A Cap	16	B Reset
5	A In	17	B Hold
6	A Switch-In	18	V–
7	B Switch-In	19	V+
8	B In	20	A Hold
9	B Cap	21	A Reset
10	B Common	22	A Select
11	B Ground	23	A Switch-Common
12	B Out	24	A Switch-Out

Substrate Bias: Ground.

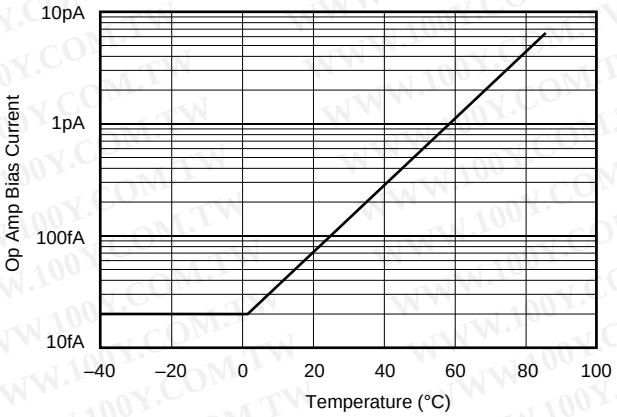
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	132 x 157 ±5	3.35 x 3.99 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		None

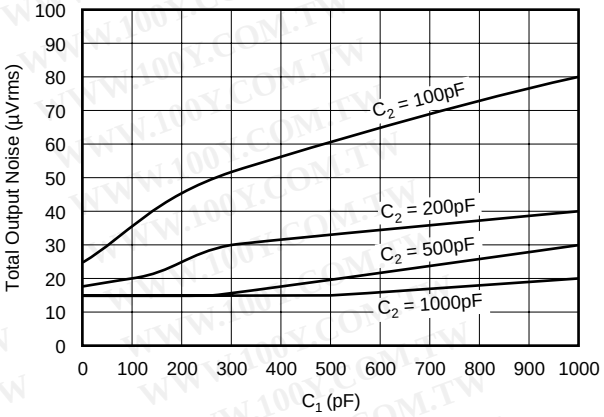
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V+ = +5V, V– = –15V, $C_{INTEGRATION}$ = $C_{INTERNAL}$ = 100pF, unless otherwise noted.

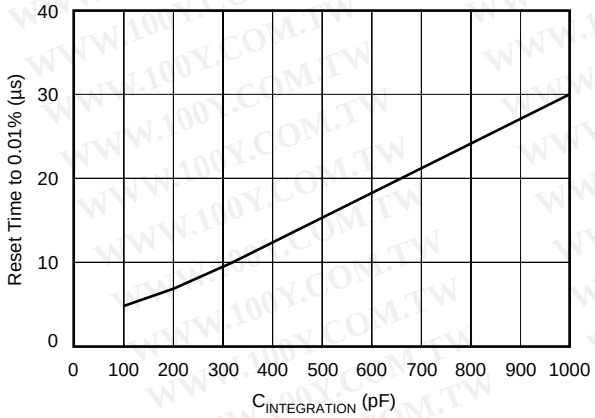
BIAS CURRENT vs TEMPERATURE



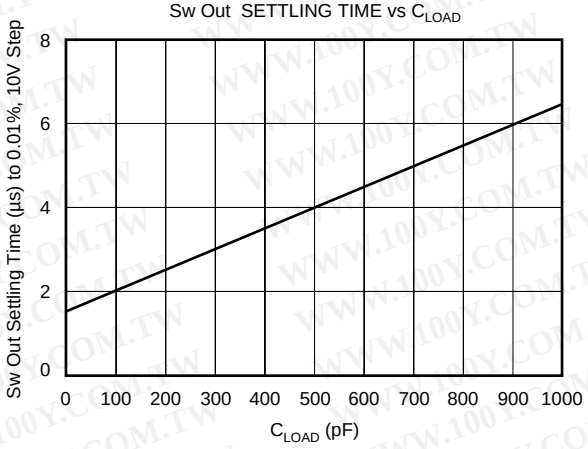
TOTAL OUTPUT NOISE vs C_1 and C_2



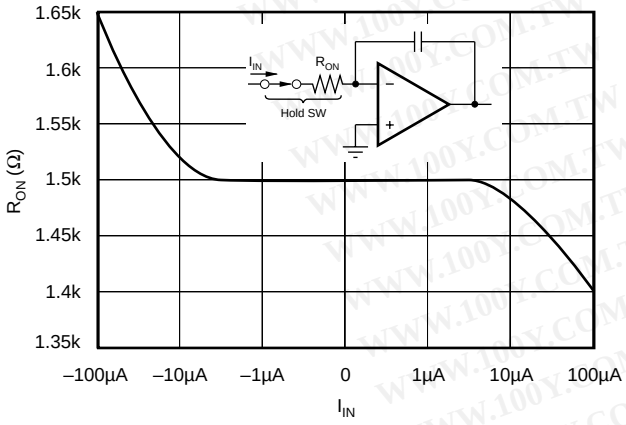
RESET TIME vs $C_{INTEGRATION}$



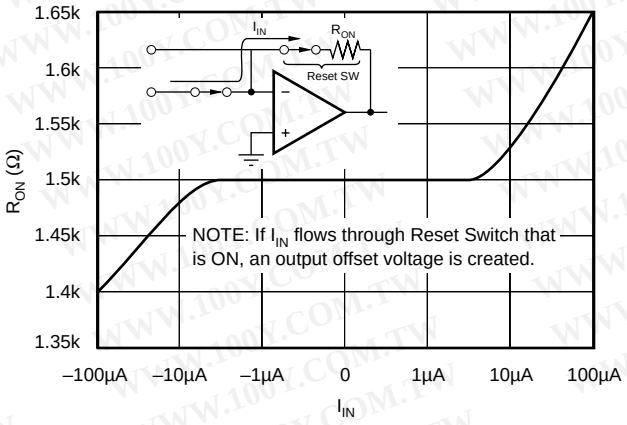
Sw Out SETTLING TIME vs C_{LOAD}



HOLD SWITCH R_{ON} vs INPUT CURRENT



RESET SWITCH R_{ON} vs INPUT CURRENT



APPLICATIONS INFORMATION

BASIC CIRCUIT CONNECTION

Basic Layout

As with any precision circuit, careful layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance—especially at the analog and digital input pins.

Figures 1a and 1b illustrate the basic connections needed for operation. Figures 1c and 1d illustrate the addition of external integration capacitors and input guards.

Leakage currents between printed circuit board traces can easily exceed the input bias current of the ACF2101. A circuit board "guard" pattern reduces leakage effects by surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential. Leakage will flow harmlessly to the low impedance node. Figure 2a and 2b show printed circuit patterns that can be used to guard critical pins. Note that traces leading to these pins should also be guarded.

Improper handling or cleaning may increase droop. Contamination from handling parts and circuit boards can be removed with cleaning solvents and de-ionized water.

Pinout

The pinout for the DIP and SOIC package of the ACF2101 is different. The pinouts for the different packages are shown in several figures in this data sheet.

Power Supplies

The ACF2101 can operate from supplies that range from +4.5V and –10V to ±18V. Since the output voltage integrates negatively from ground, a positive supply of +5V is sufficient to attain specified performance. Using +5V and –15V power supplies reduces power dissipation by one-half of that at ±15V.

Power supply connections should be bypassed with good high-frequency capacitors, such as 1µF solid tantalum capacitors, positioned close to the power supply pins.

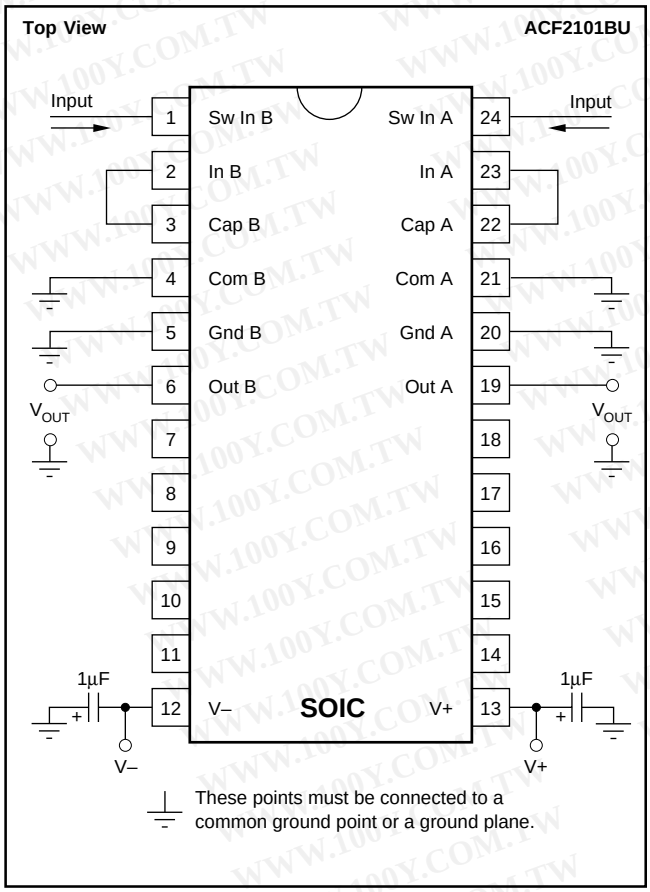


FIGURE 1a. Basic Circuit Connections, **SOIC package**.

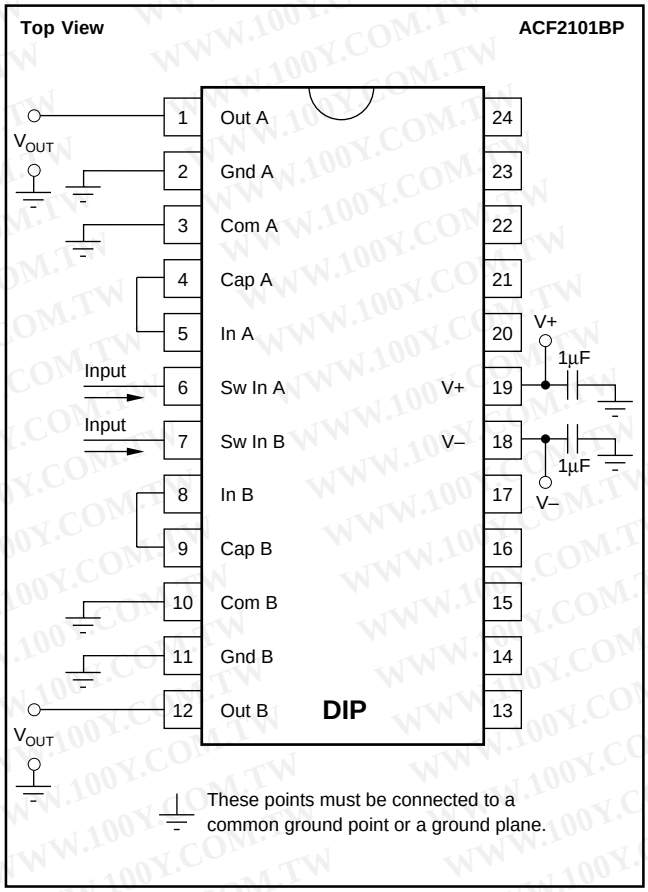


FIGURE 1b. Basic Circuit Connections, **DIP**.

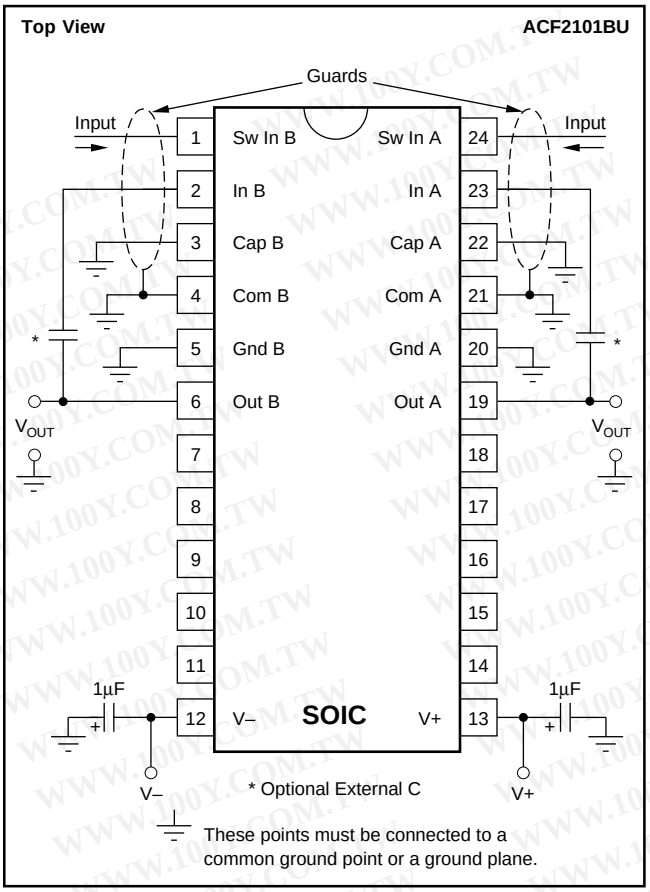


FIGURE 1c. Circuit Connections with External Capacitors and Guarding, **SOIC package**.

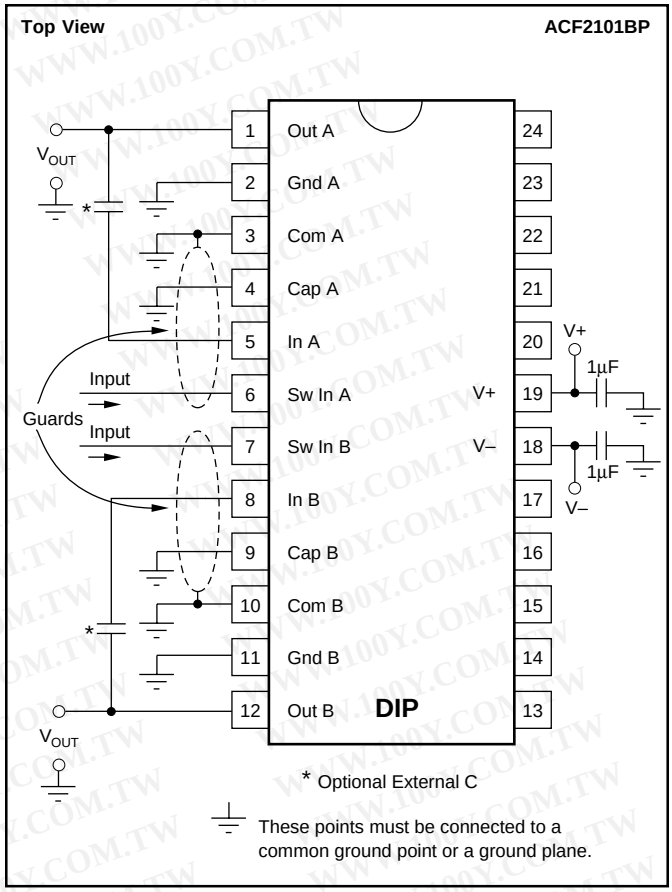


FIGURE 1d. Circuit Connections with External Capacitors and Guarding, **DIP**.

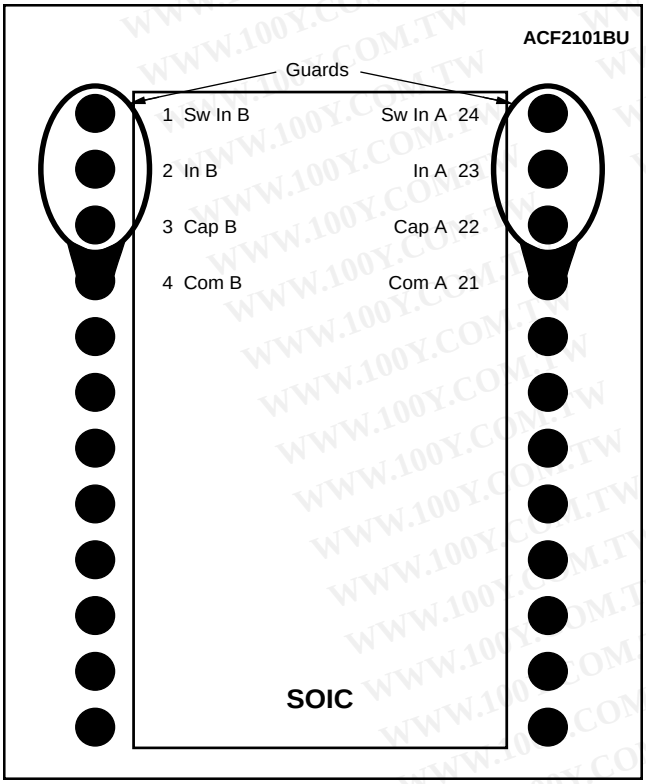


FIGURE 2a. PC Board Layout Showing “Guard” Traces for Input, **SOIC package**. Both top and bottom of board should be guarded.

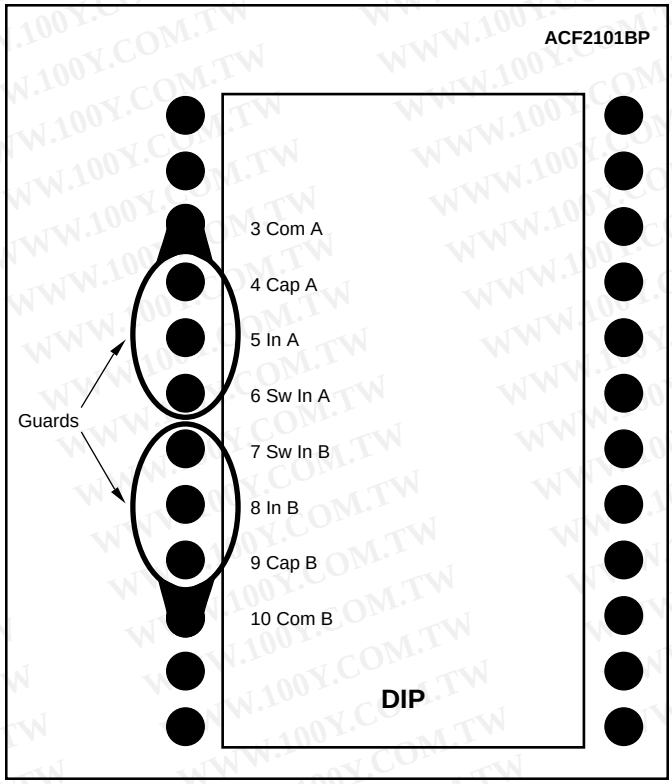


FIGURE 2b. PC Board Layout Showing “Guard” Traces for Input, **DIP**. Both top and bottom of board should be guarded.

MODES OF OPERATION

The three basic modes of operation of each integrator are controlled by the Hold and Reset switches. In Integrate mode, the output voltage integrates negatively toward –10V. In Hold mode, the output voltage remains at the present value, except for output droop. In Reset mode, the integration capacitor is discharged and the output voltage is driven to analog common. See Figure 4.

SWITCHES

Each integrator includes four switches: a Hold switch, a Reset switch, and two output Select switches. See Figure 3.

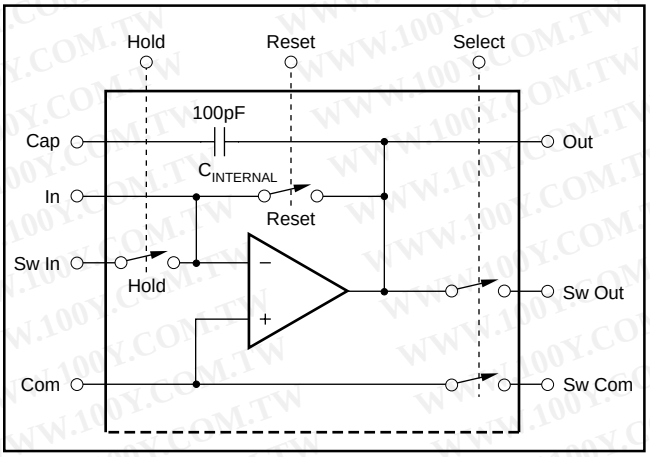
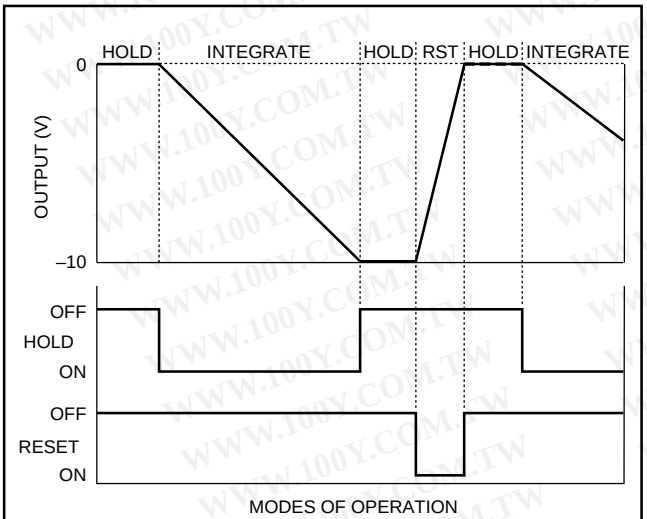


FIGURE 3. Switch Control Lines on One Channel of Two in ACF2101.



SWITCH	MODE OF OPERATION		
	Integrate	Hold	Reset
Hold Switch	ON	OFF	ON/OFF
Reset Switch	OFF	OFF	ON

ON: Switch shorted; Logic 0 input. OFF: Switch open; Logic 1 input.

FIGURE 4. Modes of Operation.

Hold and Reset Switches

To use the Hold switch, connect the input current to the "Sw In" pin. The Hold switch disconnects the input current, and holds the output voltage at a fixed level. For direct input, connect the input current to the "In" pin that bypasses the Hold switch and connects directly to the input summing junction. If the Hold switch is not used, the switch should be in the off mode and the "Sw In" pin should be connected to analog common.

The Reset switch is used to discharge the integration capacitor before the start of a new integration period. See Typical Performance Curve showing Reset Time vs $C_{INTEGRATION}$.

Select Switches

The two Select switches can be used to multiplex the outputs when multiple integrators are connected to a common bus. Figure 5 shows a number of ACF2101s multiplexed together into an A/D converter. The output settling time is determined by the Select switch "on" resistance of 250Ω and the total output capacitance. The total output capacitance includes the ACF2101 output capacitances plus the capacitance of the interconnections to the A/D converter.

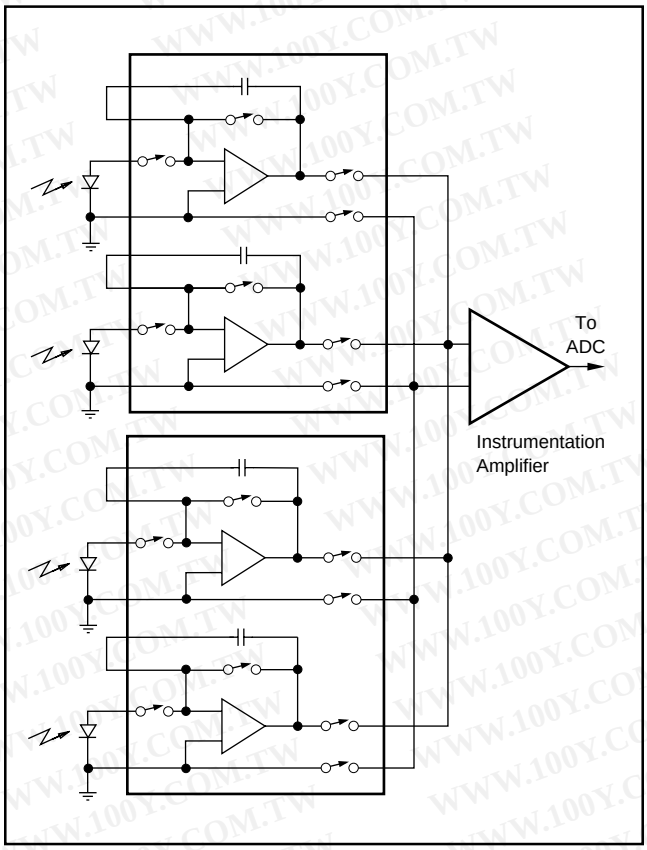


FIGURE 5. ACF2101s in Multiplexed Operation.

OUTPUT VOLTAGE

The integrator output voltage range is from +0.5V to –10V. The output voltage (V_{OUT}) can be calculated as:

$$V_{OUT} = \frac{I_{IN} \times \Delta t}{C_{INT}}$$

V_{OUT} = the maximum output voltage (in volts)
C_{INT} = the integration capacitance (in farads)
I_{IN} = the input current (in amperes)
Δt = the integration time (in seconds)

Examples of Component Values for –10V Output

i_{IN} (µA)	Δt (s)	C_{INT} (pF)	V_{OUT} (V)
0.01	100m	100	–10
0.1	10m	100	–10
1	1m	100	–10
10	100µ	100	–10
100	10µ	100	–10
10	1m	1000	–10
100	100µ	1000	–10

OUTPUT OVERLOAD

When the output to the ACF2101 integrates to the negative limit, the output voltage smoothly limits at approximately 1.5V from the negative power supply, and reset time will increase by approximately 5µs for overload recovery. For fastest reset time avoid integrating to the negative limit.

EXTERNAL CAPACITOR

An external integration capacitor may be used instead of or in addition to the internal 100pF integration capacitor. Since the transfer function depends upon the characteristics of the integration capacitor, it must be carefully selected. An external integration capacitor should have low voltage coefficient, temperature coefficient, memory, and leakage current. The optimum selection depends upon the requirements of the specific application. Suitable types include NPO ceramic, polycarbonate, polystyrene, and silver mica. If the internal integration capacitor is not used, the Cap pin should be connected to common.

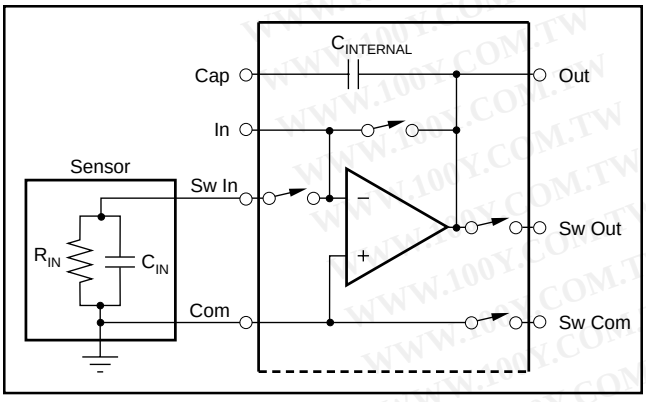


FIGURE 6. Capacitance of Circuit at Input of Integrator.

NOISE

The total output noise for a specific application of the ACF2101 is the rms total of the noise in the modes used: Integrate noise (e_{nI}), Hold noise (e_{nH}) and Reset noise (e_{nR}). The noise in both the Hold (e_{nH}) and Reset (e_{nR}) modes is 10µVrms. The noise in the Integrate mode (e_{nI}) is directly proportional to one plus the ratio of C_{IN} to $C_{INTEGRATION}$, where C_{IN} is the capacitance of the circuit at the input of the integrator and $C_{INTEGRATION} = C_{INTERNAL} + C_{EXTERNAL}$ and is the integration capacitance:

$$\text{Integrate output noise } (e_{nI}) = (10\mu\text{Vrms}) \times (1 + C_{IN}/C_{INTEGRATION})$$

Therefore, for very low C_{IN}, the Integrate noise will approach 10µVrms. The total noise when in the Hold mode after proceeding through Reset and Integrate modes is approximated as shown below.

$$\text{Total Noise} = \sqrt{e_{nI}^2 + e_{nH}^2 + e_{nR}^2}$$

See Typical Performance Curve showing Total Output Noise vs C_{IN} and $C_{INTEGRATION}$ for more accurate noise data under specific circumstances. If only the Integrate and Reset modes are used, the total noise is the rms sum of the noise of the two modes as shown below.

$$\text{Total Noise} = \sqrt{e_{nI}^2 + e_{nR}^2}$$

DYNAMIC CHARACTERISTICS

Frequency Response

The ACF2101 switched integrator is a sampled system controlled by the sampling frequency (fs), which is usually dominated by the integration time. Input signals above the Nyquist frequency (fs/2) create errors by being aliased into the sampled frequency bandwidth. The sampled frequency bandwidth of the switched integrator has a –3dB characteristic at fs/2.26 and a null at fs and harmonics 2fs, 3fs, 4fs, etc. This characteristic is often used to eliminate known interference.

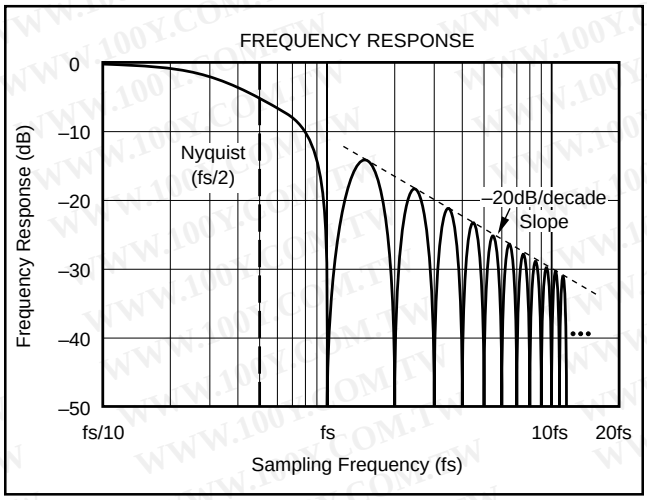


FIGURE 7. Frequency Response.

Charge Transfer

Charge transfer is the charge that is coupled from the logic control inputs through circuit capacitance to the integration capacitor when the Hold and Reset switches change mode. Careful printed circuit layout must be used to minimize external coupling from digital to analog circuitry and the resulting charge transfer. Charge transfer results in a DC charge offset error voltage. The ACF2101 switches are compensated to reduce charge transfer errors.

Since the ACF2101 switches contribute equal and opposite charge for positive and negative logic input transitions, the total error due to charge transfer is determined by the switching sequence. For each switch, a logic transition results in a specific charge (and offset voltage) while an opposite going logic transition results in an opposite charge (and opposite offset voltage). Thus, if the Hold switch is turned on and off during one integration cycle, the total charge transfer at the end of the sequence due to the Hold switch is essentially zero.

The amount of charge transfer to the integration capacitor is constant for each switch. Therefore, the charge offset error voltage is lower for larger integration capacitors. The ACF2101's 0.1pC charge transfer results in a 1mV charge offset voltage when using the 100pF internal integration capacitor. The offset voltage will change linearly with the integration capacitance. That is, 50pF will result in a 2mV charge offset and 200pF in a 0.5mV charge offset.

Droop

Droop is the change in the output voltage over time as a result of the bias current of the amplifier, leakage of the integration capacitor and leakage of the Reset and Hold switches. Droop occurs in both the Integrate and Hold modes of operation. Careful printed circuit layout must be used to minimize external leakage currents as discussed previously.

The droop is calculated by the equation:

$$\text{Droop} = \frac{100\text{fA}}{C_{\text{INTEGRATION}}}$$

where $C_{\text{INTEGRATION}} = C_{\text{INTERNAL}} + C_{\text{EXTERNAL}}$ and is the integration capacitance in farads and the result is in volts per second. For the internal integration capacitance of 100pF, the droop is calculated as:

$$\text{Droop} = \frac{100 \text{ X } 10^{-15}}{100 \text{ X } 10^{-12}} = 1\text{mV/s or } 1\text{nV/}\mu\text{s}$$

Droop increases by a factor of 2 for each 10°C increase above 25°C. See the typical performance curve showing Bias Current vs Temperature.

Capacitive Loads

Any capacitive load can be safely driven through the multiplexed output of the ACF2101. As with any op amp, however, best dynamic performance of the ACF2101 can be achieved by minimizing the capacitive load. See the typical performance curve showing settling time as a function of capacitive load for more information. A large capacitive load is often useful in reducing the noise of systems not requiring the full bandwidth of the ACF2101.

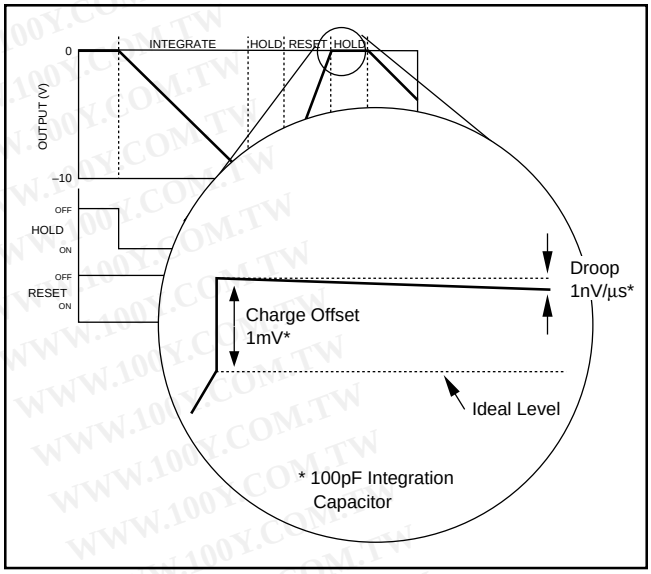


FIGURE 8. Droop and Charge Offset Effects.

PROGRAMMABLE I TO V CONVERTER EXAMPLE

Figure 10 illustrates the use of the ACF2101 as a programmable current to voltage converter. The output of the circuit, V_{OUT}, is a DC level for a constant current input. The timing diagram shown in Figure 9 shows V_{OUT} for an input current that varies from one sample to the next. This circuit offers wide dynamic range without the use of extremely large resistors. An ACF2101 and an OPA2107 op amp are configured to convert a low level input current to an output voltage. The equivalent gain of the converter is determined by the frequency of the digital input signal, f_S. The inherent integrating function of the ACF2101 is very useful for rejection of noise such as power line pickup.

The ACF2101 integrates the current signal for the period of f_S. The magnitude of the ramp voltage at the output of the ACF2101 is a function of the frequency of f_S and the value of the integration capacitor, $C_{\text{INTEGRATION}}$. The ACF2101's 100pF internal capacitor is used for $C_{\text{INTEGRATION}}$ in this example. The effect is that f_S controls the equivalent feedback resistance of a transconductance (current-to-voltage) amplifier. The equivalent feedback resistance range can vary over a large range of at least 1MΩ to 1GΩ as illustrated in the accompanying table. Larger equivalent feedback resistances can be obtained if internal capacitances smaller than 100pF are used with the ACF2101.

A simplified equation for the operation of this circuit is:

$$V_{OUT} = I_{SENSOR} \text{ X } R_{PROGRAM}$$

Where:

V_{OUT} is the voltage at the output of the OPA2107,
I_{SENSOR} is the current into the ACF2101, and
$R_{PROGRAM}$ is the equivalent feedback resistance of the circuit calculated by the equation,

$$R_{PROGRAM} = 1/(f_S \text{ X } C_{\text{INTEGRATION}}) = 1/(f_S \text{ X } 100\text{pF})$$

For $C_{INTEGRATION}$ = 100pF, $R_{PROGRAM}$ is calculated below:

f_S	$R_{PROGRAM}$
10kHz	1MΩ
1kHz	10MΩ
100Hz	100MΩ
60Hz	167MΩ
50Hz	200MΩ
10Hz	1GΩ

At the end of the integration cycle, the Hold switch of the ACF2101 is opened to hold a constant value at the output of the ACF2101. The constant value output voltage of the ACF2101 is transferred onto a 10nF capacitor by closing the ACF2101's Select switch. The Select switch is then opened which holds the voltage on the 10nF capacitor during the next integration cycle and creates a DC output. With this operation, the Select switch of the ACF2101 and the 10nF capacitor form a Sample/Hold (S/H) circuit. The OPA2107 is used to buffer the Sample/Hold output. The charge injection of the Select switch creates a small offset voltage, of approximately 1mV in this example. The 10nF capacitor was chosen as a large value to minimize this offset voltage.

After the Select switch opens, the ACF2101 is reset by momentarily closing the Reset switch. The ACF2101's Hold switch is then closed to begin another integration cycle. During the period of time that the Hold switch is open, the input signal current is stored on the input capacitance of the sensor (C_{IN}). During this time, the input signal current creates a voltage across the sensor. This voltage should be kept below 500mV. When the Hold switch is closed, the charge that has collected on C_{IN} will be transferred to the integration capacitor, $C_{INTEGRATION}$, with no loss of signal. Therefore, one integration cycle ends and the next integration cycle begins when the Hold switch is opened.

If 100% of signal acquisition is not required, or not wanted, the Hold switch may be left closed, or the direct input to the ACF2101 used. In this mode of operation, an integration cycle ends when the Select switch is opened and the next integration cycle begins when the Reset switch is opened.

Figure 11 shows a simple digital pattern generator which can be used to create the timing signals to control the ACF2101 circuit of Figure 10. This circuit creates signals to control the Select, Reset and Hold switches at a rate controlled by the frequency of f_S. Figure 9 shows the timing diagram for these circuits.

In a sampled data system, the output of the ACF2101 at the output of the Select switch can be converted to digital when the ACF2101 is in the Hold mode. In this situation, of course, the 10nF capacitor and the OPA2107 op amp are not required.

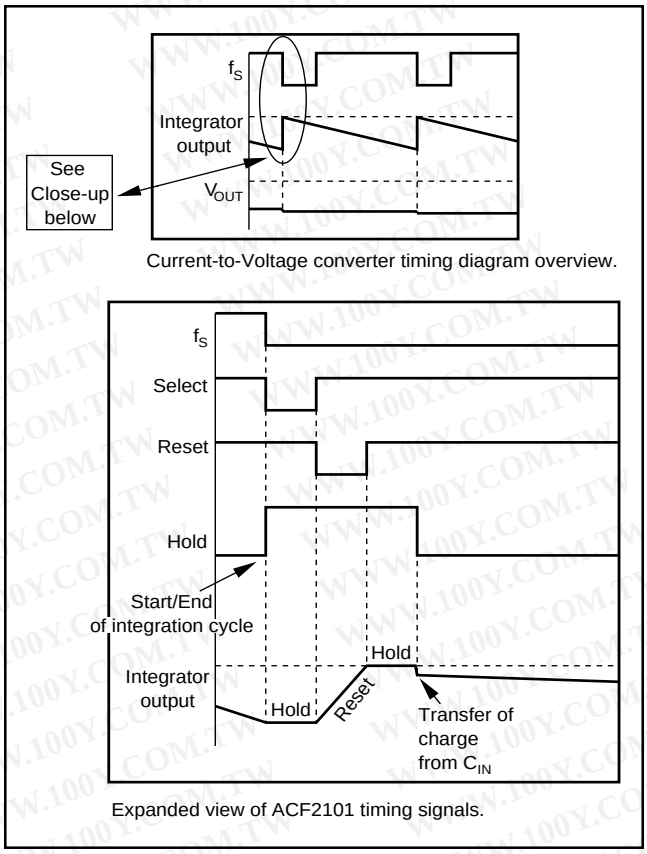


FIGURE 9. ACF2101 Current-to-Voltage Converter Timing Diagram.

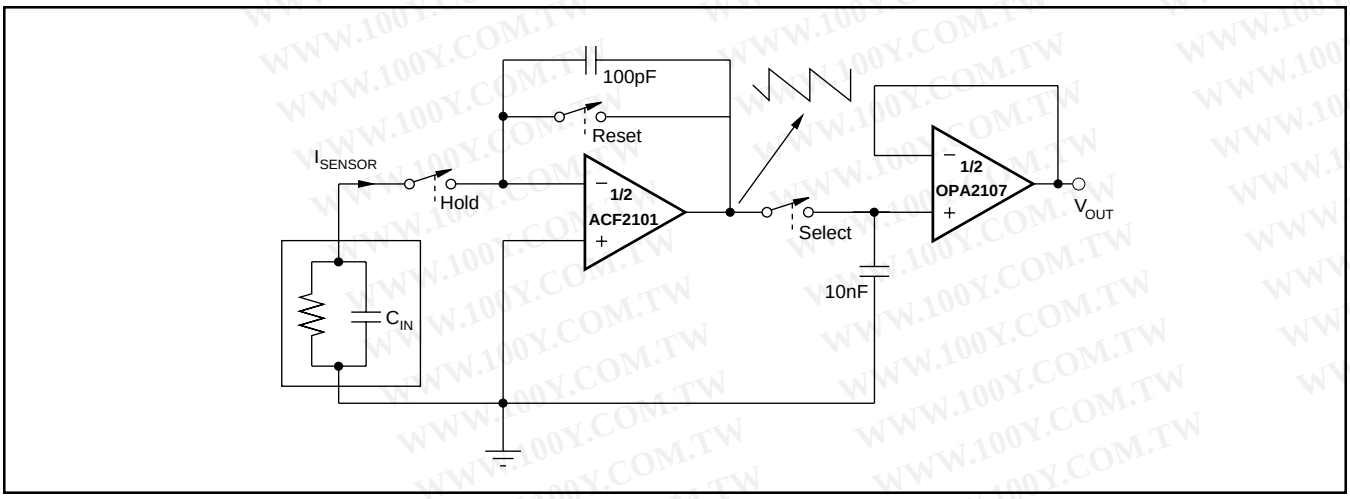


FIGURE 10. Programmable Current-to-Voltage Converter.

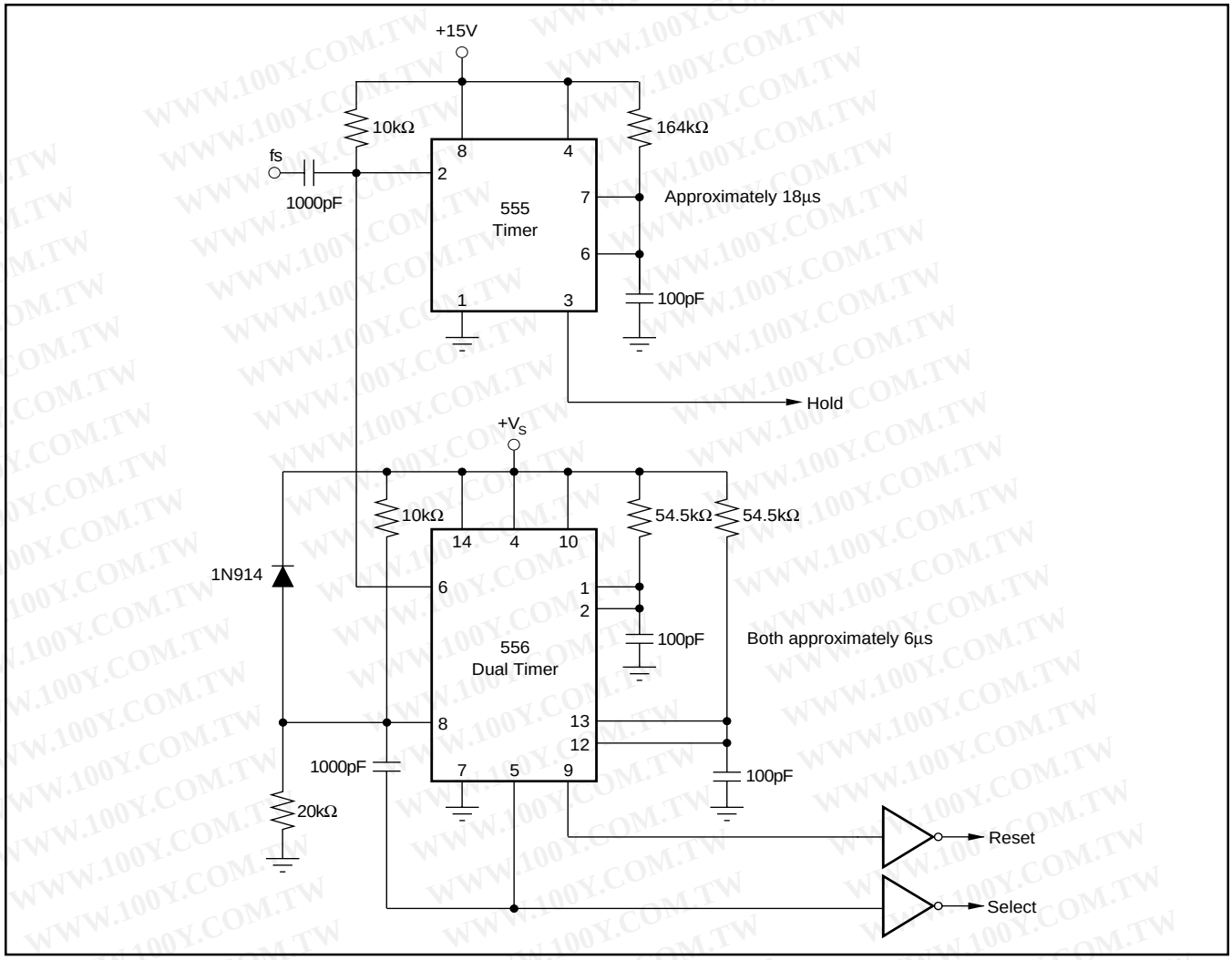


FIGURE 11. Timing Generator.

VOLTAGE INPUT EXAMPLE

Figure 12 illustrates the use of the ACF2101 with a voltage input. This approach is useful in applications where a constant current source is needed. For example, the ACF2101 can be configured in a bipolar mode by using the current generated by a voltage reference as an offset current. In the example in Figure 12, a 10V reference (REF102) is used in series with a 400kΩ resistor to generate a constant +25µA input current to the ACF2101. The ACF2101 will operate as expected in this configuration except in the Hold mode. When the Hold switch is opened, the input to the ACF2101 becomes high impedance and consequently the Sw In node will try to go to 10V. The Hold switch is specified to have a withstand voltage of +0.5V. When the voltage at the Sw In node exceeds +0.5V the Hold switch will begin to conduct again. This will not cause damage to the switch, however, the output will start to unexpectedly integrate again. The addition of either C_1 or D_1 in the circuit is critical for proper Hold mode operation. C_1 will divert the charge being generated by the voltage source in series with the resistor. C_1 is selected so that the maximum voltage does not exceed 0.4V. When the Hold switch is closed again, the charge collected by C_1 is transferred to the integration capacitor. D_1 will divert the charge being generated by the voltage source and resistor to ground. When the Hold switch closes again, the charge stored on the parasitic capacitor of the diode is transferred to the integration capacitor. D_1 should be selected so that the on voltage of the diode does not exceed 0.4V.

DEMONSTRATION BOARD AND MACROMODEL

Demonstration boards are available to speed prototyping. The demonstration board, DEM-ACF2101BP-C includes a programmable timing generator making it easy to do a quick evaluation.

A Spice-based macromodel is also available. Request AB-020 for Application Bulletin and Burr-Brown's Spice Macromodel diskette.

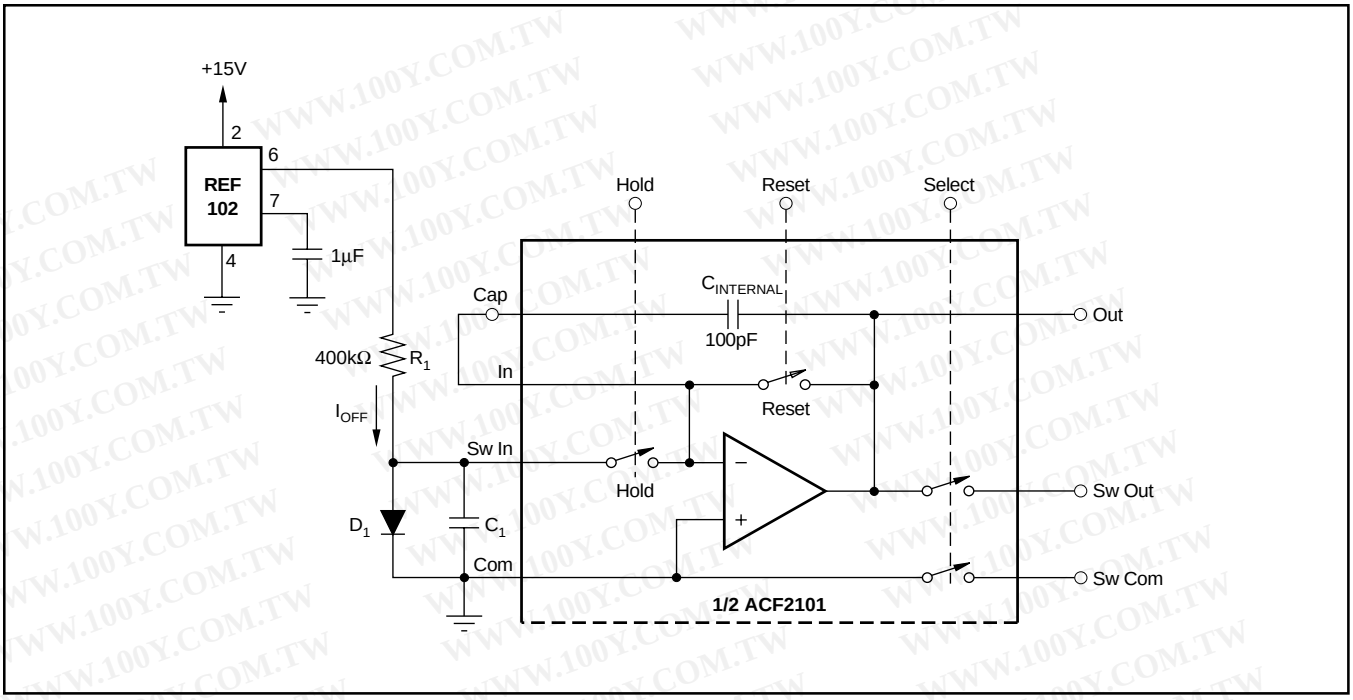


FIGURE 12. Using the ACF2101 with a Voltage Source.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ACF2101BP	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	Replaced by ACF2101BU
ACF2101BU	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Contact TI Distributor or Sales Office
ACF2101BUE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Contact TI Distributor or Sales Office

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ACTIVE: Product device recommended for new designs.
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NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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