ISO7842 High-Performance, 8000 V_{PK} Reinforced Quad Channel Digital Isolator

1 Features

- Signaling Rate: Up to 100 Mbps
- Wide Supply Range: 2.25 V to 5.5 V
- Wide Temperature Range: –55°C to 125°C
- Low Power Consumption, Typical 1.7 mA per Channel at 1 Mbps
- Low Propagation Delay: 11 ns Typical (5 V Supplies)
- Industry leading CMTI: ±100 kV/μs
- Robust Electromagnetic Compatibility (EMC)
- System-Level ESD, EFT, and Surge Immunity
- Low Emissions
- Isolation Barrier Life: > 25 Years
- Wide Body SOIC-16 Package
- Safety and Regulatory Approvals:
  - 5.7 kV_{RMS} Isolation for 1 minute per UL 1577
  - CSA Component Acceptance Notice #5A, IEC 60950-1 and IEC 61010-1 End Equipment Standards
  - 8000 V_{PK} V_{IOTM} and 2121 $V_{PK}V_{IORM}$ Reinforced Isolation per DIN V VDE 0884-10
  - GB4943.1-2011 CQC Certification
  - All Agencies Approvals Planned

2 Applications

- Industrial Automation
- Motor Control
- Power Supplies
- Solar Inverters
- Medical Equipment
- Hybrid Electric Vehicles

3 Description

The ISO7842 is a high-performance, quad-channel digital isolator with 8000 V_{PK} isolation voltage. This device is being reviewed for reinforced isolation certification by VDE and CSA. This isolator provides high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/O's. Each isolation channel has a logic input and output buffer separated by silicon dioxide (SiO_2) insulation barrier. This device comes with enable pins on each side which can be used to put the respective outputs in high impedance for multi master driving applications and to reduce power consumption. ISO7842 has two forward and two reverse-direction channels. In case of input power or signal loss, default output is 'high' for this device. See *Device Functional Modes* for further details. Used in conjunction with isolated power supplies, this device prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through innovative chip design and layout techniques, electromagnetic compatibility of ISO7842 has been significantly enhanced to ease system-level ESD, EFT, Surge and Emissions compliance. ISO7842 is currently available in a 16-pin SOIC wide-body (DW) package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7842	SOIC (16)	10.30mm x 7.50mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic

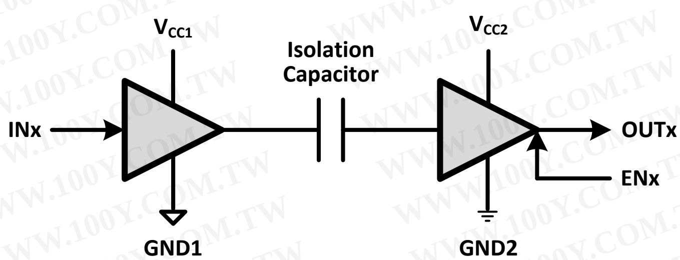
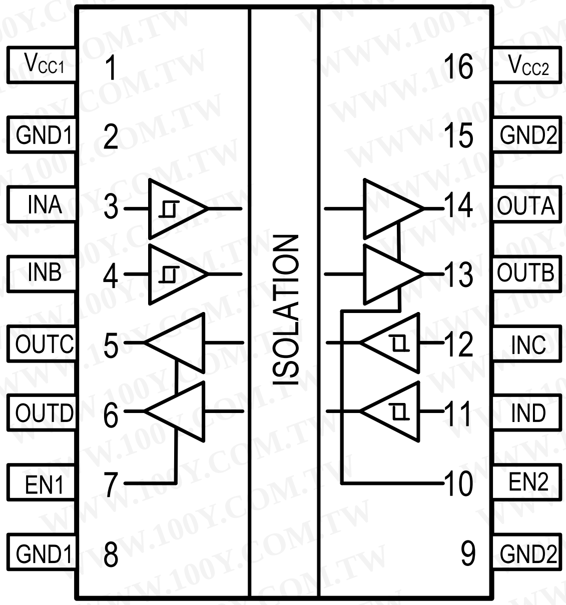


Table of Contents

5 Revision History

Changes from Original (october 2014) to Revision A	Page
• Changed Feature From: All Agencies Approvals Pending To: All Agencies Approvals Planned	1
• Changed statement in the Description From; "This device is certified to meet reinforced isolation requirements by VDE and CSA." To: "This device is being reviewed for reinforced isolation certification by VDE and CSA."	1
• Changed R_{IO} MIN value From: 10^9 To: 10^{11} in the IEC Insulation and Safety-Related Specifications for DW-16 Package table	13
• Changed the first row of information in the Regulatory Information (All Certifications Planned) table	14
• Added a link to the SLAA353 Isolation Glossary	20

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
INA	3	I	Input, channel A
INB	4	I	Input, channel B
INC	12	I	Input, channel C
IND	11	I	Input, channel D
OUTA	14	O	Output, channel A
OUTB	13	O	Output, channel B
OUTC	5	O	Output, channel C
OUTD	6	O	Output, channel D
EN1	7	I	Output enable 1. Output pins on side-1 are enabled when EN1 is high or in high impedance state when EN1 is low.
EN2	10	I	Output enable 2. Output pins on side-2 are enabled when EN2 is high or in high impedance state when EN2 is low.
V_{CC1}	1	–	Power supply, V_{CC1}
V_{CC2}	16	–	Power supply, V_{CC2}
GND1	2, 8	–	Ground connection for V_{CC1}
GND2	9, 15	–	Ground connection for V_{CC2}

7 Specifications

7.1 Absolute Maximum Ratings[1]

PARAMETER		MIN	MAX	UNIT
Supply voltage[2]	V_{CC1}, V_{CC2}	–0.5	6	V
Voltage	INx, OUTx, ENx	–0.5	V_{CCx} + 0.5	V
Output Current	I_O	-15	15	mA
Surge Immunity	Supports IEC 61000-4-5		12.8	kV
Maximum junction temperature	T_J		150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	–6	6	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	–1.5	1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.25		5.5	V
I_{OH}	High-level output current	V_{CCX}[1] = 5 V	-4			mA
		V_{CCX}[1] = 3.3 V	-2			
		V_{CCX}[1] = 2.5 V	-1			
I_{OL}	Low-level output current	V_{CCX}[1] = 5 V			4	mA
		V_{CCX}[1] = 3.3 V			2	
		V_{CCX}[1] = 2.5 V			1	
V_{IH}	High-level input voltage		0.7 x V_{CCX}[1]		V_{CCX}[1]	V
V_{IL}	Low-level input voltage		0		0.3 x V_{CCX}[1]	V
t_{ui}	Input pulse duration		7			ns
DR	Signaling rate		0		100	Mbps
T_J	Junction temperature[2]		-55		150	°C
T_A	Ambient temperature		-55	25	125	°C

(1) V_{CCx} is supply voltage, V_{CC1} or V_{CC2}, for the channel being measured.
(2) To maintain the recommended operating conditions for T_J, see the *Thermal Information* table.

7.4 Thermal Information

THERMAL METRIC			DW (16 Pins)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance		75.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance		37.8	
$R_{\theta JB}$	Junction-to-board thermal resistance		39.8	
ψ_{JT}	Junction-to-top characterization parameter		13.4	
ψ_{JB}	Junction-to-board characterization parameter		39.3	
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance		n/a	
P_D	Maximum Power Dissipation by ISO7842	$V_{CC1} = V_{CC2} = 5.5V$, $T_J = 150°C$, $C_L = 15pF$, Input a 50 MHz 50% duty cycle square wave	200	mW
P_{D1}	Maximum Power Dissipation by Side-1 of ISO7842		100	
P_{D2}	Maximum Power Dissipation by Side-2 of ISO7842		100	

7.5 Electrical Characteristics, 5 V

V_{CC1} = V_{CC2} = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 7		V_{CCX} (1) – 0.4	V_{CCX} (1) – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 7			0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis			0.1 x V_{CCX} (1)			V
I_{IH}	High-level input current	V_{IH} = V_{CCX} (1) at INx or ENx				10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx		-10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCX} (1) or 0 V; see Figure 10		50	100		kV/µs
I_{CC1}, I_{CC2}	Supply current(1)	Disable;EN1 = EN2 = 0 V	DC Signal: V_I = V_{CCX} (1)		1.1	1.6	mA
I_{CC1}, I_{CC2}		Disable;EN1 = EN2 = 0 V	DC Signal: V_I = 0 V		3.5	5.1	
I_{CC1}, I_{CC2}		DC Signal	DC Signal: V_I = V_{CCX} (1)		2	2.8	
I_{CC1}, I_{CC2}		DC Signal	DC Signal: V_I = 0 V		4.5	6.5	
I_{CC1}, I_{CC2}		1 Mbps	AC Signal: All channels switching with square wave clock input; C_L = 15 pF		3.4	4.8	
I_{CC1}, I_{CC2}		10 Mbps			4.4	5.9	
I_{CC1}, I_{CC2}		100 Mbps			14.8	18	

(1) V_{CCx} is supply voltage, V_{CC1} or V_{CC2}, for the channel being measured.

7.6 Switching Characteristics, 5 V

V_{CC1} = V_{CC2} = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 7	6	10.7	16	ns
PWD(1)	Pulse width distortion $\|t_{PHL} – t_{PLH}\|$			0.55	4.1	
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	Same-direction Channels			2.5	
$t_{sk(pp)}$ (3)	Part-to-part skew time				4.5	
t_r	Output signal rise time	See Figure 7		1.7	3.9	
t_f	Output signal fall time			1.9	3.9	
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 8		12	20	
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output			12	20	
t_{PZH}	Enable Propagation Delay, high impedance-to-high output			10	20	
t_{PZL}	Enable Propagation Delay, high impedance-to-low output			2	2.5	µs
t_{fs}	Default output delay time from input power loss	Measured from the time VCC goes below 1.7 V. See Figure 9		0.2	9	µs
t_{ie}	Time interval error	2^{16} - 1 PRBS data at 100 Mbps		0.90		ns

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.7 Electrical Characteristics, 3.3 V

V_{CC1} = V_{CC2} = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA; see Figure 7		V_{CCX} (1) – 0.4	V_{CCX} (1) – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA; see Figure 7			0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis			0.1 x V_{CCX} (1)			V
I_{IH}	High-level input current	V_{IH} = V_{CCX} (1) at INx or ENx				10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx		-10			μA
CMTI	Common-mode transient immunity	V_I = V_{CCX} (1) or 0 V; see Figure 10		50	100		kV/μs
I_{CC1}, I_{CC2}	Supply current	Disable;EN1 = EN2 = 0 V	DC Signal: V_I = V_{CCx} (1)		1.1	1.6	mA
I_{CC1}, I_{CC2}		Disable;EN1 = EN2 = 0 V	DC Signal: V_I = 0 V		3.5	5.1	
I_{CC1}, I_{CC2}		DC Signal	DC Signal: V_I = V_{CCx} (1)		2	2.8	
I_{CC1}, I_{CC2}		DC Signal	DC Signal: V_I = 0 V		4.5	6.5	
I_{CC1}, I_{CC2}		1 Mbps	AC Signal: All channels switching with square wave clock input; C_L = 15 pF		3.3	4.7	
I_{CC1}, I_{CC2}		10 Mbps			4.1	5.5	
I_{CC1}, I_{CC2}		100 Mbps			11.6	13.5	

(1) V_{CCx} is supply voltage, V_{CC1} or V_{CC2}, for the channel being measured.

7.8 Switching Characteristics, 3.3 V

V_{CC1} = V_{CC2} = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 7	6	10.8	16	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} – t_{PLH} \rvert$			0.7	4.2	
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	Same-direction Channels			2.2	
$t_{sk(pp)}$ (3)	Part-to-part skew time				4.5	
t_r	Output signal rise time	See Figure 7		0.8	3	
t_f	Output signal fall time			0.8	3	
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 8		17	32	
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output			17	32	
t_{PZH}	Enable Propagation Delay, high impedance-to-high output			13	20	
t_{PZL}	Enable Propagation Delay, high impedance-to-low output			2	2.5	μs
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 9		0.2	9	μs
t_{ie}	Time interval error	2^{16} - 1 PRBS data at 100 Mbps		0.91		ns

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.9 Electrical Characteristics, 2.5 V

V_{CC1} = V_{CC2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA; see Figure 7		V_{CCX} (1) – 0.4	V_{CCX} (1) – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA; see Figure 7			0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis			0.1 x V_{CCX} (1)			V
I_{IH}	High-level input current	V_{IH} = V_{CCX} (1) at INx or ENx				10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx		-10			μA
CMTI	Common-mode transient immunity	V_I = V_{CCX} (1) or 0 V; see Figure 10		50	100		kV/μs
I_{CC1}, I_{CC2}	Supply current	Disable;EN1 = EN2 = 0 V	DC Signal: V_I = V_{CCX} (1)		1.1	1.6	mA
I_{CC1}, I_{CC2}		Disable;EN1 = EN2 = 0 V	DC Signal: V_I = 0 V		3.5	5.1	
I_{CC1}, I_{CC2}		DC Signal	DC Signal: V_I = V_{CCX} (1)		2	2.8	
I_{CC1}, I_{CC2}		DC Signal	DC Signal: V_I = 0 V		4.5	6.5	
I_{CC1}, I_{CC2}		1 Mbps	AC Signal: All channels switching with square wave clock input; C_L = 15 pF		3.3	4.7	
I_{CC1}, I_{CC2}		10 Mbps			3.9	5.3	
I_{CC1}, I_{CC2}		100 Mbps			9.5	11.1	

(1) V_{CCX} is supply voltage, V_{CC1} or V_{CC2}, for the channel being measured.

7.10 Switching Characteristics, 2.5 V

V_{CC1} = V_{CC2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 7	7.5	11.7	17.5	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} – t_{PLH} \rvert$	See Figure 7		0.66	4.2	ns
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	Same-direction Channels			2.2	ns
$t_{sk(pp)}$ (3)	Part-to-part skew time				4.5	ns
t_r	Output signal rise time	See Figure 7		1	3.5	ns
t_f	Output signal fall time	See Figure 7		1.2	3.5	ns
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 8		22	45	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output	See Figure 8		22	45	ns
t_{PZH}	Enable Propagation Delay, high impedance-to-high output	See Figure 8		18	45	ns
t_{PZL}	Enable Propagation Delay, high impedance-to-low output	See Figure 8		2	2.5	μs
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 9		0.2	9	μs
t_{ie}	Time interval error	2^{16} - 1 PRBS data at 100 Mbps		0.91		ns

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.11 Typical Characteristics

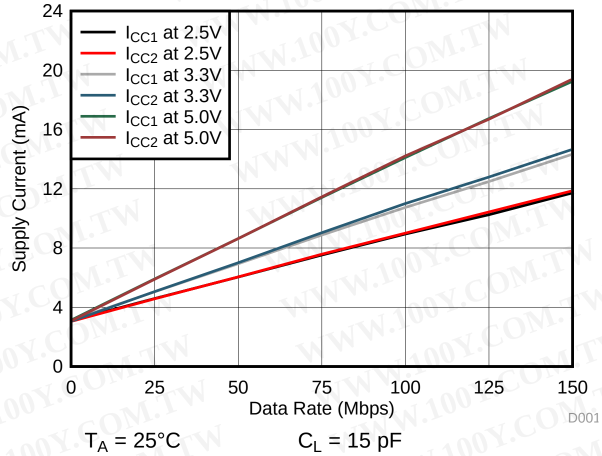


Figure 1. Supply Current vs Data Rate (with 15 pF Load)

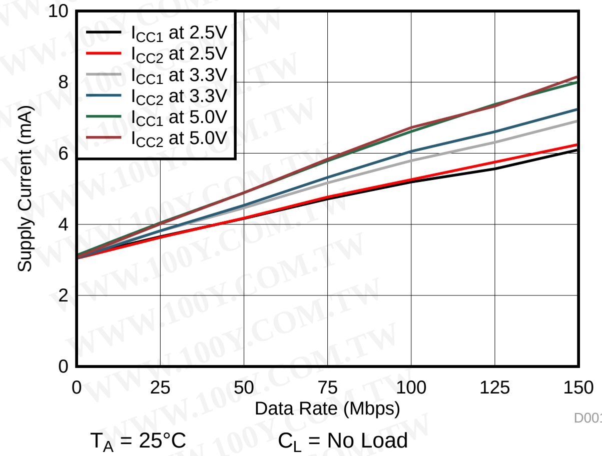


Figure 2. Supply Current vs Data Rate (with No Load)

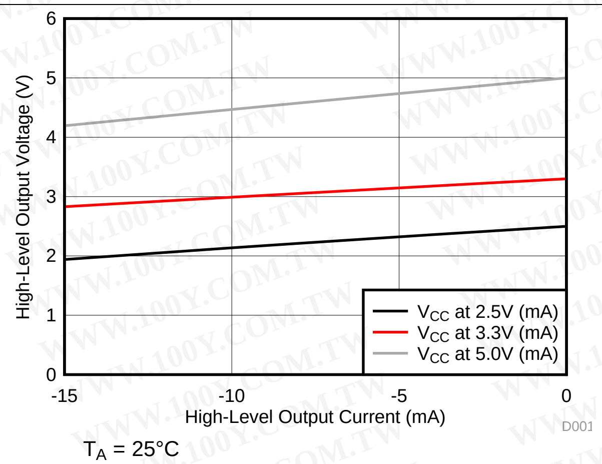


Figure 3. High-Level Output Voltage vs High-level Output Current

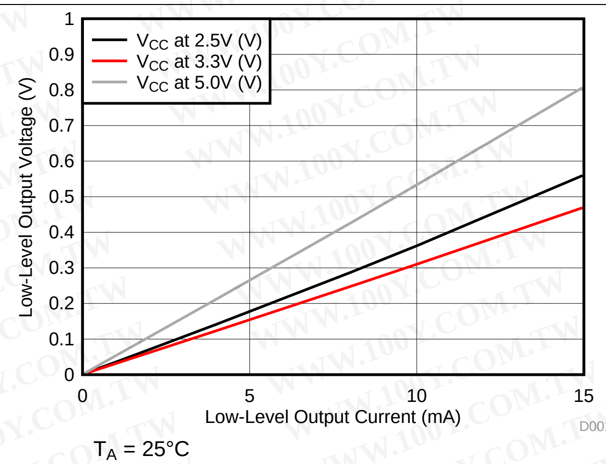


Figure 4. Low-Level Output Voltage vs Low-Level Output Current

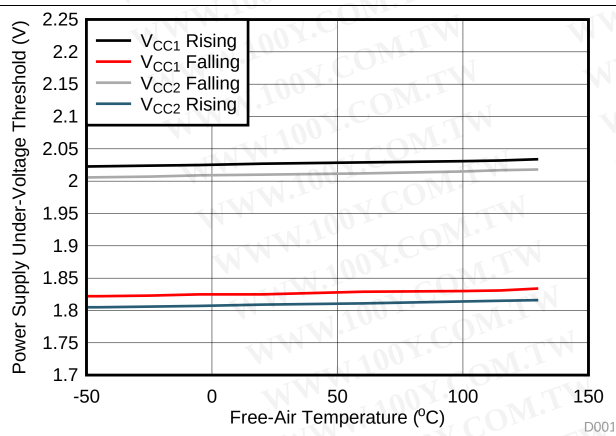


Figure 5. Power Supply Undervoltage Threshold vs Free-Air Temperature

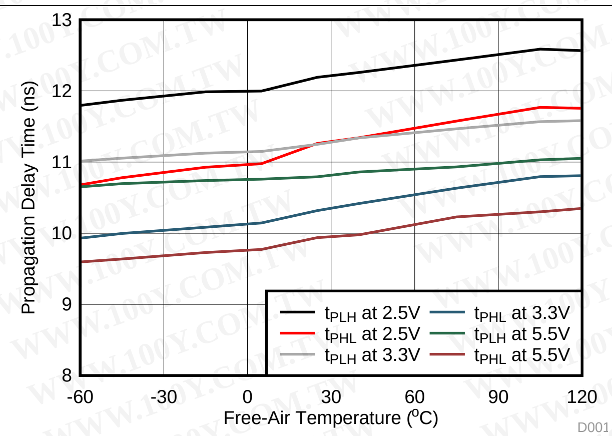
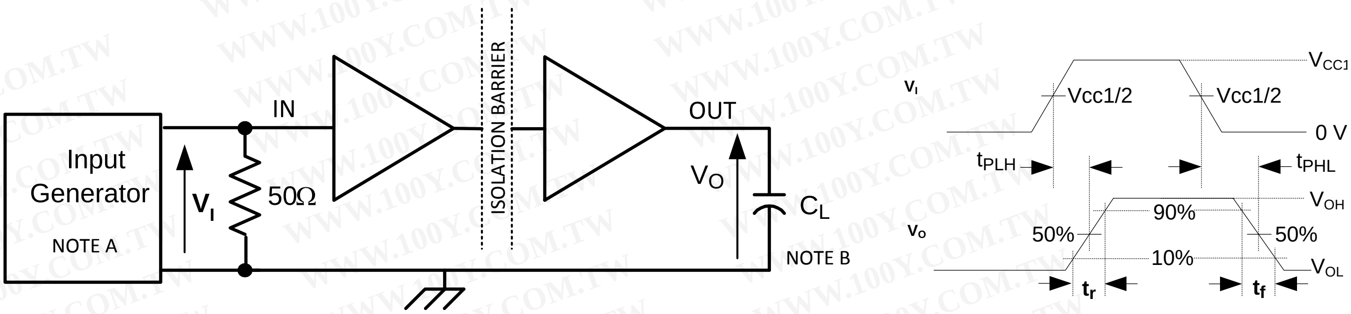


Figure 6. Propagation Delay Time vs Free-Air Temperature

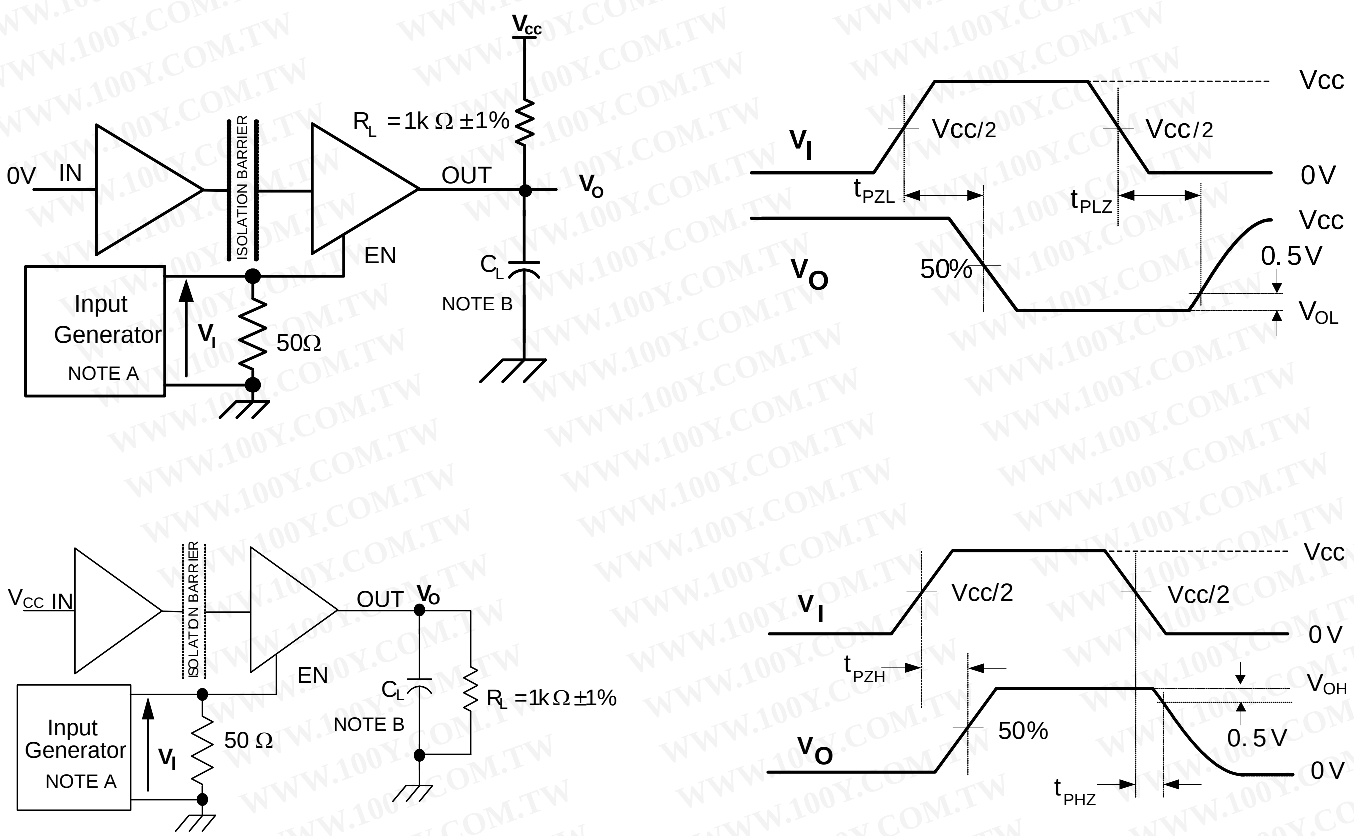
8 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 7. Switching Characteristics Test Circuit and Voltage Waveforms

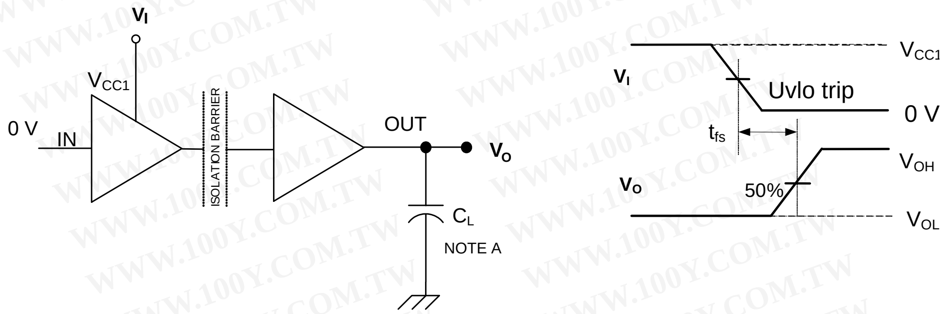


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

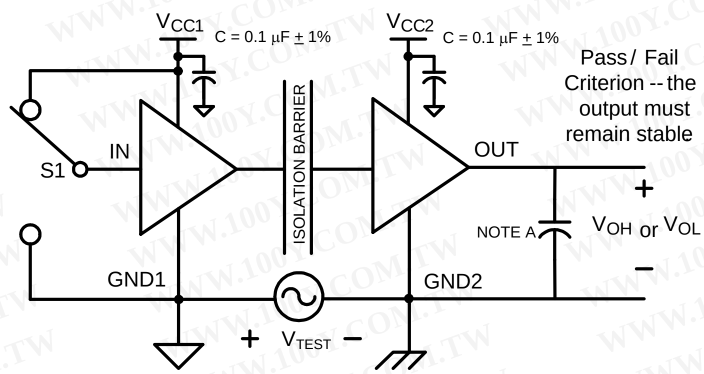
Figure 8. Enable/Disable Propagation Delay Time Test Circuit and Waveform

Parameter Measurement Information (continued)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 9. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 10. Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Overview

ISO7842 employs an ON-OFF Keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the EN pin is low then the output goes to high impedance. ISO7842 also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 11, shows a functional block diagram of a typical channel.

9.2 Functional Block Diagram

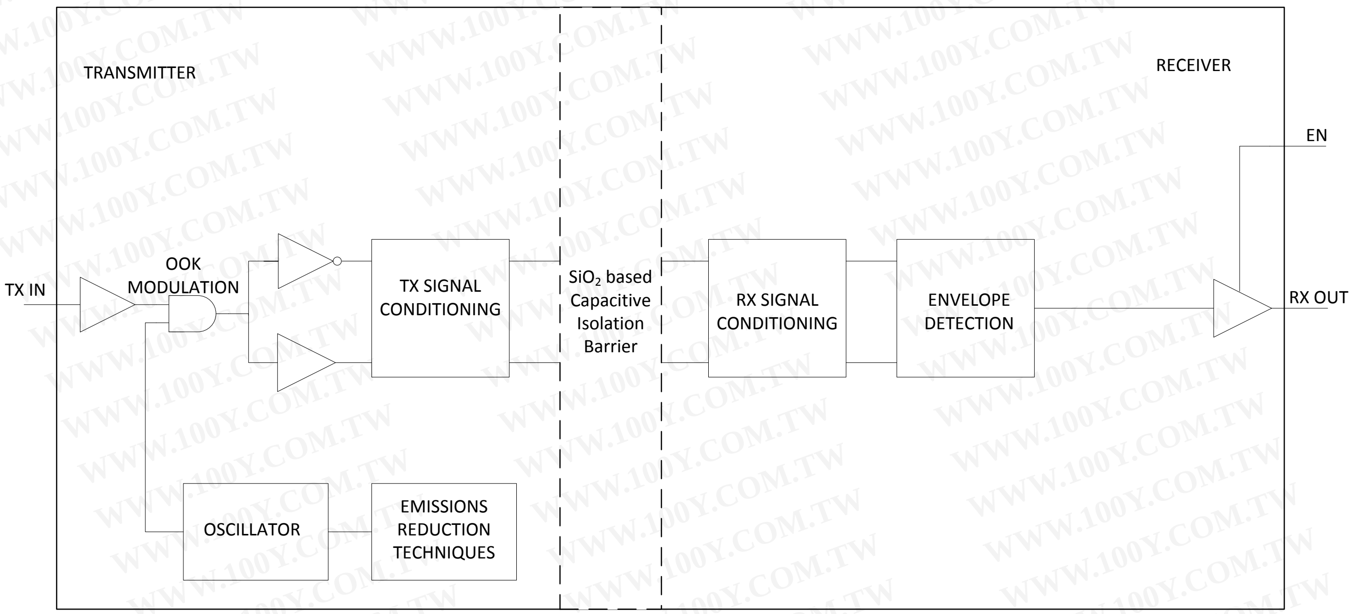


Figure 11. Conceptual Block Diagram of a Digital Capacitive Isolator

Also a conceptual detail of how the ON/OFF Keying scheme works is shown in Figure 12.

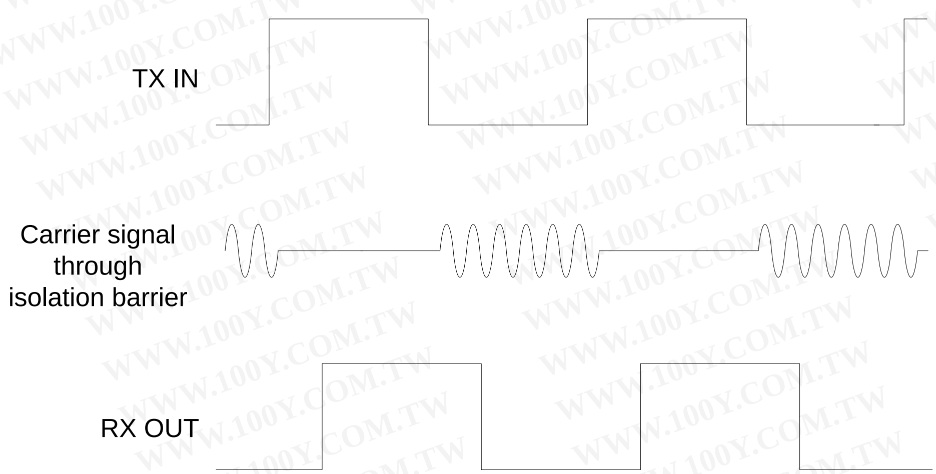


Figure 12. On-Off Keying (OOK) Based Modulation Scheme

9.3 Feature Description

PRODUCT	CHANNEL DIRECTION	RATED ISOLATION	MAX DATA RATE	DEFAULT OUTPUT
ISO7842	2 Forward, 2 Reverse	5700 V_{RMS} / 8000 V_{PK} (1)	100 Mbps	High

(1) See the *Regulatory Information* section for detailed isolation ratings.

9.3.1 High Voltage Feature Description

9.3.1.1 IEC Insulation and Safety-Related Specifications for DW-16 Package

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	8			mm
L(I02)(1)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface	8			mm
CTI	Tracking resistance (comparative tracking index)	UL 746A	>600			V
	Minimum internal gap (internal clearance)	Distance through the insulation	21	25		μm
R_{IO}	Isolation resistance, input to output(2)	V_{IO} = 500 V, T_A = 25°C	10^{12}			Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ max	10^{11}			Ω
C_{IO}	Barrier capacitance, input to output(2)	V_{IO} = 0.4 x sin (2πft), f = 1 MHz		2		pF
C_I	Input capacitance(3)	V_I = V_{CCX}/2 + 0.4 x sin (2πft), f = 1 MHz, V_{CC} = 5 V		2		pF

(1) Per JEDEC package dimensions.
(2) All pins on each side of the barrier tied together creating a two-terminal device.
(3) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

9.3.1.2 DIN V VDE 0884-10 (VDE V 0884-10) and UL 1577 Insulation Characteristics

PARAMETER[1]		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IOWM}	Maximum isolation working voltage		1500	V_{RMS}
V_{IORM}	Maximum repetitive peak voltage per DIN V VDE 0884-10		2121	V_{PK}
V_{PR}	Input-to-output test voltage per DIN V VDE 0884-10	After Input/Output safety test subgroup 2/3, $V_{PR} = V_{IORM}$ x 1.2, t = 10 s, Partial discharge < 5 pC	2545	V_{PK}
		Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM}$ x 1.6, t = 10 s, Partial Discharge < 5 pC	3394	
		Method b1,After environmental tests subgroup 1, $V_{PR} = V_{IORM}$ x 1.875, t = 1 s (100% Production test) Partial discharge < 5 pC	3977	
V_{IOTM}	Maximum transient overvoltage per DIN V VDE 0884-10	$V_{TEST} = V_{IOTM}$ t = 60 sec (qualification) t= 1 sec (100% production)	8000	V_{PK}
V_{ISO}	Withstand isolation voltage per UL 1577	$V_{TEST} = V_{ISO}$, t = 60 sec (qualification)	5700	V_{RMS}
		V_{TEST} = 1.2 x V_{ISO}, t = 1 sec (100% production)	6840	
R_S	Isolation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

9.3.1.3 IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	I
Installation classification	Rated mains voltage ≤ 600 V_{RMS}	I–IV
	Rated mains voltage ≤ 1000 V_{RMS}	I–III

9.3.1.4 Regulatory Information (All Certifications Planned)

VDE	CSA	UL	CQC
DIN V VDE 0884-10 (VDE 0884-10): 2006-12	CSA Component Acceptance Notice #5A	UL 1577 Component Recognition Program	GB 4943.1-2011
Reinforced insulation Maximum transient overvoltage, 8000 V_{PK} Maximum repetitive peak voltage, 2121 V_{PK} Maximum surge voltage, 8000 V_{PK}	Reinforced insulation per IEC 61010-1 (3rd Ed.), 600 V_{RMS} max working voltage Reinforced insulation per CSA 60950-1-07 and IEC 60950-1 (2nd Ed.), 800 V_{RMS} max working voltage 2 MOPP (Means of Patient Protection) per IEC 60601-1 (3rd Ed.), 250 V_{RMS} (354 V_{PK}) max working voltage	Single protection, 5700 V_{RMS} [1]	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage
Agency Approval Planned	Agency Approval Planned	Agency Approval Planned	Agency Approval Planned

(1) Production tested ≥ 6840 V_{RMS} for 1 second in accordance with UL 1577.

9.3.1.5 IEC Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I	Safety input, output, or supply current	$R_{θJA}$ = 78.4°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			301	mA
		$R_{θJA}$ = 78.4°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			460	
		$R_{θJA}$ = 78.4°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C			602	
T_S	Maximum case temperature				150	°C

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolut Maximun Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a High-K Test Board for Leaded Surface-Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

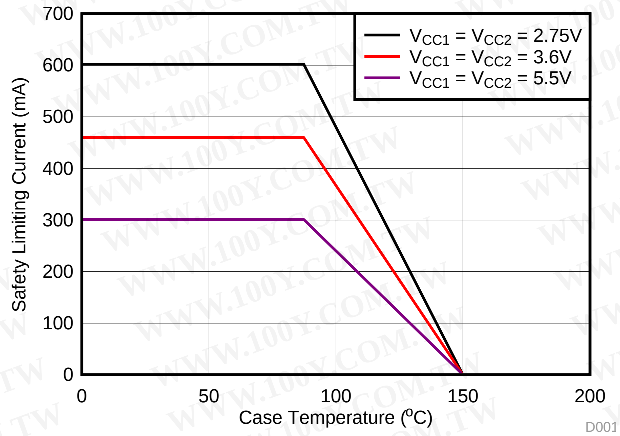


Figure 13. $θ_{JC}$ Thermal Derating Curve per DIN V VDE 0884-10

9.4 Device Functional Modes

ISO7842 functional modes are shown in Table 1.

Table 1. Function Table(1)

INPUT-SIDE V_I	OUTPUT-SIDE V_O	INPUT (INx)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	COMMENTS
PU(1)	PU(1)	H	H or Open	H	Normal Operation: A channel output assumes the logic state of its input.
		L	H or Open	L	
		Open	H or Open	H	Default mode: When INx is open, the corresponding channel output goes to its default high logic state.
X	PU(1)	X	L	Z	A low value of Output Enable causes the outputs to be high-impedance
PD(1)	PU(1)	X	H or Open	H	Default mode: When V_I is unpowered, a channel output assumes the logic state based on the selected default option. When V_I transitions from unpowered to powered-up, a channel output assumes the logic state of its input. When V_I transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD(1)	X	X	Undetermined	When V_O is unpowered, a channel output is undetermined (2). When V_O transitions from unpowered to powered-up, a channel output assumes the logic state of its input

(1) PU = Powered up ($V_{CC} \geq 2.25$ V); PD = Powered down ($V_{CC} \leq 1.7$ V); X = Irrelevant; H = High level; L = Low level
(2) The outputs are in undetermined state when 1.7 V < V_{CCx} < 2.25 V.

10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ISO7842 is a high-performance, quad-channel digital isolator with 5.7 kV_{RMS} isolation voltage. The device comes with enable pins on each side which can be used to put the respective outputs in high impedance for multi master driving applications and reduce power consumption

10.2 Typical Application

Unlike optocouplers, which need external components to improve performance, provide bias, or limit current, ISO7842 only needs two external bypass capacitors to operate.

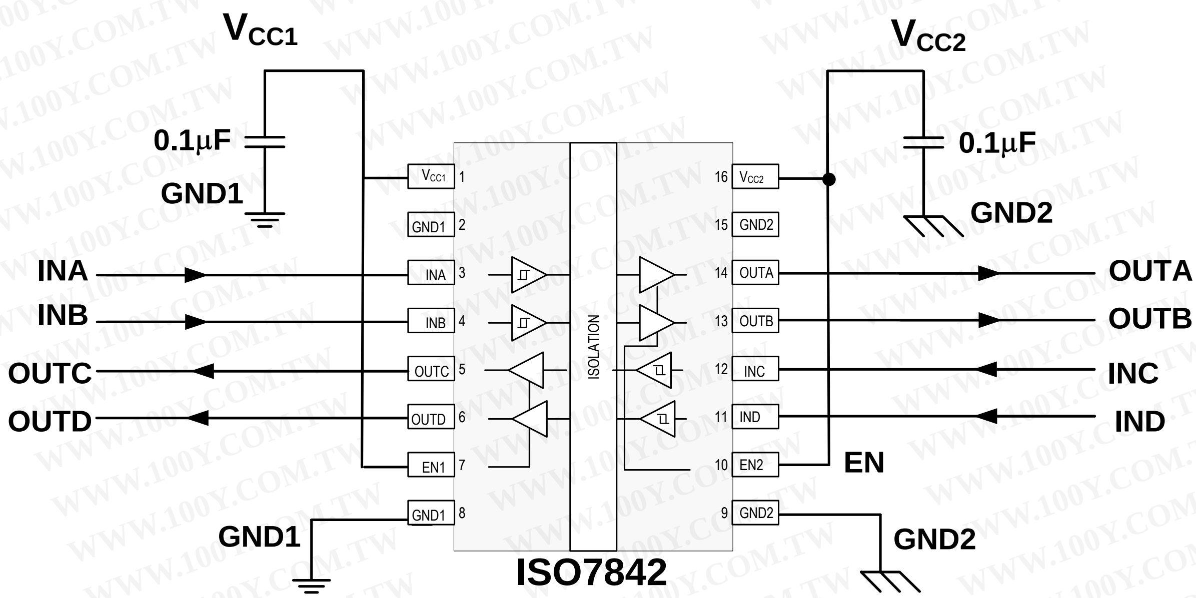


Figure 14. Isolated Data Acquisition System for Process Control

10.2.1 Design Requirements

For this example, use the parameters shown in Table 2.

Table 2. Design Parameters

PARAMETER	VALUE
Input voltage	2.25 V to 5.5 V
Decoupling capacitors between V_{CC1} and GND1	0.1 µF
Decoupling capacitors from V_{CC2} and GND2	0.1 µF

10.2.2 Detailed Design Procedure

10.2.2.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO7842 incorporate many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

10.2.3 Application Performance Curve

Typical eye diagram of ISO7842 indicate low jitter and wide open eye at the maximum data rate of 100 Mbps.

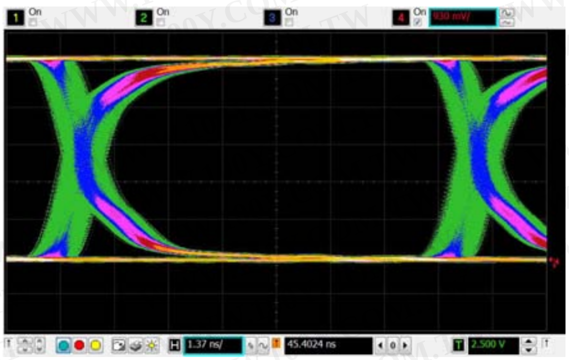


Figure 15. Eye Diagram at 100 Mbps PRBS, 5 V and 25°C

11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1 µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 datasheet (SLLSEA0) .

12 Layout

12.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing flammability-characteristics.

12.2 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 16). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see Application Note SLLA284, *Digital Isolator Design Guide*.

12.3 Layout Example

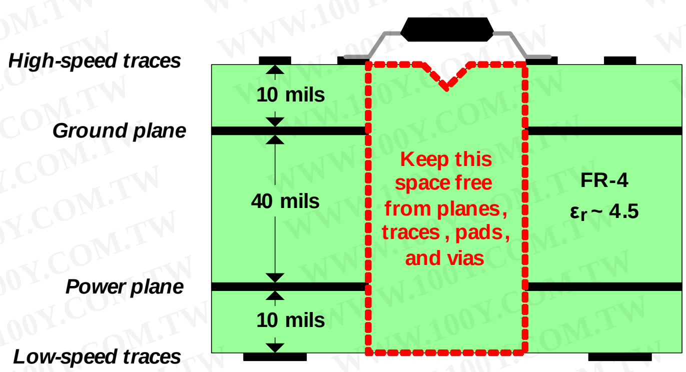


Figure 16. Layout Example

13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

See the *Isolation Glossary* (SLLA353)

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7842DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7842	Samples
ISO7842DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7842	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265