LM8272 Dual RRIO, High Output Current & Unlimited Cap Load Op Amp in Miniature Package

Check for Samples: LM8272

FEATURES

(V_S = 12V, T_A = 25°C, Typical values unless specified).

- **GBWP 15MHz**
- **Wide supply voltage range 2.5V to 24V**
- **Slew rate 15V/µs**
- **Supply current/channel 0.95mA**
- **Cap load tolerance Unlimited**
- **Output short circuit current ±130mA**
- **Output current (1V from rails) ±65mA**
- **Input common mode voltage 0.3V beyond rails**
- **Input voltage noise 15nV/√Hz**
- **Input current noise 1.4pA/√Hz**

APPLICATIONS

- **TFT-LCD flat panel V_{COM} driver**
- **A/D converter buffer**
- **High side/low side sensing**
- **Headphone amplifier**

DESCRIPTION

The LM8272 is a Rail-to-Rail input and output Op Amp which can operate with a wide supply voltage range. This device has high output current drive, greater than Rail-to-Rail input common mode voltage range, unlimited capacitive load drive capability while requiring only 0.95mA/channel supply current. It is specifically designed to handle the requirements of flat panel TFT panel V_{COM} driver applications as well as being suitable for other low power, and medium speed applications which require ease of use and enhanced performance over existing devices.

Greater than Rail-to-Rail input common mode voltage range with 50dB of Common Mode Rejection, allows high side and low side sensing, among many applications, without having any concerns over exceeding the range and no compromise in accuracy. Exceptionally wide operating supply voltage range of 2.5V to 24V alleviates any concerns over functionality under extreme conditions and offers flexibility of use in multitude of applications. In addition, most device parameters are insensitive to power supply variations; this design enhancement is yet another step in simplifying its usage.

The LM8272 is offered in the 8-pin VSSOP package.

Connection Diagram

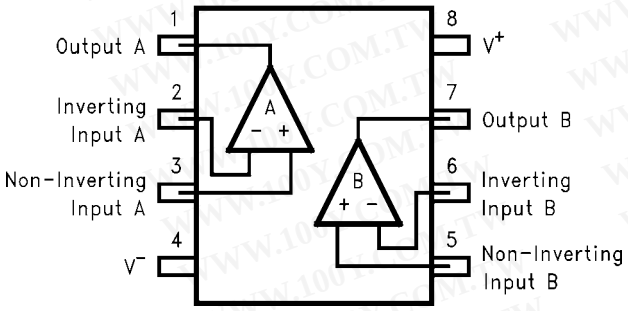


Figure 1. 8-Pin VSSOP
Top View

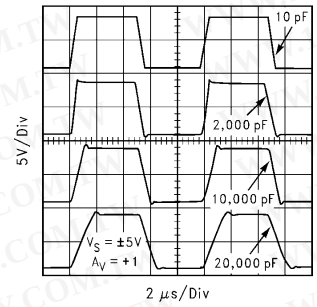


Figure 2. Large Signal Step Response for Various Cap. Load

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance		2KV(3) 200V(4)
V_{IN} Differential		+/−10V
Output Short Circuit Duration		See(5)(6)
Supply Voltage (V^+ - V^-)		27V
Voltage at Input/Output pins		V^+ +0.3V, V^- −0.3V
Storage Temperature Range		−65°C to +150°C
Junction Temperature(7)		+150°C
Soldering Information:	Infrared or Convection (20 sec.)	235°C
	Wave Soldering (10 sec.)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Rating indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human body model, 1.5kΩ in series with 100pF.
(4) Machine Model, 0Ω is series with 200pF.
(5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(6) Output short circuit duration is infinite for VS ≤ 6V at room temperature and below. For VS 6V, allowable short circuit duration is 1.5ms.
(7) The maximum power dissipation is a function of TJ(max), θJA, and TA. The maximum allowable power dissipation at any ambient temperature is PD = (TJ(max) - TA)/ θJA. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings

Supply Voltage (V^+ - V^-)		2.5V to 24V
Junction Temperature Range(1)		−40°C to +85°C
Package Thermal Resistance, θ_{JA},(1)	8-Pin VSSOP	235C/W

(1) The maximum power dissipation is a function of TJ(max), θJA, and TA. The maximum allowable power dissipation at any ambient temperature is PD = (TJ(max) - TA)/ θJA. All numbers apply for packages soldered directly onto a PC board.

5V Electrical Characteristics

Unless otherwise specified, all limited guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ(1)	Limit(2)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V & V_{CM} = 4.5V	+/−0.7	+/−5 **+/− 7**	mV max
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0.5V & V_{CM} = 4.5V(3)	+/−2	—	µV/°C
I_B	Input Bias Current	See (4)	—	±2.00 **±2.70**	µA max
I_{OS}	Input Offset Current		20	250 **400**	nA max
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from 0V to 5V	80	64 **61**	dB min
+PSRR	Positive Power Supply Rejection Ratio	V^+ from 4.5V to 13V	100	78 **74**	dB min
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB	−0.3	−0.1 **0.0**	V max
			5.3	5.1 **5.0**	V min
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5 to 4.5V, R_L = 10kΩ to V^+/2	80	64 **60**	dB min

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.
(3) Offset voltage average drift determined by dividing the change in VOS at temperature extremes into the total temperature change.
(4) Positive current corresponds to current flowing into the device.

5V Electrical Characteristics (continued)

Unless otherwise specified, all limited guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (1)	Limit (2)	Units
V_O	Output Swing High	R_L = 10kΩ to V^-	4.93	4.85	V min
		I_{SOURCE} = 5mA	4.85	4.70	
	Output Swing Low	R_L = 10kΩ to V^+	215	250	mV max
		I_{SINK} = 5mA	300	350	
I_{SC}	Output Short Circuit Current	Sourcing to V^- V_{ID} = 200mV (5)	100	—	mA
		Sinking to V^+ V_{ID} = −200mV (5)	100	—	
I_{OUT}	Output Current	V_{ID} = ±200mV, V_O = 1V from rails	±55	—	mA
I_S	Supply Current (Both Channel)	No load, V_{CM} = 0.5V	1.8	2.3 **2.8**	mA max
SR	Slew Rate (6)	A_V = +1, V_I = $5V_{PP}$	12	—	V/µs
f_u	Unity Gain Frequency	V_I = 10mVp, R_L = 2KΩ to V^+/2	7.5	—	MHz
GBWP	Gain-Bandwidth Product	f = 50KHz	13	—	MHz
Phi_m	Phase Margin	V_I = 10mVp, R_L = 2kΩ to V^+/2	55	—	deg
e_n	Input-Referred Voltage Noise	f = 2KHz, R_S = 50Ω	15	—	nV/√Hz
i_n	Input-Referred Current Noise	f = 2KHz	1.4	—	pA/√Hz
f_{max}	Full Power Bandwidth	Z_L = (20pF || 10kΩ) to V^+/2	700	—	KHz

(5) Short circuit test is a momentary test. Output short circuit duration is infinite for V_S ≤ 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.
(6) Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

12V Electrical Characteristics

Unless otherwise specified, all limited guaranteed for T_J = 25°C, V^+ = 12V, V^- = 0V, V_{CM} = 6V, V_O = 6V, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (1)	Limit (2)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V & V_{CM} = 11.5V	+/−0.7	+/−7 **+/− 9**	mV max
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0.5V & V_{CM} = 11.5V (3)	+/−2	—	µV/°C
I_B	Input Bias Current	See (4)	—	±2.00 **±2.80**	µA max
I_{OS}	Input Offset Current		30	275 **550**	nA max
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from 0V to 12V	88	74 **72**	dB min
+PSRR	Positive Power Supply Rejection Ratio	V^+ from 4.5V to 13V, V_{CM} = 0.5V	100	78 **74**	dB min
−PSRR	Negative Power Supply Rejection Ratio		85	—	dB
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB	−0.3	−0.1 **0**	V max
			12.3	12.1 **12.0**	V min
A_{VOL}	Large Signal Voltage Gain	V_O = 1V to 11V R_L = 10kΩ to V^+/2	83	74 **70**	dB min

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.
(3) Offset voltage average drift determined by dividing the change in VOS at temperature extremes into the total temperature change.
(4) Positive current corresponds to current flowing into the device.

12V Electrical Characteristics (continued)

Unless otherwise specified, all limited guaranteed for T_J = 25°C, V^+ = 12V, V^- = 0V, V_{CM} = 6V, V_O = 6V, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ(1)	Limit(2)	Units
V_O	Output Swing High	R_L 10kΩ to V^+/2	11.8	11.7	V min
		I_{SOURCE} = 5mA	11.6	11.5	
	Output Swing Low	R_L = 10kΩ to V^+/2	0.25	0.3	V max
		I_{SINK} = 5mA	.40	.45	
I_{SC}	Output Short Circuit Current	Sourcing to V^- V_{ID} = 200mV (5)	130	110	mA min
		Sinking to V^+ V_{ID} = 200mV (5)	130	110	
I_{OUT}	Output Current	V_{ID} = ±200mV, V_O = 1V from rails	±65	—	mA
I_S	Supply Current (Both Channel)	No load, V_{CM} = 0.5V	1.9	2.4 **2.9**	mA max
SR	Slew Rate(6)	A_V = +1, V_I = 10V_{PP}, C_L = 10pF	15	—	V/µs
		A_V = +1, V_I = 10V_{PP}, C_L = 0.1µF	1	—	
R_{OUT}	Close Loop Output Resistance	A_V = +1, f = 100KHz	3	—	Ω
f_u	Unity Gain Frequency	V_I = 10mVp, R_L = 2kΩ to V^+/2	8	—	MHz
GBWP	Gain-Bandwidth Product	f = 50KHz	15	—	MHz
Phi_m	Phase Margin	V_I = 10mVp, R_L = 2kΩ to V^+/2	57	—	Deg
GM	Gain Margin	V_I = 10mVp, R_L = 2kΩ to V^+/2	20	—	dB
−3dB BW	Small Signal -3db Bandwidth	A_V = +1, R_L = 2kΩ to V^+/2	12.5	—	MHz
		A_V = +1, R_L = 600Ω to V^+/2	10.5	—	
		A_V = +10, R_L = 600Ω to V^+/2	1.0	—	
e_n	Input-Referred Voltage Noise	f = 2KHz, R_S = 50Ω	15	—	nV/√Hz
i_n	Input-Referred Current Noise	f = 2KHz	1.4	—	pA/√Hz
f_{max}	Full Power Bandwidth	Z_L = (20pF || 10kΩ) to V^+/2	300	—	KHz
THD+N	Total Harmonic Distortion +Noise	A_V = +2, R_L = 2kΩ to V^+/2 V_O = 8V_{PP}, V_S = ±5V	0.02	—	%
CT Rej.	Cross-Talk Rejection	f = 5MHz, Driver R_L = 10kΩ to V^+/2	68	—	dB

(5) Short circuit test is a momentary test. Output short circuit duration is infinite for VS ≤ 6V at room temperature and below. For VS > 6V, allowable short circuit duration is 1.5ms.

(6) Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

Typical Performance Characteristics

V_{OS} Distribution

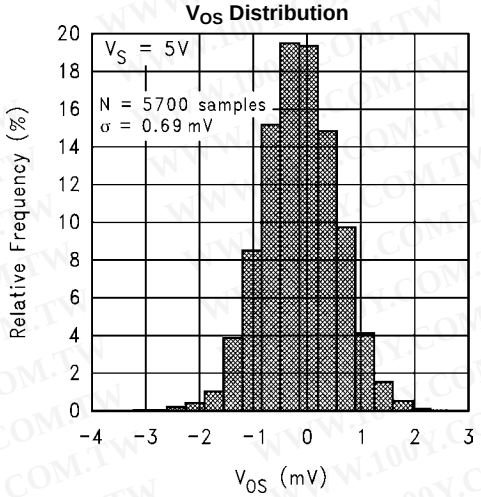


Figure 3.

V_{OS} vs. V_{CM} for 3 Representative Units

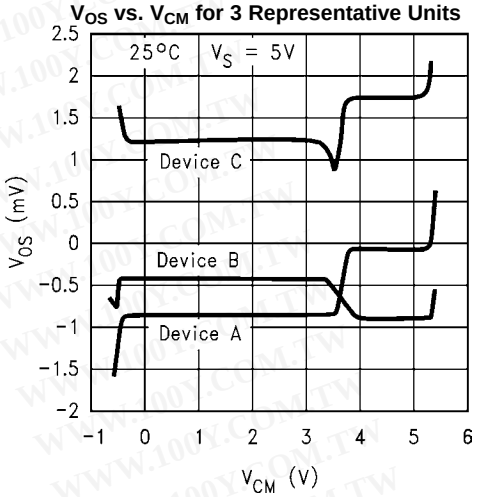


Figure 4.

V_{OS} vs. V_{CM} for 3 Representative Units

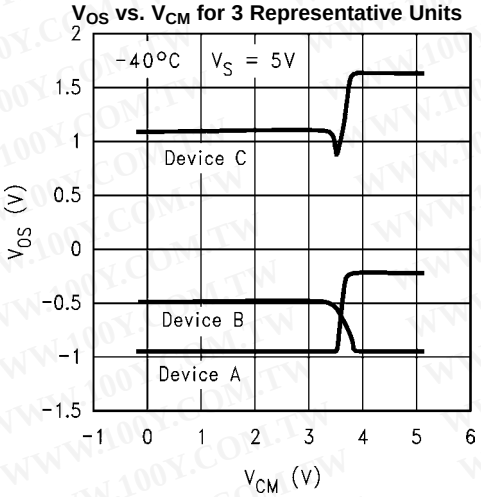


Figure 5.

V_{OS} vs. V_{CM} for 3 Representative Units

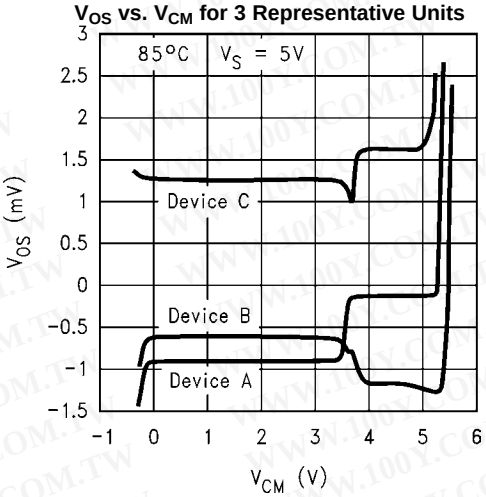


Figure 6.

V_{OS} vs. V_S for 3 Representative Units

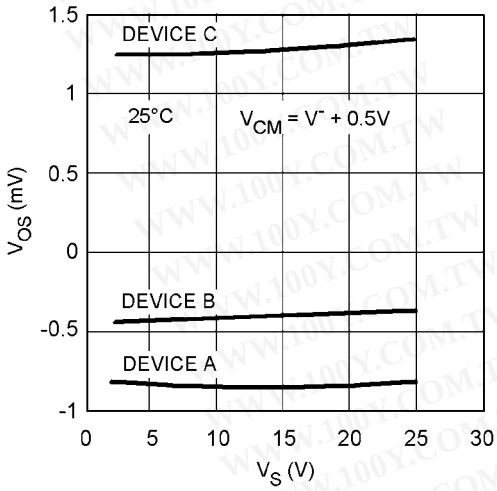


Figure 7.

V_{OS} vs. V_S for 3 Representative Units

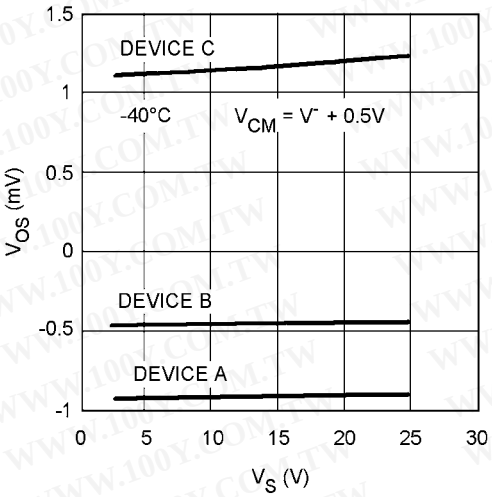


Figure 8.

Typical Performance Characteristics (continued)

V_{OS} vs. V_S for 3 Representative Units

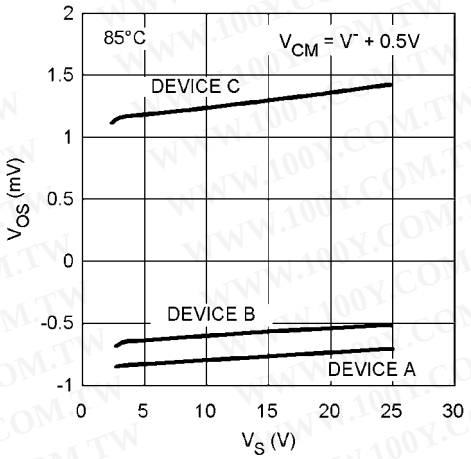


Figure 9.

I_B vs. V_S

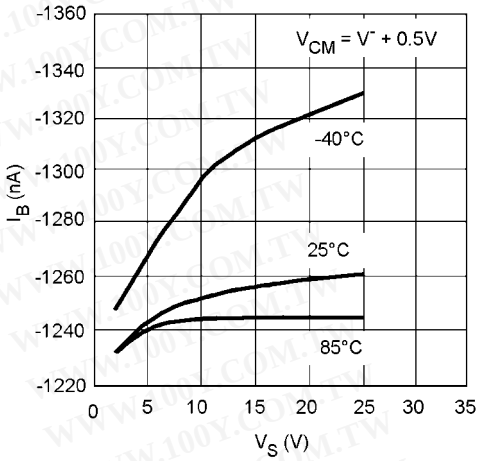


Figure 10.

I_B vs. V_S

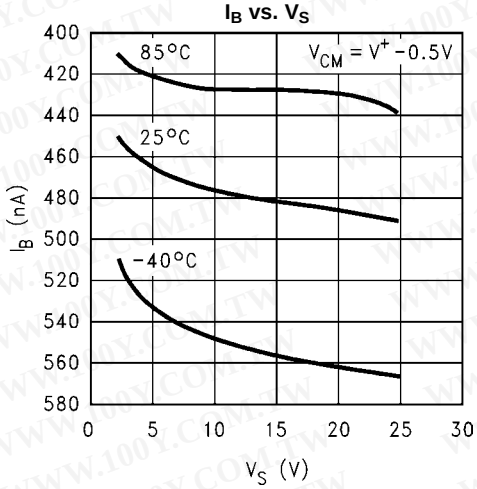


Figure 11.

I_S vs. V_{CM}

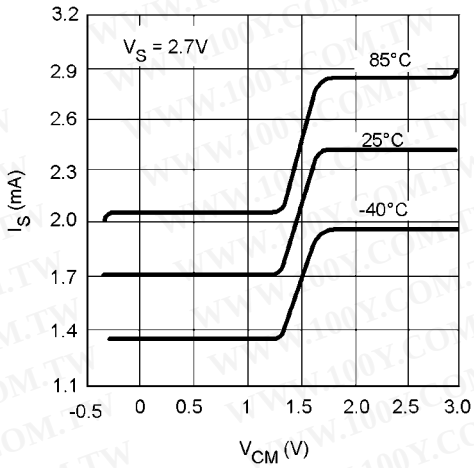


Figure 12.

I_S vs. V_{CM}

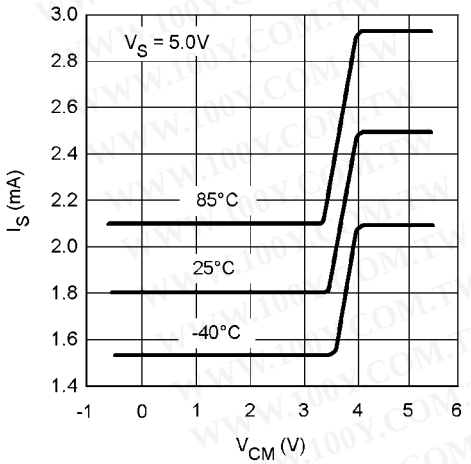


Figure 13.

I_S vs. V_S

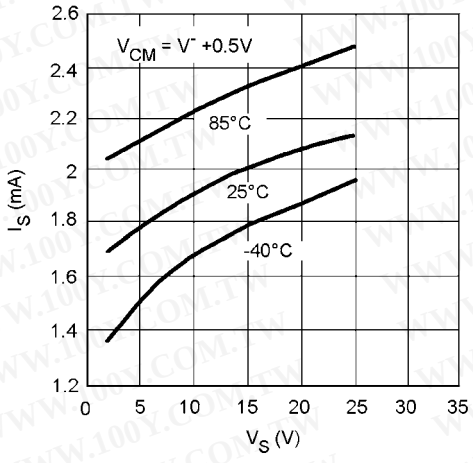


Figure 14.

Typical Performance Characteristics (continued)

I_S vs. V_S

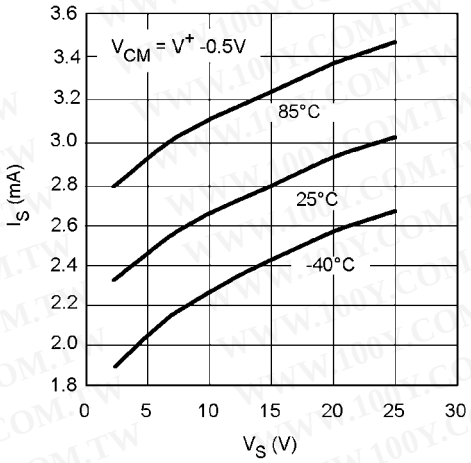


Figure 15.

CMRR vs. Frequency

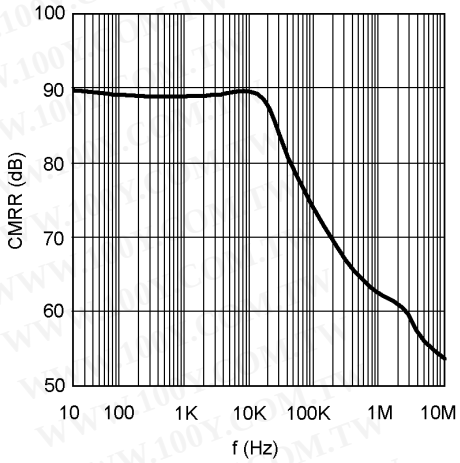


Figure 16.

+PSRR vs. Frequency

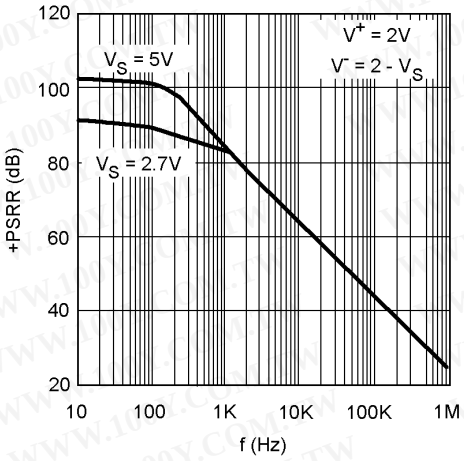


Figure 17.

−PSRR vs. Frequency

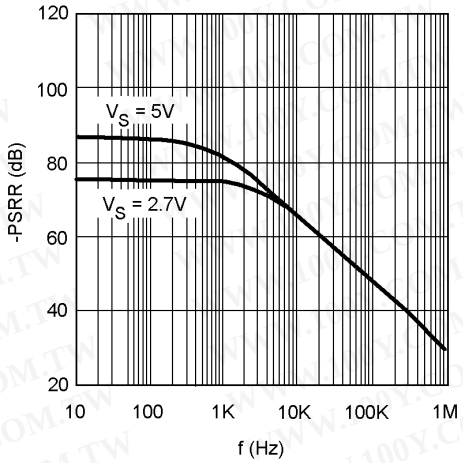


Figure 18.

Open Loop Gain/Phase for Various Supplies

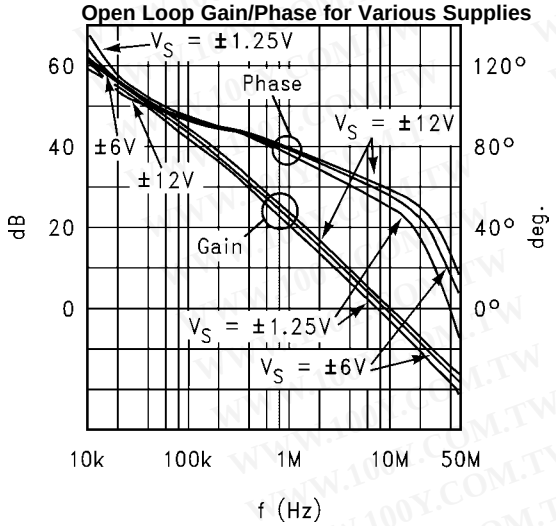


Figure 19.

Closed Loop Frequency Response for Various Gains

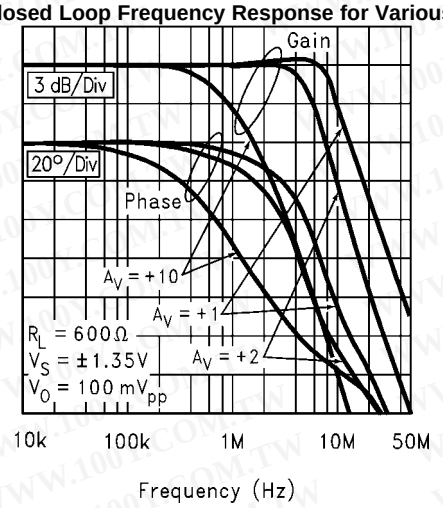


Figure 20.

Typical Performance Characteristics (continued)

Closed Loop Frequency Response for Various Gains

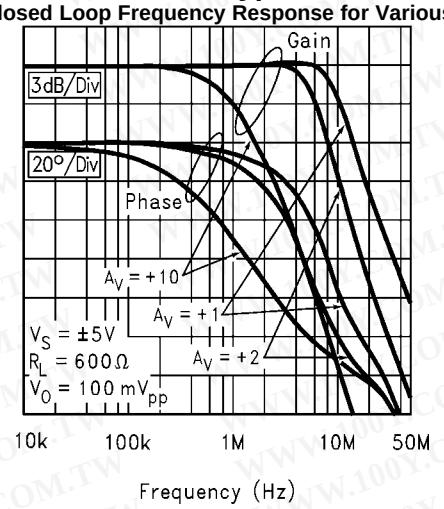


Figure 21.

Closed Loop Frequency Response for Various Gains R_L

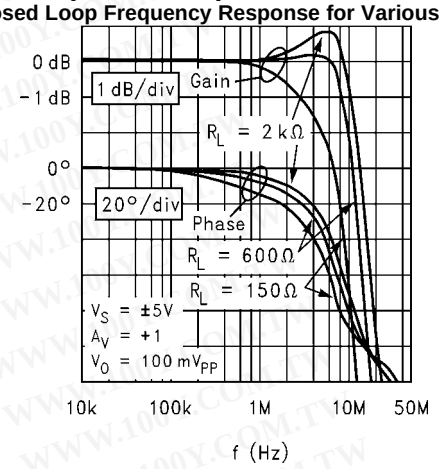


Figure 22.

Maximum Output Swing vs. Load (1% Distortion)

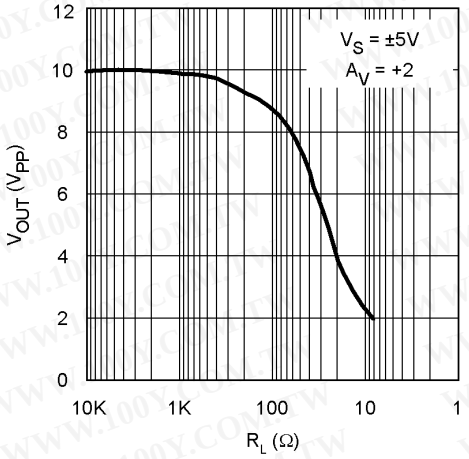


Figure 23.

Maximum Output Swing vs. Frequency (1% Distortion)

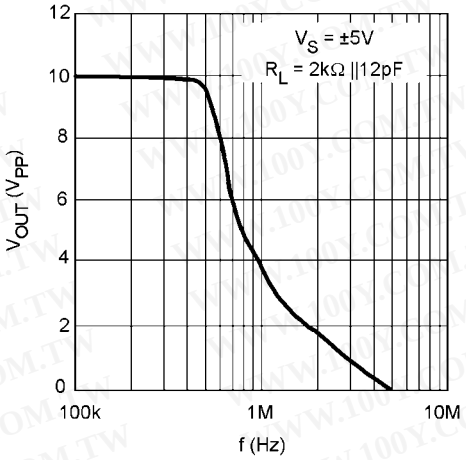


Figure 24.

Closed Loop Small Signal Frequency Response for Various C_L

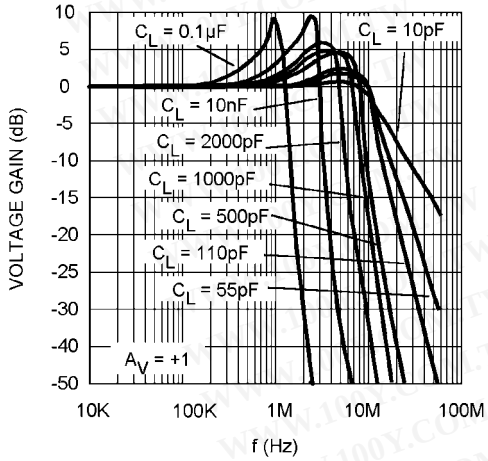


Figure 25.

Overshoot vs. Cap Load

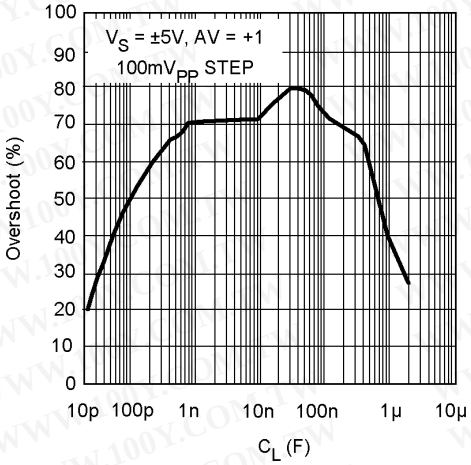


Figure 26.

Typical Performance Characteristics (continued)

Settling Time (±1%) & Slew Rate vs. Cap Load

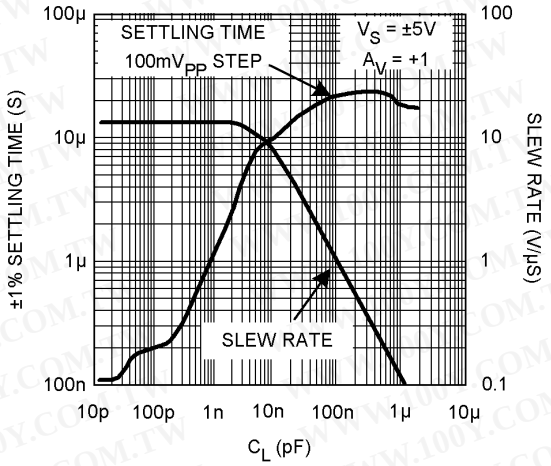


Figure 27.

V_{OUT} from V^+ vs. I_{SOURCE}

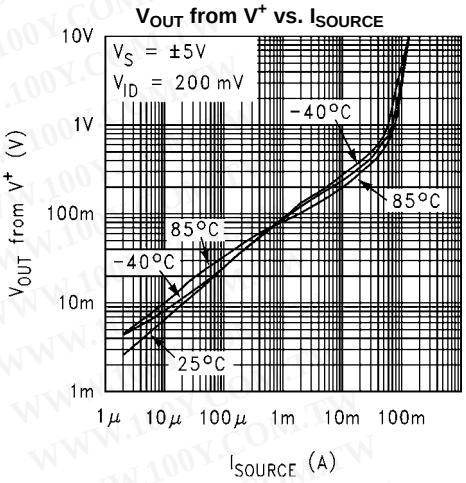


Figure 28.

V_{OUT} from V^- vs. I_{SINK}

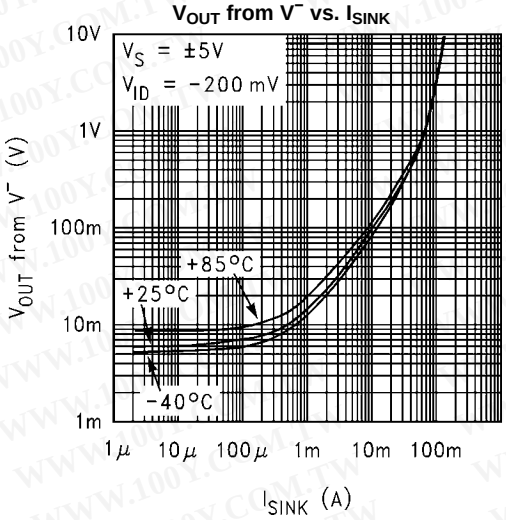


Figure 29.

Step Response for Various Amplitudes

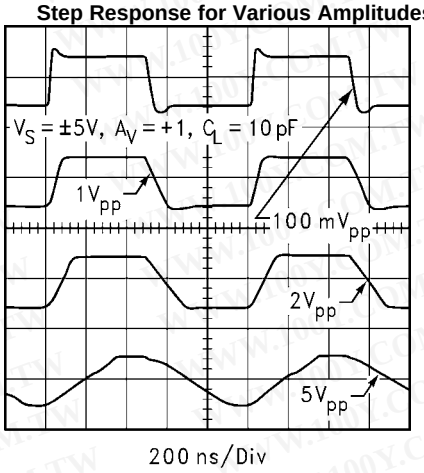


Figure 30.

Step Response for Various Amplitudes

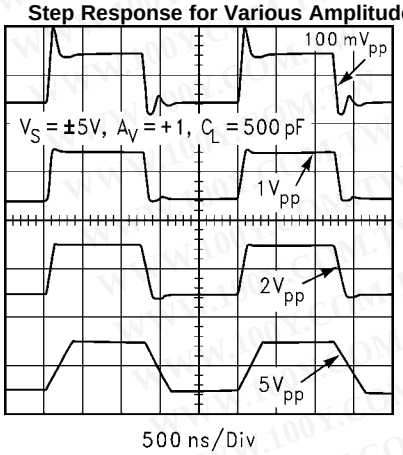


Figure 31.

Large Signal Step Response for Various Cap Loads

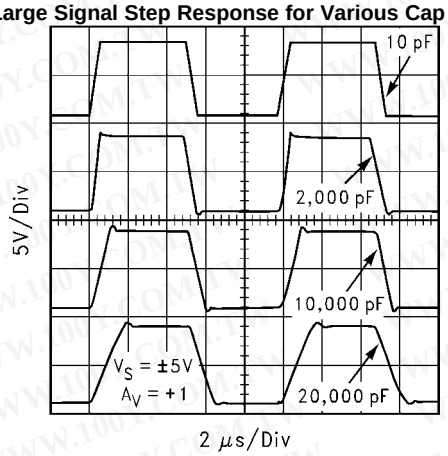


Figure 32.

Typical Performance Characteristics (continued)

THD+N vs. Input Amplitude for Various Frequency

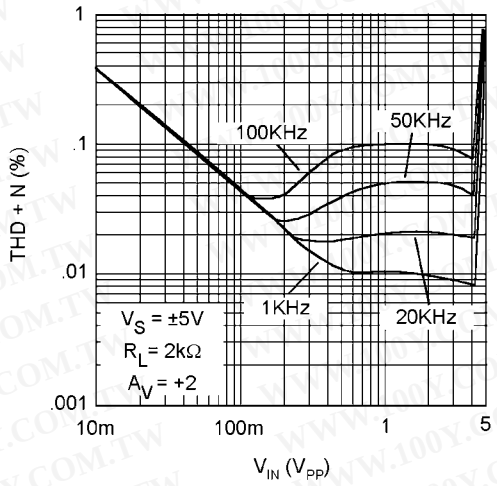


Figure 33.

Input Referred Noise Density

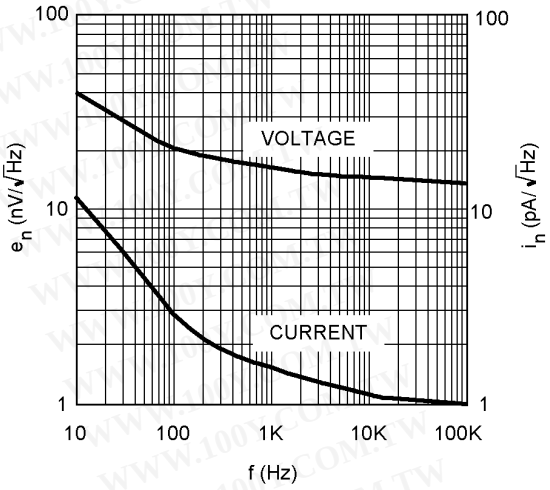


Figure 34.

Closed Loop Output Impedance vs. Frequency

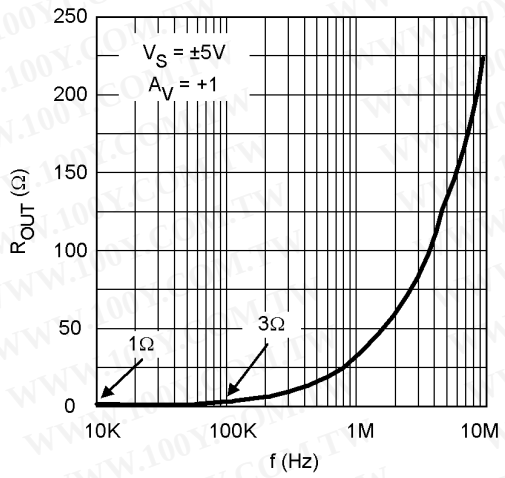


Figure 35.

Crosstalk Rejection vs. Frequency

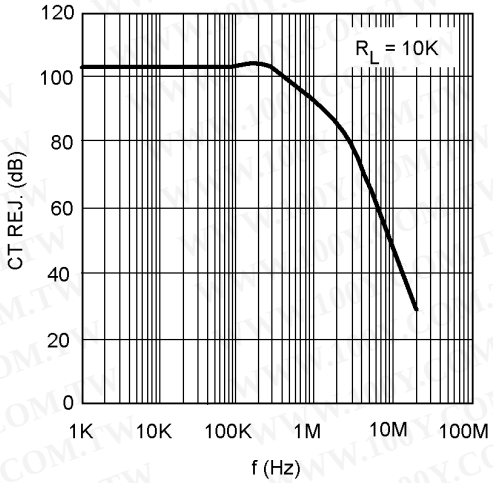


Figure 36.

APPLICATION NOTES

BLOCK DIAGRAM AND OPERATIONAL DESCRIPTION

A) INPUT STAGE:

As can be seen from the simplified schematic in Figure 37, the input stage consists of two distinct differential pairs (Q1-Q2 and Q3-Q4) in order to accommodate the full Rail-to-Rail input common mode voltage range. The voltage drop across R5, R6, R7 and R8 is kept to less than 200mV in order to allow the input to exceed the supply rails. Q13 acts as a switch to steer current away from Q3-Q4 and into Q1-Q2, as the input increases beyond 1.4 of V^+. This in turn shifts the signal path from the bottom stage differential pair to the top one and causes a subsequent increase in the supply current.

In transitioning from one stage to another, certain input stage parameters (V_{OS}, I_b, I_{OS}, e_n, and i_n) are determined based on which differential pair is "on" at the time. Input Bias current, I_b, will change in value and polarity as the input crosses the transition region. In addition, parameter such as PSRR and CMRR which involve the input offset voltage will also be effected by changes in V_{CM} across the differential pair transition region.

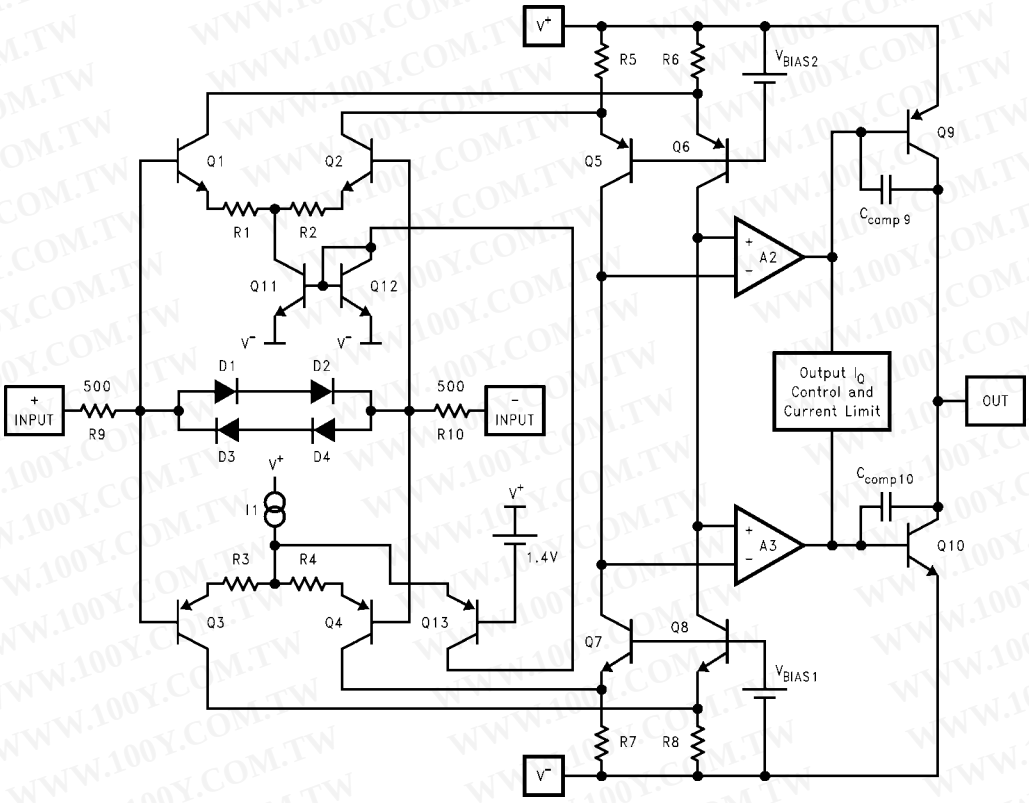


Figure 37. Simplified Schematic Diagram

The input stage is protected with the combination of R9-R10 and D1, D2, D3 and D4 against differential input over-voltages. This fault condition could otherwise harm the differential pairs or cause offset voltage shift in case of prolonged over voltage. As shown in Figure 38, if this voltage reaches approximately ±1.4V at 25°C, the diodes turn on and current flow is limited by the internal series resistors (R9 and R10). The Absolute Maximum Rating of ±10V differential on V_{IN} still needs to be observed. With temperature variation, the point were the diodes turn on will change at the rate of 5mV/°C

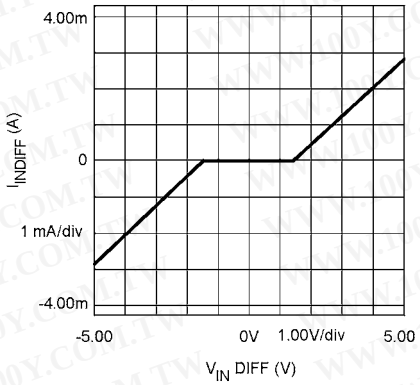


Figure 38. Input Stage Current vs. Differential Input Voltage

B) OUTPUT STAGE:

The output stage (see Figure 37) is comprised of complimentary NPN and PNP common-emitter stages to permit voltage swing to within a $V_{ce(sat)}$ of either supply rail. Q9 supplies the sourcing and Q10 supplies the sinking current load. Output current limiting is achieved by limiting the V_{ce} of Q9 and Q10; using this approach to current limiting, alleviates the draw back to the conventional scheme which requires one V_{be} reduction in output swing.

The frequency compensation circuit includes Miller capacitors from collector to base of each output transistor (see Figure 37, C_{comp9} and C_{comp10}). At light capacitive loads, the high frequency gain of the output transistors is high, and the Miller effect increases the effective value of the capacitors thereby stabilizing the Op Amp. Large capacitive loads greatly decrease the high frequency gain of the output transistors thus lowering the effective internal Miller capacitance - the internal pole frequency increases at the same time a low frequency pole is created at the Op Amp output due to the large load capacitor. In this fashion, the internal dominant pole compensation, which works by reducing the loop gain to less than 0dB when the phase shift around the feedback loop is more than 180°, varies with the amount of capacitive load and becomes less dominant when the load capacitor has increased enough. Hence the Op Amp is very stable even at high values of load capacitance resulting in the uncharacteristic feature of stability under all capacitive loads.

C) OUTPUT VOLTAGE SWING CLOSE TO V^-:

The LM8272's output stage design allows voltage swings to within millivolts of either supply rail for maximum flexibility and improved useful range. Because of this design architecture, as can be seen from Figure 37 diagram, with Output approaching either supply rail, either Q9 or Q10 Collector-Base junction reverse bias will decrease. With output less than a V_{be} from either rail, the corresponding output transistor operates near saturation. In this mode of operation, the transistor will exhibit higher junction capacitance and lower f_t which will reduce Phase Margin. With the Noise Gain (NG = 1 + Rf/Rg, Rf & Rg are external gain setting resistors) of 2 or higher, there is sufficient Phase Margin that this reduction (in Phase Margin) is of no consequence. However, with lower Noise Gain (<2) and with less than 150mV voltage to the supply rail, if the output loading is light, the Phase Margin reduction could result in unwanted oscillations.

In the case of the LM8272, due to inherent architectural specifics, the oscillation occurs only with respect to Q10 when output swings to within 150mV of V^-. However, if Q10 collector current is larger than its idle value of a few microamps, the Phase Margin loss becomes insignificant. In this case, 300µA is the required Q10 collector current to remedy this situation. Therefore, when all the aforementioned critical conditions are present at the same time (NG < 2, V_{OUT} < 150mV from supply rails, & output load is light) it is possible to ensure stability by adding a load resistor to the output to provide the necessary Q10 minimum Collector Current (300µA).

For 12V (or ±6V) operation, for example, add a 39kΩ resistor from the output to V^+ to cause 300µA output sinking current and ensure stability. This is equivalent to about 15% increase in total quiescent power dissipation.

DRIVING CAPACTIVE LOADS:

The LM8272 is specifically designed to drive unlimited capacitive loads without oscillations (see Settling Time and Slew Rate vs. Cap load plot, Figure 27). In addition, the output current handling capability of the device allows for good slewing characteristics even with large capacitive loads (Settling Time and Slew Rate vs. Cap Load plot). The combination of these features is ideal for applications such as TFT flat panel buffers, A/D converter input amplifiers, etc.

However, as in most Op Amps, addition of a series isolation resistor between the Op Amp and the capacitive load improves the settling and overshoot performance.

Output current drive is an important parameter when driving capacitive loads. This parameter will determine how fast the output voltage can change. Referring to the Settling Time and Slew Rate vs. Cap Load plot, (Figure 27), two distinct regions can be identified. Below about 10,000pF, the output Slew Rate is solely determined by the Op Amp's compensation capacitor value and available current into that capacitor. Beyond 10nF, the Slew Rate is determined by the Op Amp's available output current. An estimate of positive and negative slew rates for loads larger than 100nF can be made by dividing the short circuit current value by the capacitor.

ESTIMATING THE OUTPUT VOLTAGE SWING

It is important to keep in mind that the steady state output current will be less than the current available when there is an input overdrive present. For steady state conditions, Figure 39 and Figure 40 plots can be used to predict the output swing. These plots also show several load lines corresponding to loads tied between the output and ground. In each case, the intersection of the device plot at the appropriate temperature with the load line would be the typical output swing possible for that load. For example, a 600Ω load can accommodate an output swing to within 100mV of V^- and to 250mV of V^+ (V_S = ±5V) corresponding to a typical 9.65V_{PP} unclipped swing.

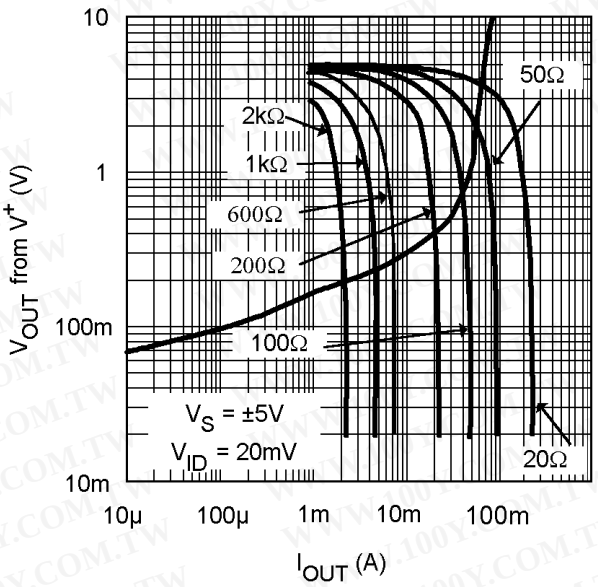


Figure 39. Steady State Output Sourcing Characteristics with Load Lines

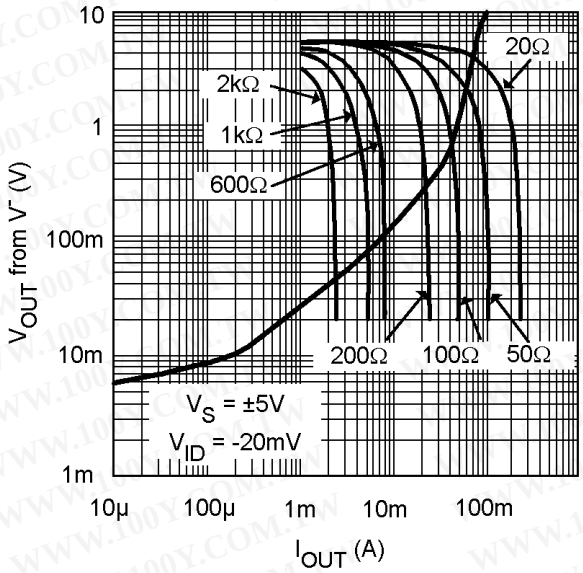


Figure 40. Steady State Output Sinking Characteristics with Load Lines

OUTPUT SHORT CIRCUIT CURRENT AND DISSIPATION ISSUES:

The LM8272 output stage is designed for maximum output current capability. Even though momentary output shorts to ground and either supply can be tolerated at all operating voltages, longer lasting short conditions can cause the junction temperature to rise beyond the absolute maximum rating of the device, especially at higher supply voltage conditions. Below supply voltage of 6V, output short circuit condition can be tolerated indefinitely.

With the Op Amp tied to a load, the device power dissipation consists of the quiescent power due to the supply current flow into the device, in addition to power dissipation due to the load current. The load portion of the power itself could include an average value (due to a DC load current) and an AC component. DC load current would flow if there is an output voltage offset, or the output AC average current is non-zero, or if the Op Amp operates in a single supply application where the output is maintained somewhere in the range of linear operation. Therefore:

$P_{total} = P_Q + P_{DC} + P_{AC}$

$P_Q = I_S \cdot V_S$ Op Amp Quiescent Power Dissipation

$P_{DC} = I_O \cdot (V_r - V_o)$ DC Load Power

P_{AC} = See Table 1 below AC Load Power

where:

- I_S: Supply Current
- V_S: Total Supply Voltage ($V^+ - V^-$)
- V_O: Average Output Voltage
- V_r: V^+ for sourcing and V^- for sinking current

Table 1 below shows the maximum AC component of the load power dissipated by the Op Amp for standard Sinusoidal, Triangular, and Square Waveforms:

Table 1. Normalized AC Power Dissipated in the Output Stage for Standard Waveforms

P_{AC} (W.Ω/V^2)		
Sinusoidal	Triangular	Square
50.7×10^{-3}	46.9×10^{-3}	62.5×10^{-3}

The table entries are normalized to V_S^2/R_L. To figure out the AC load current component of power dissipation, simply multiply the table entry corresponding to the output waveform by the factor V_S^2/R_L. For example, with ±12V supplies, a 600Ω load, and triangular waveform power dissipation in the output stage is calculated as:

$$P_{AC} = (46.9 \times 10^{-3}) \cdot [24^2/600] = 45.0mW$$

OTHER APPLICATION HINTS:

The use of supply decoupling is mandatory in most applications. As with most relatively high speed/high output current Op Amps, best results are achieved when each supply line is decoupled with two capacitors; a small value ceramic capacitor (~0.01µF) placed very close to the supply lead in addition to a large value Tantalum or Aluminum (> 4.7µF). The large capacitor can be shared by more than one device if necessary. The small ceramic capacitor maintains low supply impedance at high frequencies while the large capacitor will act as the charge "bucket" for fast load current spikes at the Op Amp output. The combination of these capacitors will provide supply decoupling and will help keep the Op Amp oscillation free under any load.

LM8272 ADVANTAGES:

Compared to other Rail-to-Rail Input/Output devices, the LM8272 offers several advantages such as:

- Improved cross over distortion
- Nearly constant supply current throughout the output voltage swing range and close to either rail.
- Nearly constant Unity gain frequency (f_u) and Phase Margin (Phi_m) for all operating supplies and load conditions.
- No output phase reversal under input overload condition.

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM8272MM	ACTIVE	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	A60	Samples
LM8272MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A60	Samples
LM8272MMX	ACTIVE	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 85	A60	Samples
LM8272MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A60	Samples

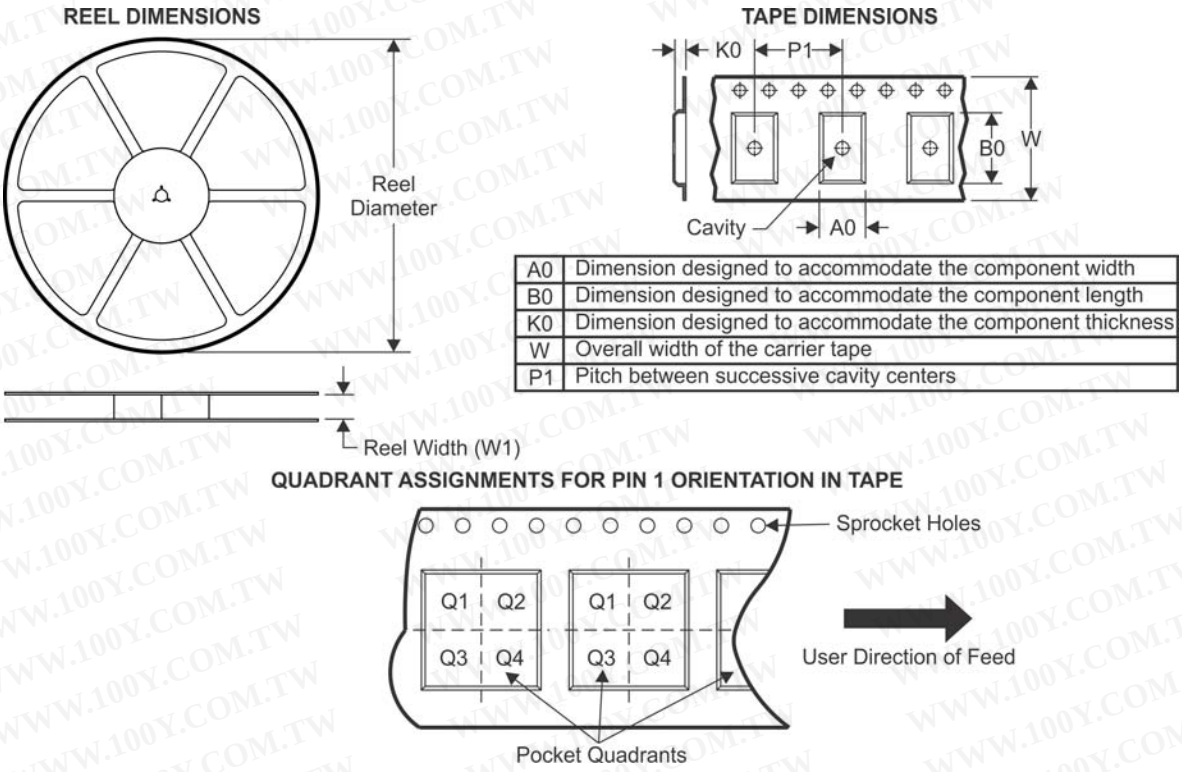
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

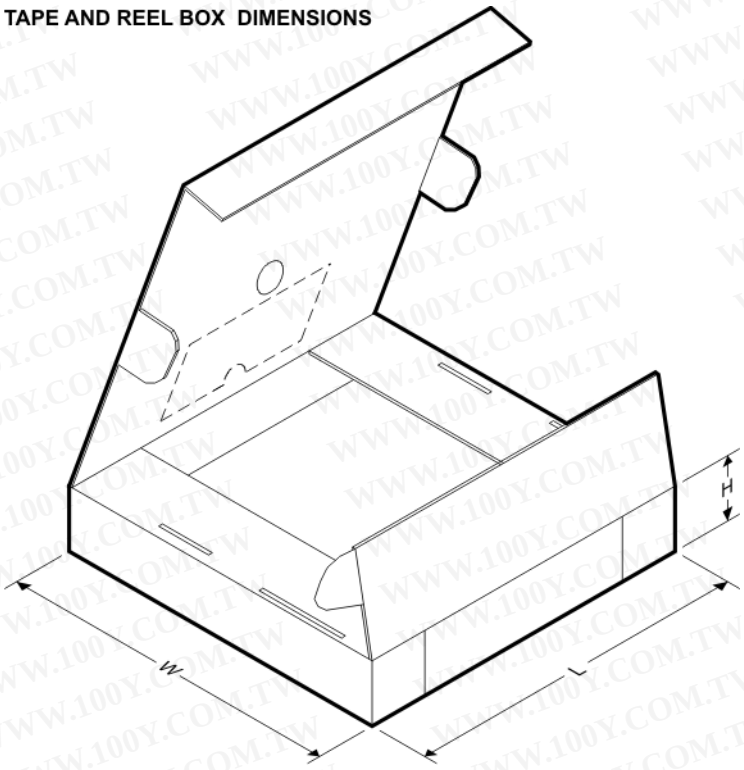


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM8272MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM8272MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM8272MMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM8272MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

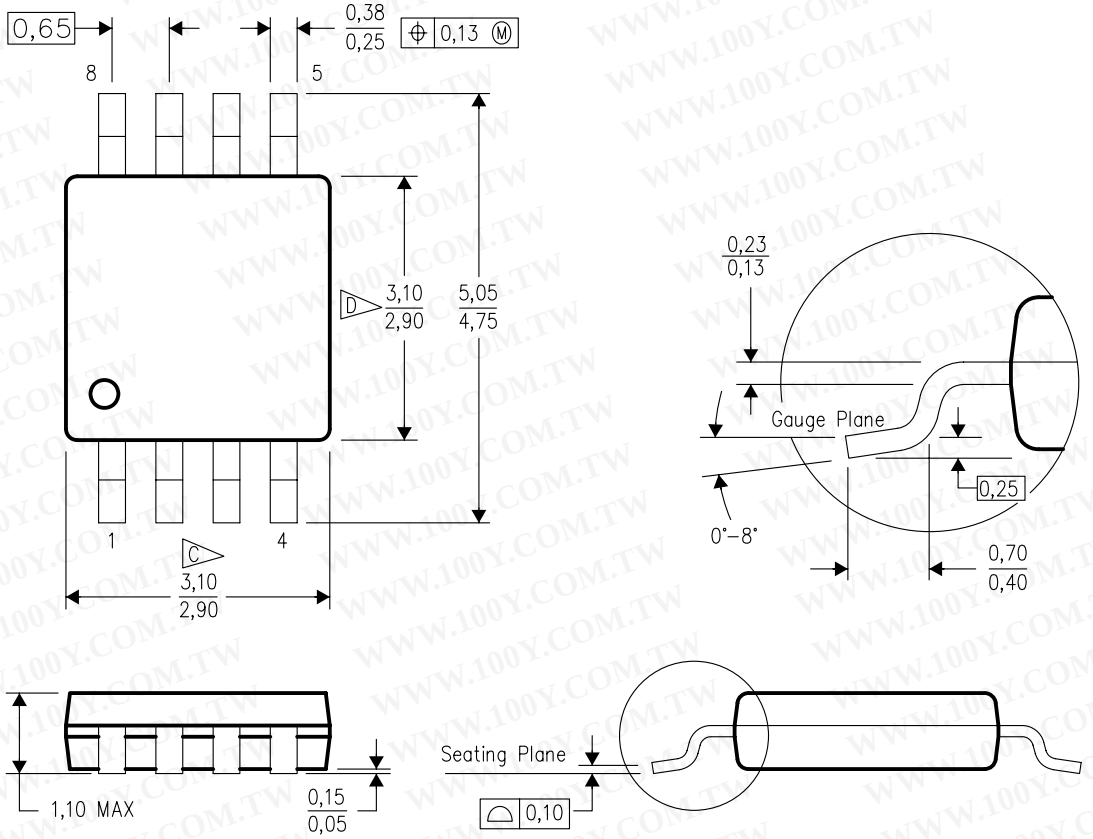
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM8272MM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM8272MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM8272MMX	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM8272MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

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