SLOS463A-APRIL 2005-REVISED JULY 2005

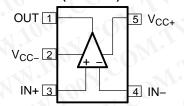
#### **FEATURES**

- 2.7-V and 5-V Performance
- Low Offset Voltage . . . 0.4 mV Typ, 3 mV Max
- Input Common-Mode Range . . . 200 mV Beyond the Rails
- Rail-to-Rail Swing Into 600  $\Omega$
- Gain Bandwidth . . . 5 MHz Typ
- Slew Rate . . . 5 V/μs Typ
- Turn-On Time From Shutdown . . . <10  $\mu$ s
- Shutdown Current . . . 0.2 μA Typ
- Space-Saving Packages
  - SOT-23-5/6
  - SC-70

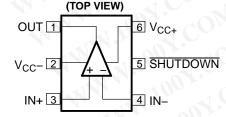
#### **APPLICATIONS**

- Wireless Phones, Mobile Phones, PDAs
- GSM/TDMA/CDMA Power Amp Control
- AGC, RF Power Detectors
- Temperature Compensation
- Wireless LANs
- Bluetooth
- HomeRF

#### LMV710 DBV (SOT-23-5) OR DCK (SC-70) PACKAGE (TOP VIEW)



#### LMV711/LMV715 DBV (SOT-23-6) OR DCK (SC-70) PACKAGE



勝 特 力 材 料 886-3-5753170 胜特力电子(上海) 86-21-34970699 胜特力电子(深圳) 86-755-83298787 Http://www.100y.com.tw

#### DESCRIPTION/ORDERING INFORMATION

The LMV710, LMV711, and LMV715 are single BiCMOS operational amplifiers designed to meet the demands of low power, low cost, and small size required by battery-powered portable electronics. These devices have an input common-mode voltage range that exceeds the rails, rail-to-rail output, and high output-current drive. The devices offer a bandwidth of 5 MHz and a slew rate of 5  $V/\mu s$ .

On the LMV711 and LMV715, a separate shutdown pin can be used to disable the device and reduce the supply current to 0.2 µA typical. The device features a turn-on time of less than 10 µs. It is an ideal solution for power-sensitive applications, such as cellular phones, pagers, palm computers, etc.

The LMV710I, LMV711I, and LMV715I are characterized for operation from -40°C to 85°C.

#### **ORDERING INFORMATION**

T <sub>A</sub>	PACK	AGE <sup>(1)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
100.	SOT-23-5 – DBV	Reel of 3000	LMV710IDBVR	RB4_
	SC-70 - DCK	Reel of 3000	LMV710IDCKR	RE_
4000 1- 0500	SOT-23-6 – DBV Reel of 3000		LMV711IDBVR	RB5_
–40°C to 85°C	SC-70 - DCK	Reel of 3000	LMV711IDCKR	RF_
	SOT-23-6 - DBV	Reel of 3000	LMV715IDBVR	4B9_
	SC-70 - DCK	Reel of 3000	LMV715IDCKR	RL_

Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

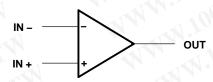
(2) DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.



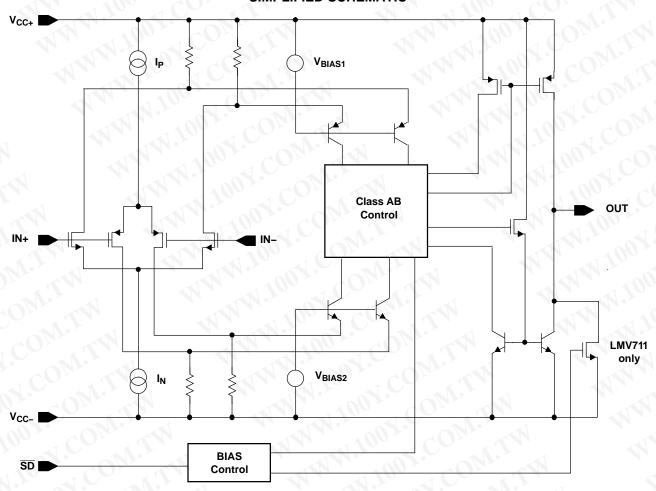
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.







#### SIMPLIFIED SCHEMATIC





#### Absolute Maximum Ratings (1)

over operating free-air temperature range (unless otherwise noted)

	10, 11,		100	MIN	MAX	UNIT	
V <sub>CC+</sub> - V <sub>CC-</sub>	Supply voltage (2)		100		6	V	
V <sub>ID</sub>	Differential input voltage <sup>(3)</sup>	M	11.100	of LCO	V		
VI	Input voltage (either input)		110	V <sub>CC</sub> - 0.4	$V_{CC+} + 0.4$	V	
Vo	Output voltage	ltage					
l <sub>l</sub>	Input current <sup>(4)</sup>			1 C	±10	mA	
	NA. 100 r. COAr.	DDV neekens	5 pin	007			
	Deckage thermal impedance (5) (6)	DBV package	6 pin	N.Y	0C/M		
$ heta_{JA}$	Package thermal impedance (5)(6)	DCK poskogo	5 pin	100	°C/W		
		DCK package	6 pin	AN.			
T <sub>J</sub>	Operating virtual junction temperature			1 100	150	°C	
T <sub>stg</sub>	Storage temperature range	N. AN		-65	150	°C	

- Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltage values (except differential voltages and V<sub>CC</sub> specified for the measurement of I<sub>OS</sub>) are with respect to the network GND.
- Differential voltages are at IN+ with respect to IN-.
- Excessive input current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs unless some
- Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability. The package thermal impedance is calculated in accordance with JESD 51-7.

#### **Recommended Operating Conditions**

		MIN N	IAX UNIT
$V_{CC+} - V_{CC-}$	Supply voltage	2.7	5 V
T <sub>A</sub>	Operating free-air temperature	-40	85 °C

#### **ESD Protection**

N. M.	M. M. M.	TYP	UNIT
Human-Body Model	100, CO; LM	TBD	V
Machine Model		TBD	V





#### **Electrical Characteristics**

 $\rm V_{CC+}$  = 2.7 V,  $\rm V_{CC-}$  = GND,  $\rm V_{IC}$  = 1.35 V, and  $\rm R_L > 1~M\Omega$  (unless otherwise noted)

	PARAMETER	TEST CONDITIO	NS	TA	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_{IC} = 0.85 \text{ V and } 1.85 \text{ V}$	v - 1	25°C		0.4	3	mV
VIO	input offset voltage	VIC = 0.00 V and 1.00	V	–40°C to 85°C	100	1	3.2	IIIV
I <sub>IB</sub>	Input bias current			25°C	7.	4		pA
CMRR	Common-mode rejection ratio	0 ≤ V <sub>IC</sub> ≤ 2.7 V		25°C	50	75		dB
Civilata	Common-mode rejection ratio	0 5 V   C 5 2.1 V		-40°C to 85°C	45			UD
		$2.7 \text{ V} \le \text{V}_{\text{CC+}} \le 5 \text{ V},$		25°C	70	110		
k .	Supply-voltage rejection ratio	$V_{IC} = 0.85 \text{ V}$		–40°C to 85°C	68		7 / 1	dB
k <sub>SVR</sub>	Supply-voltage rejection ratio	$2.7 \text{ V} \le \text{V}_{\text{CC+}} \le 5 \text{ V},$		25°C	70	95		ub.
	1 100 1 C	$V_{IC} = 1.85 \text{ V}$		–40°C to 85°C	68	1 (		
V <sub>ICR</sub>	Common-mode input voltage range	CMRR ≥ 50 dB		25°C	-0.2 to 2.9	-0.3 to 3		V
		Sourcing V = 0		25°C	15	28		
L	Output about almost accommod (1)	Sourcing V <sub>O</sub> = 0		-40°C to 85°C	12	100	-1	
los	Output short circuit current <sup>(1)</sup>	Sinking V F V		25°C	25	40	07.	mA
	11 11 10	Sinking $V_0 = 5 \text{ V}$		-40°C to 85°C	22	AN A	_41	
	MA IN 1	CON	V <sub>OH</sub>	25°C -40°C to 85°C	2.62	2.68	100	
		$R_L = 10 \text{ k}\Omega \text{ to } 1.35 \text{ V}$		25°C		0.01	0.12	
		V		–40°C to 85°C		- 1	0.15	
Vo	Output voltage			25°C	2.52	2.55	-11	O A
		D 000 0 to 4.05 V	V <sub>OH</sub>	-40°C to 85°C	2.5	*		
		$R_L = 600 \Omega$ to 1.35 V	V <sub>OL</sub>	25°C		0.05	0.23	
		107	-40°C to 85°C			0.3		
V <sub>O(SD)</sub>	Output voltage level in shutdown mode	LMV711 only		25°C		50	200	mV
I <sub>O(SD)</sub>	Output leakage current in shutdown mode	LMV715 only	11.	25°C	N	1		pA
C <sub>O(SD)</sub>	Output capacitance in shutdown mode	LMV715 only	NO I	25°C		32		pF
		ON mode		25°C		1.22	1.7	mA
I <sub>CC</sub>	Supply current	ON mode		-40°C to 85°C			1.9	ША
		Shutdown mode, SHDI	$0 = \overline{V}$	25°C		0.002	10	μΑ
		Sourcing $R_L = 10 \text{ k}\Omega$ ,		25°C	80	115		
		$V_0 = 1.35 \text{ V to } 2.3 \text{ V}$	M.	–40°C to 85°C	76	-1		
		Sinking $R_L = 10 \text{ k}\Omega$ ,		25°C	80	113		
$A_V$	Large-signal voltage gain	$V_0 = 0.4 \text{ V to } 1.35 \text{ V}$		-40°C to 85°C	76			dB
~∨	Large-signal voltage gain	Sourcing $R_L = 600 \Omega$ ,		25°C	80	110	7	uБ
		$V_0 = 1.35 \text{ V} \text{ to } 2.2 \text{ V}$		-40°C to 85°C	76	Zir.		
		Sinking $R_L = 600 \Omega$ ,		25°C	80	100	1	
	100, CO <sub>2</sub>	$V_0 = 0.5 \text{ V to } 1.35 \text{ V}$	$V_0 = 0.5 \text{ V to } 1.35 \text{ V}$			OA		N
SR (2)	Slew rate		114	25°C		5	1.	V/μs
GBWP	Gain bandwidth product			25°C	20	5		MHz
$\Phi_{m}$	Phase margin	Mr.		25°C		60		deg
T <sub>(on)</sub>	Amplifier turn-on time			25°C	100	<10		μs

Shorting the output to either supply rails will adversely affect reliability. Number specified is the slower of the positive and negative slew rates.

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#### **Electrical Characteristics (continued)**

 $V_{CC+}$  = 2.7 V,  $V_{CC-}$  = GND,  $V_{IC}$  = 1.35 V, and  $R_L$  > 1 M $\Omega$  (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT	
SHDN	Shutdown pin voltago rango	V <sub>(ON)</sub>	25°C	2.4 to 2.7	1.5 to 2.7		V	
SHIDIN	Shutdown pin voltage range	V <sub>(OFF)</sub>	25 0	7.	0 to 1	0 to 0.8	N	
$V_n$	Input referred voltage noise	f = 1 kHz	25°C		20	1.	nV/√ <del>Hz</del>	

#### **Electrical Characteristics**

 $V_{CC+} = 3.2 \text{ V}, V_{CC-} = \text{GND}, \text{ and } V_{IC} = 1.6 \text{ V} \text{ (unless otherwise noted)}$ 

	PARAMETER	TEST CONDITI	TA	MIN	TYP	MAX	UNIT	
				25°C	2.95	3		101.
V <sub>O</sub> Output vol	Output value	( C = m A	V <sub>OH</sub>	-40°C to 85°C	2.92	00	1	V
	Output voltage	$I_O = 6.5 \text{ mA}$		25°C	M.	0.01	0.18	
.4			V <sub>OL</sub>	-40°C to 85°C		700	0.25	





#### **Electrical Characteristics**

 $\rm V_{CC+}$  = 5 V,  $\rm V_{CC-}$  = GND,  $\rm V_{IC}$  = 2.5 V, and  $\rm R_{L}$  > 1  $\rm M\Omega$  (unless otherwise noted)

1	PARAMETER	TEST CONDITIO	NS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	V <sub>IC</sub> = 0.85 V and 1.85	v	25°C		0.4	3	mV
VIO	input onset voltage	V <sub>IC</sub> = 0.00 V and 1.00		–40°C to 85°C	1 CV	1	3.2	
I <sub>IB</sub>	Input bias current			25°C	1.	4		pA
CMRR	Common-mode rejection ratio	$0 \le V_{IC} \le 2.7 \text{ V}$		25°C	50	75		dB
OWNER	Common mode rejection ratio	0 = V <sub>1</sub> C = 2.1 V		-40°C to 85°C	48			ub
		$2.7 \text{ V} \le \text{V}_{\text{CC+}} \le 5 \text{ V},$		25°C	70	110		
k	Supply-voltage rejection ratio	$V_{IC} = 0.85 \text{ V}$	–40°C to 85°C	68		7	dB	
k <sub>SVR</sub>	Suppry-voltage rejection ratio	$2.7 \text{ V} \le \text{V}_{\text{CC+}} \le 5 \text{ V},$		25°C	70	95		UD.
<	1 1 1 C	$V_{IC} = 1.85 \text{ V}$		–40°C to 85°C	68	1 (		
V <sub>ICR</sub>	Common-mode input voltage range	CMRR ≥ 50 dB		25°C	-0.2 to 5.2	-0.3 to 5.3		V
		Sourcing V = 0		25°C	25	35		
Lz	Output abort circuit aureaut(1)	Sourcing V <sub>O</sub> = 0		-40°C to 85°C	21	1700	_1	m ^
los	Output short circuit current <sup>(1)</sup>	Sinking V = F V	N	25°C	25	40		mA
1	11, 11, 10	Sinking $V_0 = 5 \text{ V}$		-40°C to 85°C	21	- N.		100
		10, 40 h	V	25°C	4.92	4.98	400	
		D 4010 to 4.05 V	V <sub>OH</sub>	-40°C to 85°C	4.9	IN		
		$R_L = 10 \text{ k}\Omega \text{ to } 1.35 \text{ V}$	· ·	25°C		0.01	0.12	
	Output valtage	$V_{OH}$ $R_{L} = 600 \Omega \text{ to } 1.35 \text{ V}$	V <sub>OL</sub>	–40°C to 85°C			0.15	
Vo	Output voltage		\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	25°C	4.82	4.85	411	V
			VOH	-40°C to 85°C	4.8		MA.	
		$R_L = 600  \Omega  1.35  V$	V	25°C		0.05	0.23	
		11 100 2.	V <sub>OL</sub>	-40°C to 85°C			0.3	
V <sub>O(SD)</sub>	Output voltage level in shutdown mode	LMV711 only		25°C		50	200	mV
I <sub>O(SD)</sub>	Output leakage current in shutdown mode	LMV715 only	11.	25°C	N	1		pA
C <sub>O(SD)</sub>	Output capacitance in shutdown mode	LMV715 only		25°C		32		pF
		ON mode		25°C		1.17	1.7	mA
I <sub>CC</sub>	Supply current	ON mode	200	-40°C to 85°C			1.9	IIIA
		Shutdown mode, SHD	$\overline{N} = 0$	25°C		0.2	10	μΑ
		Sourcing $R_L = 10 \text{ k}\Omega$ ,		25°C	80	123		
		$V_0 = 1.35 \text{ V to } 2.3 \text{ V}$	M.	–40°C to 85°C	76	- 1		
		Sinking $R_L = 10 \text{ k}\Omega$ ,		25°C	80	120		
^	Large-signal voltage gain	$V_0 = 0.4 \text{ V to } 1.35 \text{ V}$		-40°C to 85°C	76			dB
$A_V$	Large-Signal Voltage gain	Sourcing $R_L = 600 \Omega$ ,		25°C	80	110		uБ
		$V_0 = 1.35 \text{ V to } 2.2 \text{ V}$		-40°C to 85°C	76			
		Sinking $R_L = 600 \Omega$ ,	AN .	25°C	80	118		
		$V_0 = 0.5 \text{ V} \text{ to } 1.35 \text{ V}$		-40°C to 85°C	76	02,		
SR <sup>(2)</sup>	Slew rate	- 41	114	25°C		5	1.7	V/μs
GBWP	Gain bandwidth product			25°C	20	5		MHz
$\Phi_{m}$	Phase margin			25°C		60		deg
T <sub>(on)</sub>	Amplifier turn-on time			25°C	100	<10	Ω,	μs

Shorting the output to either supply rails will adversely affect reliability. Number specified is the slower of the positive and negative slew rates. (2)



#### **Electrical Characteristics (continued)**

 $V_{CC+}$  = 5 V,  $V_{CC-}$  = GND,  $V_{IC}$  = 2.5 V, and  $R_L$  > 1 M $\Omega$  (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
SHDN	Shutdown pin voltage range	V <sub>(ON)</sub>	25°C	2.4 to 5	2.4 to 5 2 to 5 0 to 1.5 0 to 0.8		V
SHUN	Shuldown pin voltage range	V <sub>(OFF)</sub>	25 0	7.			N
V <sub>n</sub>	Input referred voltage noise	f = 1 kHz	25°C		20	1.	nV/√ <del>Hz</del>

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#### TYPICAL PERFORMANCE CHARACTERISTICS

#### **GRAPH PREVIEWS**

- Figure 1. Supply Current vs Supply Voltage (ON Mode)
- Figure 2. LMV711/LMV715 Supply Current vs Supply Voltage (Shutdown Mode)
- Figure 3. Output Positive Swing vs Supply Voltage  $R_1 = 600 \Omega$ )
- Figure 4. Output Negative Swing vs Supply Voltage  $R_1 = 600 \Omega$ )
- Figure 5. Output Positive Swing vs Supply Voltage  $R_1 = 10 \text{ k}\Omega$ )
- Figure 6. Output Negative Swing vs Supply Voltage  $R_1 = 10 \text{ k}\Omega$ )
- Figure 7. Output Positive Swing vs Supply Voltage ( $I_{SRC} = 7 \text{ mA}$ )
- Figure 8. Output Negative Swing vs Supply Voltage ( $I_{SINK} = 7 \text{ mA}$ )
- Figure 9. Input Voltage Noise vs Frequency
- Figure 10. PSRR vs Frequency
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- Figure 12. LMV711/LMV715 Turn-On Characteristics
- Figure 13. Sourcing Current vs Output Voltage
- Figure 14. Sinking Current vs Output Voltage
- Figure 15. THD+N vs Frequency (V<sub>CC</sub> = 5 V)
- Figure 16. THD+N vs Frequency ( $V_{CC} = 2.7 \text{ V}$ )
- Figure 17. THD+N vs  $V_{OUT}$  ( $V_{CC+} = \pm 2.5 \text{ V}$ )
- Figure 18. THD+N vs  $V_{OUT}$  ( $V_{CC\pm} = \pm 1.35 \text{ V}$ )
- Figure 19.  $C_{CM}$  vs  $V_{CM}$  ( $V_{CC} = 2.7$  V)
- Figure 20.  $C_{CM}$  vs  $V_{CM}$  ( $V_{CC} = 5 \text{ V}$ )
- Figure 21.  $C_{DIFF}$  vs  $V_{CM}$  ( $V_{CC} = 2.7 \text{ V}$ )
- Figure 22.  $C_{DIFF}$  vs  $V_{CM}$  ( $V_{CC} = 5 \text{ V}$ )
- Figure 23. Open-Loop Frequency Response (V<sub>CC±</sub> = ±1.35 V)
- Figure 24. Open-Loop Frequency Response ( $V_{CC\pm} = \pm 1.6 \text{ V}$ )
- Figure 25. Open-Loop Frequency Response ( $V_{CC+} = \pm 2.5 \text{ V}$ )
- Figure 26. Open-Loop Frequency Response ( $V_{CC\pm} = \pm 1.35 \text{ V}$ )
- Figure 27. Open-Loop Frequency Response ( $V_{CC+} = \pm 1.6 \text{ V}$ )
- Figure 28. Open-Loop Frequency Response ( $V_{CC+} = \pm 2.5 \text{ V}$ )
- Figure 29. Noninverting Large Signal Pulse Response
- Figure 30. Noninverting Small Signal Pulse Response Figure
- Figure 31. Inverting Large Signal Pulse Response
- Figure 32. Inverting Small Signal Pulse Response
- Figure 33.  $V_{OS}$  vs  $V_{CM}$  ( $V_{CC} = 2.7 \text{ V}$ )
- Figure 34.  $V_{OS}$  vs  $V_{CM}$  ( $V_{CC} = 5$  V)

#### **PACKAGE OPTION ADDENDUM**





#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
LMV710IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV710IDBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV710IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV710IDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV710IDCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV710IDCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV711IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV711IDBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV711IDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV711IDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV711IDCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV711IDCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV715IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV715IDBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV715IDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV715IDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV715IDCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV715IDCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): Tl's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



#### PACKAGE OPTION ADDENDUM

18-Mar-2008

package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

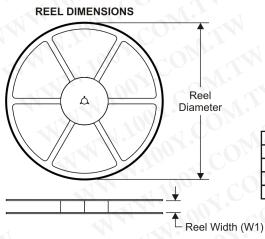
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#### PACKAGE MATERIALS INFORMATION

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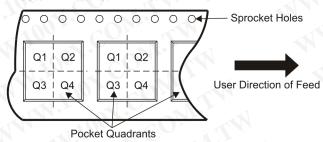
#### TAPE AND REEL INFORMATION



# TAPE DIMENSIONS KO P1 BO W Cavity A0

١	Α0	Dimension designed to accommodate the component width
1	B0	Dimension designed to accommodate the component length
	K0	Dimension designed to accommodate the component thickness
Ì	W	Overall width of the carrier tape
1	P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



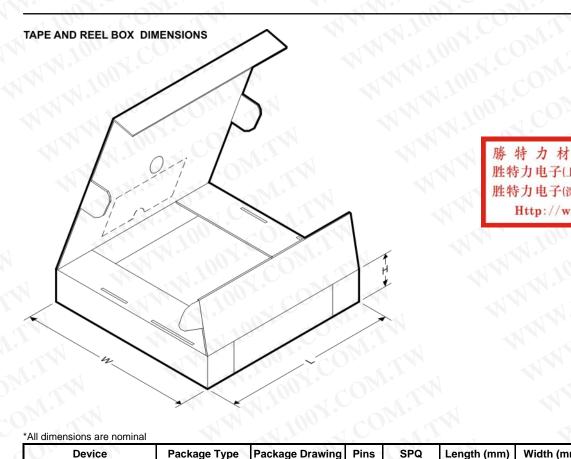
#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV710IDBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV710IDCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
LMV711IDBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV711IDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
LMV715IDBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV715IDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3

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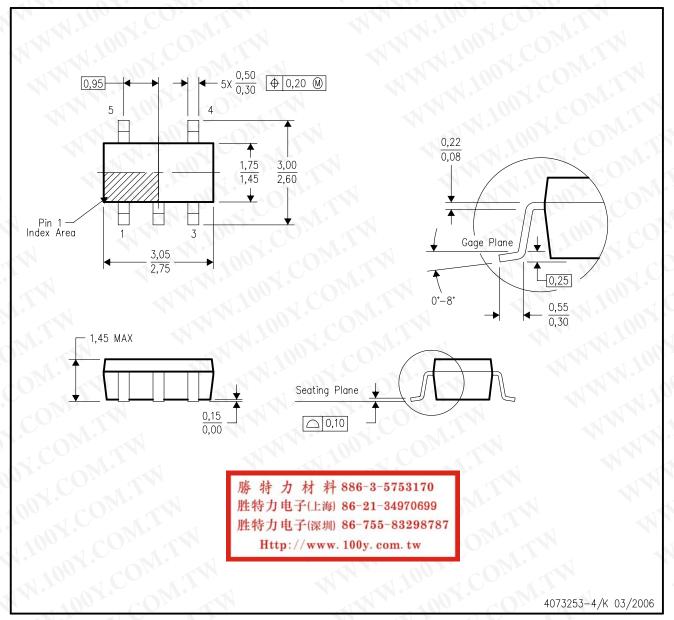
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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm
LMV710IDBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
LMV710IDCKR	SC70	DCK	5	3000	203.0	203.0	35.0
LMV711IDBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
LMV711IDCKR	SC70	DCK	6	3000	203.0	203.0	35.0
LMV715IDBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
LMV715IDCKR	SC70	DCK	6	3000	203.0	203.0	35.0

# DBV (R-PDSO-G5)

#### PLASTIC SMALL-OUTLINE PACKAGE

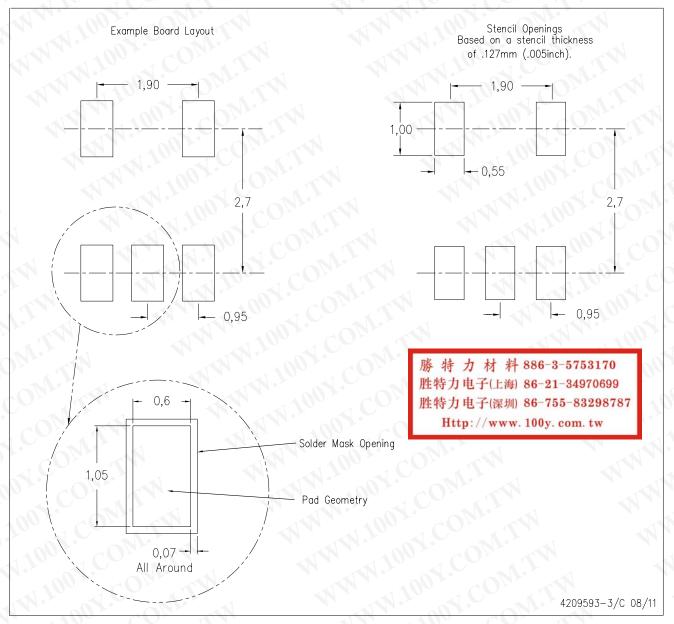


- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA



# DBV (R-PDSO-G5)

# PLASTIC SMALL OUTLINE

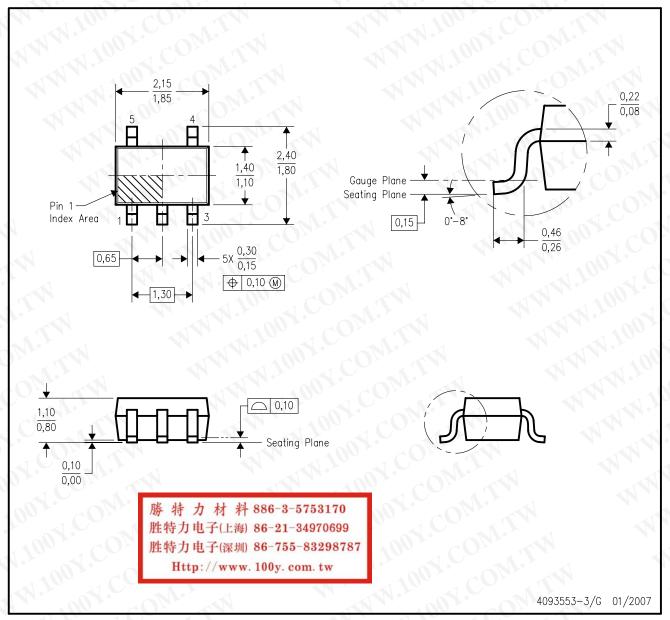


- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



# DCK (R-PDSO-G5)

# PLASTIC SMALL-OUTLINE PACKAGE



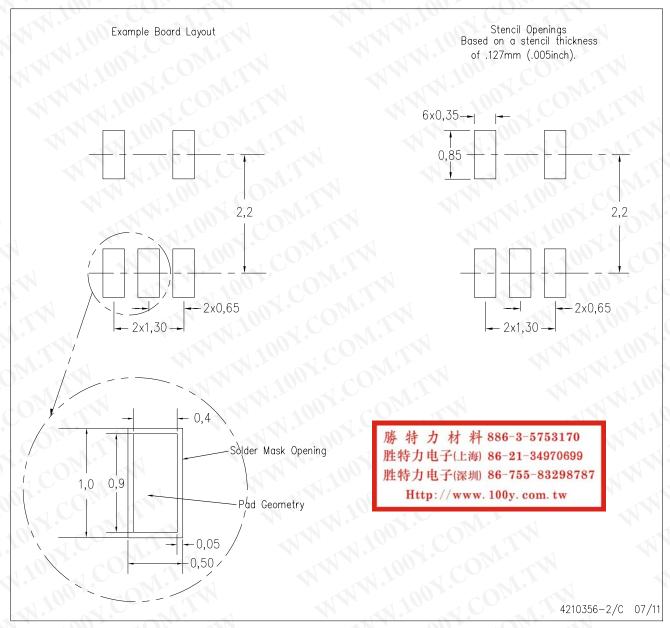
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.



### DCK (R-PDSO-G5)

#### PLASTIC SMALL OUTLINE

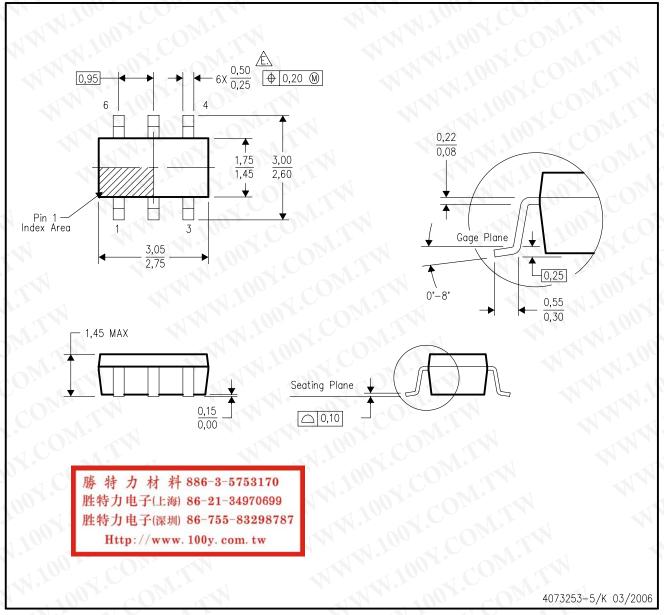


- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



# DBV (R-PDSO-G6)

#### PLASTIC SMALL-OUTLINE PACKAGE

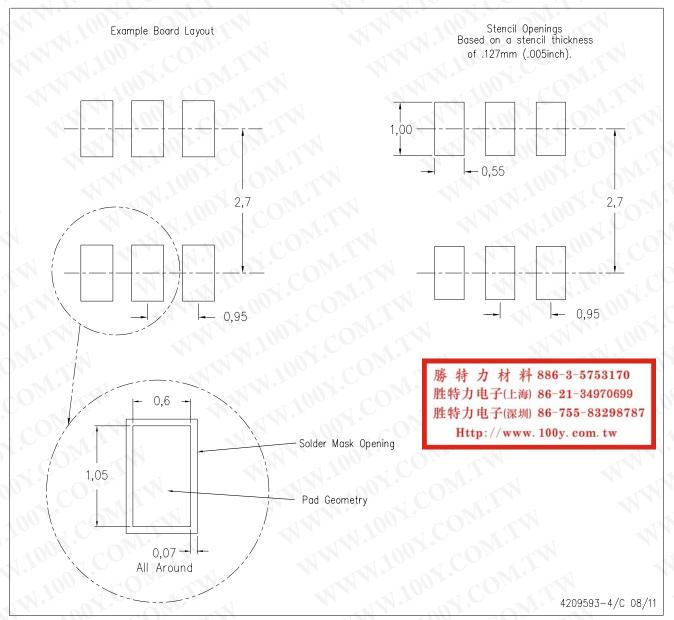


- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- Falls within JEDEC MO-178 Variation AB, except minimum lead width.



# DBV (R-PDSO-G6)

# PLASTIC SMALL OUTLINE

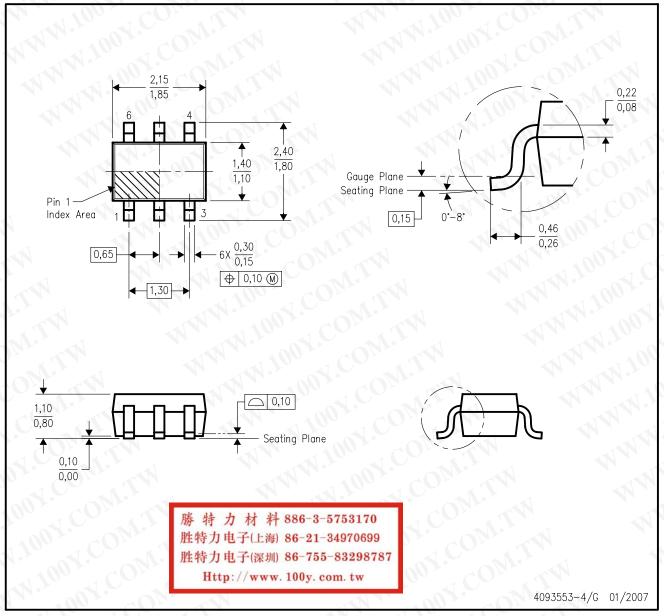


- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



# DCK (R-PDSO-G6)

# PLASTIC SMALL-OUTLINE PACKAGE



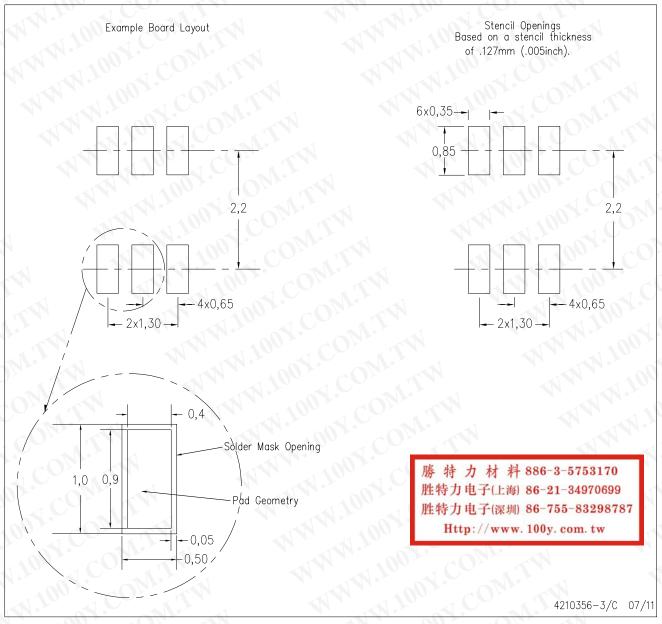
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AB.



## DCK (R-PDSO-G6)

#### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



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