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胜特力电子(上海) 86-21-34970699
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

LPV7215Q Micropower, CMOS Input, RRIO, 1.8V, Push-Pull Output Comparator

Check for Samples: LPV7215

FEATURES

- **(For V^+ = 1.8V, Typical Unless Otherwise Noted)**
- **Ultra Low Power Consumption 580 nA**
- **Wide Supply Voltage Range 1.8V to 5.5V**
- **Propagation Delay 4.5 µs**
- **Push-Pull Output Current Drive @ 5V 19 mA**
- **Temperature Range −40°C to 125°C**
- **Rail-to-Rail Input**
- **Tiny 5-Pin SOT23 and SC70 Packages**

APPLICATIONS

- **RC Timers**
- **Window Detectors**
- **IR Receiver**
- **Multivibrators**
- **Alarm and Monitoring Circuits**

DESCRIPTION

The LPV7215Q is an ultra low-power comparator with a typical power supply current of 580 nA. It has the best-in-class power supply current versus propagation delay performance available among TI's low-power comparators. The propagation delay is as low as 4.5 microseconds with 100 mV overdrive at 1.8V supply.

Designed to operate over a wide range of supply voltages, from 1.8V to 5.5V, with ensured operation at 1.8V, 2.7V and 5.0V, the LPV7215Q is ideal for use in a variety of battery-powered applications. With rail-to-rail common mode voltage range, the LPV7215Q is well suited for single-supply operation.

Featuring a push-pull output stage, the LPV7215Q allows for operation with absolute minimum power consumption when driving any capacitive or resistive load.

Available in a choice of space-saving packages, the LPV7215Q is ideal for use in handheld electronics and mobile phone applications. The LPV7215Q is manufactured with TI's advanced VIP50 process.

TYPICAL APPLICATION

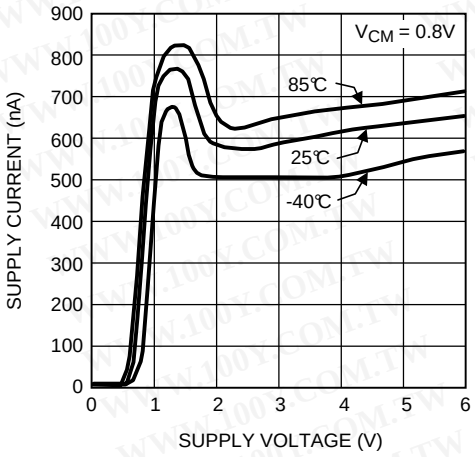

Figure 1. Supply Current vs. Supply Voltage

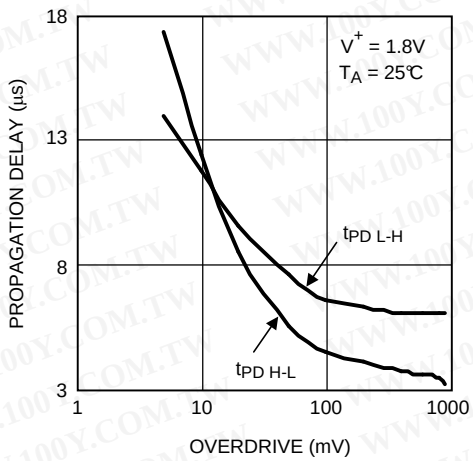

Figure 2. Propagation Delay vs. Overdrive

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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ABSOLUTE MAXIMUM RATINGS (1)(2)

ESD Tolerance (3)	Human Body Model	2000V
	Machine Model	200V
V_{IN} Differential		±2.5V
Supply Voltage (V^+ - V^-)		6V
Voltage at Input/Output pins		V^+ +0.3V, V^- −0.3V
Storage Temperature Range		−65°C to +150°C
Junction Temperature (4)		+150°C
Soldering Information	Infrared or Convection (20 sec)	235°C
	Wave Soldering Lead Temp. (10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

OPERATING RATINGS (1)

Temperature Range (2)		−40°C to 125°C
Supply Voltage (V^+ – V^-)		1.8V to 5.5V
Package Thermal Resistance (θ_{JA} (2))	5-Pin SC70	456°C/W
	5-Pin SOT-23	234°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

1.8V ELECTRICAL CHARACTERISTICS (1)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 1.8V, V^- = 0V, and V_{CM} = V^+/2, V_O= V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
I_S	Supply Current	V_{CM} = 0.3V		580	750 **1050**	nA
		V_{CM} = 1.5V		790	980 **1300**	
V_{OS}	Input Offset Voltage	V_{CM} = 0V		±0.3	±6 **±8**	mV
		V_{CM} = 1.8V		±0.4	±5 **±7**	
TCV_{OS}	Input Offset Average Drift	See (4)		±1		µV/C
I_B	Input Bias Current (5)	V_{CM} = 1.6V		−40		fA
I_{OS}	Input Offset Current			10		fA

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.

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1.8V ELECTRICAL CHARACTERISTICS [1] (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 1.8V, V^- = 0V, and V_{CM} = V^+/2, V_O= V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min [2]	Typ [3]	Max [2]	Units
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 0.7V	66 **62**	88		dB
		V_{CM} Stepped from 1.2V to 1.8V	68 **62**	87		
		V_{CM} Stepped from 0V to 1.8V	44 **43**	77		
PSRR	Power Supply Rejection Ratio	V^+ = 1.8V to 5.5V, V_{CM} = 0V	66 **63**	82		dB
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 40 dB	**−0.1**		**1.9**	V
A_V	Voltage Gain			120		dB
V_O	Output Swing High	I_O = 500 µA	1.63 **1.58**	1.69		V
		I_O = 1 mA	1.46 **1.37**	1.60		
	Output Swing Low	I_O = −500 µA		88	180 **230**	mV
		I_O = −1 mA		180	310 **400**	
I_{OUT}	Output Current	Source V_O = V^+/2	1.75 **1.3**	2.26		mA
		Sink V_O = V^+/2	2.35 **1.45**	3.1		
	Propagation Delay (High to Low)	Overdrive = 10 mV		13		µs
		Overdrive = 100 mV		4.5	6.5 **9**	
	Propagation Delay (Low to High)	Overdrive = 10 mV		12.5		µs
		Overdrive = 100 mV		6.6	9 **12**	
t_{rise}	Rise Time	Overdrive = 10 mV C_L = 30 pF, R_L = 1 MΩ		80		ns
		Overdrive = 100 mV C_L = 30 pF, R_L = 1 MΩ		75		
t_{fall}	Fall Time	Overdrive = 10 mV C_L = 30 pF, R_L = 1 MΩ		70		ns
		Overdrive = 100 mV C_L = 30 pF, R_L = 1 MΩ		65		

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2.7V ELECTRICAL CHARACTERISTICS (1)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 2.7V, V^- = 0V, and V_{CM} = V^+/2, V_O= V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
I_S	Supply Current	V_{CM} = 0.3V		605	780 **1100**	nA
		V_{CM} = 2.4V		815	1010 **1350**	
V_{OS}	Input Offset Voltage	V_{CM} = 0V		±0.3	±6 **±8**	mV
		V_{CM} = 2.7V		±0.3	±5 **±7**	
TCV_{OS}	Input Offset Average Drift	See (4)		±1		µV/C
I_B	Input Bias Current (5)	V_{CM} = 1.8V		−40		fA
I_{OS}	Input Offset Current			20		fA
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 1.6V	72 **66**	90		dB
		V_{CM} Stepped from 2.1V to 2.7V	71 **63**	94		
		V_{CM} Stepped from 0V to 2.7V	47 **46**	80		
PSRR	Power Supply Rejection Ratio	V^+ = 1.8V to 5.5V, V_{CM} = 0V	66 **63**	82		dB
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 40 dB	**−0.1**		**2.8**	V
A_V	Voltage Gain			120		dB
V_O	Output Swing High	I_O = 500 µA	2.57 **2.53**	2.62		V
		I_O = 1 mA	2.47 **2.40**	2.53		
	Output Swing Low	I_O = −500 µA		60	130 **190**	mV
		I_O = −1 mA		120	250 **330**	
I_{OUT}	Output Current	Source V_O = V^+/2	4.5 **3.4**	5.7		mA
		Sink V_O = V^+/2	5.6 **3.2**	7.5		
	Propagation Delay (High to Low)	Overdrive = 10 mV		14.5		µs
		Overdrive = 100 mV		5.8	8.5 **10.5**	
	Propagation Delay (Low to High)	Overdrive = 10 mV		15		
		Overdrive = 100 mV		7.5	10 **12.5**	
t_{rise}	Rise Time	Overdrive = 10 mV C_L = 30 pF, R_L = 1 MΩ		90		ns
		Overdrive = 100 mV C_L = 30 pF, R_L = 1 MΩ		85		

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.

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2.7V ELECTRICAL CHARACTERISTICS (1) (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 2.7V, V^- = 0V, and V_{CM} = V^+/2, V_O= V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
t_{fall}	Fall Time	Overdrive = 10 mV C_L = 30 pF, R_L = 1 MΩ		85		ns
		Overdrive = 100 mV C_L = 30 pF, R_L = 1 MΩ		75		

5V ELECTRICAL CHARACTERISTICS (1)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 5V, V^- = 0V, and V_{CM} = V^+/2, V_O= V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
I_S	Supply Current	V_{CM} = 0.3V		612	790 **1150**	nA
		V_{CM} = 4.7V		825	1030 **1400**	
V_{OS}	Input Offset Voltage	V_{CM} = 0V		±0.3	±6 **±8**	mV
		V_{CM} = 5V			±5 **±7**	
TCV_{OS}	Input Offset Average Drift	See (4)		±1		µV/C
I_B	Input Bias Current (5)	V_{CM} = 4.5V		−400		fA
I_{OS}	Input Offset Current			20		fA
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 3.9V	72 **66**	98		dB
		V_{CM} Stepped from 4.4V to 5V	73 **67**	92		
		V_{CM} Stepped from 0V to 5V	53 **49**	82		
PSRR	Power Supply Rejection Ratio	V^+ = 1.8V to 5.5V, V_{CM} = 0V	66 **63**	82		dB
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 40 dB	**−0.1**		**5.1**	V
A_V	Voltage Gain			120		dB
V_O	Output Swing High	I_O = 500 µA	4.9 **4.86**	4.94		V
		I_O = 1 mA	4.82 **4.77**	4.89		
	Output Swing Low	I_O = −500 µA		43	90 **130**	mV
		I_O = −1 mA		88	170 **230**	
I_{OUT}	Output Current	Source V_O = V^+/2	13.0 **7.5**	17		mA
		Sink V_O = V^+/2	14.5 **8.5**	19		

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.

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5V ELECTRICAL CHARACTERISTICS [1] (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 5V, V^- = 0V, and V_{CM} = V^+/2, V_O= V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min [2]	Typ [3]	Max [2]	Units
	Propagation Delay (High to Low)	Overdrive = 10 mV		18		µs
		Overdrive = 100 mV		7.7	13.5 **16**	
	Propagation Delay (Low to High)	Overdrive = 10 mV		30		µs
		Overdrive = 100 mV		12	15 **20**	
t_{rise}	Rise Time	Overdrive = 10 mV C_L = 30 pF, R_L = 1 MΩ		100		ns
		Overdrive = 100 mV C_L = 30 pF, R_L = 1 MΩ		100		
t_{fall}	Fall Time	Overdrive = 10 mV C_L = 30 pF, R_L = 1 MΩ		115		ns
		Overdrive = 100 mV C_L = 30 pF, R_L = 1 MΩ		95		

CONNECTION DIAGRAM

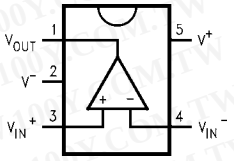
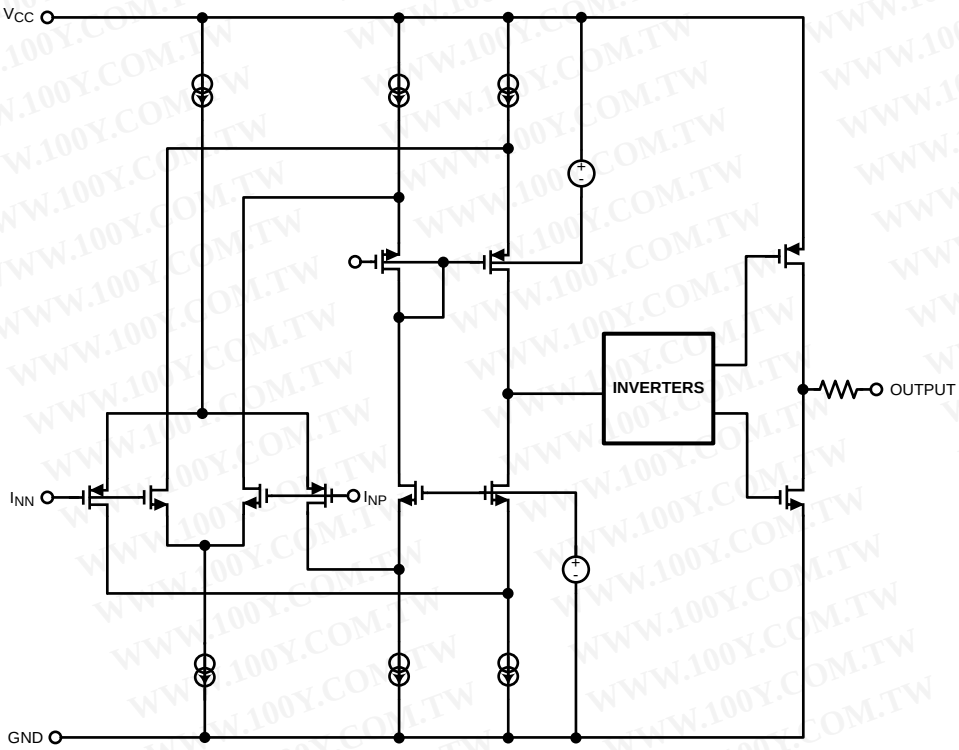


Figure 3. SC70/SOT-23 (Top View)

Simplified Schematic Diagram



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TYPICAL PERFORMANCE CHARACTERISTICS

At T_J = 25°C unless otherwise specified.

Supply Current vs. Supply Voltage

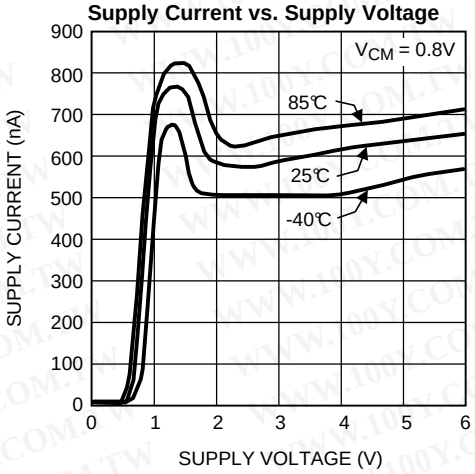

Figure 4.

Supply Current vs. Common Mode Input

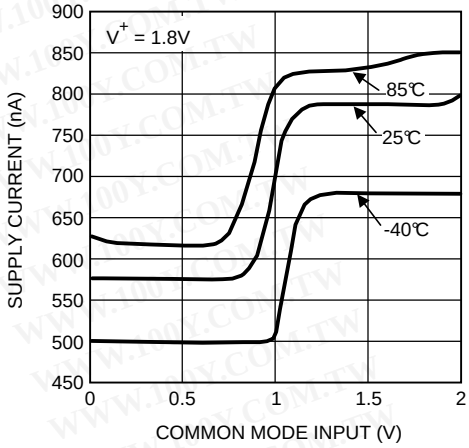

Figure 5.

Supply Current vs. Common Mode Input

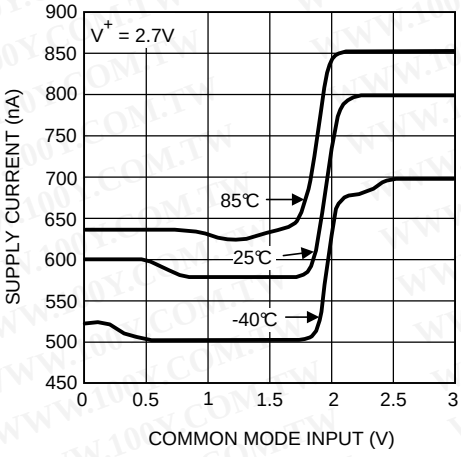

Figure 6.

Supply Current vs. Common Mode Input

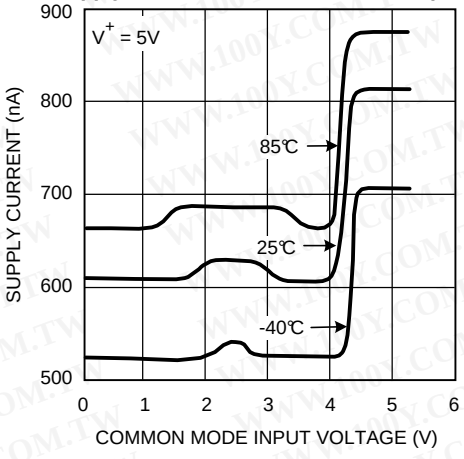

Figure 7.

Short Circuit Sinking Current vs. Supply Voltage

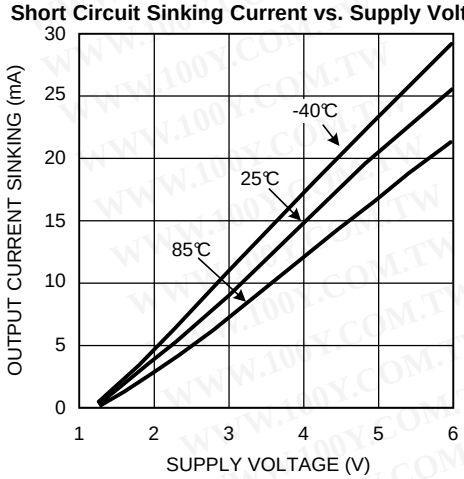

Figure 8.

Short Circuit Sourcing Current vs. Supply Voltage

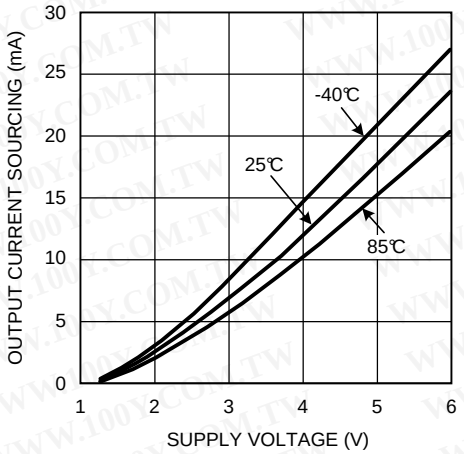

Figure 9.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C unless otherwise specified.

Output Voltage Low vs. Sink Current

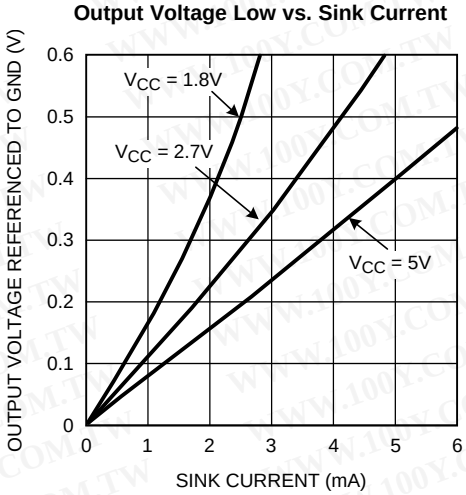

Figure 10.

Output Voltage Low vs. Sink Current

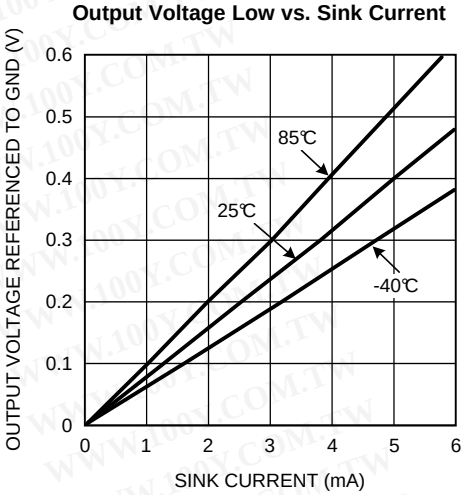

Figure 11.

Output Voltage High vs. Source Current

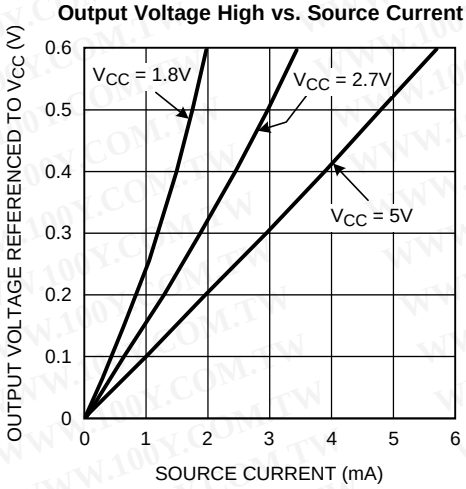

Figure 12.

Output Voltage High vs. Source Current

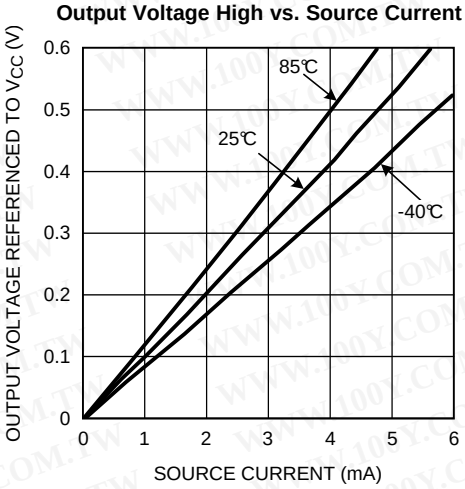

Figure 13.

Propagation Delay vs. Supply Voltage

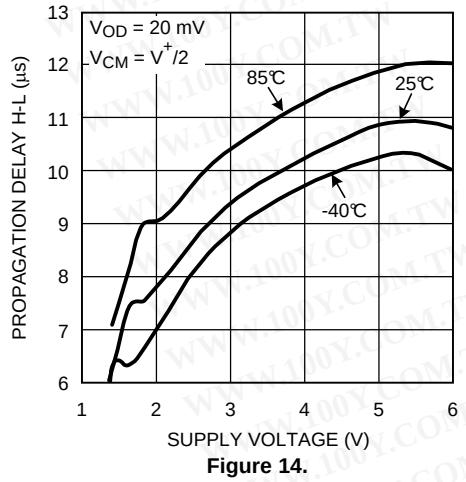

Figure 14.

Propagation Delay vs. Supply Voltage

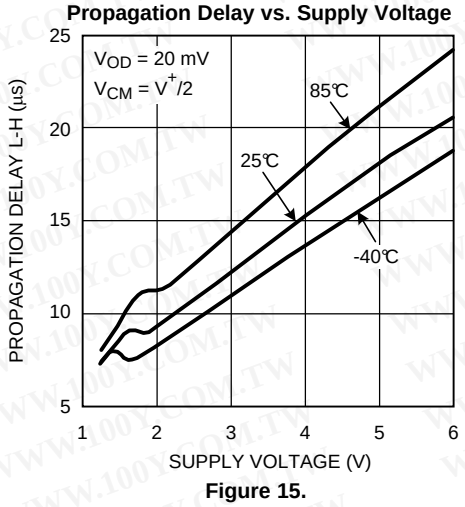

Figure 15.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C unless otherwise specified.

Propagation Delay vs. Overdrive

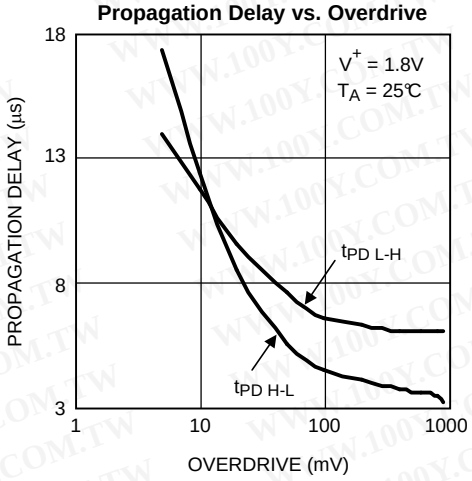

Figure 16.

Propagation Delay vs. Overdrive

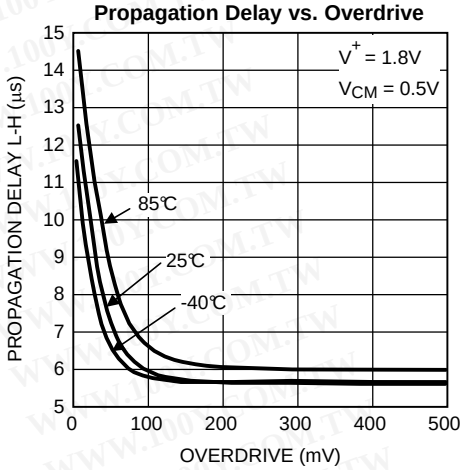

Figure 17.

Propagation Delay vs. Overdrive

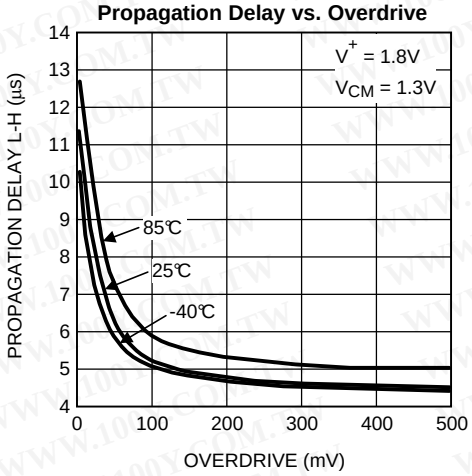

Figure 18.

Propagation Delay vs. Overdrive

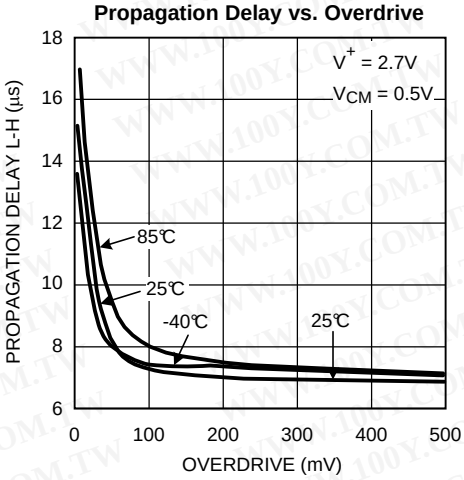

Figure 19.

Propagation Delay vs. Overdrive

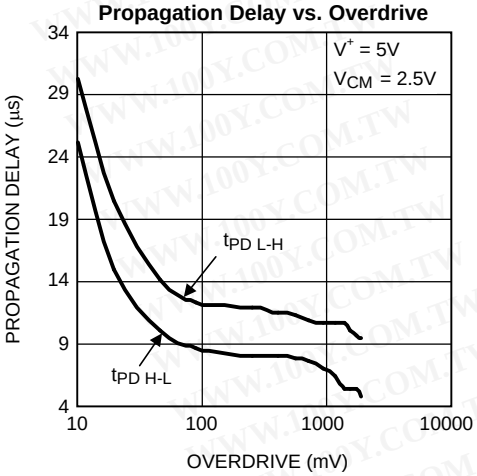

Figure 20.

Propagation Delay vs. Overdrive

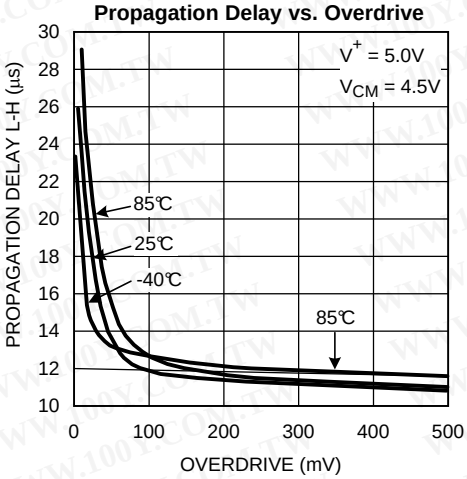

Figure 21.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C unless otherwise specified.

Propagation Delay vs. Overdrive

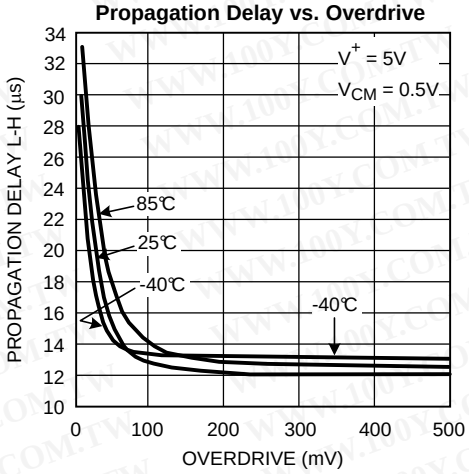

Figure 22.

Propagation Delay vs. Resistive Load

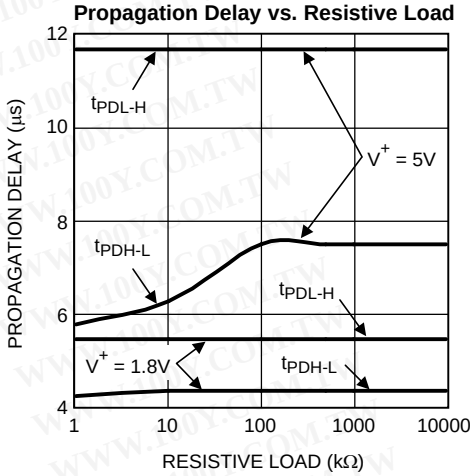

Figure 23.

I_{BIAS} vs. V_{CM}

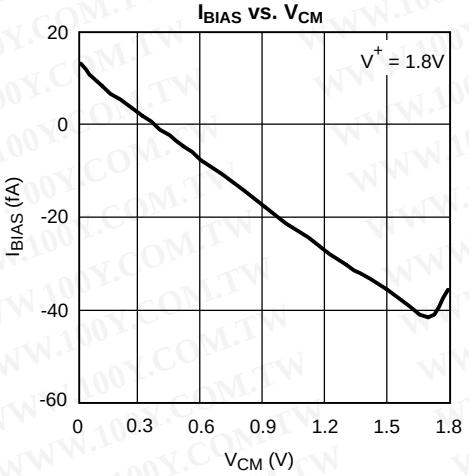

Figure 24.

I_{BIAS} vs. V_{CM}

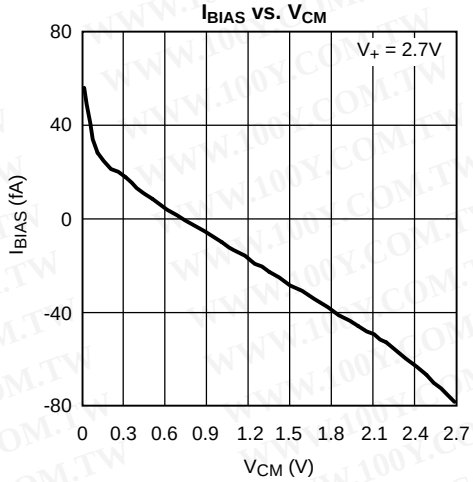

Figure 25.

I_{BIAS} vs. V_{CM}

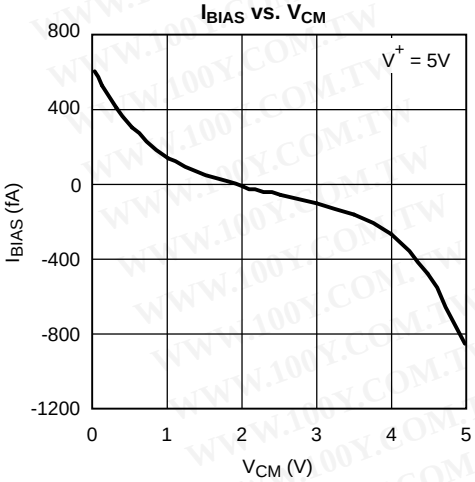

Figure 26.

Propagation Delay vs. Common Mode Input

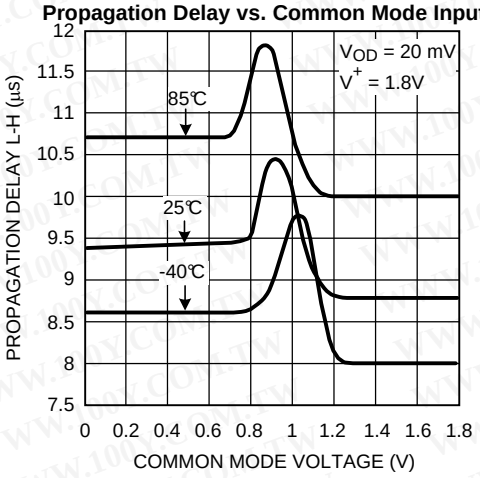

Figure 27.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C unless otherwise specified.

Propagation Delay vs. Common Mode Input

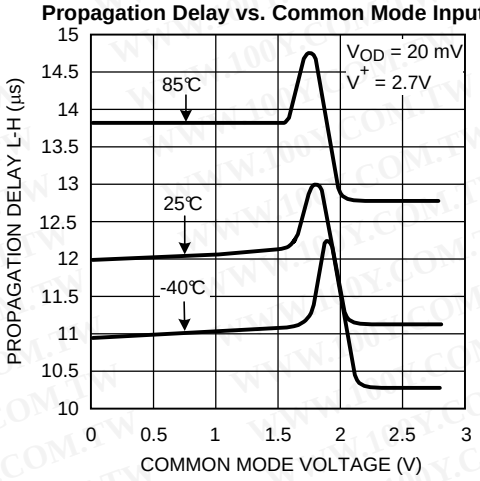

Figure 28.

Propagation Delay vs. Common Mode Input

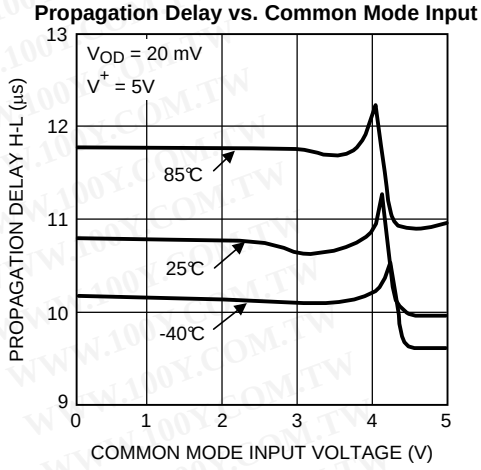

Figure 29.

Propagation Delay vs. Common Mode Input

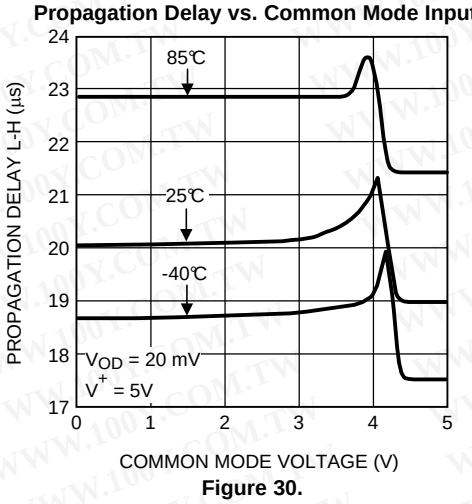

Figure 30.

Offset Voltage vs. Common Mode Input

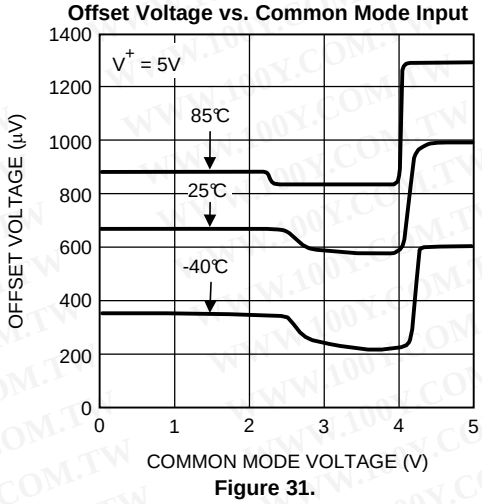

Figure 31.

APPLICATION INFORMATION

Low supply current and fast propagation delay distinguish the LPV7215Q from other low power comparators.

INPUT STAGE

The LPV7215Q has rail-to-rail input common mode voltage range. It can operate at any differential input voltage within this limit as long as the differential voltage is greater than zero. A differential input of zero volts may result in oscillation.

The differential input stage of the comparator is a pair of PMOS and NMOS transistors, therefore, no current flows into the device. The input bias current measured is the leakage current in the MOS transistors and input protection diodes. This low bias current allows the comparator to interface with a variety of circuitry and devices with minimal concern about matching the input resistances.

The input to the comparator is protected from excessive voltage by internal ESD diodes connected to both supply rails. This protects the circuit from both ESD events, as well as signals that significantly exceed the supply voltages. When this occurs the ESD protection diodes will become forward biased and will draw current into these structures, resulting in no input current to the terminals of the comparator. Until this occurs, there is essentially no input current to the diodes. As a result, placing a large resistor in series with an input that may be exposed to large voltages, will limit the input current but have no other noticeable effect.

OUTPUT STAGE

The LPV7215Q has a MOS push-pull rail-to-rail output stage. The push-pull transistor configuration of the output keeps the total system power consumption to a minimum. The only current consumed by the LPV7215Q is the less than 1 µA supply current and the current going directly into the load. No power is wasted through the pull-up resistor when the output is low. The output stage is specifically designed with deadtime between the time when one transistor is turned off and the other is turned on (break-before-make) in order to minimize shoot through currents. The internal logic controls the break-before-make timing of the output transistors. The break-before-make delay varies with temperature and power condition.

OUTPUT CURRENT

Even though the LPV7215Q uses less than 1 µA supply current, the outputs are able to drive very large currents. The LPV7215Q can source up to 17 mA and can sink up to 19 mA, when operated at 5V supply. This large current handling capability allows driving heavy loads directly.

RESPONSE TIME

Depending upon the amount of overdrive, the propagation delay will be typically 6 to 30 µs. The curves showing propagation delay vs. overdrive in the TYPICAL PERFORMANCE CHARACTERISTICS section shows the delay time when the input is preset with 100 mV across the inputs and then is driven the other way by 10 mV to 500 mV.

The output signal can show a step during switching depending on the load. A fast RC time constant due to both small capacitive and resistive loads will show a significant step in the output signal. A slow RC time constant due to either a large resistive or capacitive load will have a clipped corner on the output signal. The step is observed more prominently during a falling transition from high to low.

The plot in Figure 32 shows the output for single 5V supply with a 100 kΩ resistor. The step is at 1.3V.

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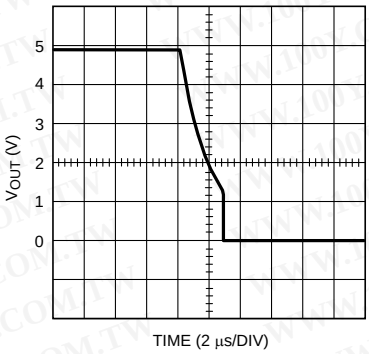

Figure 32. Output Signal without Capacitive Load

The plot in Figure 33 shows the output signal when a 20 pF capacitor is added as a load. The step is at about 2.5V.

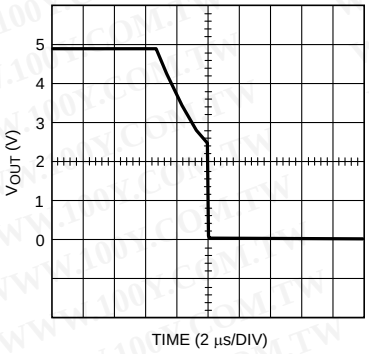

Figure 33. Output Signal with 20 pF Load

CAPACITIVE AND RESISTIVE LOADS

The propagation delay is not affected by capacitive loads at the output of the LPV7215Q. However, resistive loads slightly affect the propagation delay on the falling edge by a reduction of almost 2 µs depending on the load resistance value.

NOISE

Most comparators have rather low gain. This allows the output to spend time between high and low when the input signal changes slowly. The result is that the output may oscillate between high and low when the differential input is near zero. The exceptionally high gain of this comparator, 120 dB, eliminates this problem. Less than 1 µV of change on the input will drive the output from one rail to the other rail. If the input signal is noisy, the output cannot ignore the noise unless some hysteresis is provided by positive feedback. (See section on adding hysteresis.)

LAYOUT/BYPASS CAPACITORS

Proper grounding and the use of a ground plane will help to ensure the specified performance of the LPV7215Q. Minimizing trace lengths, reducing unwanted parasitic capacitance and using surface-mount components will also help.

Comparators are very sensitive to input noise. To minimize supply noise, power supplies should be capacitively decoupled by a 0.01 µF ceramic capacitor in parallel with a 10 µF electrolytic capacitor.

HYSTERESIS

In order to improve propagation delay when low overdrive is needed hysteresis can be added.

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INVERTING COMPARATOR WITH HYSTERESIS

The inverting comparator with hysteresis requires a three resistor network that is referenced to the supply voltage V^+ of the comparator as shown in Figure 34. When V_{IN} at the inverting input is less than V_A, the voltage at the non-inverting node of the comparator ($V_{IN} < V_A$), the output voltage is high (for simplicity assume V_O switches as high as V^+). The three network resistors can be represented as $R_1//R_3$ in series with R_2.

The lower input trip voltage V_{A1} is defined as

$$V_{A1} = V_{CC}R_2 / ((R_1//R_3) + R_2)$$

When V_{IN} is greater than V_A, the output voltage is low or very close to ground. In this case the three network resistors can be presented as $R_2//R_3$ in series with R_1.

The upper trip voltage V_{A2} is defined as

$$V_{A2} = V_{CC} (R_2//R_3) / ((R_1 + (R_2//R_3)$$

The total hysteresis provided by the network is defined as $\Delta V_A = V_{A1} - V_{A2}$

$$\Delta V_A = \frac{+V_{CC}R_1R_2}{R_1R_2 + R_1R_3 + R_2R_3}$$

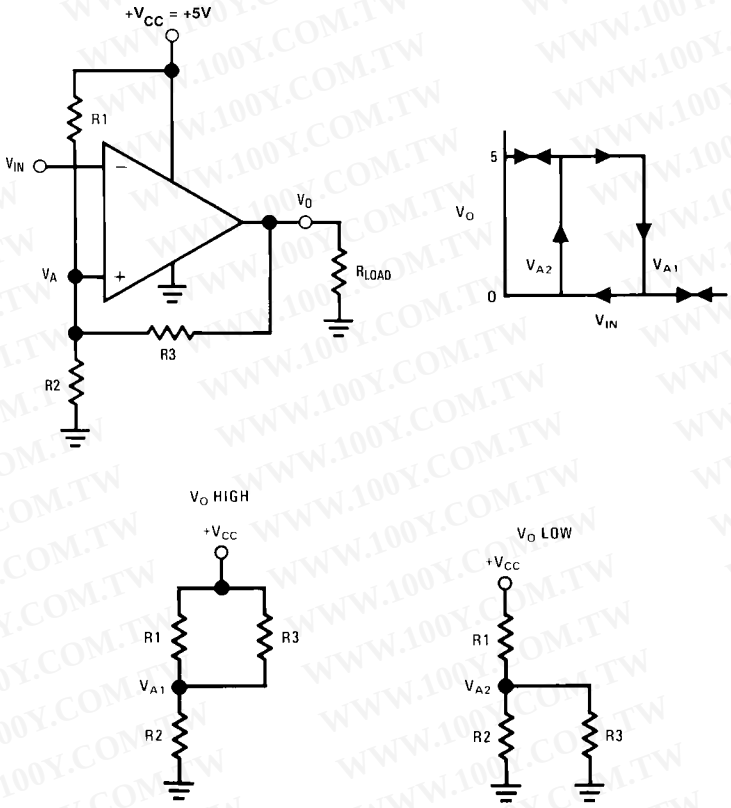

Figure 34. Inverting Comparator with Hysteresis

NON-INVERTING COMPARATOR WITH HYSTERESIS

A non-inverting comparator with hysteresis requires a two resistor network, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise up to V_{IN1} where V_{IN1} is calculated by.

$$V_{IN1} = \frac{V_{REF} (R_1 + R_2)}{R_2}$$

As soon as V_O switches to V_{CC}, V_A will step to a value greater than V_{REF}, which is given by

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$$V_A = V_{IN} + \frac{(V_{CC}-V_{IN1})\,R_1}{R_1 + R_2}$$

To make the comparator switch back to it's low state, V_{IN} must equal V_{REF} before V_A will again equal V_{REF}. V_{IN2} can be calculated by

$$V_{IN2} = \frac{V_{REF}\,(R_1 + R_2) - V_{CC}\,R_1}{R_2}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}.

$$\Delta V_{IN} = V_{CC}R_1/R_2$$

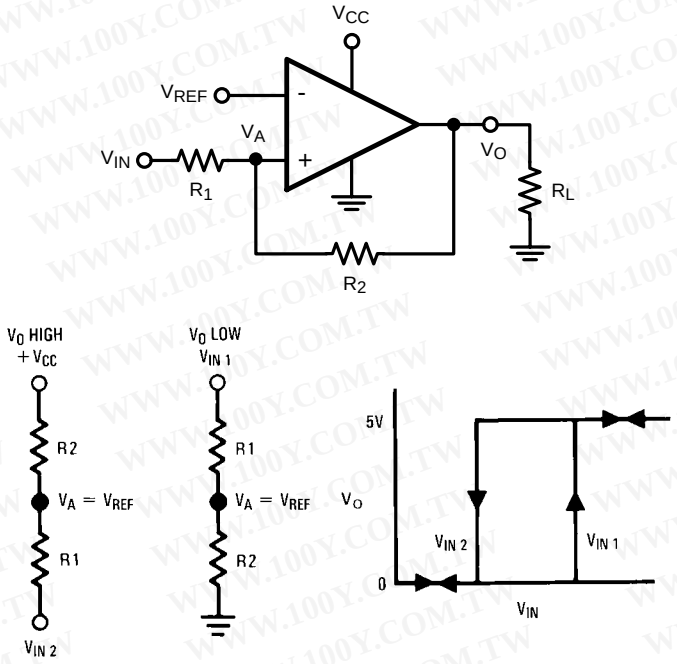

Figure 35. Non-Inverting Comparator with Hysteresis

ZERO CROSSING DETECTOR

In a zero crossing detector circuit, the inverting input is connected to ground and the non-inverting input is connected to a 100 mV_{PP} AC signal. As the signal at the non-inverting input crosses 0V, the comparator's output changes state.

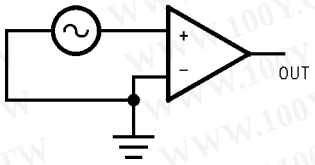

Figure 36. Zero Crossing Detector

To improve switching times and to center the input threshold to ground a small amount of positive feedback is added to the circuit. The voltage divider, R_4 and R_5, establishes a reference voltage, V_1, at the positive input. By making the series resistance, R_1 plus R_2 equal to R_5, the switching condition, $V_1 = V_2$, will be satisfied when $V_{IN} = 0$. The positive feedback resistor, R_6, is made very large with respect to R_5 ($R_6 = 2000\ R_5$). The resultant hysteresis established by this network is very small ($\Delta V_1 < 10$ mV) but it is sufficient to insure rapid output voltage transitions. Diode D_1 is used to insure that the inverting input terminal of the comparator never goes below approximately −100 mV. As the input terminal goes negative, D_1 will forward bias, clamping the node between R_1 and R_2 to approximately −700 mV. This sets up a voltage divider with R_2 and R_3 preventing V_2 from going below ground. The maximum negative input overdrive is limited by the current handling ability of D_1.

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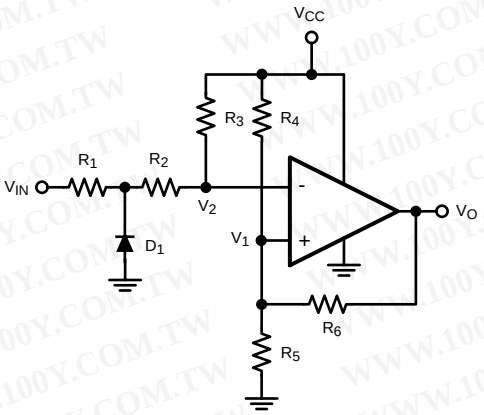

Figure 37. Zero Crossing Detector with Positive Feedback

THRESHOLD DETECTOR

Instead of tying the inverting input to 0V, the inverting input can be tied to a reference voltage. As the input on the non-inverting input passes the V_{REF} threshold, the comparator's output changes state. It is important to use a stable reference voltage to ensure a consistent switching point.

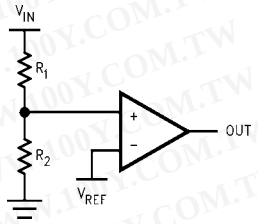

Figure 38. Threshold Detector

CRYSTAL OSCILLATOR

A simple crystal oscillator using the LPV7215Q is shown in Figure 39. Resistors R_1 and R_2 set the bias point at the comparator's non-inverting input. Resistors, R_3 and R_4 and capacitor C_1 set the inverting input node at an appropriate DC average level based on the output. The crystal's path provides resonant positive feedback and stable oscillation occurs. The output duty cycle for this circuit is roughly 50%, but it is affected by resistor tolerances and to a lesser extent by the comparator offset.

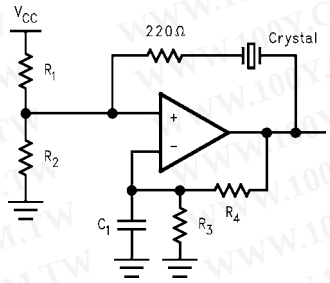

Figure 39. Crystal Oscillator

IR RECEIVER

The LPV7215Q can also be used as an infrared receiver. The infrared photo diode creates a current relative to the amount of infrared light present. The current creates a voltage across R_D. When this voltage level crosses the voltage applied by the voltage divider to the inverting input, the output transitions.

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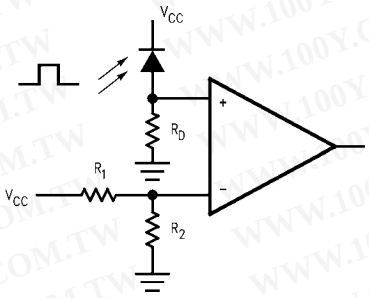

Figure 40. IR Receiver

SQUARE WAVE GENERATOR

A typical application for a comparator is as a square wave oscillator. The circuit in Figure 41 generates a square wave whose period is set by the RC time constant of the capacitor C_1 and resistor R_4. The maximum frequency is limited by the large signal propagation delay of the comparator and by the capacitive loading at the output, which limits the output slew rate.

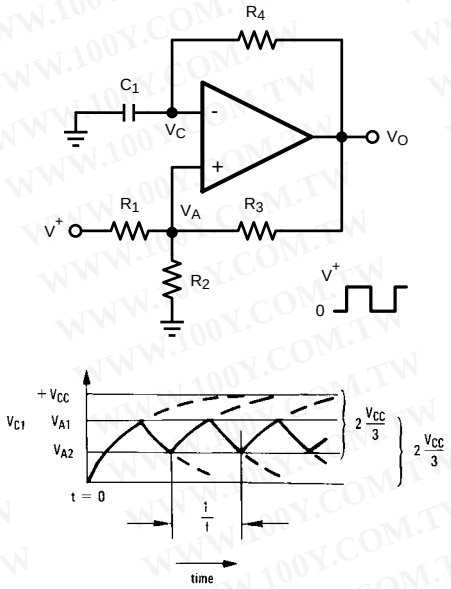

Figure 41. Square Wave Oscillator

Consider the output of Figure 41 to be high to analyze the circuit. That implies that the inverted input (V_C) is lower than the non-inverting input (V_A). This causes the C_1 to be charged through R_4, and the voltage V_C increases until it is equal to the non-inverting input. The value of V_A at this point is

$$V_{A1} = \frac{V_{CC}.R_2}{R_2 + R_1||R_3}$$

If $R_1 = R_2 = R_3$ then $V_{A1} = 2V_{CC}/3$

At this point the comparator switches pulling down the output to the negative rail. The value of V_A at this point is

$$V_{A2} = \frac{V_{CC}\,(R_2||R_3)}{R_1 + (R_2||R_3)}$$

If $R_1 = R_2 = R_3$ then $V_{A2} = V_{CC}/3$

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The capacitor C_1 now discharges through R_4, and the voltage V_C decreases until it is equal to V_{A2}, at which point the comparator switches again, bringing it back to the initial stage. The time period is equal to twice the time it takes to discharge C_1 from $2V_{CC}/3$ to $V_{CC}/3$, which is given by $R_4C_1 \cdot \ln 2$. Hence the formula for the frequency is:

$F = 1/(2 \cdot R_4 \cdot C_1 \cdot \ln 2)$

WINDOW DETECTOR

A window detector monitors the input signal to determine if it falls between two voltage levels.

The comparator outputs A and B are high only when

$V_{REF1} < V_{IN} < V_{REF2}$ "or within the window."

where these are defined as

$$V_{REF1} = R_3/(R_1+R_2+R_3) * V^+$$
$$V_{REF2} = (R_2+R_3)/(R_1+R_2+R_3) * V^+ \quad (1)$$

Others names for window detectors are: threshold detector, level detectors, and amplitude trigger or detector.

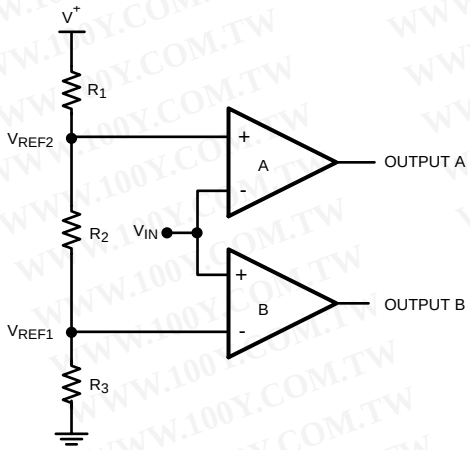

Figure 42. Window Detector

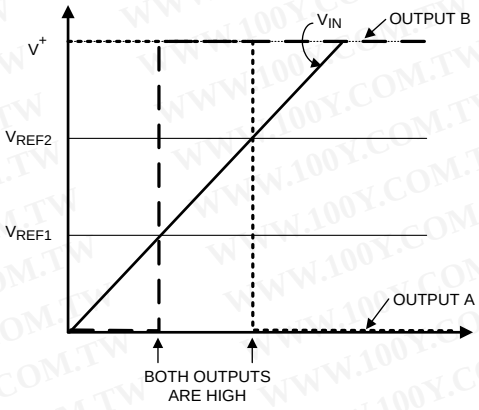

Figure 43. Window Detector Output Signal

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REVISION HISTORY

Changes from Revision H (April 2013) to Revision I	Page
• Changed layout of National Data Sheet to TI format	18

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LPV7215MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C30A	Samples
LPV7215MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C30A	Samples
LPV7215MG	ACTIVE	SC70	DCK	5	1000	TBD	Call TI	Call TI	-40 to 85	C37	Samples
LPV7215MG/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C37	Samples
LPV7215MGX/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C37	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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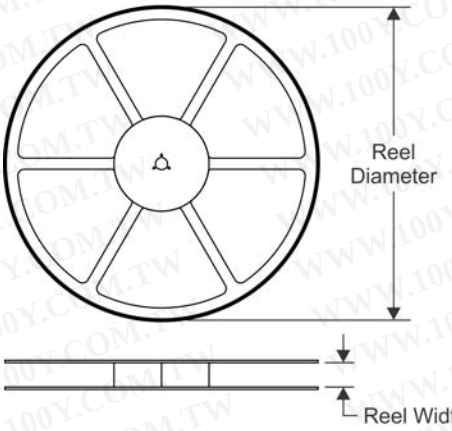
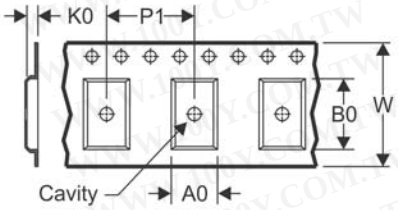
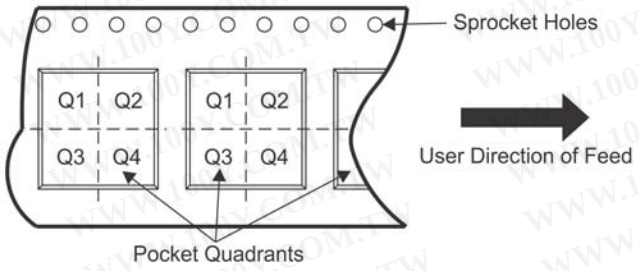


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

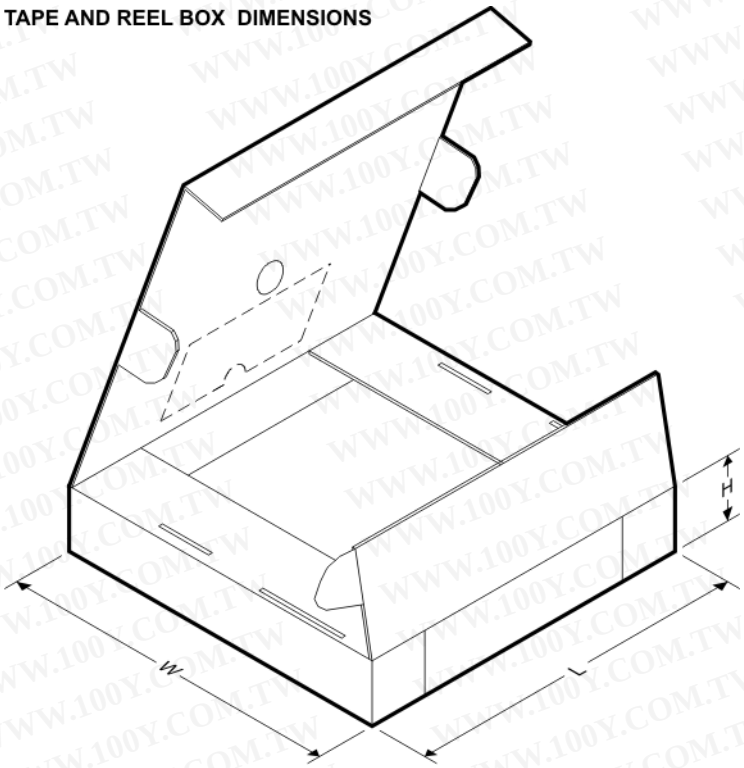
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPV7215MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LPV7215MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LPV7215MG	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV7215MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV7215MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

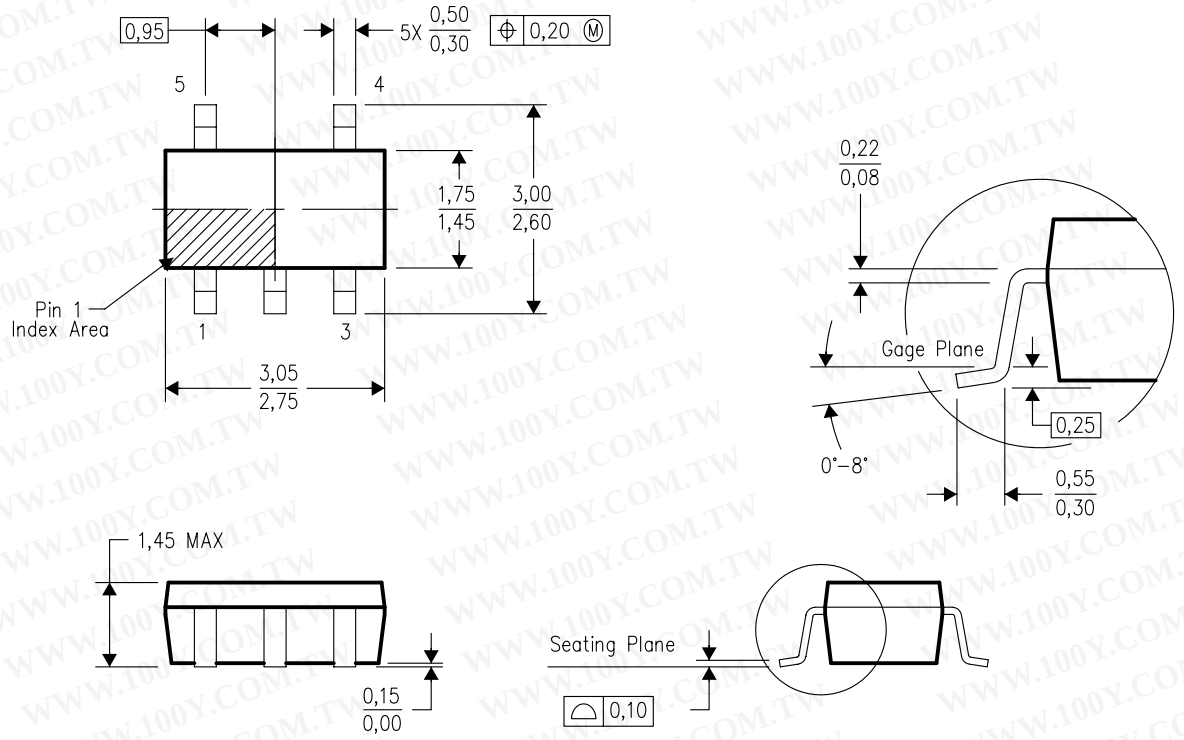
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPV7215MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LPV7215MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LPV7215MG	SC70	DCK	5	1000	210.0	185.0	35.0
LPV7215MG/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LPV7215MGX/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0

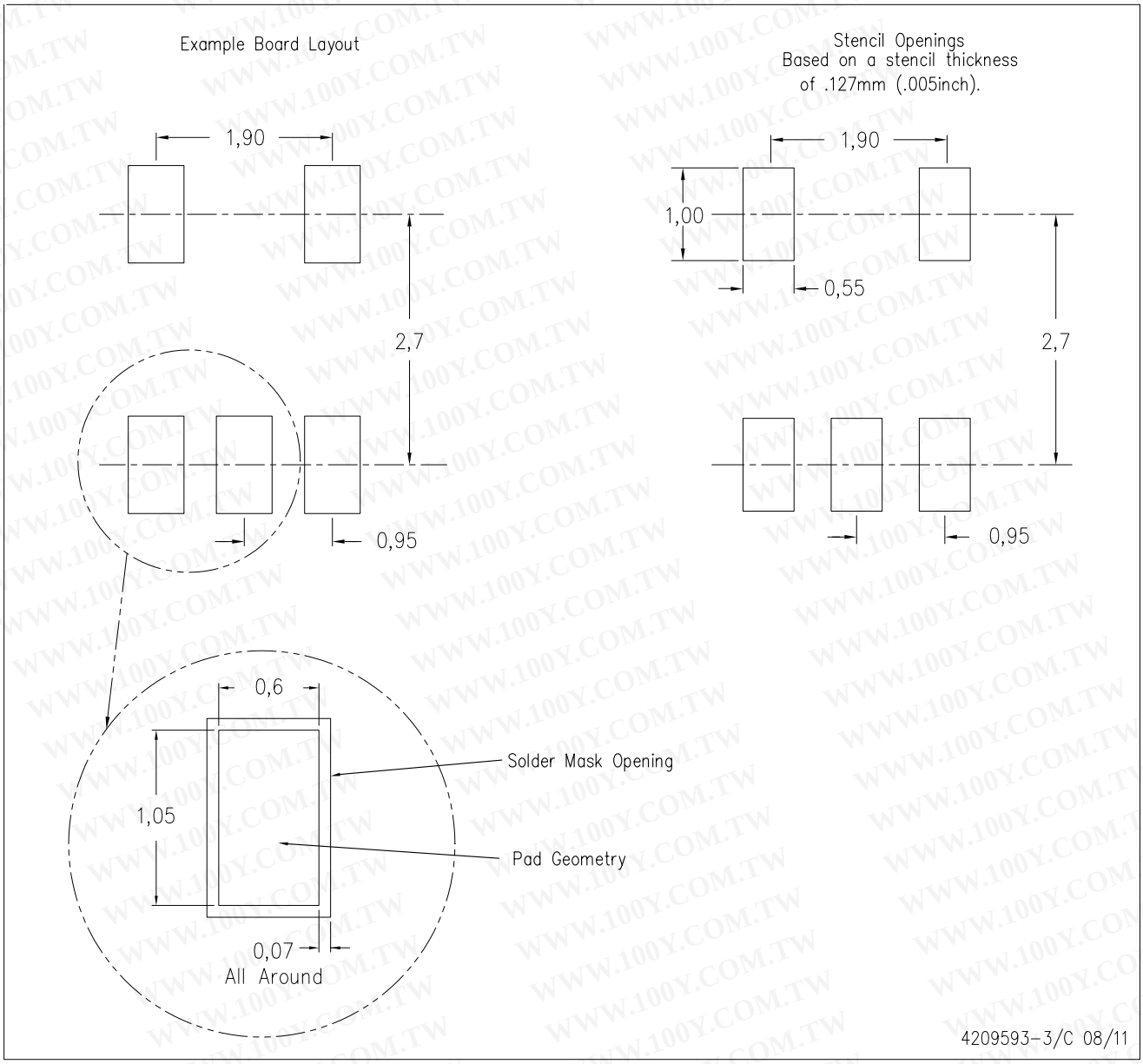
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

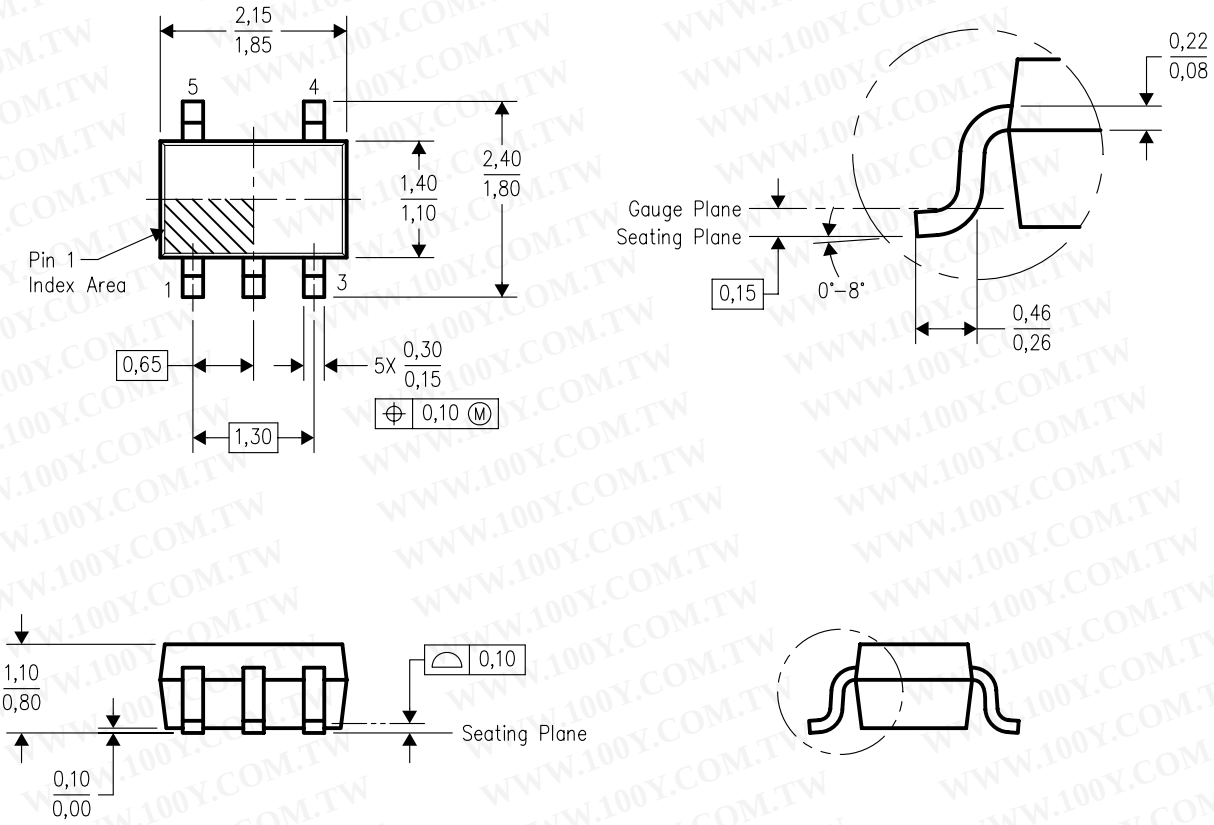
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

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