



**ABSOLUTE MAXIMUM RATINGS**

		VALUE	UNIT
VDD	Positive DC Supply Voltage, VDD	0.0 to +5.50	V
–VDD	Negative DC Supply Voltage, –VDD	–5.5 to 0	V
P <sub>in</sub>	RF Input Power	10	dBm
T <sub>J</sub>	Junction Temperature	200	°C
P <sub>d</sub>	Power Dissipation	1	W
	Digital Input Pins	–0.3 to 5.5	V
θ <sub>JC</sub>	Thermal Resistance Junction to Case <sup>(1)</sup>	9.01	°C/W
T <sub>stg</sub>	Storage Temperature	–40 to 105	°C
T <sub>op</sub>	Operating Temperature	–40 to 85	°C
	Lead Temperature	260	°C

(1) Thermal resistance is junction to ambient assuming thermal pad with 16 thermal vias under package metal base. See Recommended PCB layout.

**DC SPECIFICATIONS**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD	Positive Supply Voltage		4.75	5	5.25	V
IDD	Positive Supply Current (Total)			170	185	mA
VNEG	Negative Supply Voltage		–5.25	–5	–4.75	V
INEG	Negative Supply Current		–6	3	6	mA
I <sub>VDD2</sub>	Supply Current RF 2, pin 2			48		mA
I <sub>LO</sub>	Supply Current, LO, pin 14			50		mA
I <sub>IF</sub>	Supply Current, IF	Pins 17, 18, and 26 combined.		44		mA
I <sub>VDD1</sub>	Supply Current RF1, pin 31			28		
V <sub>IH</sub>	Input High Voltage		2.5	5		V
V <sub>IL</sub>	Input Low Voltage				0.8	V
I <sub>IH</sub>	Input High Current				300	μA
I <sub>IL</sub>	Input Low Current		–50			μA

**ELECTRICAL CHARACTERISTICS<sup>(1)</sup>**

 Unless otherwise stated VDD = 5.0 V, VNEG = –5 V, External Filter loss = 2 dB, T<sub>A</sub> = 25°C

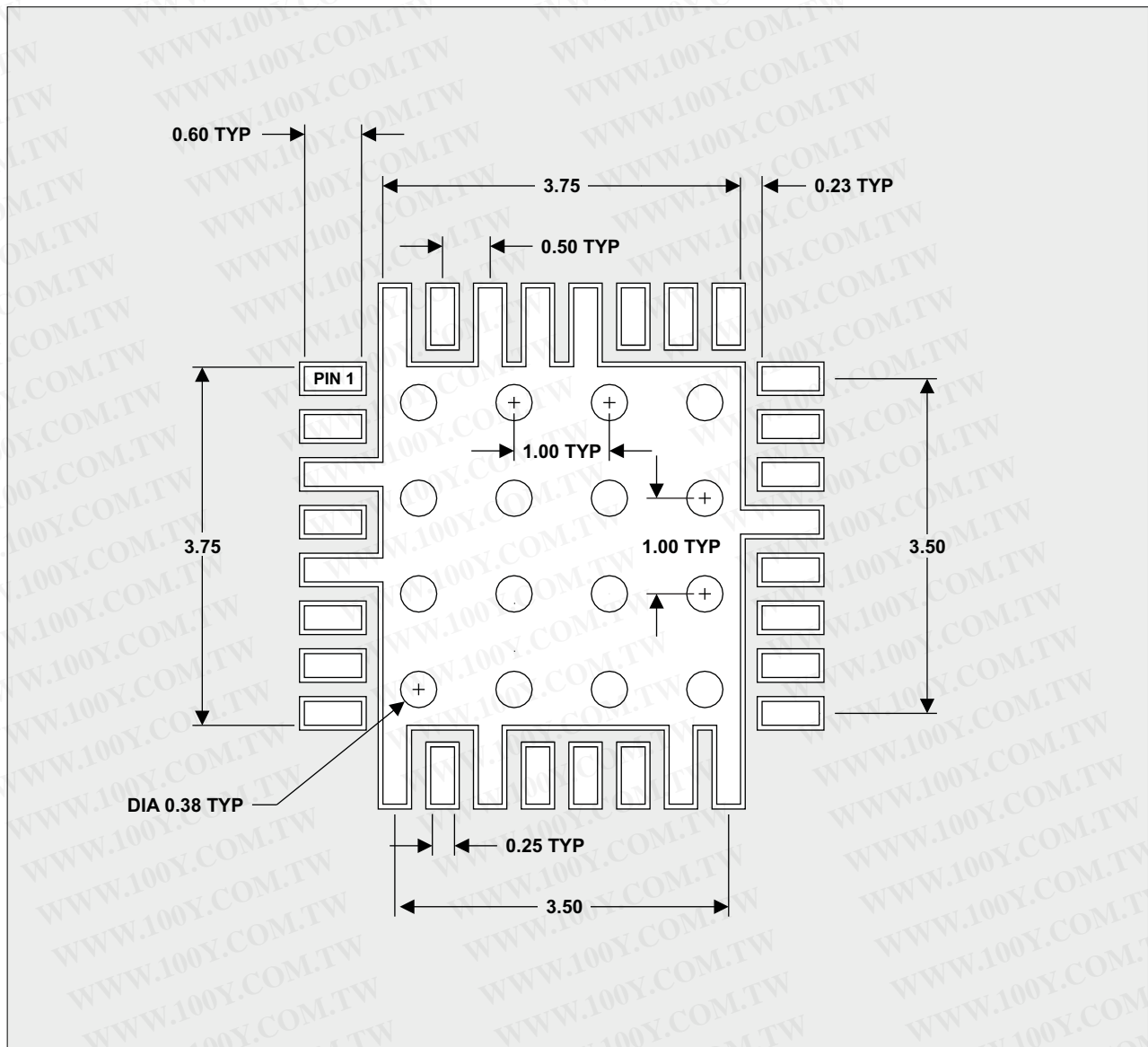
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F <sub>IF</sub>	IF input frequency			325		MHz
F <sub>RF</sub>	RF output frequency		2100		2700	MHz
G	Gain	UCATTN = TTL High, Input IF Impedance is 100 Ω differential	20			dB
	Switched attenuator range	Valid at 2.5 GHz	15	16	17	dB
G <sub>NB</sub>	Gain flatness / 6 MHz				0.2	dB
OP-1dB	Output power at 1 dB compression, high gain	UCATTN = TTL High		14		dBm
OIP3	Output third order intercept point, high gain	UCATTN = TTL High		24		dBm
	Gain: IF to MXRO	UCATTN = TTL High		1		dB
	Gain: RFI to RFO	UCATTN = TTL High		19		dB
Z <sub>RF</sub>	RF output impedance	Differential		50		Ω
RL <sub>RF</sub>	RF output: return loss	Z = 50 Ω, P <sub>LO</sub> = 3 dBm, F <sub>RF</sub> = 2100-2700 MHz		–10		dB
Z <sub>LO</sub>	LO input impedance	Differential		100		Ω
P <sub>LO</sub>	LO input power	Referenced to 100 Ω differential	–3	0	3	dB
RL <sub>LO</sub>	LO input return loss	Referenced to 100 Ω differential, LO input = 3 dBm		–10		dB
Z <sub>IF</sub>	IF input impedance	Differential		100		Ω
RL <sub>IF</sub>	IF1 input return loss	Referenced to 100 Ω differential		–10		dB
	LO to RFO: leakage <sup>(1)</sup>	LO input = 0 dBm		–20		dBm

(1) Performance is sensitive to impedance termination and board layout.

### TERMINAL FUNCTIONS

TERMINAL		I/O	TYPE	DESCRIPTION
NO.	NAME			
1	IADJ			Not connected for normal operation. Amplifier Bias Adjustment. Do not ground this pin or connect to any other pin.
2	VDD2	I	Power	RF amplifier bias +5 V
3, 5, 9, 11, 15, 16, 21, 28–30, 32	GND			Ground
4	UCATTN	I	Digital	Logic high is high gain, Logic low reduces gain by 16 dB. Normally set high.
6	RFO	O	Analog	RF output from RF amplifier
7	LOADJ1			Not connected for normal operation. LO common gate bias adjustment. Do not ground this pin or connect to any other pin.
8	VNEG	I	Power	Negative bias used for enable circuitry -5 V. This pin can be grounded if the user does not use the UCEN pin to turnoff the amplifier. If the VNEG is grounded the UCEN pin should be tied high.
10	LOADJ2			Not connected for normal operation. LO amplifier bias adjustment. Do not ground this pin or connect to any other pin.
12	LOP	I	Analog	LO input, Positive, Internally ac coupled
13	LON	I	Analog	LO input, Negative, Internally ac coupled.
14	VDDLO	I	Power	Positive power for LO amplifier, +5 V.
17	VDDIFN	I	Analog	VDD supply for IF amplifier, negative, +5 V
18	VDDIFP	I	Analog	VDD supply for IF amplifier, positive, +5 V
19	IFIP	I	Analog	IF input, positive, dc coupled, Typical dc voltage is 1.2 V.
20	IFIN	I	Analog	IF input, negative, dc coupled Typical dc voltage is 1.2 V.
22	MXRO	O	Analog	Output of mixer (after balun) 50 $\Omega$ impedance with high impedance DC ground.
23	UCEN		Digital	Set HIGH to enable IF amplifier and RF amplifiers
24	MXRADJ	I	Analog	Normally grounded. Provide 0 $\Omega$ jumper to ground.
25	IFADJ	I		Not connected for normal operation. IF amplifier bias adjustment. Do not ground this pin or connect to any other pin.
26	VDDIF	I	Power	Positive supply for IF bias circuitry +5 V
27	RFI	I	Analog	Input to RF amplifier, 50 $\Omega$ impedance, Internally AC coupled
31	VDDI	I	Power	RF amplifier bias +5 V
Back	GND			Back of package has metal base that must be grounded for thermal and RF performance.

**RECOMMENDED PCB LAYOUT**



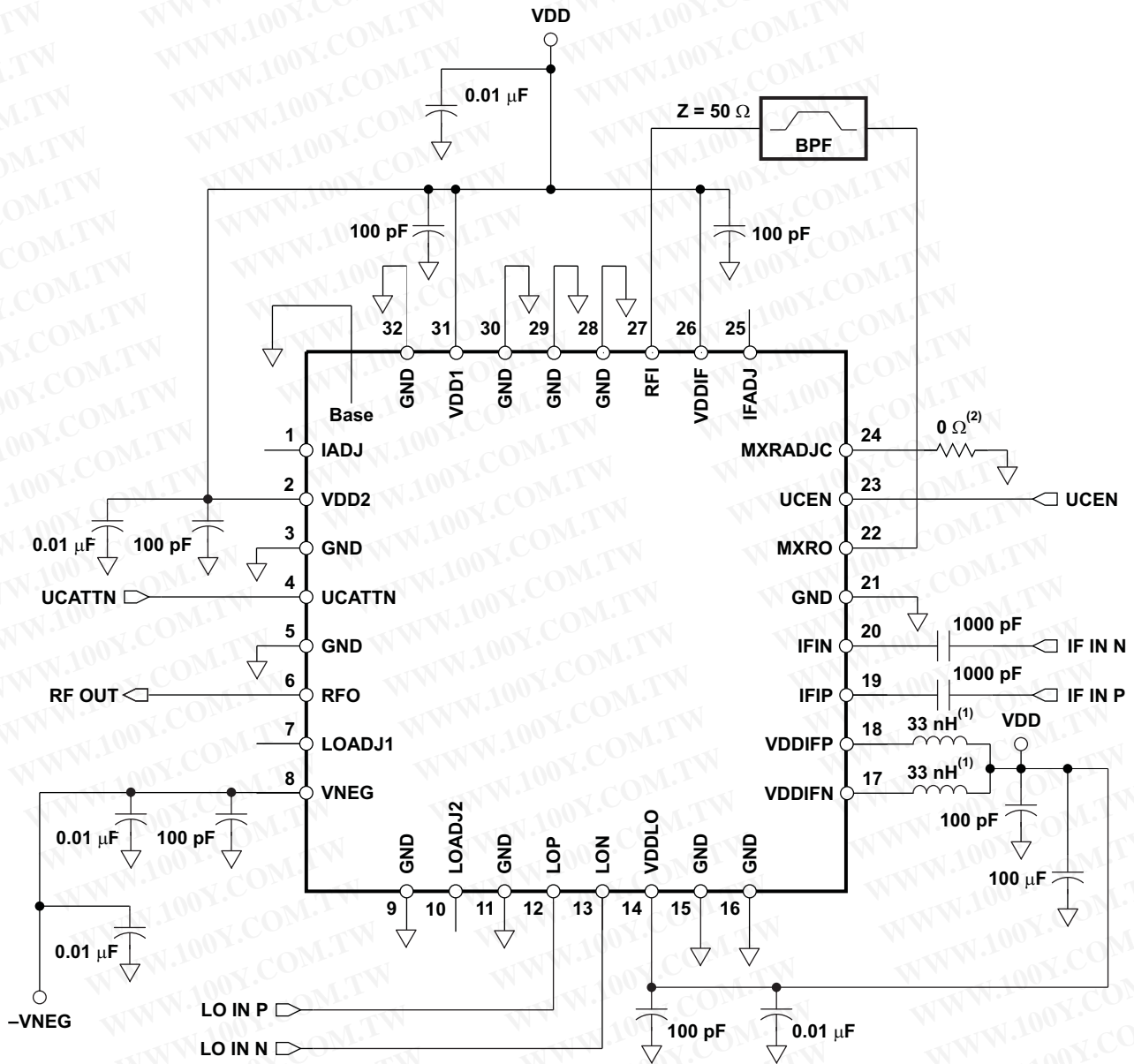

**Solder Mask. No Solder Mask Under Chip, On Lead Pads or On Ground Connections.**

**Notes:** 9 Via Holes, Each 0.38 mm.  
**DIMENSIONS in mm**

M0022-03

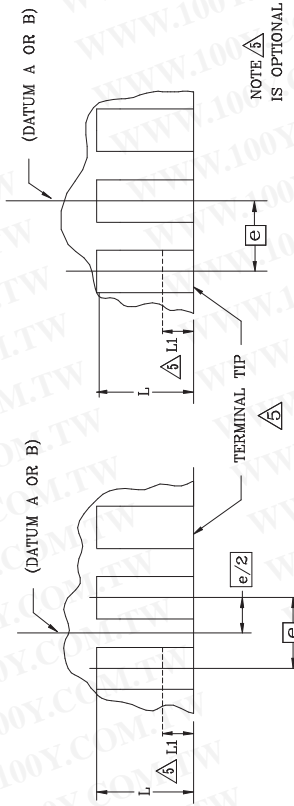
- A. Four layer Board, Starting material: two: 10 mil core FR4 with 1 oz copper, both sides, pressed with 8 mil thick prepreg. Via plating ½ oz copper plate, final plate White immersion tin. Final thickness: 0.033" to 0.037" thick.

APPLICATION SCHEMATIC



S0196-01

APPLICATION INFORMATION



ODD TERMINAL/SIDE

DETAIL B

EVEN TERMINAL/SIDE

PACKAGE REF.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
b	0.225	0.250	0.275
D	4.90	5.00	5.10
D2	3.650	3.800	3.950
E	4.90	5.00	5.10
E2	3.650	3.800	3.950
e	0.50 BSC.		
L	0.35	0.40	0.45
N	32		
ND	8		
NE	8		

SYMBOL	COMMON DIMENSIONS		NOM.	MAX.
	MIN.	MAX.		
A1	0	0.02	0.05	
A3	0.25 REF.			
k	0.20	-		
TOLERANCES OF FORM AND POSITION				
aaa	0.15			
bbb	0.10			
ccc	0.10			

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
  2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
  3. N IS THE TOTAL NUMBER OF TERMINALS
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.

- △ DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 IS THE TERMINAL PULL BACK FROM PACKAGE EDGE, UP TO 0.1mm IS ACCEPTABLE. L1 IS OPTIONAL.
- △ ND AND NE REFER TO THE NUMBER OF TERMINAL ON EACH D AND E SIDE RESPECTIVELY.

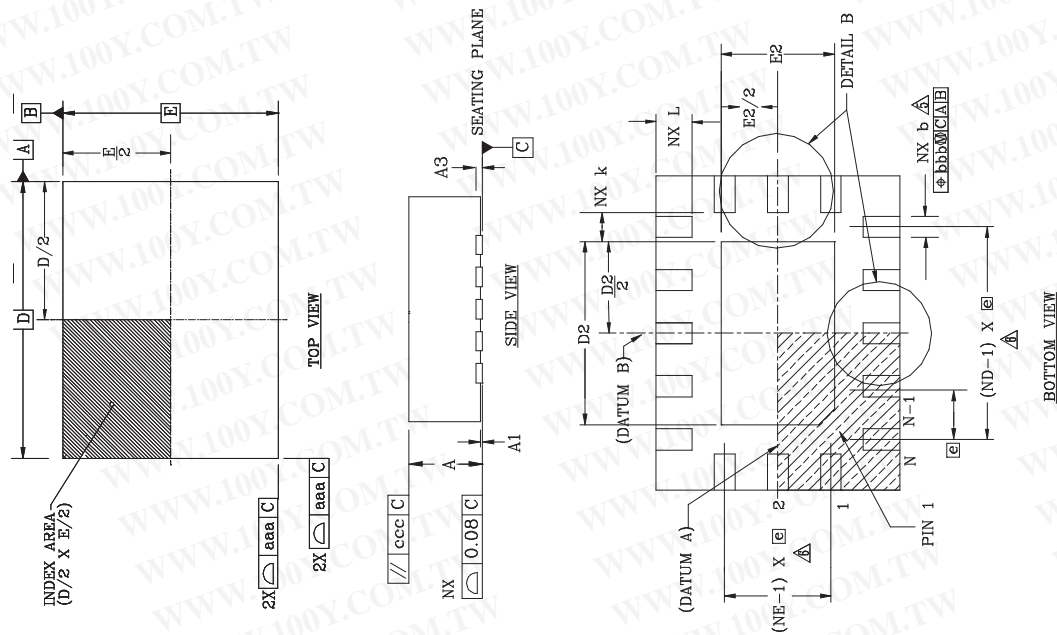


Figure 3. Package Outline: 5 mm x 5 mm LPCC 32-Pin Leadless Package

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TRF1122IRTMR	ACTIVE	VQFN	RTM	32	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		TRF 1122	<a href="#">Samples</a>
TRF1122IRTMRG3	ACTIVE	VQFN	RTM	32	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		TRF 1122	<a href="#">Samples</a>
TRF1122IRTMT	ACTIVE	VQFN	RTM	32	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		TRF 1122	<a href="#">Samples</a>
TRF1122IRTMGTG3	ACTIVE	VQFN	RTM	32	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		TRF 1122	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

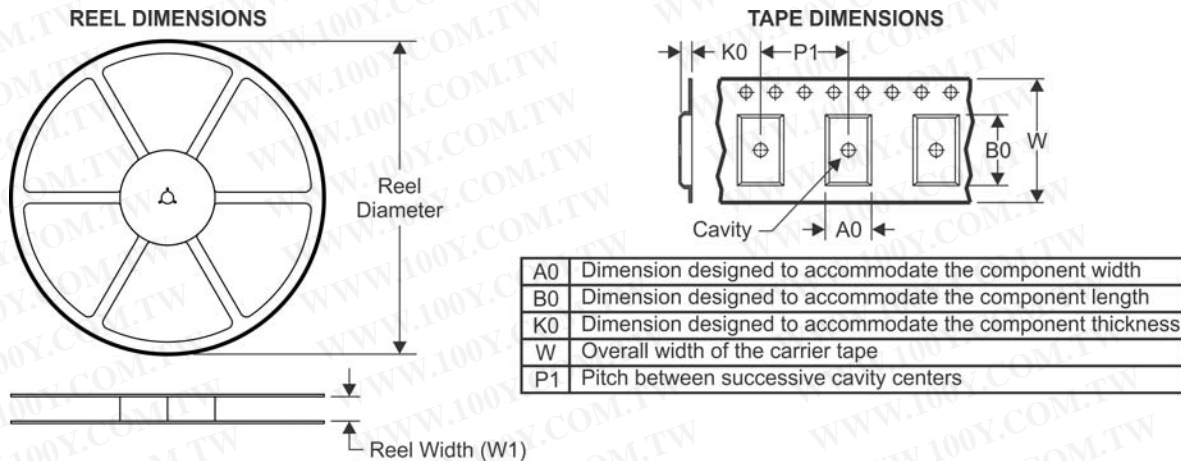
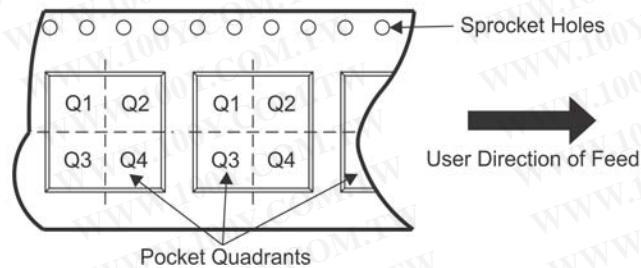
(4) Only one of markings shown within the brackets will appear on the physical device.

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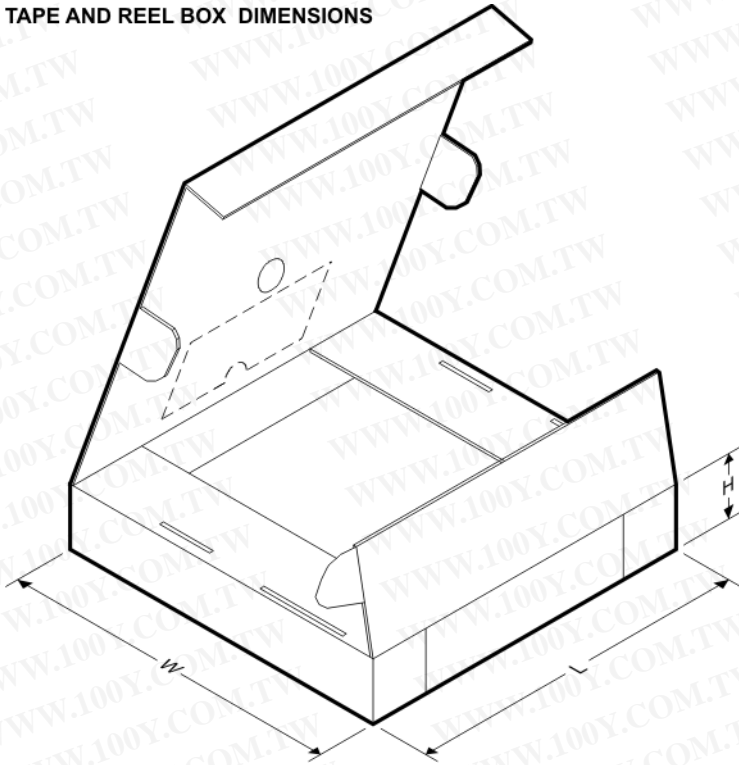




**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF1122IRTMR	VQFN	RTM	32	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TRF1122IRTMT	VQFN	RTM	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF1122IRTMR	VQFN	RTM	32	2500	338.1	338.1	20.6
TRF1122IRTMT	VQFN	RTM	32	250	210.0	185.0	35.0



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