Section 20 Electrical Specifications

20.1 Absolute Maximum Ratings

Table 20-1 lists the absolute maximum ratings.

Table 20-1 Absolute Maximum Ratings

Vcc	1.004- 70	
	-0.3 to +7.0	V
VPP	-0.3 to +13.5	V
Vin	-0.3 to Vcc + 0.3	٧
Vin	-0.3 to AVcc + 0.3	V
AVcc	-0.3 to +7.0	V
VAN	-0.3 to AVcc + 0.3	V
Topr	Regular specifications: -20 to +75	°C
	Wide-range specifications: -40 to +85	°C
Tstg	-55 to +125	°C
	AVCC VAN Topr	AVcc

Note: Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions.

20.2 Electrical Characteristics

20.2.1 DC Characteristics

Table 20-2 lists the DC characteristics.

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Table 20-2 DC Characteristics

Conditions: $VCC = 5.0V \pm 10\%*1$, $AVCC = 5.0V \pm 10\%, *1 VSS = AVSS = 0V$,

 $T_a = -20 \text{ to } +75^{\circ}\text{C}$ (Regular Specifications) $T_a = -40 \text{ to } +85^{\circ}\text{C}$ (Wide-Range Specifications)

Item	W.100X.CON	Sym- bol	Min	Тур	Max	Unit	Measurement Conditions
Input High voltage	RES, STBY,	VIH	Vcc - 0.7	1411	Vcc+0.3	V	WT
. *	MD2, MD1, MD0		<u> </u>	TXX.	11.10	CO_i	- TAN
	EXTAL		Vcc × 0.7	\overline{M}	Vcc+0.3	V	M.L
	Port 8		2.2	-(1)	AVcc+0.3	V	WTI
	Other input pins (except port 7)		2.2	- 1	Vcc+0.3	o¥.C	ON.TW
Input Low voltage	RES, STBY, MD2, MD1, MD0	VIL	-0.3		0.5	VY.	COM.TW
	Other input pins (except port 7)	MY.CC	-0.3	_	0.8	1 V U	Y.COM.TV
Schmitt trigger	Port 7	VT-	1.0	_	2.5	V	COM
input voltage	1 3.1	VT+	2.0		3.5	V	a_{I}
input voltage		VT+-VT	0.4	N_	- 4/1/1/1	٧	OUX.CO.
Input leakage	RES	lin	COMP.		10.0	μА	Vin = 0.5 to
current	STBY, NMI, MD2, MD1, MD0	W.1003	V.COM.	TW	1.0	μА	Vcc-0.5V
	port 8	W.100	OA'COM	NT.	1.0	μА	Vin = 0.5 to AVcc-0.5V
Leakage current	Port 9,	ITSI	OOY.CO	\TT	1.0	μΑ	Vin = 0.5 to
in 3-state (off state)	ports 7 to 1				W	W	Vcc-0.5V
Input pull-up MOS current	Ports 6 and 5	– I P	50	MO	200	μА	Vin = 0V
Output High	All output pins	Voн	Vcc-0.5	cO1	1.2	V	IOH = -200μA
Voltage	WT		3.5		1-17	٧	IOH = -1 mA
Output Low	All output pins	VOL	121.	V.CU	0.4	٧	lol = 1.6mA
Voltage	Port 4	-	21 W. Jac	-7.C(1.0	V	IOL = 8mA
MARKET TOOK	TI		10	0.7°	1.2	٧	loL = 10mA
Input capacitance	RES	Cin	VAL MAN	. <u>L</u>	60	ρF	Vin = 0 V
W.100	NMI	-	T.WW.	00	30	рF	f = 1MHz
	All input pins except RES, NA	- 41	MMM	100,	15 COM. 1	pF	Ta = 25°C

Note: *1 AVcc must be connected to a power supply line, even when the A/D converter is not used.

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Table 20-2 DC Characteristics (cont)

	Sym-	Min	Tvp	Max	Unit	Measurement Conditions
Normal operation	lcc	_	20	30	mA	f = 6MHz
		_	25	40	mA	f = 8MHz
		_	30	50	mA	f = 10MHz
Sleep mode			12	20	mA	f = 6MHz
		_	16	25	mA	f = 8MHz
		_	20	30	mA	f = 10MHz
Standby		N-	0.01	5.0	μА	Ta ≤ 50°C
			_	20	μА	Ta > 50°C
During A/D	Alcc	170	1.2	2.0	mA	Y.O. OM.TW
conversion						
While waiting		· F.	0.01	5.0	μА	COM
11/1/	VRAM	2.0	_	7/1/4	٧	001. VII
	Standby During A/D conversion	Normal operation ICC Sleep mode Standby During A/D Alcc conversion While waiting	bol Min Normal operation Icc — - — — Sleep mode — — Standby — — During A/D conversion Alcc — While waiting — —	bol Min Typ Normal operation Icc - 20 - 25 - 30 Sleep mode - 12 - 16 - 20 - 20 Standby - 0.01 - - During A/D conversion Alcc - 1.2 While waiting - 0.01	bol Min Typ Max Normal operation Icc - 20 30 - 25 40 - 30 50 Sleep mode - 12 20 - 16 25 - 20 30 Standby - 0.01 5.0 During A/D Alcc - 1.2 2.0 conversion - 0.01 5.0 While waiting - 0.01 5.0	bol Min Typ Max Unit Normal operation Icc - 20 30 mA - 25 40 mA - 30 50 mA Sleep mode - 12 20 mA - 16 25 mA - 20 30 mA Standby - 0.01 5.0 μA During A/D Alcc - 1.2 2.0 mA conversion - 0.01 5.0 μA

^{*2} Current dissipation values assume that VIH min = VCC - 0.5V, VIL max = 0.5V, all output pins are in the no-load state, and all MOS input pull-ups are off.

Table 20-3 Allowable Output Current Sink Values

Conditions: $VCC = 5.0V \pm 10\%$, $AVCC = 5.0V \pm 10\%$, VSS = AVSS = 0V,

 $T_a = -20 \text{ to } +75^{\circ}\text{C} \text{ (Regular Specifications)}$

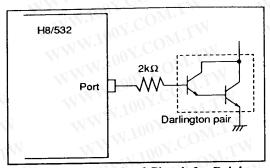
 $T_a = -40 \text{ to } +85^{\circ}\text{C}$ (Wide-Range Specifications)

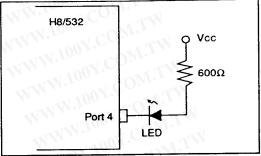
Item		Symbol	Min	Тур	Max	Unit
Allowable output Low	Port 4	loL	M_{T_T}	_	10	mA
current sink (per pin)	Other output pins		7.1	_	2.0	mA
Allowable output Low	Port 4, total of 8 pins	Σίοι	25	√\ -	40	mA
current sink (total)	Total of all other output pins		O-1/1	TW	80	mA
Allowable output High current sink (per pin)	All output pins	-Юн	$^{\circ}C_{D_{D}}$	LTW	2.0	mA
Allowable output High current sink (total)	Total of all output pins	Σ- І ОН	v.co	W I	25	mA

Note: To avoid degrading the reliability of the chip, be careful not to exceed the output current sink values in table 20-3. In particular, when driving a Darlington transistor pair or LED directly, be sure to insert a current-limiting resistor in the output path. See figures 20-1 and 20-2.

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Darlington Transistor Pair

Figure 20-1 Example of Circuit for Driving a Figure 20-2 Example of Circuit for Driving an LED

20.2.2 AC Characteristics

The AC characteristics of the H8/532 chip are listed in three tables. Bus timing parameters are given in table 20-4, control signal timing parameters in table 20-5, and timing parameters of the on-chip supporting modules in table 20-6.

Table 20-4 Bus Timing

Conditions: VCC = $5.0V \pm 10\%$, AVCC = $5.0V \pm 10\%$, $\emptyset = 0.5$ to 10MHz, Vss = 0V

 $T_a = -20 \text{ to } +75^{\circ}\text{C}$ (Regular Specifications)

 $T_a = -40 \text{ to } +85^{\circ}\text{C}$ (Wide-Range Specifications)

	6M	Hz	8M	Hz	10	VIHZ		Measurement
Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
tcyc	166.7	2000	125	2000	100	2000	ns	See figure 20-4
tCL	65	100.	45	V Ī ·r	35		ns	W.100 -1 C
tch	65	-n01	45	TIT	35		ns	1007.0
tCr		15	<+ C¹	15	oTN.	15	ns	MAN. OUX.
tcf		15) <u>-</u>	15	<u> </u>	15	ns	-WW.Io
tAD	17/	70	101	65	3.1	65	ns	N 100 x
TAH	30	71	25	$C_{D_{\hat{r}}}$	20	11	ns	-WW W
tDSD1	_	70	In.	60	17.	40	ns	- TWW.Io
tDSD2	_ ///	70	400	60	- 1.1	50	ns	- W 10
tDSD3	- <	70		60) <u>F</u>	50	ns	- 1/1/1/1/1/1/1/1/1/1/1/1/1/1/1/1/1/1/1/
tDSWW	200	- wil	150	C	120	4 <u>2</u>	ns	- WW.
tAS1	25	M.,	20	g_{TT} .	15	1-11	ns	
	toyc toL tCH tCr tCf tAD tAH tDSD1 tDSD2 tDSD3 tDSWW	Symbol Min toyc 166.7 tCL 65 tCH 65 tCr - tAD - tAH 30 tDSD1 - tDSD2 - tDSD3 - tDSWW 200	toyc 166.7 2000 tCL 65 - tCH 65 - tCr - 15 tCl - 15 tCl - 70 tAD - 70 tAH 30 - tDSD1 - 70 tDSD2 - 70 tDSD3 - 70 tDSWW 200 -	Symbol Min Max Min tcyc 166.7 2000 125 tCL 65 - 45 tCr - 15 - tCr - 15 - tAD - 70 - tAH 30 - 25 tDSD1 - 70 - tDSD2 - 70 - tDSD3 - 70 - tDSWW 200 - 150	Symbol Min Max Min Max tcyc 166.7 2000 125 2000 tCL 65 - 45 - tCH 65 - 45 - tCr - 15 - 15 tCf - 70 - 65 tAD - 70 - 60 tDSD1 - 70 - 60 tDSD2 - 70 - 60 tDSD3 - 70 - 60 tDSWW 200 - 150 - 60	Symbol Min Max Min Max Min tcyc 166.7 2000 125 2000 100 tCL 65 - 45 - 35 tCr - 15 - 15 - tCr - 15 - 15 - tAD - 70 - 65 - tAH 30 - 25 - 20 tDSD1 - 70 - 60 - tDSD2 - 70 - 60 - tDSWW 200 - 150 - 120	Symbol Min Max Min Max Min Max Min Max tcyc 166.7 2000 125 2000 100 2000 tCL 65 - 45 - 35 - tCr - 15 - 15 - 15 tCr - 15 - 15 - 15 tCr - 70 - 65 - 65 tAH 30 - 25 - 20 - tDSD1 - 70 - 60 - 50 tDSD2 - 70 - 60 - 50 tDSD3 - 70 - 60 - 50 tDSWW 200 - 150 - 120 -	Symbol Min Max Min Max Min Max Min Max Unit tcyc 166.7 2000 125 2000 100 2000 ns tcl 65 - 45 - 35 - ns tcr - 15 - 15 - 15 ns tcr - 15 - 15 - 15 ns tAD - 70 - 65 - 65 ns tAH 30 - 25 - 20 - ns tDSD1 - 70 - 60 - 40 ns tDSD3 - 70 - 60 - 50 ns tDSWW 200 - 150 - 120 - ns

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Table 20-4 Bus Timing (cont)

	6MHz 8MHz 10MHz				Measurement				
tem	Symbol		Max	Min	Max	Min	Max	Unit	Conditions
Address setup time 2	tAS2	105	<u> </u>	80	_	65	Πл.	ns	See figure 20-4
Read data setup time	trds	60		50	VI //	40	<u> </u>	ns	WI.I.
Read data hold time	trdh	0	_	0		0	10,	ns	WILL
Read data access time	tACC	-M	280		190	-01	160	ns	M_{TL}
Write data delay time	twdd	70,	70		65	77	65	ns	WIII.
Write data setup time	twos	30	1700	15	_	10	M. Y.	ns	OM
Vrite data hold time	tWDH	30	177	25		20	<u>azi 10</u>	ns	-0M:1
Vait setup time	twrs	40	- 1	40		40	<u> </u>	ns	See figure 20-5
Wait hold time	twTH	10	$O_{\overline{D}/I}$	10	_	10	+11	ns	1 COM
Bus request setup time	tBRQS	40	-5M	40	_	40	- 41	ns	See figure 20-10
Bus acknowledge delay time 1	tBACD1	π¥.	70	TW	60	- 1	55	ns	Y.C. TI
Bus acknowledge delay time 2	tBACD2	U • ∢ 7	70	-	60	_	55	ns	ON COM
Bus floating delay time	tBZD	$t_{\partial\Omega,r}$	tBACD1	\vdash	tBACD	1-	tBACD	1 ns	M. COWIT
clock delay time	tED	700	20	- 1	15	-	15	ns	See figure 20-11
clock rise time	tEr	700	15	Ar.	15	-	15	ns	TO V.COM
clock fall time	tEf	a 10	15	TV.	15	-	15	ns	100 r COM.1
Read data hold time	TRDHE	0	OFY.C	0	-11	0	- 1	ns	See figure 20-6
E clock sync)									
Write data hold time	twoHE	50	700 r.	40	VE'T	30	_	ns	W.100 COM
E clock sync)									
Eclock sync)	W		1.1001	V.C	MT			<u> </u>	MAITON

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Table 20-5 Control Signal Timing

MMM.100X.COMr. Conditions: $VCC = 5.0V \pm 10\%$, $AVCC = 5.0V \pm 10\%$, $\emptyset = 0.5$ to 10MHz, VSS = 0V

Item WWW.100Y.		6MHz		z 8MHz		10	OMHz		Measurement	
	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions	
RES setup time	tRESS	200	_	200		200	<u> </u>	ns	See figure 20	
RES pulse width	tresw	6.0		6.0		6.0		tcyc	1	
Mode programming setup time	tMDS	4.0	N_	4.0	77	4.0		tcyc	LTW	
NMI setup time	tNMIS	150	7	150	7	150	$(\overline{m})_{p_{x}}$	ns	See figure 20	
NMI hold time	tNMIH	10	TZN	10	411	10	4710	ns	TIT I	
IRQo setup time	tiRQ0S	50	=xXI	50	- «X	50	<u>, y</u>	ns	Div.	
IRQ1 setup time	tIRQ1S	50	1.7	50		50	<u> 1-10'</u>	ns	OM.1	
IRQ1 hold time	tIRQ1H	10	TT	10	- 1	10	- 10	ns	TW	
NMI pulse width (for recovery from software standby mode)	tnmiw	200	om.T	200	_	200	NN.	ns	See figure 20	
Crystal oscillator settling time (reset)	tosc1	20	COM	20	_	20		ms	See figure 20-	
Crystal oscillator settling time (software standby)	tosc2	10	(.CO	10	v sv	10	<u> </u>	ms	See figure 18	

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Table 20-6 Timing Conditions of On-Chip Supporting Modules

Conditions: $VCC = 5.0V \pm 10\%$, $AVCC = 5.0V \pm 10\%$, $\emptyset = 0.5$ to 10MHz, VSS = 0V

 $T_a = -20 \text{ to } +75^{\circ}\text{C} \text{ (Regular Specifications)}$

 $T_a = -40 \text{ to } +85^{\circ}\text{C}$ (Wide-Range Specifications)

				< √ 6N	ИHz	8M	Hz	101	/Hz		Measurement
Item			Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
FRT	Timer output delay time	1007.	t FTOD		100	_ \	100	. ≼ .1	100	ns	See figure 20-14
	Timer input setup time		t FTIS	50	V-	50	WW	50	. 700	ns	W
	Timer clock input setup time Timer clock pulse width		t FTCS	50	<u>-</u>	50		50	Too	ns	See figure 20-15
			tFTCWL,	Ti							
			I FTCWH	1.5	-N	1.5	- 1	1.5		toyo	COSTI
TMR	Timer output delay time	W.IU	TTMOD	ĬŢĮ.	100		100	-70N	100	пѕ	See figure 20-16
	Timer clock input setup tir	ne	trucs	50	TV	50	_	50	ZXI.	ns	See figure 20-17
	Timer clock pulse width	11/14.	ttmcwl,)O 2-	- 17	N		W			
			TMCWH	1.5	17.	1.5	-	1.5	-	tcyc	CON
	Timer reset input setup tir	ne	TTMRS	50	417	50	_	50	-	ns	See figure 20-18
PWM	Timer output delay time	WW	tPWOD		100		100	- <	100	ns	See figure 20-19
SCI	Input clock cycle	(Async)	tScyc	2	Θ_{M_I}	2	1=	2	311	toyo	See figure 20-20
		(Sync)		4	-01	4		4	7,	toyo	100
	Input clock pulse width	W	tsckw	0.4	0.6	0.4	0.6	0.4	0.6	tScyc	100 X.C
	Transmit data delay time	(Sync)	trxd		100	Mire	100	-	100	ns	See figure 20-21
	Receive data setup time	(Sync)	trxs	100		100	77	100	_	ns	W.100
	Receive data hold time	(Sync)	trixh	100	Ţ.U	100		100	_	ns	1007.0
Port	Output data delay time		tPWD	150	100		100	N -	100	ns	See figure 20-13
	Input data setup time		t PRS	50	M.	50	T.	50	_	ns	-WW.100
	Input data hold time		tPRH	50	(4) X	50	-11	50	_	ns	1007

• Measurement Conditions for AC Characteristics

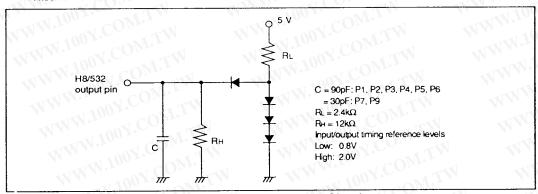


Figure 20-3 Output Load Circuit

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20.2.3 A/D Converter Characteristics

Table 20-7 lists the characteristics of the on-chip A/D converter.

Table 20-7 A/D Converter Characteristics

Conditions: $VCC = 5.0V \pm 10\%$, $AVCC = 5.0V \pm 10\%$, VSS = AVSS = 0V,

 $T_a = -20 \text{ to } +75^{\circ}\text{C}$ (Regular Specifications)

 $T_a = -40 \text{ to } +85^{\circ}\text{C}$ (Wide-Range Specifications)

	MHz		1/18	3MHz	- 400	10MHz			
Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
10	10	10	10	10	10	10	10	10	Bits
	1	23.0		TAN.	17.25	n o Y		13.8	μs
GO)	7.0	20		33 1	20		1 - E(20	рF
	V T .)	10		44	10	700		10	kΩ
	= (±2.0	_		±2.0	170	Ž,	±2.0	LSB
-√-C'	$O(N)_{Tr}$	±2.0	_		±2.0	ATT.	N.	±2.0	LSB
O.E.	VTT.	±2.0		_	±2.0	W-11	1 <u>0 -</u>	±2.0	LSB
1.1	<u> </u>	±0.5	N		±0.5		nO?	±0.5	LSB
_ <1	(4)	±2.5	< ≤		±2.5	171.		±2.5	LSE
	Min	- TO THE REAL PROPERTY OF THE PERTY OF THE P	Min Typ Max 10 10 10 23.0 20 10 ±2.0 ±2.0 ±2.0 ±2.0 ±0.5	Min Typ Max Min 10 10 10 10 23.0 20 10 ±2.0 ±2.0 ±2.0 ±0.5	Min Typ Max Min Typ 10 10 10 10 10 23.0 20 10 ±2.0 ±2.0 ±0.5	Min Typ Max Min Typ Max 10 10 10 10 10 — 23.0 — — 17.25 — 20 — — 20 — — 10 — — 10 — — ±2.0 — — ±2.0 — — ±2.0 — ±2.0 — — ±2.0 — ±2.0 — — ±0.5 — ±0.5	Min Typ Max Min Typ Max Min 10 10 10 10 10 10 23.0 17.25 20 20 10 10 10 10 12.0 12.0 12.0 12.0 12.0 12.0 12.0 12.0 12.0 12.0 12.0 12.0 12.0 12.0 12.0	Min Typ Max Min Typ Max Min Typ 10 10 10 10 10 10 10 10 — 23.0 — — 17.25 — — — — 20 — — — — — — 10 — — — — — — 10 — — — — — — +2.0 — — — — — — +2.0 — — — — — — +2.0 — — — — — — +2.0 — — — — — — — +2.0 — — — — — — — +2.0 — — — — — — — +2.0	Min Typ Max Min Typ Max Min Typ Max 10 10 10 10 10 10 10 10 — 23.0 — — 17.25 — — 13.8 — — 20 — — 20 — — 10 — — 20 — — 10 — — 10 — — +2.0 — — +2.0 — — +2.0 — — +2.0 — — +2.0 — — +2.0 — — +2.0 — — +2.0 — — +2.0 — — +2.0 — — +2.0 — — +2.0 — — +2.0 — — +2.0 — — +0.5 — <t< td=""></t<>

20.3 MCU Operational Timing

This section provides the following timing charts:

20.3.1 Bus timing	Figures 20-4 to 20-6
20.3.2 Control Signal Timing	Figures 20-7 to 20-10
20.3.3 Clock Timing	Figures 20-11 and 20-12
20.3.4 I/O Port Timing	Figure 20-13
20.3.5 16-Bit Free-Running Timer Timing	Figures 20-14 and 20-15
20.3.6 8-Bit Timer Timing	Figures 20-16 to 20-18
20.3.7 Pulse Width Modulation Timer Timing	Figure 20-19
20.3.8 Serial Communication Interface Timing	Figure 20-20 and 20-21

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20.3.1 Bus Timing

1. Basic Bus Cycle (without Wait States) in Expanded Modes

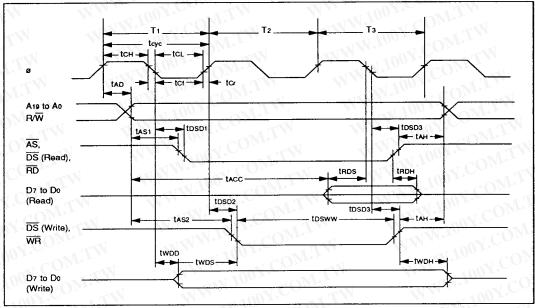


Figure 20-4 Basic Bus Cycle (without Wait States) in Expanded Modes

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2. Basic Bus Cycle (with 1 Wait State) in Expanded Modes

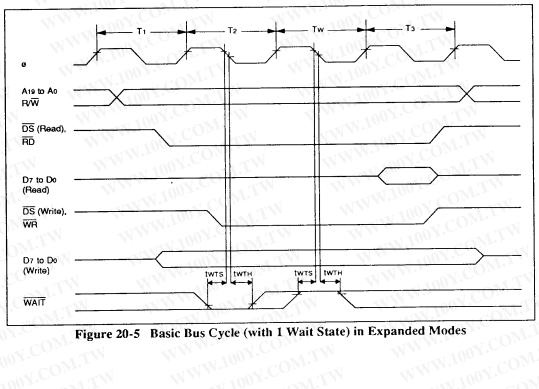


Figure 20-5 Basic Bus Cycle (with 1 Wait State) in Expanded Modes WWW.100Y.COM.TW WWW.100Y.COM.TW

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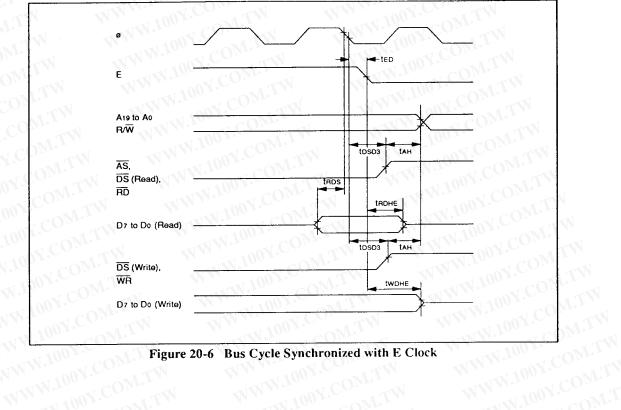
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3. Bus Cycle Synchronized with E Clock



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20.3.2 Control Signal Timing

1. Reset Input Timing

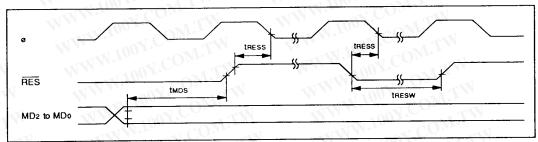


Figure 20-7 Reset Input Timing

2. Interrupt Input Timing

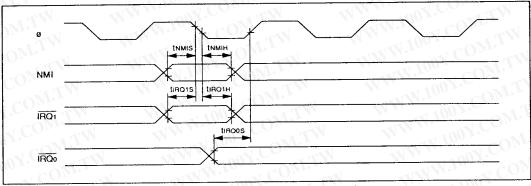


Figure 20-8 Interrupt Input Timing

3. NMI Pulse Width

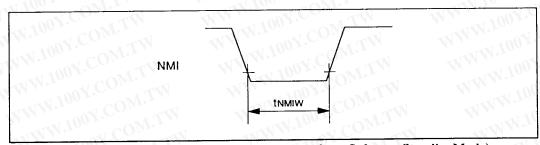


Figure 20-9 NMI Pulse Width (for Recovery from Software Standby Mode)

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4. Bus Release State Timing

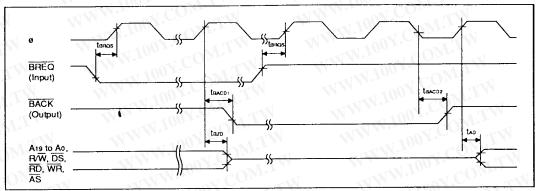


Figure 20-10 Bus Release State Timing

20.3.3 Clock Timing

1. E Clock Timing

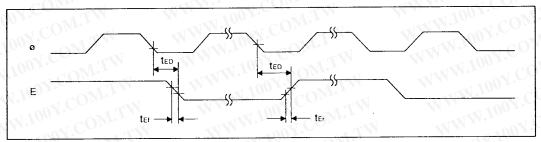
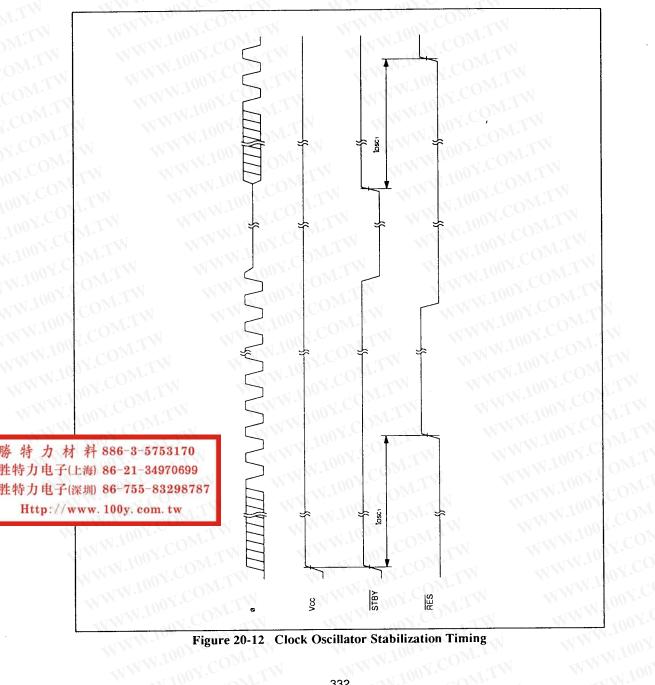


Figure 20-11 E Clock Timing

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2. Clock Oscillator Stabilization Timing



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20.3.4 I/O Port Timing

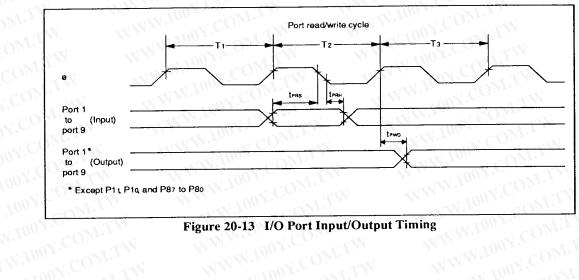


Figure 20-13 I/O Port Input/Output Timing WWW.100Y.C WWW.100Y.COM.TW

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20.3.5 16-Bit Free-Running Timer Timing

1. Free-Running Timer Input/Output Timing

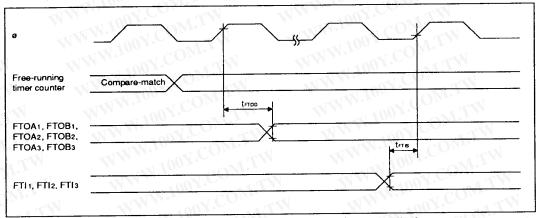


Figure 20-14 Free-Running Timer Input/Output Timing

2. External Clock Input Timing for Free-Running Timers

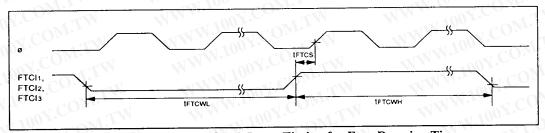


Figure 20-15 External Clock Input Timing for Free-Running Timers

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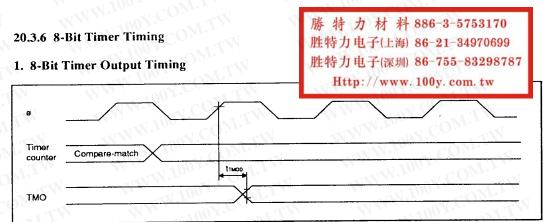


Figure 20-16 8-Bit Timer Output Timing

2. 8-Bit Timer Clock Input Timing

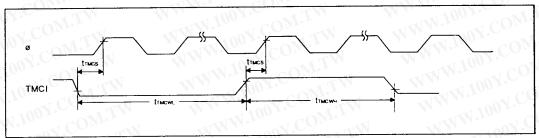


Figure 20-17 8-Bit Timer Clock Input Timing

3. 8-Bit Timer Reset Input Timing

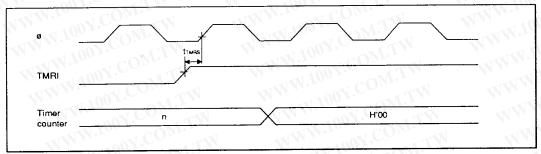


Figure 20-18 8-Bit Timer Reset Input Timing

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20.3.7 Pulse Width Modulation Timer Timing

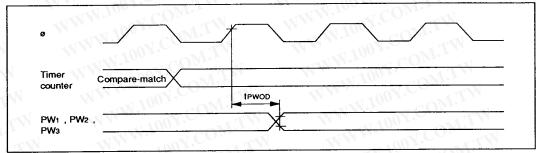


Figure 20-19 PWM Timer Output Timing

20.3.8 Serial Communication Interface Timing

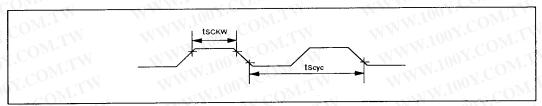


Figure 20-20 SCI Input Clock Timing

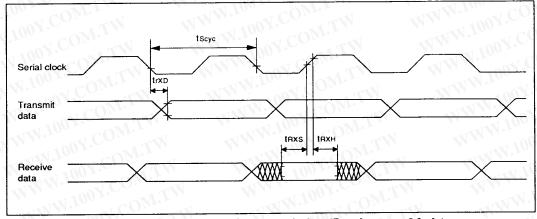


Figure 20-21 SCI Input/Output Timing (Synchronous Mode)

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