life.augmented

LIS2DW12

MEMS digital output motion sensor: high-performance ultra-low-power 3-axis "femto" accelerometer

Datasheet - production data

Features

- Ultra-low power consumption: 50 nA in power-down mode, below 1 µA in active low-power mode
- Very low noise: down to 1.3 mg RMS in low-power mode
- Multiple operating modes with multiple bandwidths
- Android stationary detection, motion detection
- Supply voltage, 1.62 V to 3.6 V
- Independent IO supply
- ±2g/±4g/±8g/±16*g* full scale
- High-speed I^2C/SPI digital output interface
- Single data conversion on demand
- 16-bit data output
- Embedded temperature sensor
- Self-test
- 32-level FIFO
- 10000 *g* high shock survivability
- ECOPACK®, RoHS and "Green" compliant

Applications

- Motion detection for wearables
- Gesture recognition and gaming
- Motion-activated functions and user interfaces
- Display orientation
- Tap/double-tap recognition
- Free-fall detection
- Smart power saving for handheld devices
- Hearing aids
- Portable healthcare devices
- Wireless sensor nodes
- Motion-enabled metering devices

Description

The LIS2DW12 is an ultra-low-power high-performance three-axis linear accelerometer belonging to the "femto" family which leverages on the robust and mature manufacturing processes already used for the production of micromachined accelerometers.

The LIS2DW12 has user-selectable full scales of ±2g/±4g/±8g/±16*g* and is capable of measuring accelerations with output data rates from 1.6 Hz to 1600 Hz.

The LIS2DW12 has an integrated 32-level first-in, first-out (FIFO) buffer allowing the user to store data in order to limit intervention by the host processor.

The embedded self-test capability allows the user to check the functioning of the sensor in the final application.

The LIS2DW12 has a dedicated internal engine to process motion and acceleration detection including free-fall, wakeup, highly configurable single/double-tap recognition, activity/inactivity, stationary/motion detection, portrait/landscape detection and 6D/4D orientation.

The LIS2DW12 is available in a small thin plastic land grid array package (LGA) and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

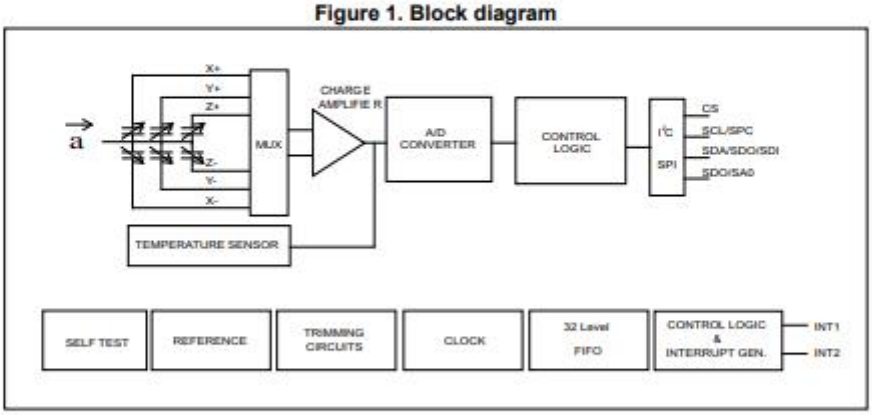
Table 1. Device summary

Order codes	Temp. range [°C]	Package	Packaging
LIS2DW12	-40 to +85	LGA-12	Tray
LIS2DW12TR	-40 to +85	LGA-12	Tape and reel

1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections

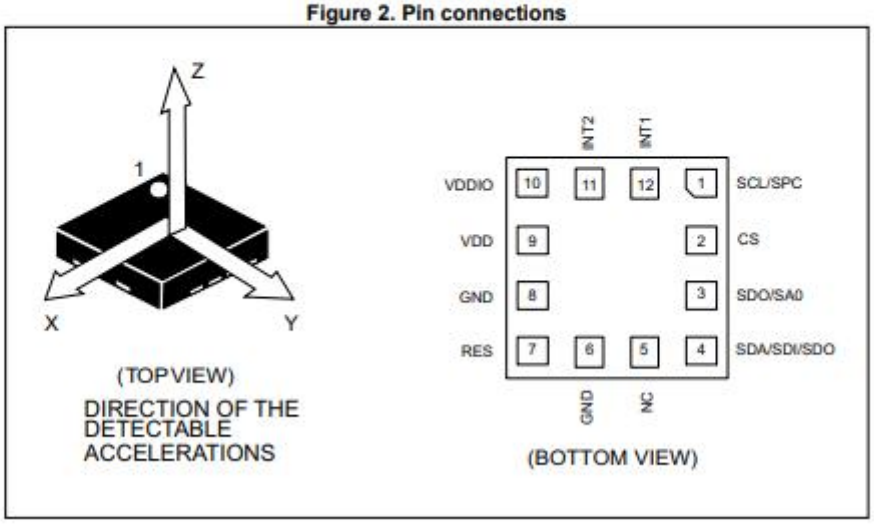


Table 2. Pin description

Pin#	Name	Function
1	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
2(1)	CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
3(1)	SDO SA0	SPI serial data output (SDO) I^2C less significant bit of the device address (SA0)
4	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
5	NC	Internally not connected. Can be tied to VDD, VDDIO, or GND.
6	GND	0 V supply
7	RES	Connect to GND
8	GND	0 V supply
9	VDD	Power supply
10	VDD_IO	Power supply for I/O pins
11	INT2	Interrupt pin 2. Clock input when selected in single data conversion on demand.
12	INT1	Interrupt pin 1

1. SDO/SA0 and CS pins are internally pulled up. Refer to *Table 3* for the internal pull-up values (typ).

2.3 Temperature sensor characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted

Table 6. Temperature sensor characteristics

Symbol	Parameter	Min.	Typ.(1)	Max.	Unit
Top	Operating temperature range	-40		+85	°C
Toff	Temperature offset(2)	-15		+15	°C
TSDr	Temperature sensor output change vs. temperature		1(3)		LSB/°C
			16(4)		
TODR	Temperature refresh rate in High-Performance Mode for all ODRs or in Low-Power Modes for ODRs equal to 200/100/50 Hz		50		Hz
	Temperature refresh rate in Low-Power Modes for ODR equal to 25 Hz		25		
	Temperature refresh rate in Low-Power Modes for ODR equal to 12.5 Hz		12.5		
	Temperature refresh rate in Low-Power Modes for ODR equal to 1.6 Hz		1.6		

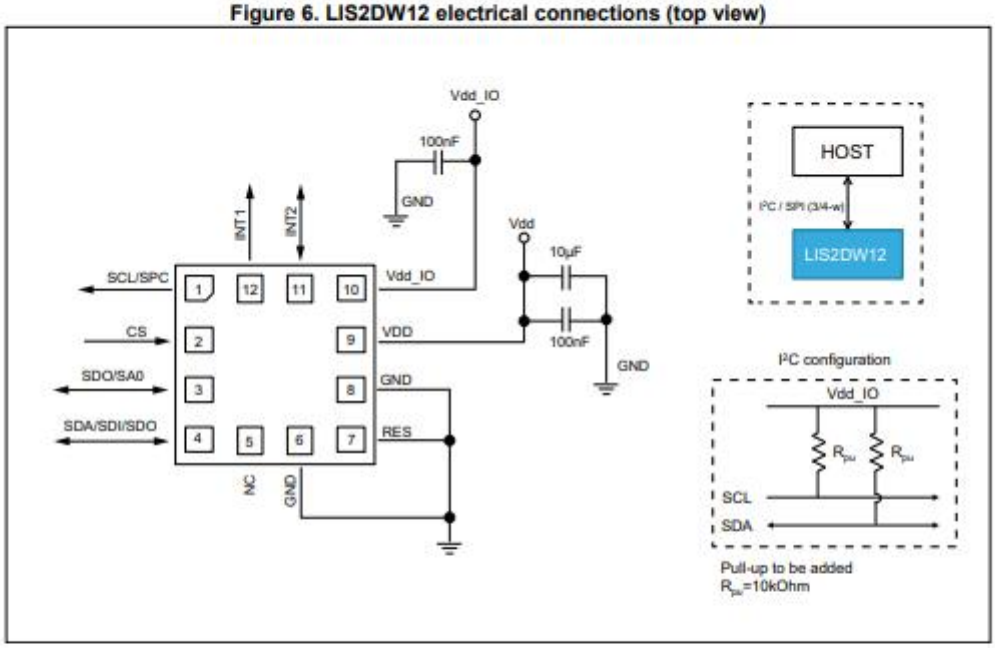
1. Typical specifications are not guaranteed.
2. The output of the temperature sensor is 0 LSB (typ.) at 25 °C.
3. 8-bit resolution.
4. 12-bit resolution.

Table 3. Internal pull-up values (typ.) for SDO/SA0 and CS pins

Vdd_IO	Resistor value for SDO/SA0 and CS pins
	Typ. (kΩ)
1.7 V	54.4
1.8 V	49.2
2.5 V	30.4
3.6 V	20.4

4 Application hints

Figure 6. LIS2DW12 electrical connections (top view)



The device core is supplied through the Vdd line while the I/O pads are supplied through the Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to pin 9 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 6*). It is possible to remove Vdd while maintaining Vdd_IO without blocking the communication bus, in this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data are selectable and accessible through the I^2C or SPI interfaces. When using the I^2C, CS must be tied high (i.e. connected to Vdd_IO).

The functions, the threshold and the timing of the two interrupt pins (INT1 and INT2) can be completely programmed by the user through the I^2C/SPI interface.

Table 13. Internal pin status

Pin #	Name	Function	Pin status
1	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)	Default: open drain
2	CS	SPI enable I^2C/SPI mode selection 1: SPI idle mode / I^2C communication enabled 0: SPI communication mode / I^2C disabled	Default: input with internal pull-up(1)
3	SDO SA0	Serial data output (SDO) I^2C less significant bit of the device address (SA0)	Default: input with internal pull-up
4	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)	Default: (SDA) input open drain
5	NC	Internally not connected. Can be tied to VDD, VDDIO, or GND.	
6	GND	0 V supply	
7	RES	Connect to GND	
8	GND	0 V supply	
9	VDD	Power supply	
10	VDD_IO	Power supply for I/O pins	
11	INT2	Interrupt pin 2. Clock input when selected in single data conversion on demand.	Default: push-pull output forced to Gnd
12	INT1	Interrupt pin 1	Default: push-pull output forced to Gnd

1. In order to disable the internal pull-up on the CS pin, write '1' to the CS_PU_DISC bit in *CTRL2 (21h)*.

2.2 Electrical characteristics

Table 5. Electrical characteristics @ Vdd = 1.8 V, T = 25 °C unless otherwise noted (1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
Vdd	Supply voltage		1.62	1.8	3.6	V
Vdd_IO	I/O pins supply voltage(3)		1.62		Vdd+0.1	V
IddHR	Current consumption in High-Performance Mode(4)	@ ODR range 12.5 Hz - 1600 Hz, 14-bit		90		µA
IddLP	Current consumption in Low-Power Mode(5)	ODR 100 Hz		5		µA
		ODR 50 Hz		3		
		ODR 12.5 Hz		1		
		ODR 1.6 Hz		0.38		
Idd_PD	Current consumption in power-down			50		nA
V_{IH}	Digital high-level input voltage		0.8*Vdd_IO			V
V_{IL}	Digital low-level input voltage				0.2*Vdd_IO	V
V_{OH}	Digital high-level output voltage	I_{OH} = 4 mA(6)	VDD_IO - 0.2 V			
V_{OL}	Digital low-level output voltage	I_{OL} = 4 mA(6)			0.2 V	

1. The product is factory calibrated at 1.8 V. The operational power supply range is from 1.62 V to 3.6 V.
2. Typical specifications are not guaranteed.
3. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses. In this condition the measurement chain is powered off.
4. Low-noise setting disabled.
5. Low-Power Mode 1. Low-noise setting disabled.
6. 4 mA is the maximum driving capability, ie. the maximum DC current that can be sourced/sunk by the digital pad in order to guarantee the correct digital output voltage levels V_{OH} and V_{OL}.

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 Soldering information

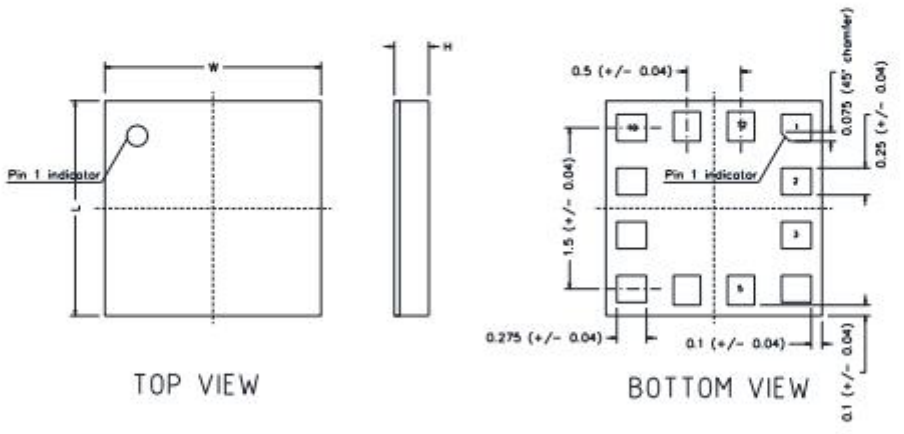
The LGA package is compliant with the ECOPACK®, RoHS and "Green" standard.

It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Land pattern and soldering recommendations are available at www.st.com.

9.2 LGA-12 package information

Figure 18. LGA-12 2.0 x 2.0 x 0.7 mm package outline and mechanical data



Dimensions are in millimeter unless otherwise specified
General Tolerance is +/-0.15mm unless otherwise specified

OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	2	±0.1
Width [W]	2	±0.1
Height [H]	0.7 MAX	/

DM00170568_2