Chapter 1 Introduction

1.1 General Terms and Conventions

The following is list of the general terms used throughout this document:

BYTE	8-bits
FIFO	First In First Out buffer; often used for elasticity buffer
MAC	Media Access Controller
RMII™	Reduced Media Independent Interface™
N/A	Not Applicable
X	Indicates that a logic state is "don't care" or undefined.
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
SMI	Serial Management Interface

1.2 General Description

The LAN8720A/LAN8720Ai is a low-power 10BASE-T/100BASE-TX physical layer (PHY) transceiver with variable I/O voltage that is compliant with the IEEE 802.3-2005 standards.

The LAN8720A/LAN8720Ai supports communication with an Ethernet MAC via a standard RMII interface. It contains a full-duplex 10-BASE-T/100BASE-TX transceiver and supports 10Mbps (10BASE-T) and 100Mbps (100BASE-TX) operation. The LAN8720A/LAN8720Ai implements auto-negotiation to automatically determine the best possible speed and duplex mode of operation. HP Auto-MDIX support allows the use of direct connect or cross-over LAN cables.

The LAN8720A/LAN8720Ai supports both IEEE 802.3-2005 compliant and vendor-specific register functions. However, no register access is required for operation. The initial configuration may be selected via the configuration pins as described in Section 3.7, "Configuration Straps," on page 31. Register-selectable configuration options may be used to further define the functionality of the transceiver.

Per IEEE 802.3-2005 standards, all digital interface pins are tolerant to 3.6V. The device can be configured to operate on a single 3.3V supply utilizing an integrated 3.3V to 1.2V linear regulator. The linear regulator may be optionally disabled, allowing usage of a high efficiency external regulator for lower system power dissipation.

The LAN8720A/LAN8720Ai is available in both extended commercial and industrial temperature range versions. A typical system application is shown in Figure 1.1.

Table 2.2 LED Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
	LED 2	LED2	O12	Link Speed LED Indication. This pin is driven active when the operating speed is 100Mbps. It is inactive when the operating speed is 10Mbps or during line isolation. **Note:** Refer to Section 3.8.1, "LEDs," on page 37 for additional LED information.
1	nINT/ REFCLKO Function Select Configuration Strap	nINTSEL	IS (PU)	This configuration strap selects the mode of the nINT/REFCLKO pin. ▪ When nINTSEL is floated or pulled to VDD2A, nINT is selected for operation on the nINT/REFCLKO pin (default). ▪ When nINTSEL is pulled low to VSS, REFCLKO is selected for operation on the nINT/REFCLKO pin. See Note 2.2 for more information on configuration straps. **Note:** Refer to See Section 3.8.1.2, "nINTSEL and LED2 Polarity Selection," on page 37 for additional information.

Note 2.2 Configuration strap values are latched on power-on reset and system reset. Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to Section 3.7, "Configuration Straps," on page 31 for additional information.

Table 2.3 Serial Management Interface (SMI) Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	SMI Data Input/Output	MDIO	VIS/ VOD8	Serial Management Interface data input/output
1	SMI Clock	MDC	VIS	Serial Management Interface clock

Table 2.4 Ethernet Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Ethernet TX/RX Positive Channel 1	TXP	AIO	Transmit/Receive Positive Channel 1
1	Ethernet TX/RX Negative Channel 1	TXN	AIO	Transmit/Receive Negative Channel 1

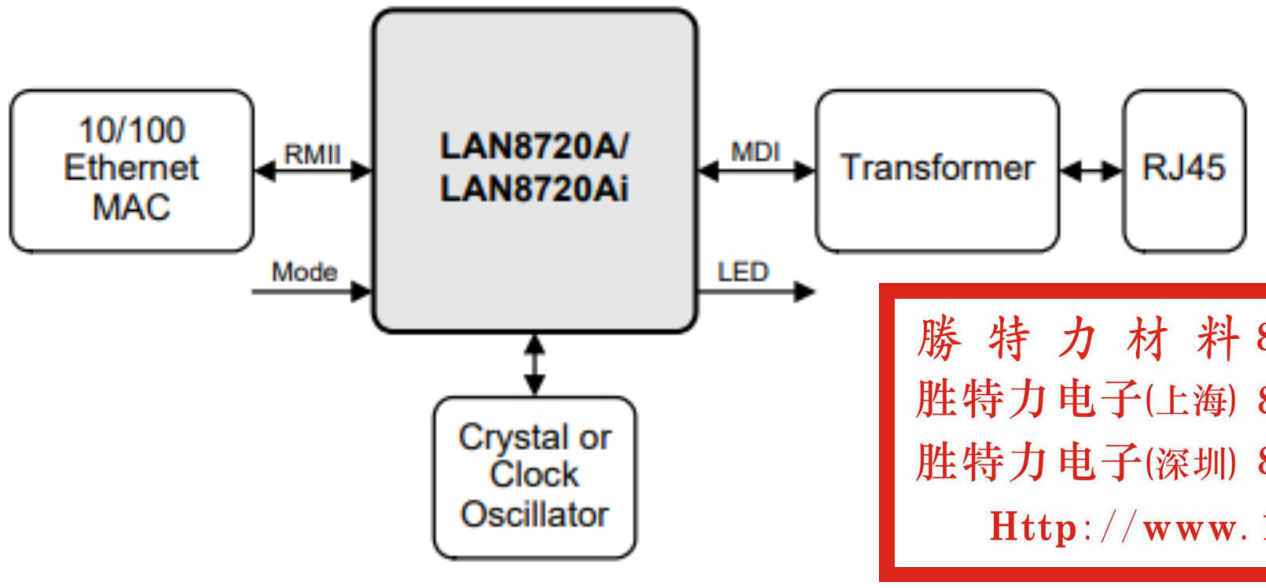


Figure 1.1 System Block Diagram

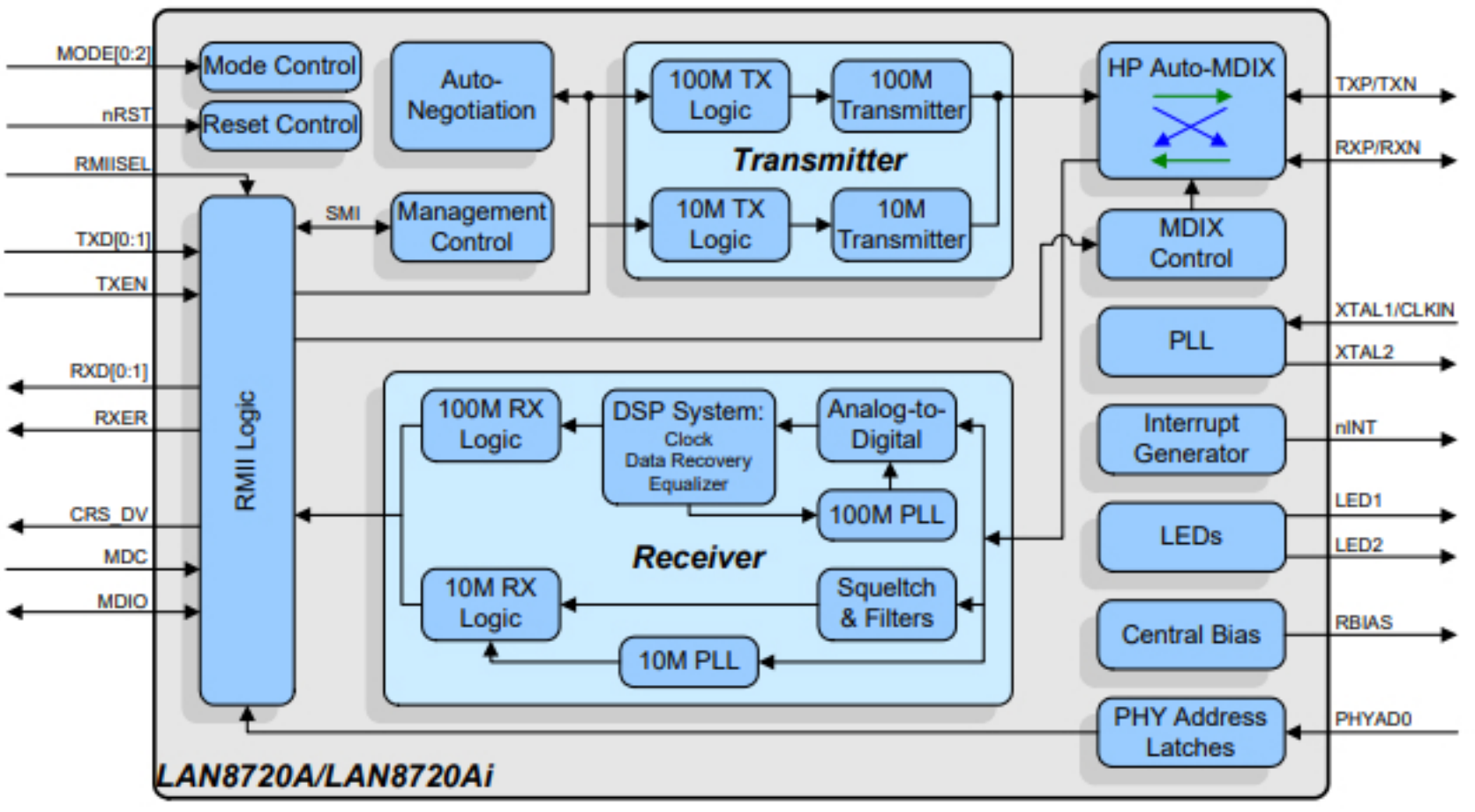
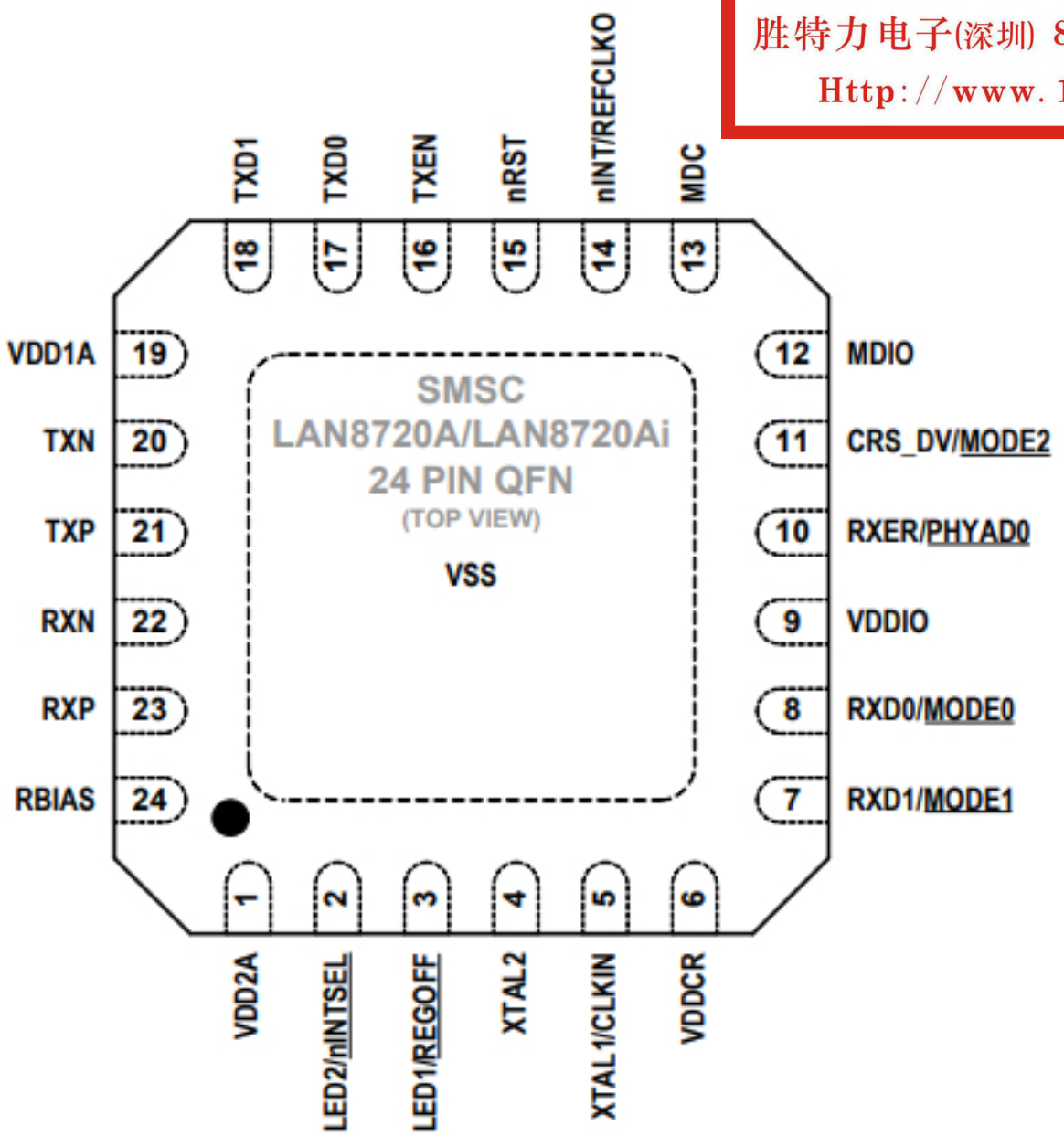


Figure 1.2 Architectural Overview

Chapter 2 Pin Description and Configuration



NOTE: Exposed pad (VSS) on bottom of package must be connected to ground

Figure 2.1 24-QFN Pin Assignments (TOP VIEW)

Note: When a lower case "n" is used at the beginning of the signal name, it indicates that the signal is active low. For example, nRST indicates that the reset signal is active low.

Note: The buffer type for each signal is indicated in the BUFFER TYPE column. A description of the buffer types is provided in Section 2.2.