LAN9252

2/3-Port EtherCAT® Slave Controller with Integrated Ethernet PHYs

Highlights

- 2/3-port EtherCAT slave controller with 3 Fieldbus Memory Management Units (FMMUs) and 4 SyncManagers
- Interfaces to most 8/16-bit embedded controllers and 32-bit embedded controllers with an 8/16-bit bus
- Integrated Ethernet PHYs with HP Auto-MDIX
- Wake on LAN (WoL) support
- Low power mode allows systems to enter sleep mode until addressed by the Master
- Cable diagnostic support
- 1.8V to 3.3V variable voltage I/O
- Integrated 1.2V regulator for single 3.3V operation
- Low pin count and small body size package

Target Applications

- Motor Motion Control
- Process/Factory Automation
- Communication Modules, Interface Cards
- Sensors
- Hydraulic & Pneumatic Valve Systems
- Operator Interfaces

Key Benefits

- Integrated high-performance 100Mbps Ethernet transceivers
  - Compliant with IEEE 802.3/802.3u (Fast Ethernet)
  - 100BASE-FX support via external fiber transceiver
  - Loop-back modes
  - Automatic polarity detection and correction
  - HP Auto-MDIX
- EtherCAT slave controller
  - Supports 3 FMMUs
  - Supports 4 SyncManagers
  - Distributed clock support allows synchronization with other EtherCAT devices
  - 4K bytes of DPRAM
- 8/16-Bit Host Bus Interface
  - Indexed register or multiplexed bus
  - Allows local host to enter sleep mode until addressed by EtherCAT Master
  - SPI / Quad SPI support
- Digital I/O Mode for optimized system cost
- 3rd port for flexible network configurations
- Comprehensive power management features
  - 3 power-down levels
  - Wake on link status change (energy detect)
  - Magic packet wakeup, Wake on LAN (WoL), wake on broadcast, wake on perfect DA
  - Wakeup indicator event signal
- Power and I/O
  - Integrated power-on reset circuit
  - Latch-up performance exceeds 150mA per EIA/JESD78, Class II
  - JEDEC Class 3A ESD performance
  - Single 3.3V power supply (integrated 1.2V regulator)
- Additional Features
  - Multifunction GPIOs
  - Ability to use low cost 25MHz crystal for reduced BOM
- Packaging
  - Pb-free RoHS compliant 64-pin QFN or 64-pin TQFP-EP
- Available in commercial, industrial, and extended industrial* temp. ranges

*Extended temp. (105ºC) is supported only in the 64-QFN with an external voltage regulator (internal regulator must be disabled) and 2.5V (typ) Ethernet magnetics.

The LAN9252 is available in commercial, industrial, and extended industrial temperature ranges. Figure 2-1 details a typical system application, while Figure 2-2 provides an internal block diagram of the LAN9252.

FIGURE 2-1: SYSTEM BLOCK DIAGRAM

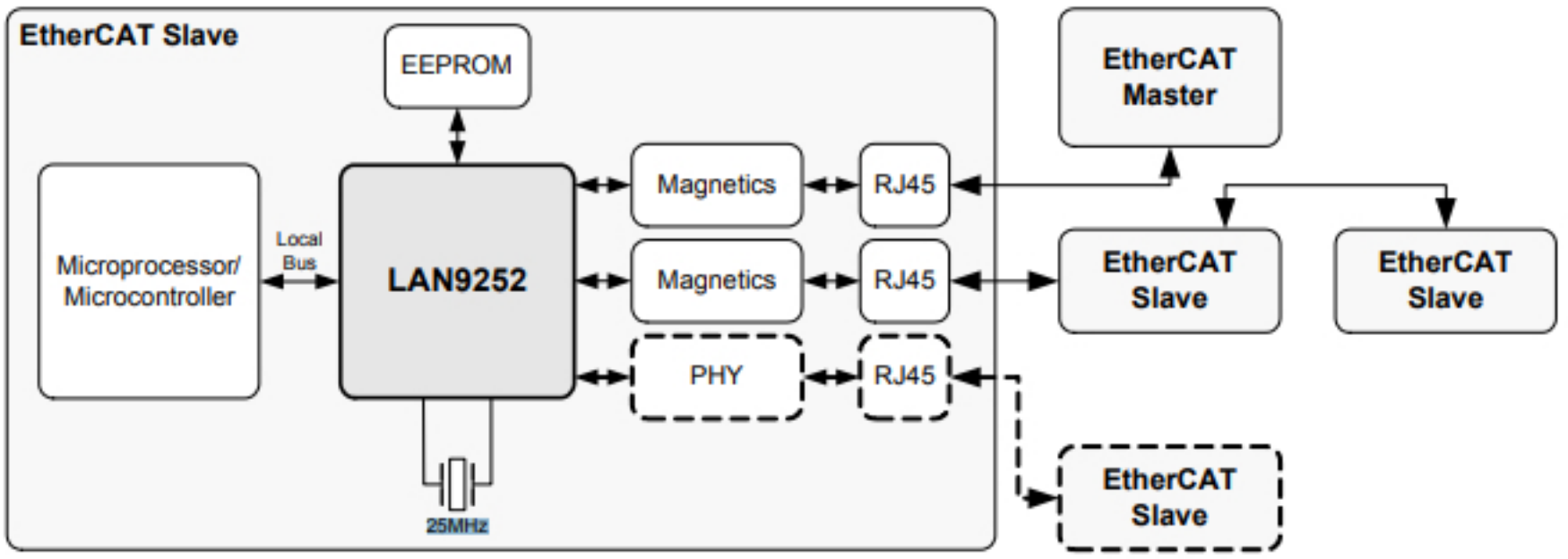
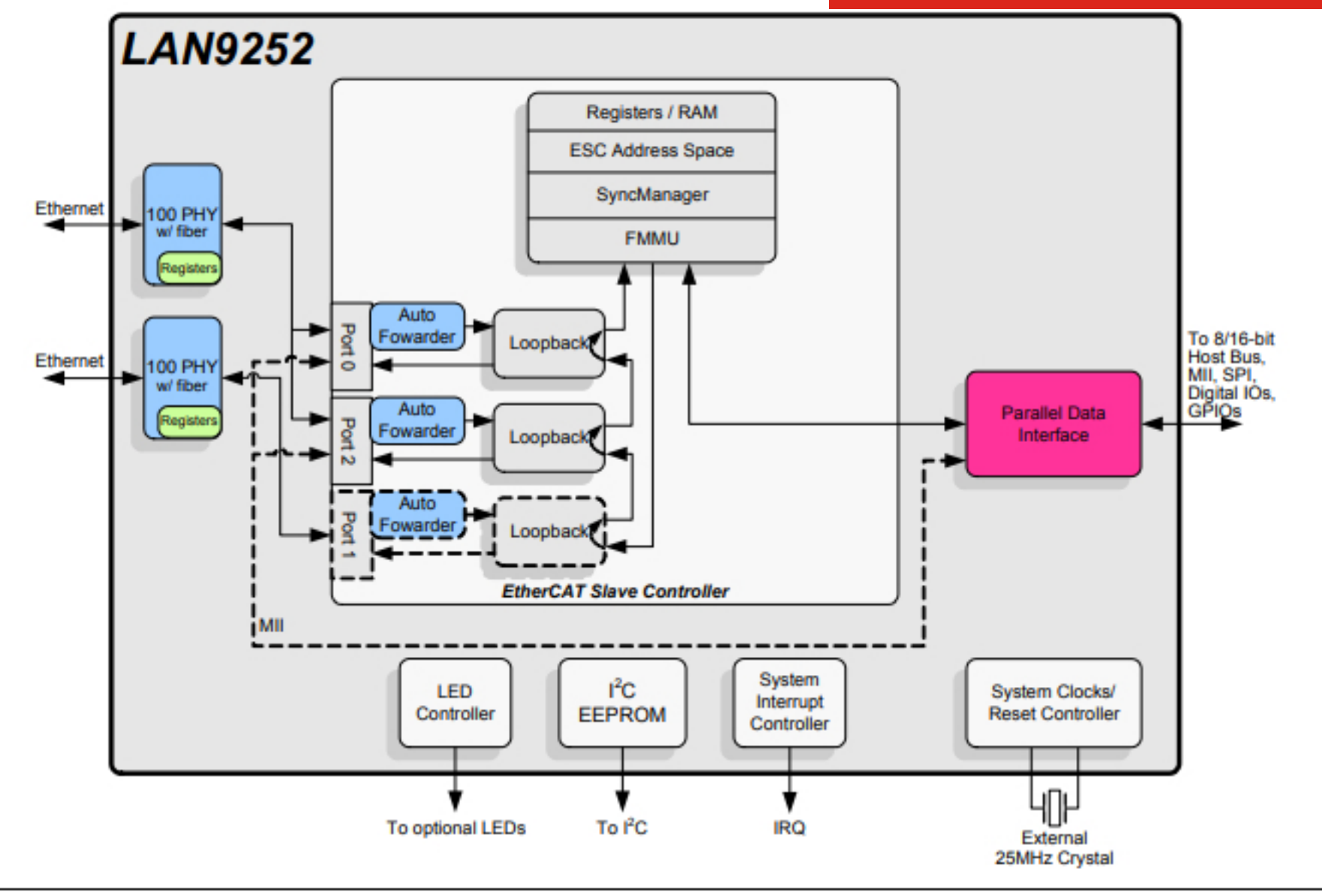


FIGURE 2-2: INTERNAL BLOCK DIAGRAM



The LAN9252 can operate in Microcontroller, Expansion, or Digital I/O mode:

Microcontroller Mode: The LAN9252 communicates with the microcontroller through an SRAM-like slave interface. The simple, yet highly functional host bus interface provides a glue-less connection to most common 8 or 16-bit microprocessors and microcontrollers as well as 32-bit microprocessors with an 8 or 16-bit external bus.

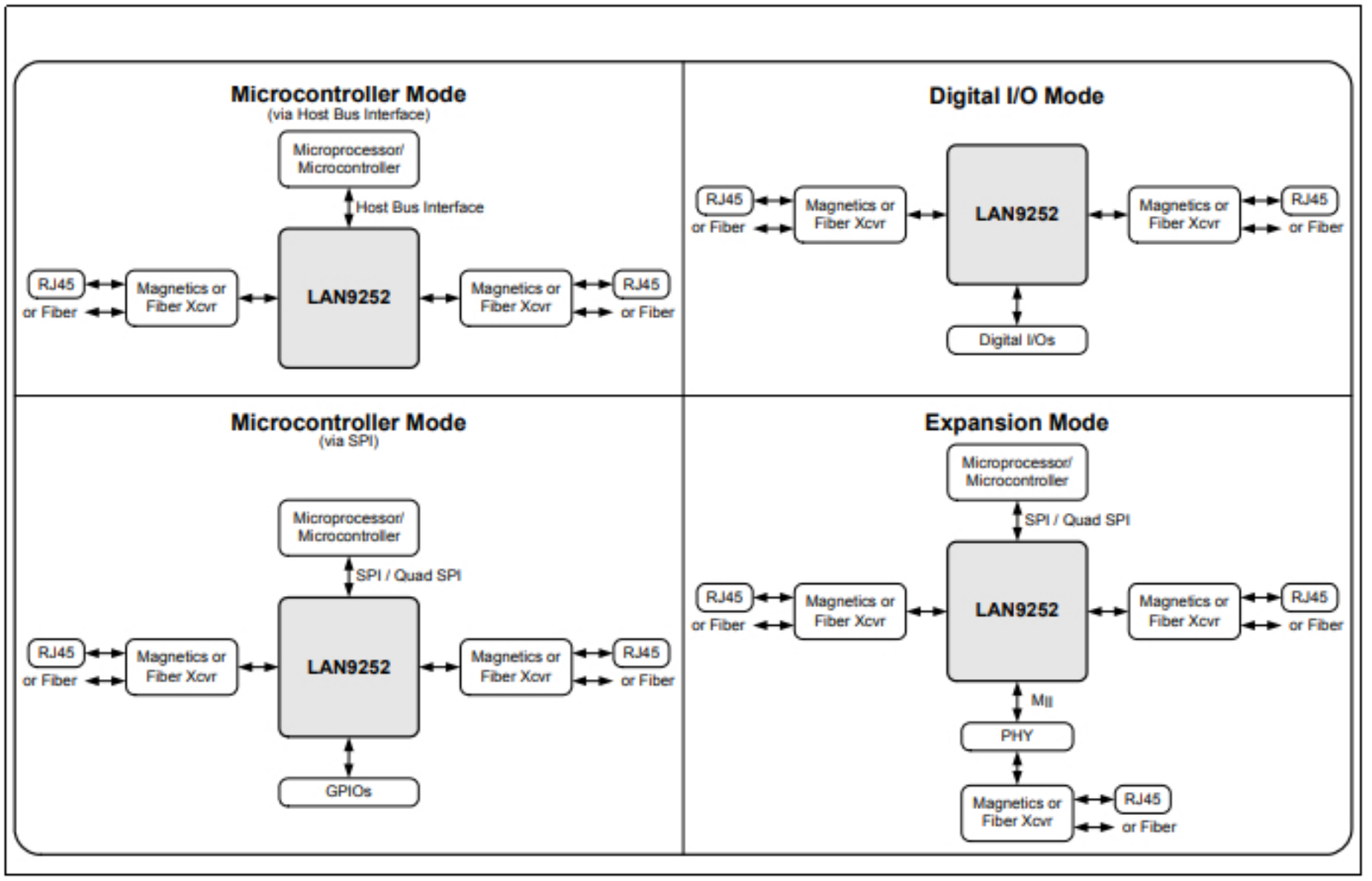
Alternatively, the device can be accessed via SPI or Quad SPI, while also providing up to 16 inputs or outputs for general purpose usage.

Expansion Mode: While the device is in SPI or Quad SPI mode, a third networking port can be enabled to provide an additional MII port. This port can be connected to an external PHY, to enable star or tree network topologies, or to another LAN9252 to create a four port solution. This port can be configured for the upstream or downstream direction.

Digital I/O Mode: For simple digital modules without microcontrollers, the LAN9252 can operate in Digital I/O Mode where 16 digital signals can be controlled or monitored by the EtherCAT master. Six control signals are also provided.

Figure 2-3 provides a system level overview of each mode of operation.

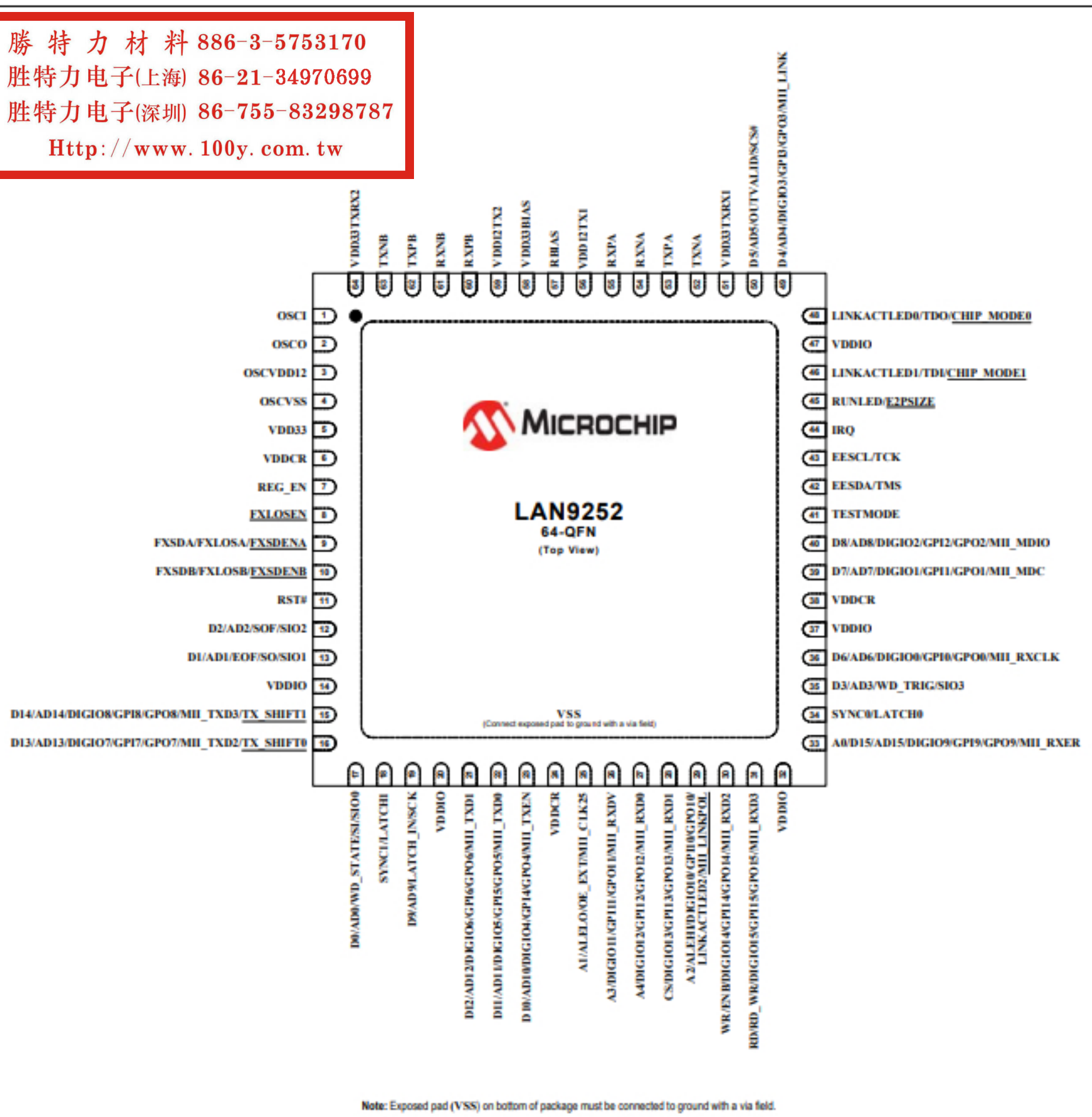
FIGURE 2-3: MODES OF OPERATION



3.0 PIN DESCRIPTIONS AND CONFIGURATION

3.1 64-QFN Pin Assignments

FIGURE 3-1: 64-QFN PIN ASSIGNMENTS (TOP VIEW)



Note: Exposed pad (VSS) on bottom of package must be connected to ground with a via field.

Note: When a "#" is used at the end of the signal name, it indicates that the signal is active low. For example, **RST#** indicates that the reset signal is active low.

The buffer type for each signal is indicated in the "Buffer Type" column of the pin description tables in Section 3.3, "Pin Descriptions". A description of the buffer types is provided in Section 1.2, "Buffer Types".