STMIPID02

Dual mode MIPI CSI-2 / SMIA CCP2 de-serializer

Features

- Dual mode camera de-serializer
- MIPI CSI-2 receivers (Rev.0.9 compliant)
  - Two camera interfaces support
  - One 1.6Gbps dual data lane receiver for main camera with selectable 1/2 lane operation
  - One 800Mbps single data lane receiver for second camera
  - Each MIPI D-PHY interface with a 400MHz DDR clock lane
  - MIPI D-PHY Pass through mode
- SMIA CCP2 receivers
  - Two camera interfaces support
  - 650Mbps class 2 receivers with selectable data/clock and data/strobe operation
- Support for MIPI CSI-2 and SMIA CCP2 RAW6, RAW7, RAW8 (Generic), RAW10 and RAW12 Raw Bayer format data unpacking
- Support for YUV, RGB and JPEG formats
- Support for SMIA 8-10, 7-10, 6-10, 8-12, 7-12 & 6-12 DPCM/PCM decompression options
- 1V8, 200MHz,12-bit parallel output interface
- HSYNC, VSYNC and continuous PCLK output data qualification signal
- Tristate-able output for dual camera systems
- Error interrupt output (D-PHY and protocol)
- MIPI CSI-2 short packet interrupt output
- 2-wires 100/400 kHz control interface (I2C compatible slave) to configure D-PHY timeouts and pixel data unpacking/decompression options
- Integrated power-on-reset cell
- Digital power supply: 1.7V to 1.9V
- Integrated 1.2V regulator for D-PHY and core logic
- VFBGA 49pin 3.0mm x 3.0mm x1.0mm F7x7 0.4mm pitch, 0.25mm ball package
- Lead-free RoHS compliant product

Description

The STMIPID02 is a dual mode MIPI CSI-2 / SMIA CCP2 de-serializer targeted at mobile camera phone applications. Manufactured using ST 65nm process, it integrates two MIPI CSI-2 / SMIA CCP2 receivers. The STMIPID02 can then support the main and the second cameras of a mobile camera phone.

One of the two MIPI CSI-2 receivers is a dual lane receiver allowing to connect high resolution / high frame rate cameras.

The SMIA CCP2 compatible receivers share the same input pins as the MIPI CSI-2 receivers.

STMIPID02's 12-bit parallel output interface is capable of outputting de-serialized pixel data at rates up to 200MHz.

Pass through mode allows STMIPID02 to be used as a standalone MIPI D-PHY physical layer device.

With this device an host with a standard 8-bit, 10-bit or 12-bit parallel input interface can be connected to camera modules with either a MIPI CSI-2 or a SMIA CCP2 low voltage, fully differential bit-serial, low EMI interface.

An interrupt output for every MIPI CSI-2 short packet.

Power management is simplified by the presence of an integrated 1.2V regulator to supply the MIPI D-PHY receiver and core logic.

STMIPID02 is fully configurable via an I2C compatible slave control I/F.

1 Block diagrams

Figure 1. Block diagram

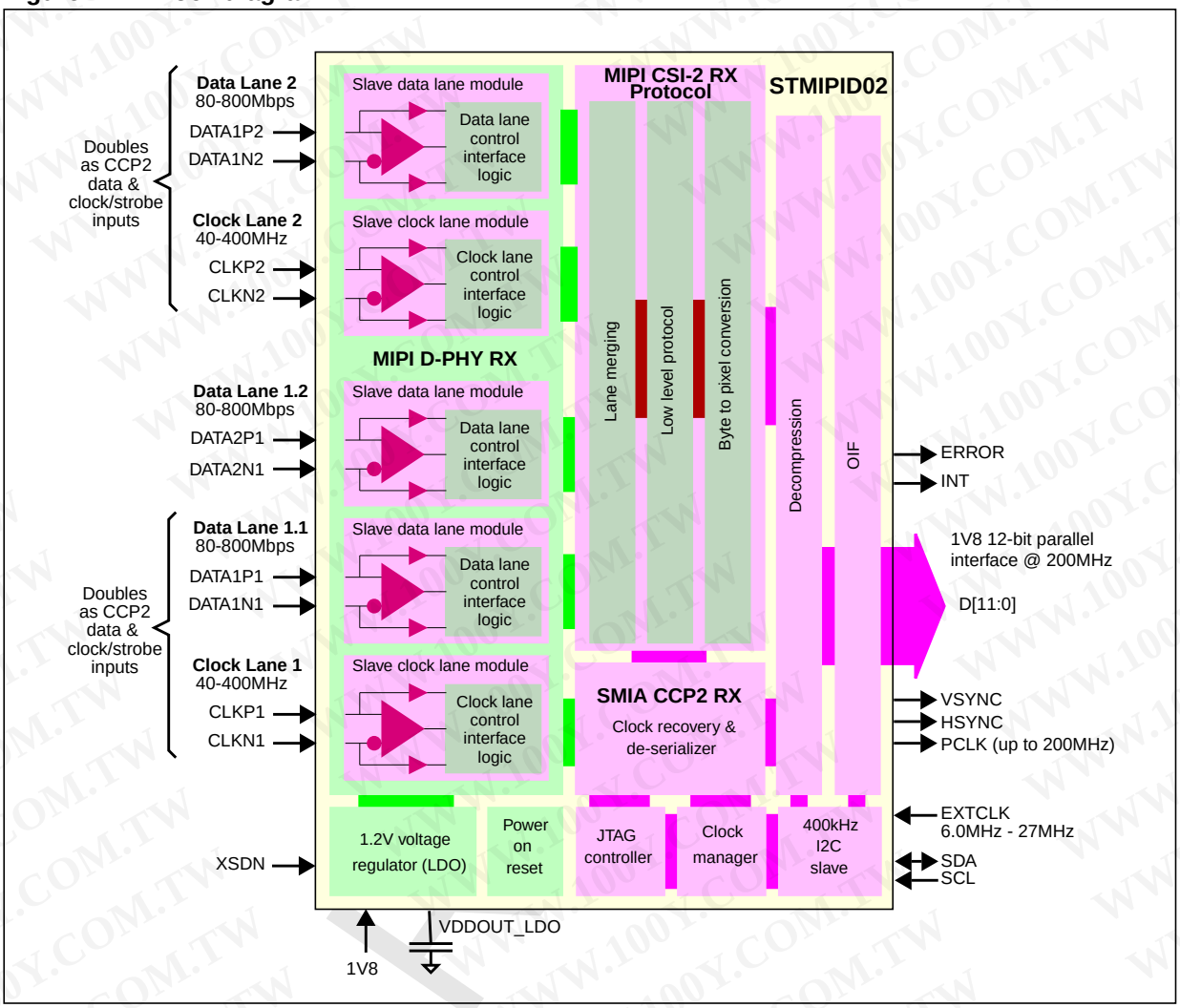


Figure 2. MIPI CSI-2 application diagram

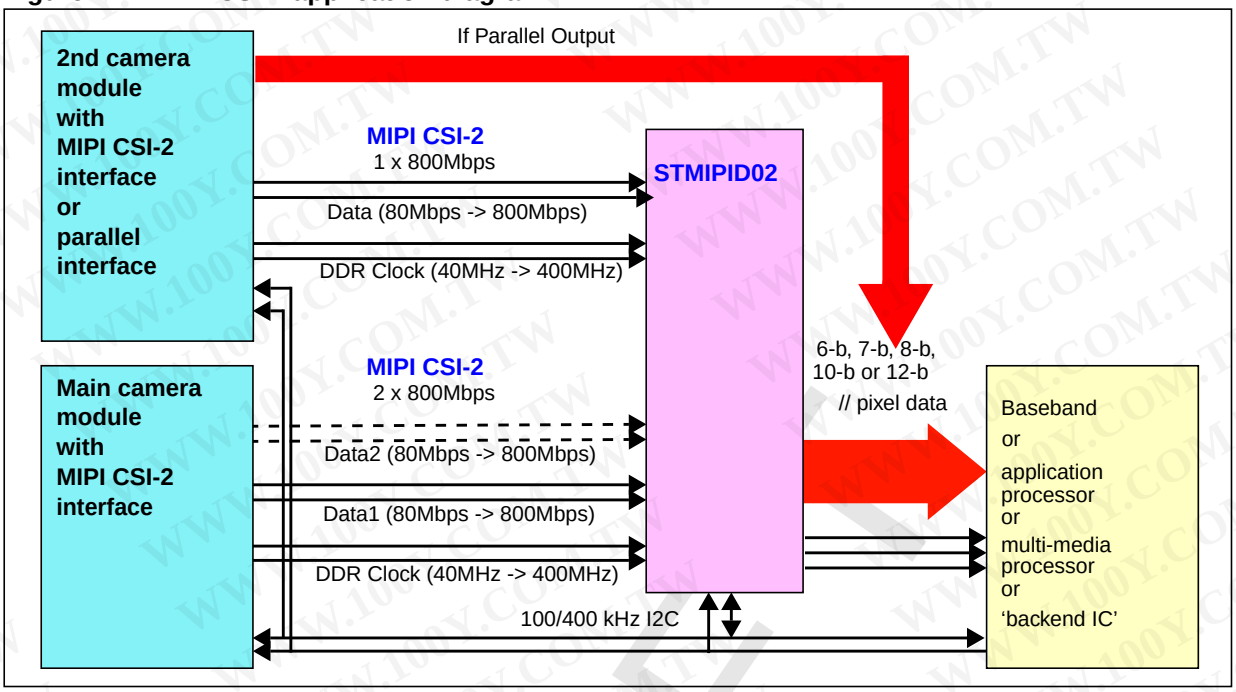
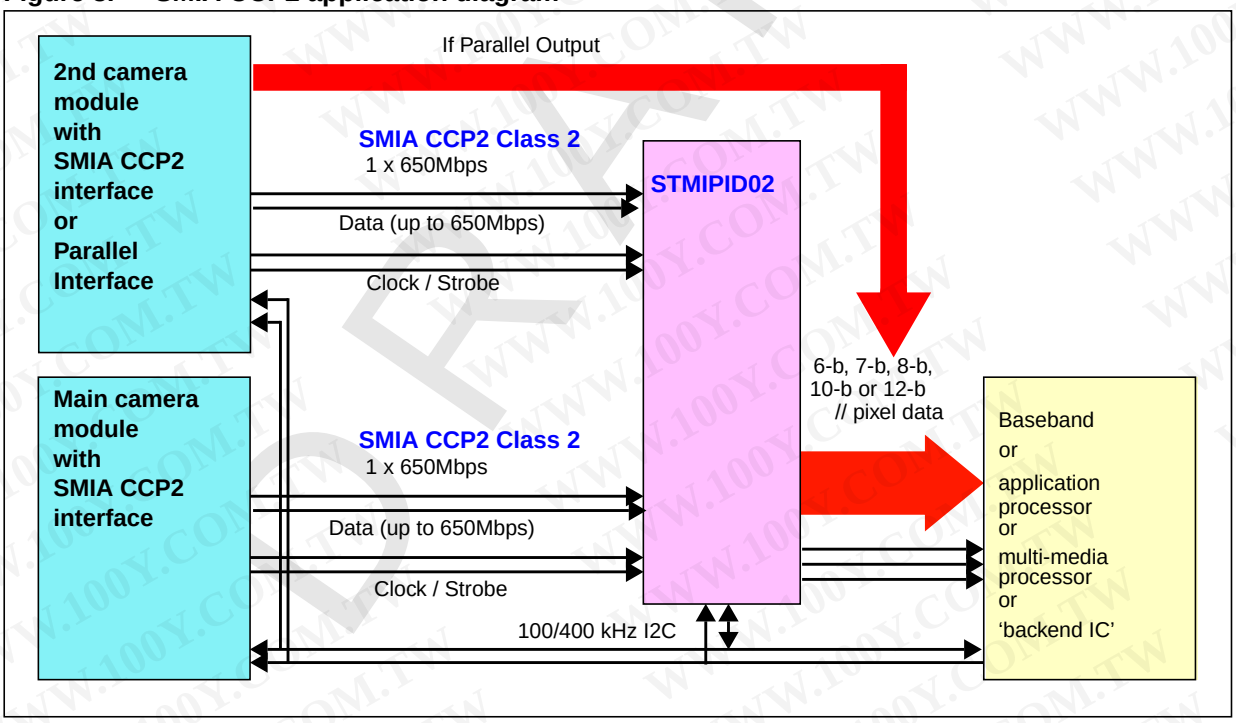


Figure 3. SMIA CCP2 application diagram



2 Output video port

Features

- 1V8, 12-bit parallel video output port
- Up to 200MHz output pixel rate
- Separate horizontal and vertical synchronization outputs
- Fully programmable synchronization signals – both position and polarity
- Tri-state output control allows multiple camera systems. Port disabled upon reset.

HSYNC and VSYNC output polarities are programmable. The description and the figures below assume the default (reset) positions and polarity.

The host uses rising edge of PCLK to sample both the data and the synchronization lanes.

By default VSYNC envelopes all lines of valid image data.

HSYNC is active on all lines including during the vertical frame blanking period.

Since the output data bus is 12 bits wide and we may have output stream with less than 12 bits per pixels (i.e. RAW6/7/8/10) the data can be placed on lower bits of the bus or upper bits of the bus.

This is controlled by Mode_Reg1[7] (address 0x14).

Figure 4. Data Types for different data formats supported between our Tx and Rx

Data Type (also as per register inside Rx)	As supported inside Rx registers	Parallel Output bits
RAW6	RAW6	6bits at output I/f
RAW7	RAW7	7bits output I/f
RAW8	RAW8	8bits output I/f
RAW10	RAW10	10bits output I/f
RAW12	RAW12	12bits output I/f
RAW10 (as 10-6 compressed)	RAW6 (with decompression 6-10 enabled)	10bits output I/f
RAW10 (as 10-7)	RAW7	10bits output I/f
RAW10 (as 10-8)	RAW8	10bits output I/f
RAW12 (as 12-8)	RAW8	12bits output I/f
RGB565	RAW8	Implies 8bits output
RGB888	RAW8	Implies 8bits output
RGB444	RAW8	Implies 8bits output
YUV420 8bits	RAW8	8bits output I/f
YUV422 8bits	RAW8	8bits output I/f
YUV420 10bits	RAW10	10bits output I/f
YUV422 10bits	RAW10	10bits output I/f
Legacy YUV420 8bits	RAW8	8bits output I/f
JPEG	RAW8	8bits output I/f

Figure 5. 12-bit parallel data interface signals - Frame level

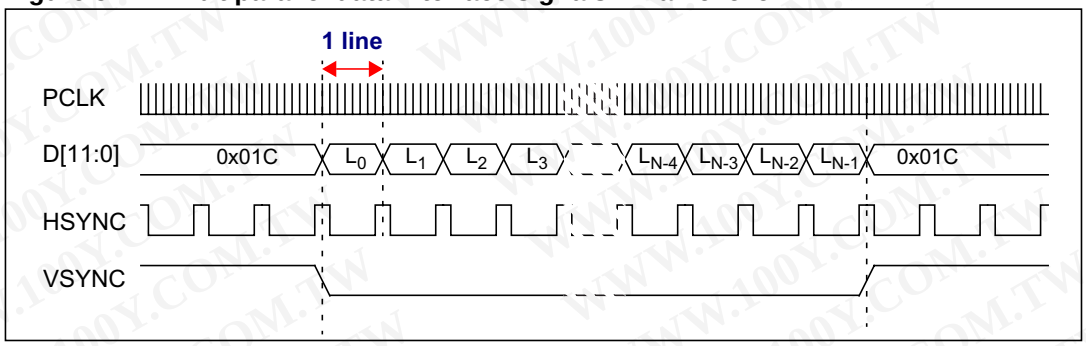
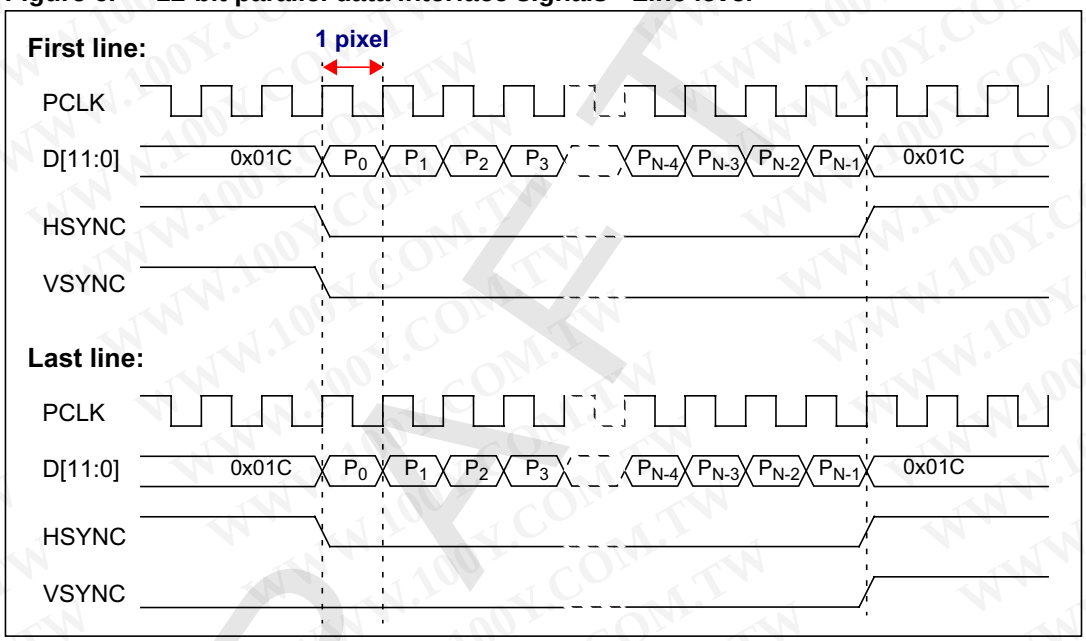
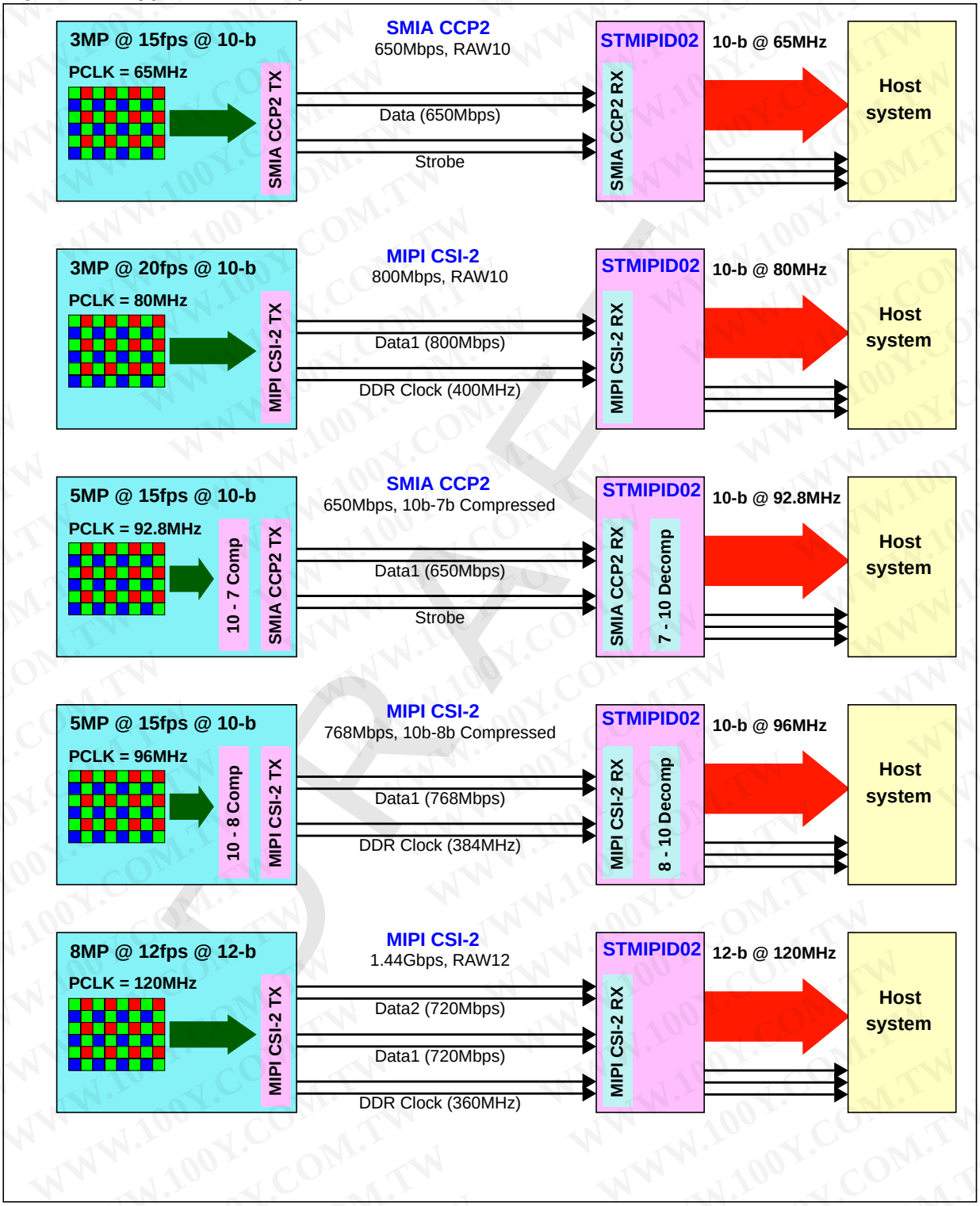


Figure 6. 12-bit parallel data interface signals - Line level



3 Application examples

Figure 7. Application examples



4 Key Technical specifications

Table 1. Technical specifications

Technology	ST 65nm CMOS
Pixel format (s)	SMIA: RAW6, RAW7, RAW8, RAW10 & RAW12 SMIA: 8-10, 7-10, 6-10, 8-12, 7-12, 6-12 DPCM/PCM decompression MIPI CSI-2: RAW6, RAW7, RAW8, RAW10 & RAW12 YUV, RGB, JPEG
Input video interface(s)	MIPI CSI-2 Interface (2x800Mbps + 1x800Mbps) SMIA CCP2 Interface (1x208Mbps Class 0 + 1x650 Mbps - Class 2)
Output video interface(s)	1V8, 200MHz, 12-bit Parallel Interface + VSYNC, HSYNC & PCLK
Control interface	100 / 400 kHz I2C
Clock input	6.0 MHz to 27 MHz
Supply voltage	Digital IO: 1.7 V - 1.9 V
Power consumption	TBC
Package type	VFBGA 3 x 3 x 1mm 49 pin F7x7 pitch 0.4mm Ball 0.25mm
Package size	3.0mm x 3.0mm x 1.0mm (wlh)
Device address	0x28

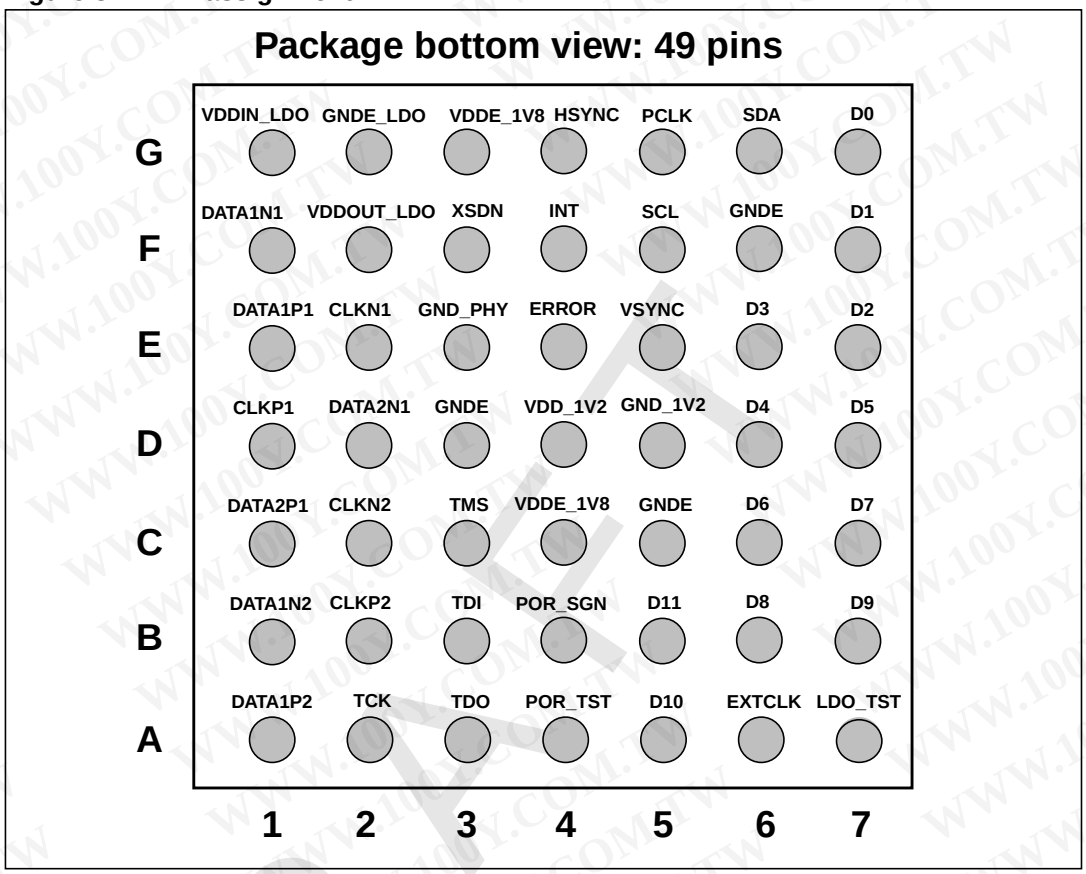
5 References

For details of the interface standards referenced in this data brief please refer to the links below

- Approved Draft of MIPI Camera Serial Interface Version 2 (CSI-2)
- Available from the Camera Working Group area of http://www.mipi.org
- Approved Draft of MIPI Source Synchronous Physical Layer Specification (D-PHY)
- Available from the PHY Working Group area of http://www.mipi.org
- SMIA1.0 Part 1: Functional Specification
- Available from http://www.smia-forum.org
- SMIA 1.0 Part 2: CCP2 Specification
- Available from http://www.smia-forum.org

6 Pin assignment

Figure 8. Pin assignment



Note: 1 The CSI-2 Clock lanes must be in the middle of the 2 data lanes

2 The PCLK, HSYNC, VSYNC must be routed in the middle of the output data bus for skew management reasons

7 Pin description

Table 2. Pin description

Pin name	Type	Description
Power supplies		
VDDE_1V8	Power	1V8 digital IO supply
VDDIN_LDO	Power	1V8 voltage regulator supply
VDD_1V2	Power	1V2 MIPI D-PHY and digital core supply
GNDE	Ground	Digital IO ground
GNDE_LDO	Ground	Voltage regulator ground
GND_PHY	Ground	D-PHY ground
GND_1V2	Ground	Digital core ground
System interface		
EXTCLK	Input	System clock input (for I2C slave) 6.0MHz - 27.0MHz
ERROR	Output	Error interrupt Indicates that an error (either D-PHY or protocol) has occurred
INT	Output	MIPI CSI-2 short packet received interrupt Indicates that a short packet has been received
XSDN	Input	Chip shutdown
Control interface		
SCL	Input	Host I2Cclock
SDA	BiDir	Host I2C data
Dual lane Input data interface		
CLKP1 CLKN1	Input	MIPI CSI-2 receiver 1 DDR clock input MIPI D-PHY physical layer Doubles as CCP2 strobe/clock input in SMIA CCP2 Class 2 mode
DATA1P1 DATA1N1	Input	MIPI CSI-2 receiver 1 data lane 1 MIPI D-PHY physical layer Doubles as CCP2 data input in SMIA CCP2 Class 2 mode
DATA2P1 DATA2N1	Input	MIPI CSI-2 receiver 1 data lane 2 MIPI D-PHY physical layer
Single lane Input data interface		
CLKP2 CLKN2	Input	MIPI CSI-2 receiver 2 DDR clock input MIPI D-PHY physical layer Doubles as CCP2 clock input in SMIA CCP2 Class 0 mode

Table 2. Pin description (continued)

Pin name	Type	Description
DATA1P2 DATA1N2	Input	MIPI CSI-2 receiver 2data lane MIPI D-PHY physical layer Doubles as CCP2 data input in SMIA CCP2 Class 0 mode
Output data interface		
D[11:0]	Output	Parallel video 12-bit data output
PCLK	Output	Pixel clock: PCLK rising edge is used to sample D[11:0], HSYNC & VSYNC. PCLK polarity is programmable
HSYNC	Output	Horizontal synchronization: HSYNC is high during active video, low during the horizontal blanking periods. HSYNC polarity is programmable
VSYNC	Output	Vertical synchronization: VSYNC is high during active video, low during the vertical blanking periods. VSYNC polarity is programmable
Power on reset		
POR_SGN	BiDir	Power on reset signal
POR_TST	Input	Power on reset test signal Should be set to ground for internal POR
Voltage regulator		
VDDOUT_LDO	Power	LDO 1.2V output
Test Interface (ST internal use)		
LDO_TST	Input	LDO regulator test mode
TDI	Input	Test data input
TMS	Input	Test mode
TCK	Input	Test clock
TDO	Output	Test data out

8 Functional Description

8.1 Power-up sequence

Please find below the timing of Power up sequence

Figure 9. Power-up sequence

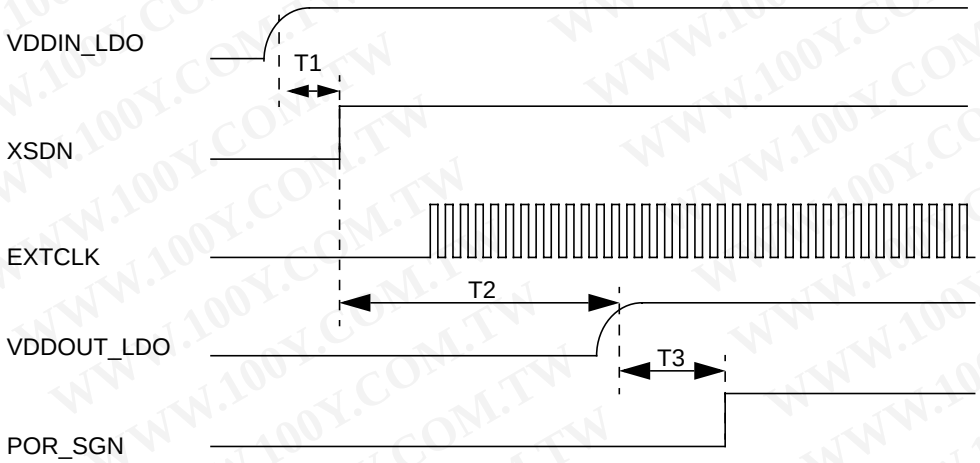


Table 3. Power-up sequence timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	Time between Power-up and LDO enable	VDDIN_LDO stable		+inf	s
T2	Time between XSDN & CORE power up (LDO out rise to 1.2V)			5	ms
T3	Time between CORE power up to 1.2V & reset generation		20		µs

8.2 User modes

8.2.1 Standard modes

Output parallel interface 12 bits of data, HSYNC, VSYNC and PCLK. It is recommended to enable the compensation macro (controlled by Mode_Reg3[5] ,address 0x36) for both standard and bypass modes.

CSI2/CSI2

- Main camera: CSI2 up to 1.6Gbps (with limitation detailed in *Section 8.3: CSI2 limitations*)
- 2nd camera: CSI2 up to 800Mbps

CSI2/CCP2

- Main camera: CSI2 up to 1.6Gbps (with limitation detailed in *Section 8.3: CSI2 limitations*)
- 2nd camera: CCP2 up to 650Mbps

CSI2/ITU-R601

- Main camera: CSI2 up to 1.6Gbps (with limitation detailed in *Section 8.3: CSI2 limitations*)
- 2nd camera: YUV directly connected to baseband parallel interface

8.2.2 Bypass modes

For any activities or applications where only PHY is needed, 8 bits data

CSI2/CSI2

- Main camera: CSI2 up to 1.6Gbps (with limitation detailed in *Section 8.3: CSI2 limitations*)
- 2nd camera: CSI2 up to 800Mbps
-

CSI2/ ITU-R601

- Main camera: CSI2 up to 1.6Gbps (with limitation detailed in *Section 8.3: CSI2 limitations*)
- 2nd camera: YUV directly connected to baseband parallel interface

8.3 CSI2 limitations

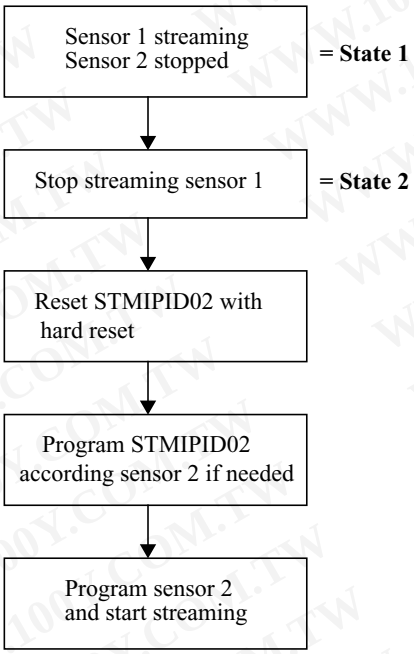
- The bandwidth is limited to 800 Mbps in RAW6/RAW7 dual lane inputs.
- This is irrespective of compression used or not.

8.4 Sensor switching mechanism

The following flow chart explains sensor switching mechanism. If one sensor is streaming & other is not we are in **state1** and if both are not streaming then we are in **state2**.

Both sensors streaming simultaneously while switching is forbidden. We have to be in **state1** or **state2** to switch sensor.

Figure 10. Sensor switching mechanism



8.5 Error signal

This is an accumulated status of all Errors found in the chip. They are as below. The individual status of error can be checked on respective I2C register bit. The status can be cleared by programming Mode_reg2[6] register.

1. All Error status from all D-PHY's
2. Checksum & ECC failures of CSI reception
3. ccp_shift_sync, ccp_false_sync & ccp_crc_error of CCP reception

8.6 INT signal

This is a status showing reception of short packet in CSI stream. User needs to clear the status by programming Clock_control_reg1[5] to observe next short packet. If the user does not clear this bit then he may miss to observe the transition on INT pin when next short packet is observed. The application of short packet interrupt is not envisioned yet.

9 Registers Description

9.1 CLOCK LANE 1 REGISTER

Register Name	Access	Local Address	Description
clk_lane_reg1	R/W	0x02	General and CSI controls of clock lane1 (CLKP1,CLKN1)

Bit No	Bit Name	Default Value	Description
7	ui_x4_clk_lane[5]	0	Unit interval time multiplied by four This signal indicates the bit period in units of 0.25 ns. If the unit interval is 3 ns, twelve (0x0C) should be programmed. This value is used to generate delays. Therefore, if the period is not a multiple of 0.25 ns, the value should be rounded down. For example, a 600 Mbit/s single lane linkuses a unit interval of 1.667 ns. Multiplying by four results in 6.667. In this case, a value of 6 (not 7) should be programmed.
6	ui_x4_clk_lane[4]		
5	ui_x4_clk_lane[3]		
4	ui_x4_clk_lane[2]		
3	ui_x4_clk_lane[1]		
2	ui_x4_clk_lane[0]		
1	swap_pins_clk_lane	0	Swap P and N pins 0= Swap disabled 1= Swap enabled (CLKP1 and CLKN1 are swapped)
0	Enable	0	Enable clock lane module (CLKP1 and CLKN1) 0= Disable clock lane 1 1= Enable clock lane 1

Register Name	Access	Local Address	Description
clk_lane_reg3	R/W	0x04	CCP/CSI controls

Bit No	Bit Name	Default Value	Description
[7:5]	Reserved	000	Reserved
4	hs_rx_term_e_subLVDS_clk_lane	0	High Speed termination enable for CCP mode (unsused in CSI mode) 0= Disable HS termination 1= Enable HS termination, mandatory for CCP mode

3	hs_rx_e_subLVDS_clk_lane	0	High Speed Receiver enable for CCP mode (unsused in CSI mode) 0= Disable HS receiver 1= Enable HS receiver, mandatory for CCP mode
2	hs_rx_wakeup_subLVDS_clk_lane	0	High Speed Receiver wake-up enable for CCP mode 0= HS-receiver in ultra low power mode 1= Enable HS receiver wake-up, mandatory for CCP mode
1	cntrl_mipi_subLVDS_clk_lane	0	Select CSI or CCP mode 0= SMIA CCP 1= MIPI CSI
0	Reserved	0	Reserved

Register Name	Access	Local Address	Description
clk_lane_wr_reg1	RO	0x01	Clock lane status

Bit No	Bit Name	Default Value	Description
[7:2]	Reserved	000000	Reserved
1	ulp_active_not_clk_lane	0	Ultra low-power state active 0= The clock lane is not in ULP state or prepare to leave ULP state 1= The clock lane has reached the ULP state.
0	stop_state_clk_lane	0	Lane in stop state This signal indicates that the lane module is in STOP state.

9.2 DATA LANE 1.1 CONTROLS

Register Name	Access	Local Address	Description
data_lane0_reg1	R/W	0x05	General controls of data lane1.1 (DATA1P1 and DATA1N1)

Bit No	Bit Name	Default Value	Description
[7:2]	Reserved	000000	Reserved
1	Swap_pins_data_lane	0	Swap P and N pins 0= Swap enabled (DATA1P1 and DATA1N1 are swapped) **1= Swap disabled**
0	Enable_data_lane	0	Enable data lane 1.1 (DATA1P1 and DATA1N1) 0= Disable data lane 1.1 1= Enable data lane 1.1

Register Name	Access	Local Address	Description
data_lane0_reg2	R/W	0x06	CCP/CSI controls

Bit No	Bit Name	Default Value	Description
[7:4]	Reserved	0000	Reserved
3	hs_rx_term_e_subLVDS	0	High Speed termination enable for CCP mode (unused in CSI mode) 0= Disable HS termination 1= Enable HS termination, mandatory for CCP mode
2	hs_rx_e_subLVDS	0	High Speed Receiver enable for CCP mode (unused in CSI mode) 0= Disable HS receiver 1= Enable HS receiver, mandatory for CCP mode
1	hs_rx_wakeup_subLVDS_data_lane	0	High Speed Receiver wake-up enable for CCP mode, ultra low power mode for CSI 0= Disable HS receiver wake-up 1= Enable HS receiver wake-up, mandatory for CCP mode

0	cntrl_mipi_subLVDS_data_lane	0	Select CSI or CCP mode 0= SMIA CCP 1= MIPI CSI

Register Name	Access	Local Address	Description
data_lane0_reg3	RO	0x07	CSI controls of data lane 1.1

Bit No	Bit Name	Default Value	Description
[7:2]	Reserved	000000	Reserved
1	ulp_active_not_data_lane	0	Ultra low-power state active 0= The clock lane is not in ULP state or prepare to leave ULP state 1= The clock lane has reached the ULP state.
0	stop_state_data_lane	0	Lane in stop state This signal indicates that the lane module is in STOP state.

Register Name	Access	Local Address	Description
data_lane0_reg4	RO	0x0C	Error status registers

Bit No	Bit Name	Default Value	Description
[7:6]	Reserved	0	Reserved.
5	err_control	0	Unexpected control sequence error This signal is asserted when an incorrect line state sequence is detected. For example, if a turn-around request or escape mode request is immediately followed by a stop state instead of the required bridge state, this signal is asserted and remains high until the next change in line state.
4	err_sync_esc	0	Escape synchronization error If the number of bits received during a low-power data transmission is not a multiple of eight when the transmission ends, this signal is asserted and remains high until the next change in line state.
3	err_esc	0	Error during escape command If an unrecognized escape entry command is received, this signal is asserted and remains high until the next change in line state.

2	err_eot_sync_hs	0	Error during high-speed end of transmission (EoT) If a high-speed transmission ends when the number of bits received during that transmission is not a multiple of eight, this signal is asserted for one cycle of 8*UI.
1	err_sot_sync_hs	0	Synchronization error during high-speed start of transmission (SoT) If the high-speed SoT leader sequence is corrupted in a way that proper synchronization cannot be expected, this error signal is asserted for one cycle of 8*UI.
0	err_sot_hs	0	Error during high-speed start of transmission (SoT) If the high-speed SoT leader sequence is corrupted, but in such a way that proper synchronization can still be achieved, this error signal is asserted for one cycle of 8*UI. This is considered to be a “soft error” in the leader sequence and confidence in the payload data is reduced.

9.3 DATA LANE 1.2 CONTROLS

Register Name	Access	Local Address	Description
data_lane1_reg1	R/W	0x09	General controls of data lane1.2 (DATA2P1,DATA2N1)

Bit No	Bit Name	Default Value	Description
[7:2]	Reserved	000000	Reserved
1	Swap_pins_data_lane	0	Swap P and N pins 0= Swap disabled 1= Swap enabled (DATA2P1 and DATA2N1 are swapped)
0	Enable_data_lane	0	Enable data lane 1.2 (DATA1P1 and DATA1N1) 0= Disable data lane 1.2 1= Enable data lane 1.2

Register Name	Access	Local Address	Description
data_lane1_reg2	R/W	0x0A	CCP/CSI controls

Bit No	Bit Name	Default Value	Description

[7:4]	Reserved	0000	Reserved
3	hs_rx_term_e_subLVDS	0	High Speed termination enable for CCP mode (unsused in CSI mode) 0= Disable HS termination 1= Enable HS termination, mandatory for CCP mode
2	hs_rx_e_subLVDS	0	High Speed Receiver enable for CCP mode (unsused in CSI mode) 0= Disable HS receiver 1= Enable HS receiver, mandatory for CCP mode
1	hs_rx_wakeup_subLVDS_data_lane	0	High Speed Receiver wake-up enable for CCP mode 0= HS-receiver in ultra low power mode 1= Enable HS receiver wake-up, mandatory for CCP mode
0	cntrl_mipi_subLVDS_data_lane	0	Select CSI or CCP mode 0= SMIA CCP 1= MIPI CSI

Register Name	Access	Local Address	Description
data_lane1_reg3	RO	0x0B	CSI controls

Bit No	Bit Name	Default Value	Description
[7:2]	Reserved	000000	Reserved
1	ulp_active_not_data_lane	0	Ultra low-power state active 0= The clock lane is not in ULP state or prepare to leave ULP state 1= The clock lane has reached the ULP state.
0	stop_state_data_lane	0	Lane in stop state This signal indicates that the lane module is in STOP state.

Register Name	Access	Local Address	Description
data_lane1_reg4	RO	0x08	Error status registers

Bit No	Bit Name	Default Value	Description

7	err_contention_lp1	0	Low power contention while trying to drive 1 This signal is asserted high when the lane module is unable to successfully drive a valid one onto one of the interconnect lines during low power transmit mode.
6	err_contention_lp0	0	Low power contention while trying to drive 0 This signal is asserted high when the lane module is unable to successfully drive a valid zero onto one of the interconnect lines during low power transmit
5	err_control	0	Unexpected control sequence error This signal is asserted when an incorrect line state sequence is detected. For example, if a turn-around request or escape mode request is immediately followed by a stop state instead of the required bridge state, this signal is asserted and remains high until the next change in line state.
4	err_sync_esc	0	Escape synchronization error If the number of bits received during a low-power data transmission is not a multiple of eight when the transmission ends, this signal is asserted and remains high until the next change in line state.
3	err_esc	0	Error during escape command If an unrecognized escape entry command is received, this signal is asserted and remains high until the next change in line state.
2	err_eot_sync_hs	0	Error during high-speed end of transmission (EoT) If a high-speed transmission ends when the number of bits received during that transmission is not a multiple of eight, this signal is asserted for one cycle of 8*UI.
1	err_sot_sync_hs	0	Synchronization error during high-speed SoT If the high-speed SoT leader sequence is corrupted in a way that proper synchronization cannot be expected, this error signal is asserted for one cycle of 8xUI.
0	err_sot_hs	0	Error during high-speed start of transmission (SoT) If the high-speed SoT leader sequence is corrupted, but in such a way that proper synchronization can still be achieved, this error signal is asserted for one cycle of 8xUI. This is considered to be a “soft error” in the leader sequence and confidence in the payload data is reduced.

9.4 CLOCK LANE 2 REGISTERS

Register Name	Access	Local Address	Description
clk_lane_reg1_c2	R/W	0x31	General and CSI controls of clock lane1 (CLKP2,CLKN2)

Bit No	Bit Name	Default Value	Description
7	ui_x4_clk_lane[5]	0	Unit interval time multiplied by four This signal indicates the bit period in units of 0.25 ns. If the unit interval is 3 ns, twelve (0x0C) should be programmed. This value is used to generate delays. Therefore, if the period is not a multiple of 0.25 ns, the value should be rounded down. For example, a 600 Mbit/s single lane linkuses a unit interval of 1.667 ns. Multiplying by four results in 6.667. In this case, a value of 6 (not 7) should be programmed.
6	ui_x4_clk_lane[4]		
5	ui_x4_clk_lane[3]		
4	ui_x4_clk_lane[2]		
3	ui_x4_clk_lane[1]		
2	ui_x4_clk_lane[0]		
1	swap_pins_clk_lane	0	Swap P and N pins 0 = Swap enabled (CLKP2 and CLKN2 are swapped) **1= Swap disabled**
0	Enable	0	Enable clock lane module (CLKP1 and CLKN1) 0= Disable clock lane 1 1= Enable clock lane 1

Register Name	Access	Local Address	Description
clk_lane_reg3_c2	R/W	0x33	CCP/CSI controls

Bit No	Bit Name	Default Value	Description
[7:4]	Reserved	0000	Reserved
3	hs_rx_term_e_subLVDS	0	High Speed termination enable for CCP mode (unsused in CSI mode) 0= Disable HS termination 1= Enable HS termination, mandatory for CCP mode

2	hs_rx_e_subLVDS	0	High Speed Receiver enable for CCP mode (unsused in CSI mode) 0= Disable HS receiver 1= Enable HS receiver, mandatory for CCP mode
1	hs_rx_wakeup_subLVDS_data_lane	0	High Speed Receiver wake-up enable for CCP mode 0= HS-receiver into an ultra low power mode 1= Enable HS receiver wake-up, mandatory for CCP mode
0	cntrl_mipi_subLVDS_data_lane	0	Select CSI or CCP mode 0= SMIA CCP 1= MIPI CSI

Register Name	Access	Local Address	Description
clk_lane_wr_reg1_c2	RO	0x3A	CSI control

Bit No	Bit Name	Default Value	Description
[7:2]	Reserved	000000	Reserved
1	ulp_active_not_data_lane	0	Ultra low-power state active 0= The clock lane is not in ULP state or prepare to leave ULP state 1= The clock lane has reached the ULP state.
0	stop_state_data_lane	0	Lane in stop state This signal indicates that the lane module is in STOP state.

9.5 DATA LANE 2 CONTROLS

Register Name	Access	Local Address	Description
data_lane3_reg1	R/W	0x34	General controls of data lane 2 (DATA1P2 and DATA1N2)

Bit No	Bit Name	Default Value	Description
[7:2]	Reserved	000000	Reserved
1	Swap_pins_data_lane	0	Swap P and N pins 0= Swap disabled 1= Swap enabled (DATA1P2 and DATA1N2 are swapped)
0	Enable_data_lane	0	Enable data lane 1.1 (DATA1P2 and DATA1N2) 0= Disable data lane 2 1= Enable data lane 2

Register Name	Access	Local Address	Description
data_lane3_reg2	R/W	0x35	CCP/CSI controls

Bit No	Bit Name	Default Value	Description
[7:4]	Reserved	0000	Reserved
3	hs_rx_term_e_subLVDS	0	High Speed termination enable for CCP mode (unsused in CSI mode) 0= Disable HS termination 1= Enable HS termination, mandatory for CCP mode
2	hs_rx_e_subLVDS	0	High Speed Receiver enable for CCP mode (unsused in CSI mode) 0= Disable HS receiver 1= Enable HS receiver, mandatory for CCP mode
1	hs_rx_wakeup_subLVDS_data_lane	0	High Speed Receiver wake-up enable for CCP mode 0= HS-receiver into an ultra low power mode 1= Enable HS receiver wake-up, mandatory for CCP mode
0	cntrl_mipi_subLVDS_data_lane	0	Select CSI or CCP mode 0= SMIA CCP 1= MIPI CSI

Register Name	Access	Local Address	Description
data_lane3_reg3	RO	0x3A	CSI control

Bit No	Bit Name	Default Value	Description
[7:2]	Reserved	000000	Reserved
1	ulp_active_not_data_lane	0	Ultra low-power state active 0= The clock lane is not in ULP state or prepare to leave ULP state 1= The clock lane has reached the ULP state.
0	stop_state_data_lane	0	Lane in stop state This signal indicates that the lane module is in STOP state.

Register Name	Access	Local Address	Description
data_lane3_reg4	RO	0x3B	Error status registers

Bit No	Bit Name	Default Value	Description
[7:6]	Reserved	0	Reserved
5	err_control	0	Unexpected control sequence error This signal is asserted when an incorrect line state sequence is detected. For example, if a turn-around request or escape mode request is immediately followed by a stop state instead of the required bridge state, this signal is asserted and remains high until the next change in line state.
4	err_sync_esc	0	Escape synchronization error If the number of bits received during a low-power data transmission is not a multiple of eight when the transmission ends, this signal is asserted and remains high until the next change in line state.
3	err_esc	0	Error during escape command If an unrecognized escape entry command is received, this signal is asserted and remains high until the next change in line state.
2	err_eot_sync_hs	0	Error during high-speed end of transmission (EoT) If a high-speed transmission ends when the number of bits received during that transmission is not a multiple of eight, this signal is asserted for one cycle of 8*UI.

1	err_sot_sync_hs	0	Synchronization error during high-speed SoT If the high-speed SoT leader sequence is corrupted in a way that proper synchronization cannot be expected, this error signal is asserted for one cycle of 8*UI.
0	err_sot_hs	0	Error during high-speed start of transmission (SoT) If the high-speed SoT leader sequence is corrupted, but in such a way that proper synchronization can still be achieved, this error signal is asserted for one cycle of 8*UI. This is considered to be a “soft error” in the leader sequence and confidence in the payload data is reduced.

9.6 CCP RX and error flag registers

Register Name	Access	Local Address	Description
ccp_rx_reg1	R/W	0x0D	Data clock/data strobe and Error control

Bit No	Bit Name	Default Value	Description
7	Delay[4]	0	Error Signals (pulses) generated are valid for short duration (4 input DDR clocks). To be able to capture this in I2C registers working on host clock, these Error pulses need to stretched (duration of pulses need to be increased). This pulse stretching is programmable. Delay value is multiplied by 16forf single lane & by 8 forf dual lane. For example: If original pulse width is 4 clocks and Register Value is 3 specifies for dual lane system . The resultant Pulse captured will be 4 (original clocks) + 3 (programmed value) * 8 (dual lane) = 28 clocks
6	Delay[3]		
5	Delay[2]		
4	Delay[1]		
3	Delay[0]		
2	Reserved	0	Reserved
1	Reserved	0	Reserved
0	DS_MODE	0	Selects between Data-Strobe mode and Data-Clock mode for the main camera. DC_MODE=0 -> Data clock mode DS_MODE= 1 -> Data strobe mode

Register Name	Access	Local Address	Description
ccp_rx_reg2	R/W	0x0E	ccp_rx module controls

Bit No	Bit Name	Default Value	Description
7	Reserved	0	Reserved
6	Clr_glue_sync_error	0	Clear sync error in CCP path
5	pix_width_ccp_rx[3]	0	Pixel width input for CCP rx. Selects between the allowed pixel widths: 6, 7, 8, 10 or 12-bit. Value of this register-slice is binary equivalents of 6, 7, 8, 10 or 12 , rest values are invalid
4	pix_width_ccp_rx[2]		
3	pix_width_ccp_rx[1]		
2	pix_width_ccp_rx[0]		

1	clr_ccp_shift_sync	0	Clear CCP shift sync flag
0	clr_ccp_crc_error	0	Clear CCP CRC error

Register Name	Access	Local Address	Description
ccp_rx_reg3	RO	0x0F	CCP channel and error flags

Bit No	Bit Name	Default Value	
7	Glue_logic_sync_error	0	Incorrect data length error flag
6	ccp_channel[3]	0	Channel ID extracted from input CCP stream
5	ccp_channel[2]		
4	ccp_channel[1]		
3	ccp_channel[0]		
2	ccp_shift_sync	0	CCP shift sync error flag
1	ccp_false_sync	0	CCP false sync error flag
0	ccp_crc_error	0	CCP CRC error flag

Register Name	Access	Local Address	Description
ccp_rx_reg1_c2	R/W	0x38	Data clock / data strobe selection for the second camera (CLKP2,CLKN2,DATA1P2,DATA1N2)

Bit No	Bit Name	Default Value	Description
[7:1]	Reserved	0000000	Reserved
0	DS MODE	0	Selects between Data-Strobe mode and Data-Clock mode for the second camera. DC MODE=0 -> Data clock mode DS MODE= 1 -> Data strobe mode

9.7 Mode control Registers

Register Name	Access	Local Address	Description
Mode_reg1	R/W	0x14	Chip mode controls

Bit No	Bit Name	Default Value	Description
7	Justification control	0	Data Justification on output Data 0= right justified (data on lower bits of bus) 1= left justified (Data on upper bits) In bypass mode, this control is invalid
6	Bypass_mode[0]	0	1= No bypass 0= Bypass pixel generation & decompression
5	Decompression[2]	0	000 = decompression disabled 001 = 6-10 010 = 7-10 011 = 8-10 100 = 8-12 101= 10-12 110 = 6-12 111 = 7-12
4	Decompression[1]		
3	Decompression[0]		
2	Lane_ctrl[1]	0	Swap data lanes 1.1 and 1.2 0= No swap, Lane1 is lane1 & lane2 is lane2 1=Lanes are swapped, Lane1 becomes lane2 & lane2 becomes lane1
1	Lane_ctrl[0]	0	0= 1-lane system 1= 2-lane system
0	Ccp/csi	0	Input selector control 0= CSI2 input stream 1= CCP input stream

Register Name	Access	Local Address	Description
Mode_reg2	R/W	0x15	Output Interface controls

Bit No	Bit Name	Default Value	Description
7	Tristate_output	0	Control to select PI in output or tristate mode 0 = Tristated output 1 = Normal output
6	Clear_Error_Signal	0	Control to reset the error flag output 0 = Reset the Error flag 1 = Do not reset keep value as it is
5	Error_signal_polarity	0	Polarity for Error signal 0 = Non Inverted 1 = Inverted
4	Clock_gating control	0	Continuous or gated clock control 0 = continuous clock 1 = clock gated
3	Output_polarity_clk	0	Polarity control of PCLK signal 0= Non Inverted 1= Inverted
2	Output_polarity_vsync	0	Polarity control of VSYNC signal 0= Non Inverted 1= Inverted
1	Output_polarity_hsync	0	Polarity control of HSYNC signal 0= Non Inverted 1= Inverted
0	Interrupt_polarity	0	Polarity for Interrupt signal 0 = Non Inverted 1 = Inverted

Register Name	Access	Local Address	Description
Mode_reg3	R/W	0x36	Output Interface controls

Bit No	Bit Name	Default Value	Description
[7:6]	Reserved	0	Reserved
5	i2c_comp_leakage	0	Enable compensation macro 0 = Disable IO compensation macro (push in IDDQ mode) 1= Enable IO compensation macro (MANDATORY to push to normal mode)
4	Reserved	0	Reserved
3	Spec_90_81_b_c2	0	For the second camera (CLKP2,CLKN2,DATA1P2,DATA1N2) 0 = 0.90Rev MIPI D-PHY Spec 1= 0.81Rev MIPI D-PHY Spec
2	Spec_90_81_b_c1	0	For the main camera (CLKP1,CLKN1,DATA1P1,DATA1N1,DATA2P1,DATA2N1) 0 = 0.90Rev MIPI D-PHY Spec 1= 0.81Rev MIPI D-PHY Spec
1	Reserved	0	Reserved
0	Camera_select	0	Camera selection 0= Main camera (CLKP1,CLKN1,DATA1P1,DATA1N1,DATA2P1,DATA2N1) 1= Second camera (CLKP2,CLKN2,DATA1P2,DATA1N2)

9.8 Clock Control Registers

Register Name	Access	Local Address	Description
Clock_control_reg1	R/W	0x16	Clear for INT & ERR

Bit No	Bit Name	Default Value	Description
[7:6]	Reserved	00	Reserved
5	Clr_csi2_interrupt	0	I2C control to clear csi2 interrupt
4	Clr_csi2_error	0	I2C control to clear csi2 error. It stops streaming data till this bit is reseted.
[3:0]	Reserved	0	Reserved

9.9 System Error Registers

Register Name	Access	Local Address	Description
Error_regs	RO	0x10	Error output registers

Bit No	Bit Name	Default Value	Description
[7:2]	Reserved	000000	Reserved
1	Checksum_failed	0	Checksum failure status in Low level protocol 0 = OK 1 = Failed
0	ECC_failed	0	ECC in low level protocol status 0 = OK 1 = Failed

9.10 Data Pipe Information

Register Name	Access	Local Address	Description
Data_ID_Wreg	RO	0x11	Data type Write registers. Refers to data type in Low Level Protocol. See CSI2 Specification for detailed explanation. 2 MSB for Virtual Channel number.

Register Name	Access	Local Address	Description
Data_ID_Rreg	R/W	0x17	Data type in Low Level Protocol See CSI2 Specification for explanation 2 MSB for Virtual Channel. Not to be used as a separate register is used for the same. Remaining 6 bits used for data type

Register Name	Access	Local Address	Description
Data_ID_Rreg_emb	R/W	0x18	Data type in Low Level Protocol See CSI2 Specification for detiled explaination for nonimage data. 2 MSB for Virtual Channel Not to be used as a separate register is used for the same. Remaining 6 bits used for data type

Protocol layer can be programmed to use data Type from these register list or from embedded data type information in data stream

Register Name	Access	Local Address	Description
Data_selection_ctrl	R/W	0x19	Virtual channel, Datatype selection and pixel width control register

Bit No	Bit Name	Default Value	Description
[7:4]	Reserved	0000	Reserved
3	Pixel width selection	0	Selection of pixel width 1 = Pixel width from I2C reg Pix_width_ctrl 0 = Pixel width extracted from data type decided with Data_selection_ctrl[2]

2	Data type	0	Selection of data type 0 = Data type from embedded short packets (readable in Data_ID_Wreg 0x11) 1 = Data type from I2C programmed register (Data_ID_Rreg)
1	VC[1]	0	Virtual channel, whose data to be retrieved and used in subsequent steps. Data for other channel is to be discarded
0	VC[0]		

Register Name	Access	Local Address	Description
Frame_no_lsb	RO	0x12	Frame numer LSByte from Frame sync short packet for CSI2 mode

Bit No	Bit Name	Default Value	Description
7	Bit 7	0	Bit 7 of frame number
6	Bit 6	0	Bit 6 of frame number
5	Bit 5	0	Bit 5 of frame number
4	Bit 4	0	Bit 4 of frame number
3	Bit 3	0	Bit 3 of frame number
2	Bit 2	0	Bit 2 of frame number
1	Bit 1	0	Bit1 of frame number
0	Bit 0	0	Bit0 of frame number

Register Name	Access	Local Address	Description
Frame_no_msb	RO	0x13	Frame number MSByte from Frame sync short packet for CSI2 mode

Bit No	Bit Name	Default Value	Description
7	Bit 15	0	Bit 15 of frame number
6	Bit 14	0	Bit 14 of frame number
5	Bit 13	0	Bit 13 of frame number
4	Bit 12	0	Bit 12 of frame number
3	Bit 11	0	Bit 11 of frame number

2	Bit10	0	Bit 10 of frame number
1	Bit 9	0	Bit 9 of frame number
0	Bit 8	0	Bit 8 of frame number

Register Name	Access	Local Address	Description
Active_line_no_lsb	R/W	0x1B	Number of active lines in image used for decompression (LSB)

Bit No	Bit Name	Default Value	Description
7	Bit 7	0	Bit 7 of active line number
6	Bit 6	0	Bit 6 of active line number
5	Bit 5	0	Bit 5 of active line number
4	Bit 4	0	Bit 4 of active line number
3	Bit 3	0	Bit 3 of active line number
2	Bit 2	0	Bit 2 of active line number
1	Bit 1	0	Bit1 of active line number
0	Bit 0	0	Bit0 of active line number

Register Name	Access	Local Address	Description
Active_line_no _msb	R/W	0x1A	Number of active lines in image used for decompression (MSB)

Bit No	Bit Name	Default Value	Description
7	Bit 15	0	Bit 15 of active line number
6	Bit 14	0	Bit 14 of active line number
5	Bit 13	0	Bit 13 of active line number
4	Bit 12	0	Bit 12 of active line number
3	Bit 11	0	Bit 11 of active line number
2	Bit10	0	Bit 10 of active line number
1	Bit 9	0	Bit9 of active line number
0	Bit 8	0	Bit8 of active line number

Register Name	Access	Local Address	Description
SOF_line_no_lsb	R/W	0x1D	Number of SOF lines in image used for decompression (LSB)

Bit No	Bit Name	Default Value	Description
7	Bit 7	0	Bit 7 of SOF line number
6	Bit 6	0	Bit 6 of SOF line number
5	Bit 5	0	Bit 5 of SOF line number
4	Bit 4	0	Bit 4 of SOF line number
3	Bit 3	0	Bit 3 of SOF line number
2	Bit 2	0	Bit 2 of SOF line number
1	Bit 1	0	Bit 1 of SOF line number
0	Bit 0	0	Bit 0 of SOF line number

Register Name	Access	Local Address	Description
SOF_line_no _msb	R/W	0x1C	Number of active lines in image used for decompression (MSB)

Bit No	Bit Name	Default Value	Description
7	Bit 15	0	Bit 15 of SOF line number
6	Bit 14	0	Bit 14 of SOF line number
5	Bit 13	0	Bit 13 of SOF line number
4	Bit 12	0	Bit 12 of SOF line number
3	Bit 11	0	Bit 11 of SOF line number
2	Bit10	0	Bit 10 of SOF line number
1	Bit 9	0	Bit 9 of SOF line number
0	Bit 8	0	Bit 8 of SOF line number

Register Name	Access	Local Address	Description
Pix_width_ctrl	R/W	0x1E	Pixel width control

Bit No	Bit Name	Default Value	Description
7	Reserved	0	
6	Reserved	0	
5	Reserved	0	
4	Dcpx_en for active pixel	0	Decompression enable for active data 0= Decompression OFF 1= Decompression ON
3	Pix_width[3]	0	Pixel width control for active data
2	Pix_width[2]		
1	Pix_width[1]		
0	Pix_width[0]		

Register Name	Access	Local Address	Description
Pix_width_ctrl_emb	R/W	0x1F	No of active lines in image used for decom-pression

Bit No	Bit Name	Default Value	Description
7	Reserved	0	
6	Reserved	0	
5	Reserved	0	
4	Dcp0_en for emb pixel	0	Decompression enable for embeded data 0= Decompression OFF 1= Decompression ON
3	Pix_width_emb[3]	0	Pixel width control for embedded data. This input will be used by STMIPID02 for recognizing the Pixel width in embedded lines of received stream.
2	Pix_width_emb[2]		
1	Pix_width_emb[1]		
0	Pix_width_emb[0]		

Register Name	Access	Local Address	Description

Data_field_LSB	RO	0x21	LSB of ECC corrected data field

Bit No	Bit Name	Default Value	Description
7	Bit 7	0	LSB of ECC corrected data field
6	Bit 6		
5	Bit 5		
4	Bit 4		
3	Bit 3		
2	Bit 2		
1	Bit 1		
0	Bit 0		

Register Name	Access	Local Address	Description
Data_Field_MSB	RO	0x20	MSB of ECC cted data field

Bit No	Bit Name	Default Value	Description
7	Bit 15	0	MSB of ECC corrected data field
6	Bit 14		
5	Bit 13		
4	Bit 12		
3	Bit 11		
2	Bit 10		
1	Bit 9		
0	Bit 8		

10 Electrical Characteristics

10.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DDE_1V8}	Digital I/O supply	-0.5 to +2.8	V
V_{DDIN_LDO}	Voltage regulator supply	-0.5 to +2.8	V
	Voltage on any signal pin	-0.5 to (V_{DD} + 0.5)	V
I_{DD}	Supply current	100	mA
	Current on any signal pin	10	mA
T_{STO}	Storage temperature	-40 to +150	°C
T_{LEAD}	Lead temperature (soldering, 10 s)	+260	°C

Caution: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

10.2 Operating conditions

Table 5. Operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DDE_1V8}	Digital I/O supply	1.7	1.8	1.9	V
V_{DDIN_LDO}	Voltage regulator supply	1.7	1.8	1.9	V
T_A	Ambient temperature	-25		+70	°C
C_{REG}	LDO output load capacitor ESR <1Ω @ 100kHz		1		µF
C_{EXT}	1.2V decoupling capacitor		10		nF

10.3 Thermal data

Table 6. Thermal data

Symbol	Parameter	Value	Unit
Rth(j-a)	Max. junction-ambient thermal resistance - VFBGA49(1)	58.4	°C/W

1. Typical, measured with the component mounted on an evaluation PC board in free air.

10.4 DC electrical characteristics

Over operating conditions unless otherwise specified.

Table 7. I/O electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ	Max.	Unit
V_{IL}	Input low voltage		-0.3		0.3 V_{DD}(1)	V
V_{IH}	Input high voltage		0.7 V_{DD}(1)		V_{DD}(1) + 0.3	V
V_{OL}	Output low voltage	I_{OL} < 2 mA I_{OL} < 3 mA on SDA,			0.2 V_{DD}(1)	V
V_{OH}	Output high voltage	-I_{OH} < 2 mA -I_{OH} < 3 mA on SDA	0.8 V_{DD}(1)			V
I_{IL}/I_{IH}	Input leakage current Input pins I/O pins	$V_{SS} < V_{IN} < V_{DD}$			± 20 ± 10	µA µA
$V_{EXTCLKDC}$	Clock input amplitude, DC	DC coupled square wave	1.5	1.8	2.4	V
$V_{EXTCLKAC}$	Clock input amplitude, AC	AC coupled sine wave	0.5	1	1.2	Vpp
C_{IN}	SCL Input capacitance	T_A = 25° C, freq. = 1 MHz			10	pF
$C_{I/O}$	SDA Input / output capacitance	T_A = 25° C, freq. = 1 MHz			10	pF
C_{IN_MIPI}	Input capacitance (Dat_xP_y, Dat_xN_y, $ClkP_x$, $ClkN_x$)				3 (TBD)	pF
C_{IN_DIG}	Input capacitance			2		pF
C_{OUT_DIG}	Output capacitance			3		pF

1. V_{DD} refers to the supply voltage (VDDE_1V8, VDDIN_LDO) to which the signal is referenced.

Table 8. Power supply specifications for VDDIN_LDO

Symbol	Parameter	Test conditions	Typ.	Max.	Unit
I_{DDPD}	V_{DD} supply current in power-down mode	V_{DD} = max; T_A = 25° C; XSDN < V_{IL}	5	TBD	µA
$I_{DDBYPASS}$	V_{DD} supply current in bypass mode	V_{DD} = max; Image format = RAW8 CSI Dual	25	TBD	mA
$I_{DDNORMAL}$	V_{DD} supply current in normal mode	V_{DD} = max; Image format = RAW8 CCP CSI Single CSI Dual	18 21 25	TBD	mA

Table 9. Power supply specifications for VDDE_1V8

Symbol	Parameter	Test Conditions	Typ.	Max.	Unit
I_{DDPD}	V_{DD} supply current in power-down mode	V_{DD} = max; T_A = 25° C; PDN < V_{IL}	5	TBD	µA
$I_{DDBYPASS}$	V_{DD} supply current in bypass mode	V_{DD} = max; CSI Dual	6	TBD	mA
$I_{DDNORMAL}$	V_{DD} supply current in normal mode	V_{DD} = max; Image format = RAW8 CCP CSI Single CSI Dual	 12 14 30	TBD	mA

Table 10. CCP2 Class 2 receiver electrical characteristics(1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CMI_SMIA}	Input common mode voltage range	Embedded R_{TI}=100Ω±10%	0.65	0.95	1.15	V
V_{IDTH_SMIA}	Input differential threshold (V_P - V_N)	Embedded R_{TI}=100Ω±10%	+/-50		+/-200	mV
t_{PWRUP}/ t_{PWRDN}	Power-up/-down time	Embedded R_{TI}=100Ω±10%			20	µs
R_{TI}	Embedded termination resistance		80	100	125	Ω

1. For further information on CCP2, please refer to the *SMIA 1.0 Part 2: CCP2 Specification*.

Table 11. CSI-2 receiver electrical characteristics(1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit

1. For further information on CSI-2, please refer to the *Approved Draft of MIPI Camera Serial Interface Version 2 (CSI-2)*.

10.5 AC electrical characteristics

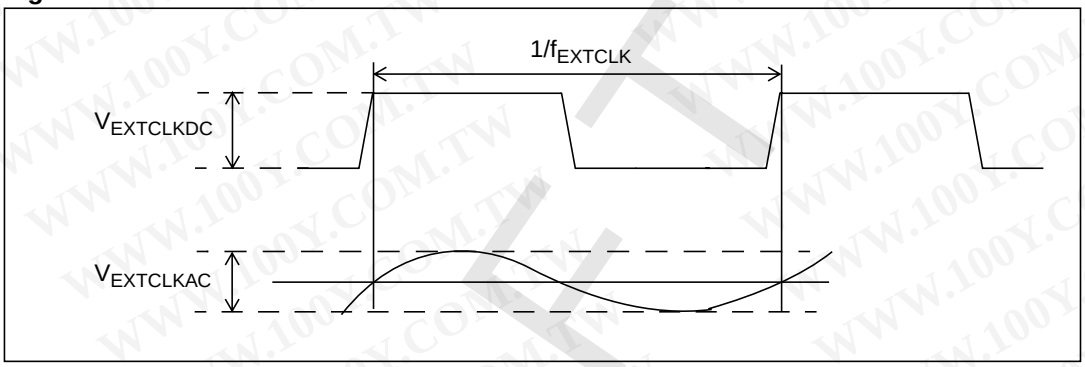
10.5.1 EXTCLK

$V_{EXTCLKAC}$ and $V_{EXTCLKDC}$ are defined in *Table 7: I/O electrical characteristics*.

Table 12. EXTCLK electrical characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{EXTCLK}	Clock frequency input 50% duty cycle - VDDE_1V8 referred	6	13	27	MHz

Figure 11. EXTCLK electrical characteristics



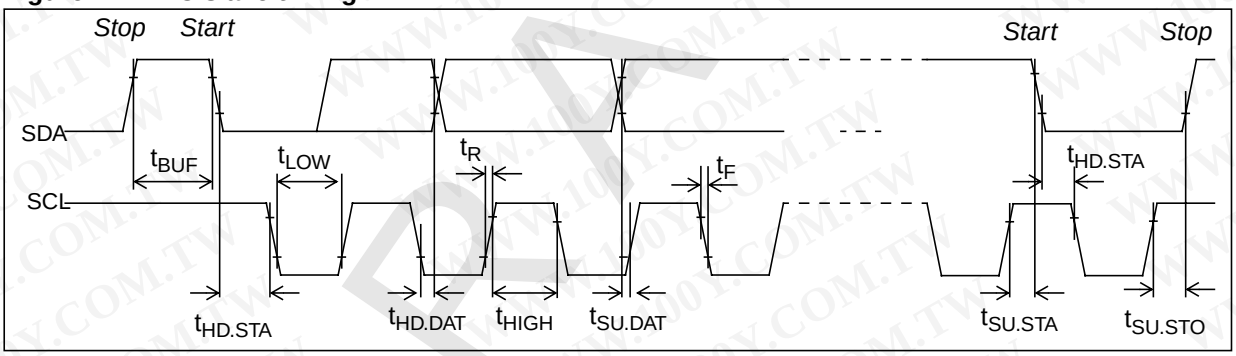
10.5.2 I2C slave timing (SCL, SDA)

Table 13. I2C slave timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{SCL}	SCL clock frequency	100		400	kHz
t_{LOW}	Clock pulse width low	1.3			µs
t_{HIGH}	Clock pulse width high	0.6			µs
t_{BUF}	Bus free time between transmissions	1.3			µs
$t_{HD.STA}$	Start hold time	0.6			µs
$t_{SU.STA}$	Start set-up time	0.6			µs
$t_{HD.DAT}$	Data hold time	0.2		0.9	µs
$t_{SU.DAT}$	Data setup time	100			ns
t_R	SCL / SDA rise time(1)			300	ns
t_F	SCL / SDA fall time(1)			300	ns
$t_{SU.STO}$	Stop setup time	0.6			µs

1. Measured from 0.3 to 0.7 or 0.7 to 0.3 V_{DD}

Figure 12. I2C slave timing



10.5.3 CCP2 serial receiver timing (DATA1P1/N1, CLKP1/N1 & DATA1P2/N2, CLKP2/N2)

Table 14. CCP2 serial receiver data/clock (Class 0) input timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{DS}	Data setup time	1			ns
t_{CKP}	Clock period	4.8			ns

Figure 13. CCP2 data/clock input timing

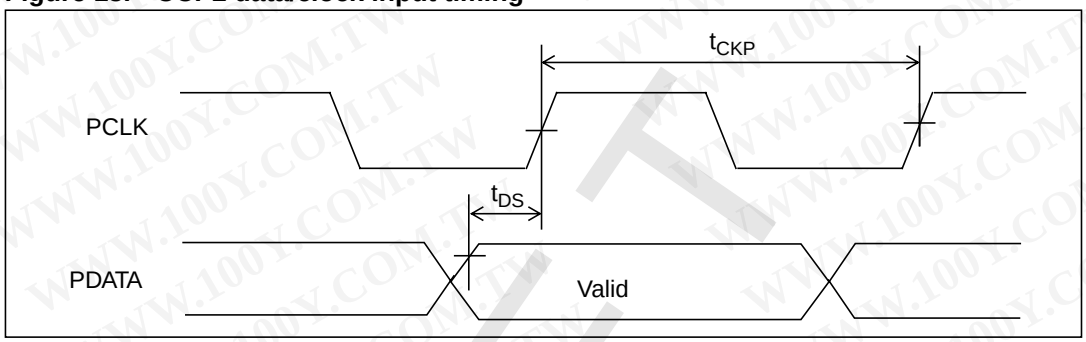
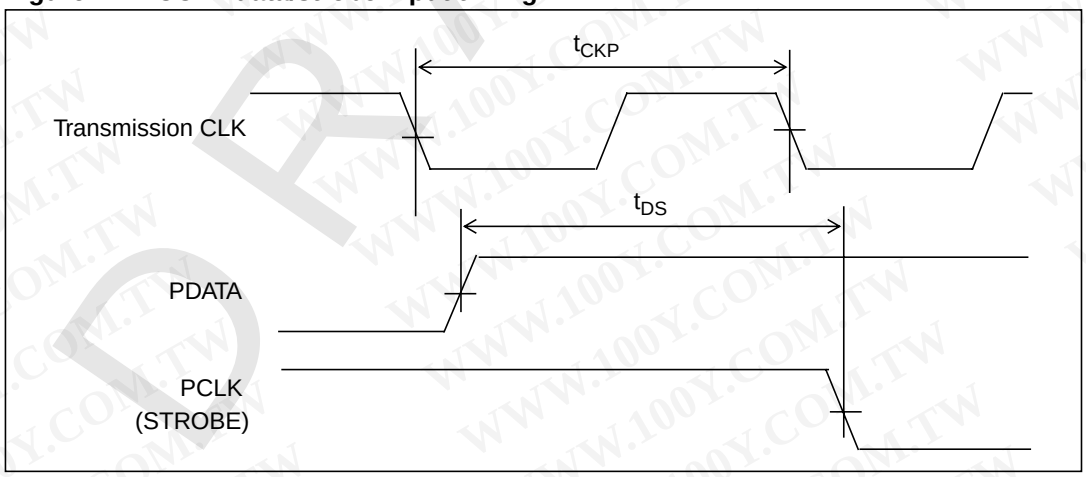


Table 15. CCP2 serial receiver data/strobe (Class 2) input timing

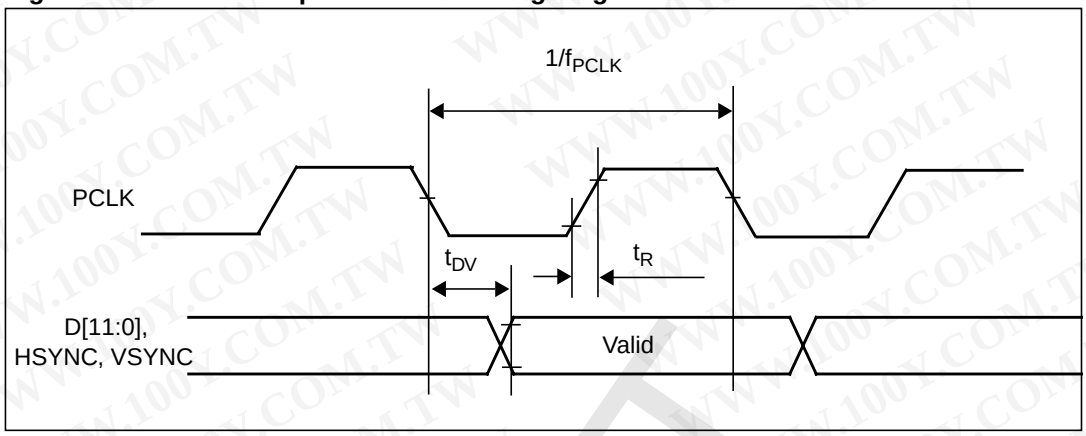
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{DS}	Data to strobe edge setup time	t_{CKP}-780	t_{CKP}	t_{CKP}+780	ps
t_{CKP}	Transmission clock period	1.56			ns

Figure 14. CCP2 data/strobe input timing



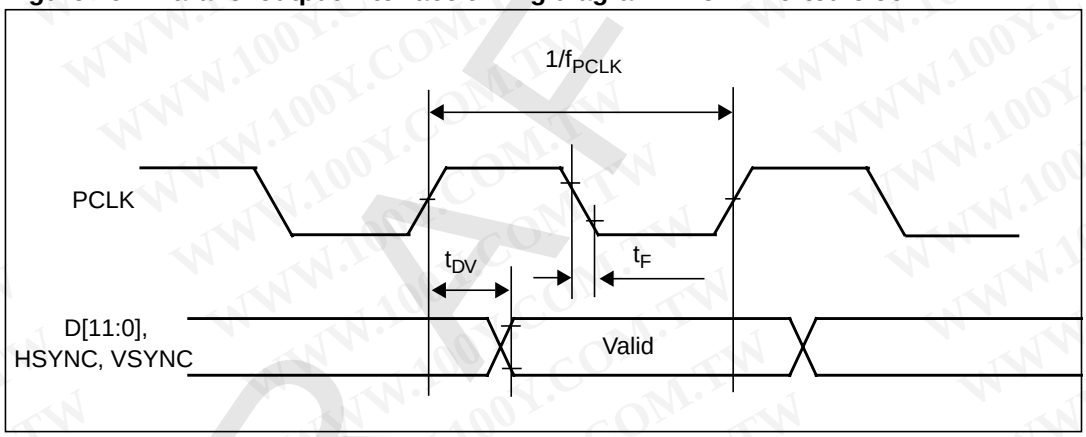
10.5.4 Parallel output interface timing

Figure 15. Parallel output interface timing diagram - Inverted clock



Note: For Inverted clock mode the valid edge to capture is positive (rising) edge.

Figure 16. Parallel output interface timing diagram - Non inverted clock



Note: For Non-Inverted clock mode the valid edge to capture is negative (falling) edge.

For Raw6/Raw7 dual lane, the bandwith is limited to 800Mbps

Table 16. Parallel output interface timing

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
f_{PCLK}	PCLK frequency				200	MHz
D_{PCLK}	PCLK duty cycle	No Bypass: -for RAW6 Dual Lane -for RAW7 Dual Lane (Jittered clock) -for RAW7 Single lane		50 66 50-60 57.14		%
		Bypass and all other modes	45	50	55	

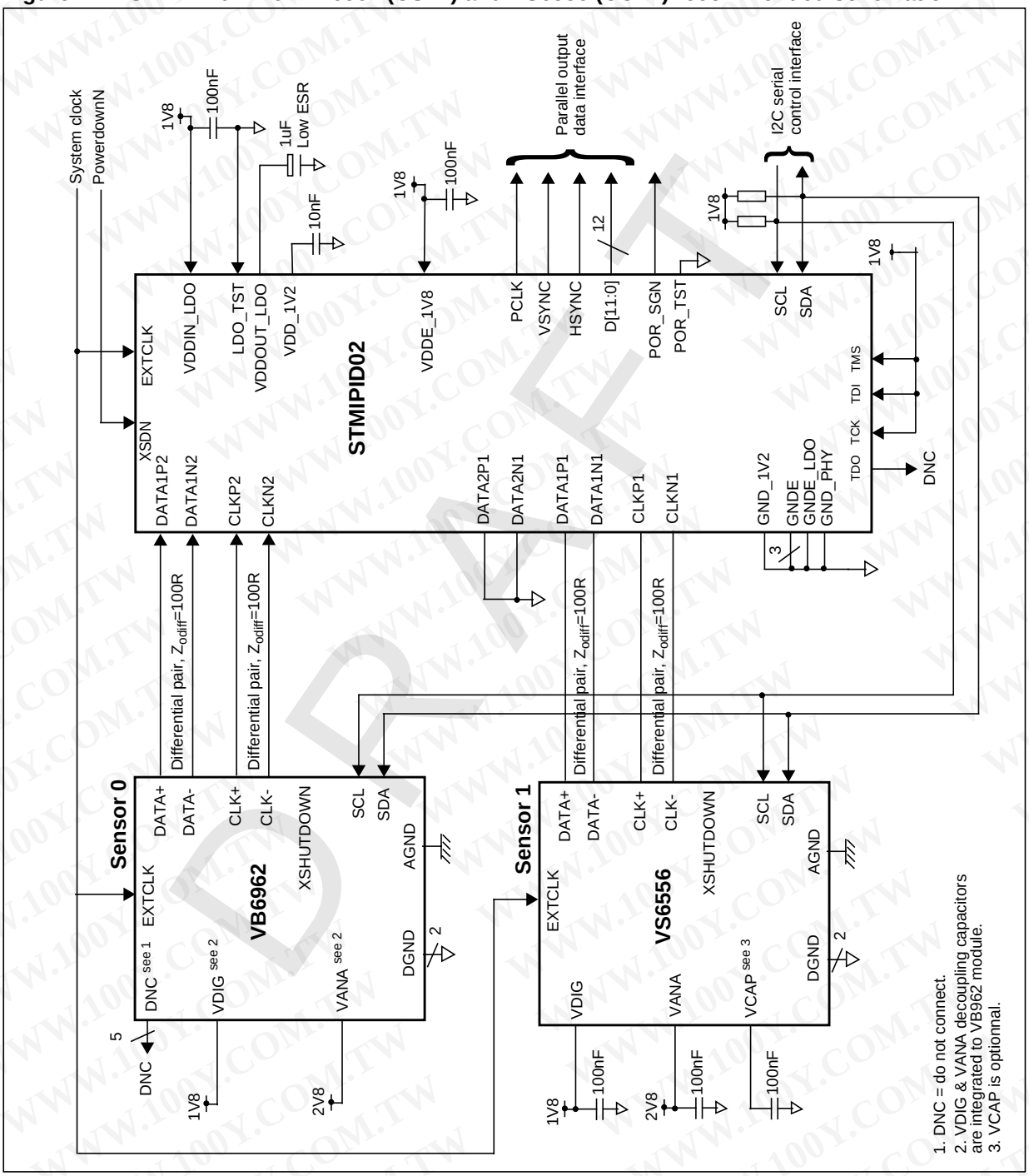
Table 16. Parallel output interface timing

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
t_R	PCLK rise time (20% - 80%)	Load capacitance, C_L = 50pF			2.1	ns
t_{DV}	PCLK to output valid		0 (TBC)		2 (TBC)	ns

11 Application Schematics

The application schematic given below show example of STMIPID02 application with a CSI-2 sensor.

Figure 17. STMIPID02 with VB6962 (CSI-2) and VS6556 (CCP2) recommended schematic



12 Package mechanical data

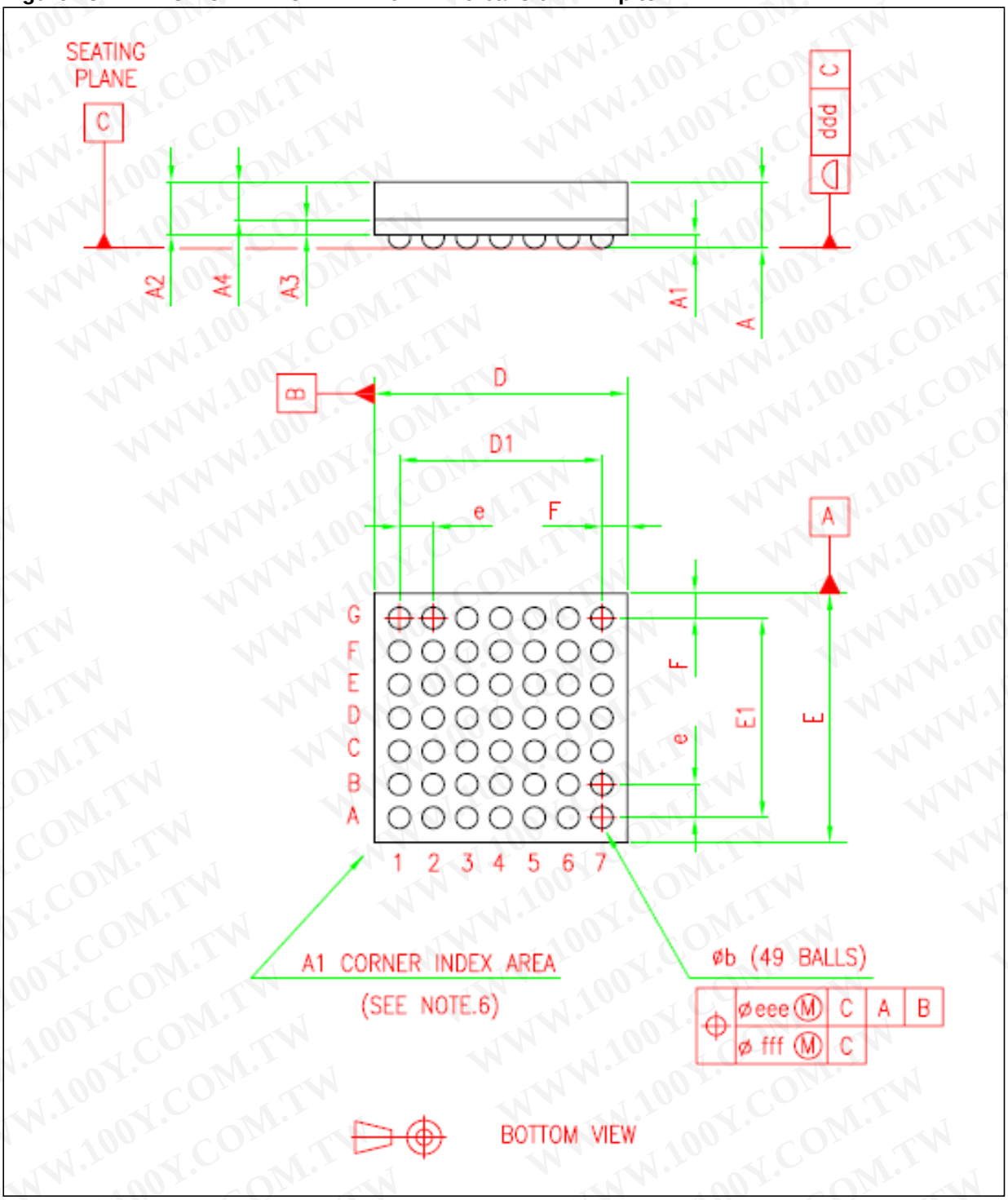
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 17. VFBGA 3 mm x 3 mm x 1.0 mm 49 balls 0.4 mm pitch

Reference	Min.	Typ.	Max.	Unit
A(1)			1.00	mm
A1	0.125			mm
A2		0.615		mm
A3		0.18		mm
A4			0.45	mm
b(2)	0.22	0.26	0.30	mm
D	2.95	3.00	3.05	mm
D1		2.40		mm
E	2.95	3.00	3.05	mm
E1		2.40		mm
e		0.40		mm
F		0.30		mm
ddd			0.08	mm
eee(3)			0.13	mm
fff(4)			0.04	mm

1. VFBGA stands for Very Thin profile Fine Pitch Ball Grid Array.
   - Very Thin profile: 0.80mm < A< = 1.00mm / Fine pitch: e < 1.00mm
   - The maximum total package height is calculated by the following methodology:
     A2 Typ + A1 Typ + square-root(A1 +A3 +A4 tolerance values)
2. The typical ball diameter before mounting is 0.25mm.
3. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
4. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above The axis of each ball must lie simultaneously in both tolerance zones.

Figure 18. VFBGA 3 mm x 3 mm x 1.0 mm 49 balls 0.4 mm pitch



Note: The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug. A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

13 PCB Layout Guide

Usual good PCB design rules should be observed for the layout of the STMIPID02.

Power and ground planes should be used to supply power to STMIPID02.

The high speed signal pairs (CLKP1, CLKN1), (DATA1P1, DATA1N1), (DATA2P1, DATA2N1), (CLKP2, CLKN2) and (DATA1P2; DATA1N2) should be routed as balanced transmission lines with a characteristic differential impedance (Zo_{diff}) of 100 Ω, and matched in length.

The difference of delay between Clock lane, Data lane1 and Data lane2 should be less than 5ps.

The total series resistance of the CSI line should be less than 5Ω.

For more details, please refer to the “MIPI Alliance Specification for D-PHY”, version 0.90.00 - 8 October 2007, Section 7 “Interconnect and Lane Configuration” & Annex B “Interconnect Design Guidelines”.

The output interface clock (PCLK) should be 50Ω adapted.

All passive components for the STMIPID02 should be placed in close proximity to the device, including the decoupling capacitors.

The recommended pull-up value of the I2C is in a range of 2480Ω to 2780Ω for a bus load capacitance below 100pF

The recommended capacitor values are:

- 10 nF on VDD1V2
- 100 nF on VDDIN_LDO and VDDE_1V8
- 1uF (low ESR <1 Ω) on VDDOUT_LDO

14 ESD Characterisctics

The device ESD sensitivity is compliant with the following specifications:

- JEDS22 A114D (Human Body Model) - +/-2 kV (class 2 compliant)
- JESD22-C101C (Charge Device Model) - +/-500 V (class III compliant)

15 Ordering information

Table 18. Ordering information

Order code	Package
STMIPID02	VFBGA 49pin 3.0mm x 3.0mm x1.0mm F7x7 0.4mm pitch, 0.25mm ball package.

16 Revision history

Table 19. Document revision history

Date	Revision	Changes
Nov-2008	0.1	Initial draft release
Nov-2008	0.2	Draft corrections
Dec-2008	0.3	Draft corrections
Dec-2008	0.4	Corrections on PCB layout guide
Jan-2009	0.5	Major corrections
Feb-2009	0.6	Major updates
Feb-2009	0.7	Registers description and OIF timings update

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