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STM32F205xx
STM32F207xx

Arm®-based 32-bit MCU, 150 DMIPs, up to 1 MB Flash/128+4KB RAM, USB OTG HS/FS, Ethernet, 17 TIMs, 3 ADCs, 15 comm. interfaces and camera

Datasheet - production data

Features

- Core: Arm® 32-bit Cortex®-M3 CPU (120 MHz max) with Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution performance from Flash memory, MPU, 150 DMIPS/1.25 DMIPS/MHz (Dhrystone 2.1)
- Memories
  - Up to 1 Mbyte of Flash memory
  - 512 bytes of OTP memory
  - Up to 128 + 4 Kbytes of SRAM
  - Flexible static memory controller that supports Compact Flash, SRAM, PSRAM, NOR and NAND memories
  - LCD parallel interface, 8080/6800 modes
- Clock, reset and supply management
  - From 1.8 to 3.6 V application supply + I/Os
  - POR, PDR, PVD and BOR
  - 4 to 26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Low-power modes
  - Sleep, Stop and Standby modes
  - V_{BAT} supply for RTC, 20 × 32 bit backup registers, and optional 4 Kbytes backup SRAM
- 3 × 12-bit, 0.5 µs ADCs with up to 24 channels and up to 6 MSPS in triple interleaved mode
- 2 × 12-bit D/A converters
- General-purpose DMA: 16-stream controller with centralized FIFOs and burst support
- Up to 17 timers
  - Up to twelve 16-bit and two 32-bit timers, up to 120 MHz, each with up to four IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
- Debug mode: Serial wire debug (SWD), JTAG, and Cortex®-M3 Embedded Trace Macrocell™

LQFP64 (10 × 10 mm)
LQFP100 (14 × 14 mm)
LQFP144 (20 × 20mm)
LQFP176 (24 × 24 mm)

WLCSP64+2
(0.400 mm pitch)

UFBGA176
(10 × 10 mm)

- Up to 140 I/O ports with interrupt capability:
  - Up to 136 fast I/Os up to 60 MHz
  - Up to 138 5 V-tolerant I/Os
- Up to 15 communication interfaces
  - Up to three I^2C interfaces (SMBus/PMBus)
  - Up to four USARTs and two UARTs (7.5 Mbit/s, ISO 7816 interface, LIN, IrDA, modem control)
  - Up to three SPIs (30 Mbit/s), two with muxed I^2S to achieve audio class accuracy via audio PLL or external PLL
  - 2 × CAN interfaces (2.0B Active)
  - SDIO interface
- Advanced connectivity
  - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
  - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
  - 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII
- 8- to 14-bit parallel camera interface (48 Mbyte/s max.)
- CRC calculation unit
- 96-bit unique ID

Table 1. Device summary

Reference	Part numbers
STM32F205xx	STM32F205RB, STM32F205RC, STM32F205RE, STM32F205RF, STM32F205RG STM32F205VB, STM32F205VC, STM32F205VE, STM32F205VF, STM32F205VG STM32F205ZC, STM32F205ZE, STM32F205ZF, STM32F205ZG
STM32F207xx	STM32F207IC, STM32F207IE, STM32F207IF, STM32F207IG STM32F207VC, STM32F207VE, STM32F207VF, STM32F207VG STM32F207ZC, STM32F207ZE, STM32F207ZF, STM32F207ZG

Table 2. STM32F205xx features and peripheral counts

Peripherals		STM32F205Rx					STM32F205Vx					STM32F205Zx			
Flash memory in Kbytes		128	256	512	768	1024	128	256	512	768	1024	256	512	768	1024
SRAM in Kbytes	System (SRAM1+SRAM2)	64 (48+16)	96 (80+16)	128 (112+16)			64 (48+16)	96 (80+16)	128 (112+16)			96 (80+16)	128 (112+16)		
	Backup	4					4					4			
FSMC memory controller		No					Yes(1)								
Ethernet		No													
Timers	General-purpose	10													
	Advanced-control	2													
	Basic	2													
	IWDG	Yes													
	WWDG	Yes													
RTC		Yes													
Random number generator		Yes													
Comm. interfaces	SPI/(I^2S)	3/(2)(2)													
	I^2C	3													
	USART UART	4 2													
	USB OTG FS	Yes													
	USB OTG HS	Yes													
	CAN	2													
Camera interface		No													
GPIOs		51					82					114			
SDIO		Yes													
12-bit ADC Number of channels		3													
		16					16					24			
12-bit DAC Number of channels		Yes 2													
Maximum CPU frequency		120 MHz													
Operating voltage		1.8 V to 3.6 V(3)													

Table 2. STM32F205xx features and peripheral counts (continued)

Peripherals	STM32F205Rx				STM32F205Vx	STM32F205Zx
Operating temperatures	Ambient temperatures: –40 to +85 °C /–40 to +105 °C					
	Junction temperature: –40 to + 125 °C					
Package	LQFP64	LQFP64 WLCSP64+2	LQFP64	LQFP64 WLCSP64+2	LQFP100	LQFP144

1. For the LQFP100 package, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).

Table 3. STM32F207xx features and peripheral counts

Peripherals		STM32F207Vx				STM32F207Zx				STM32F207Ix			
Flash memory in Kbytes		256	512	768	1024	256	512	768	1024	256	512	768	1024
SRAM in Kbytes	System (SRAM1+SRAM2)	128 (112+16)											
	Backup	4											
FSMC memory controller		Yes(1)											
Ethernet		Yes											
Timers	General-purpose	10											
	Advanced-control	2											
	Basic	2											
	IWDG	Yes											
	WWDG	Yes											
RTC		Yes											
Random number generator		Yes											

Table 3. STM32F207xx features and peripheral counts (continued)

Peripherals		STM32F207Vx	STM32F207Zx	STM32F207Ix
Comm. interfaces	SPI/(I^2S)	3/(2)[2]		
	I^2C	3		
	USART UART	4 2		
	USB OTG FS	Yes		
	USB OTG HS	Yes		
	CAN	2		
Camera interface		Yes		
GPIOs		82	114	140
SDIO		Yes		
12-bit ADC Number of channels		3		
		16	24	24
12-bit DAC Number of channels		Yes 2		
Maximum CPU frequency		120 MHz		
Operating voltage		1.8 V to 3.6 V[3]		
Operating temperatures		Ambient temperatures: –40 to +85 °C/–40 to +105 °C		
		Junction temperature: –40 to + 125 °C		
Package		LQFP100	LQFP144	LQFP176/ UFBGA176

1. For the LQFP100 package, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).

2.1 Full compatibility throughout the family

The STM32F205xx and STM32F207xx constitute the STM32F20x family, whose members are fully pin-to-pin, software and feature compatible, allowing the user to try different memory densities and peripherals for a greater degree of freedom during the development cycle.

The STM32F205xx and STM32F207xx devices maintain a close compatibility with the whole STM32F10xxx family. All functional pins are pin-to-pin compatible. The STM32F205xx and STM32F207xx, however, are not drop-in replacements for the STM32F10xxx devices: the two families do not have the same power scheme, and so their power pins are different. Nonetheless, transition from the STM32F10xxx to the STM32F20x family remains simple as only a few pins are impacted.

Figure 1, *Figure 2* and *Figure 3* provide compatible board designs between the STM32F20x and the STM32F10xxx family.

Figure 1. Compatible board design between STM32F10x and STM32F2xx for LQFP64 package

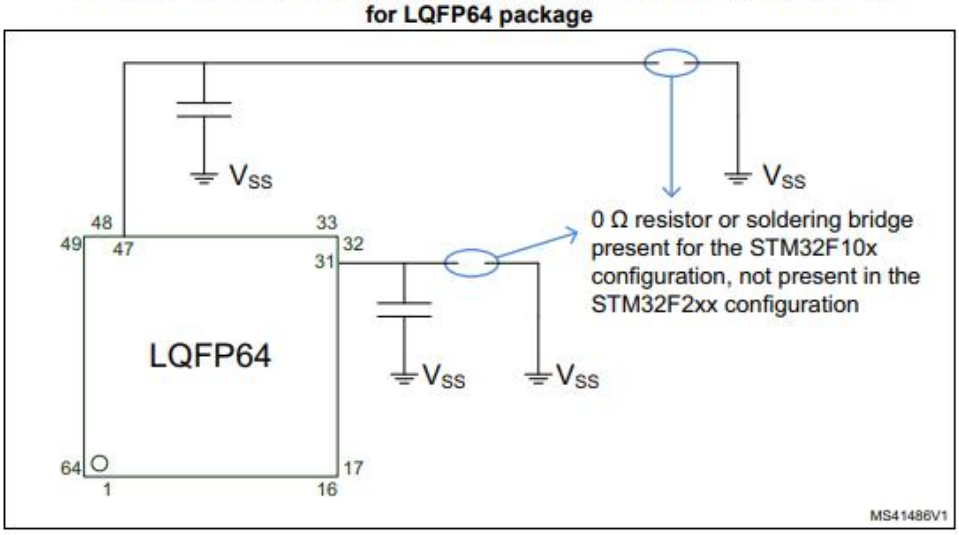
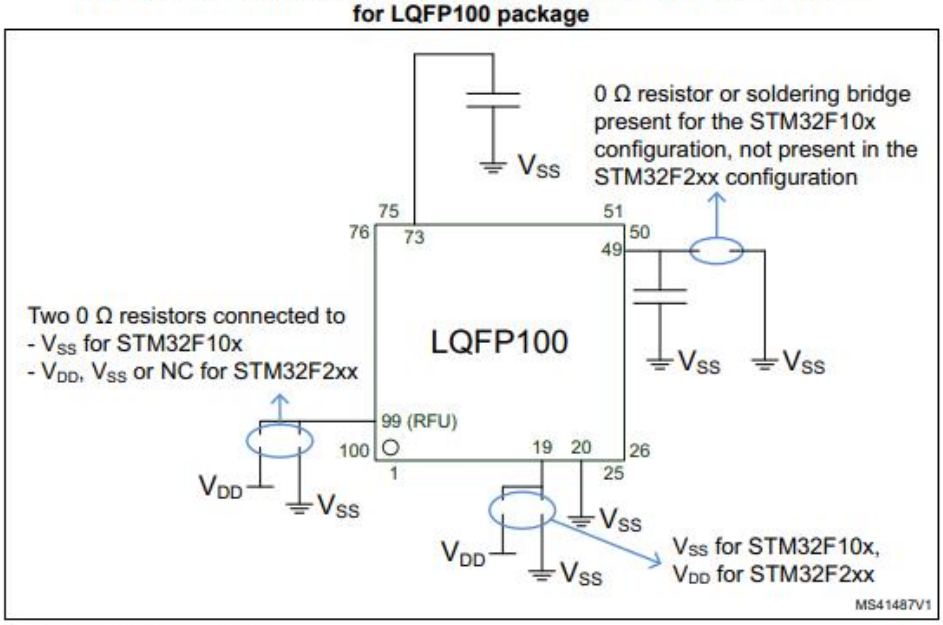
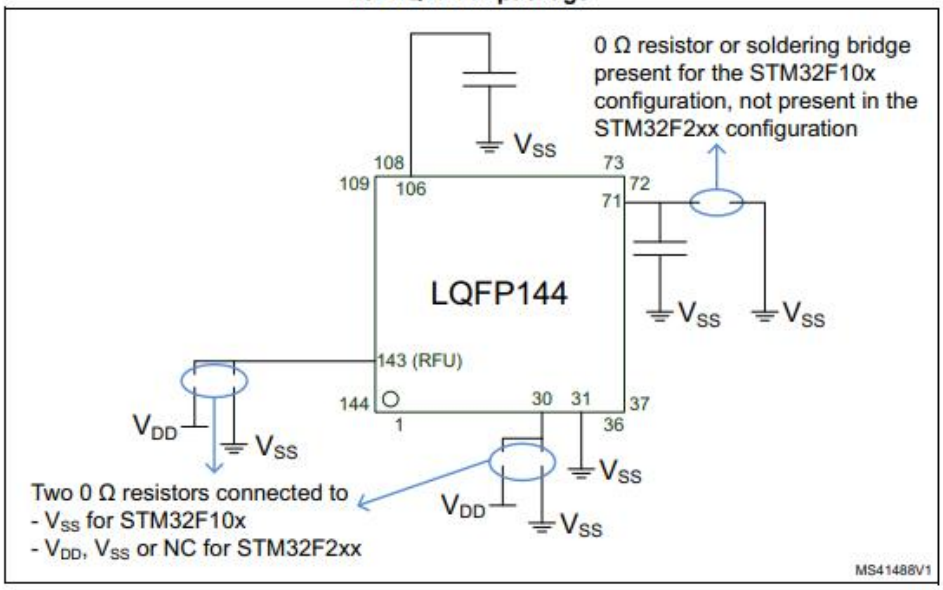


Figure 2. Compatible board design between STM32F10x and STM32F2xx for LQFP100 package



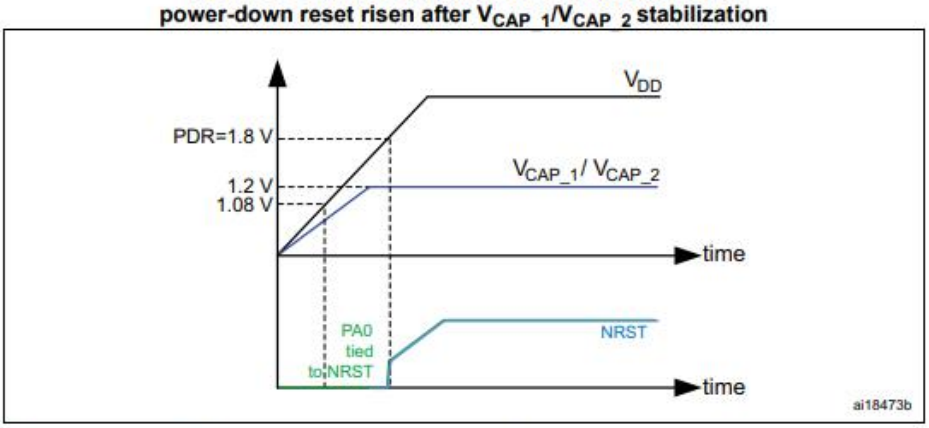
1. RFU = reserved for future use.

Figure 3. Compatible board design between STM32F10x and STM32F2xx for LQFP144 package



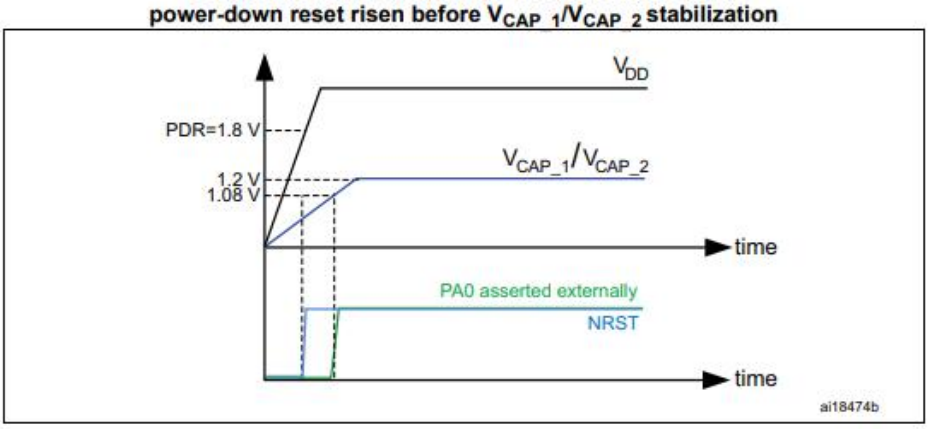
1. RFU = reserved for future use.

Figure 8. Startup in regulator OFF: slow V_{DD} slope, power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

Figure 9. Startup in regulator OFF: fast V_{DD} slope, power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization



3.16.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal reset ON/OFF availability

Package	Regulator ON / internal reset ON	Regulator OFF / internal reset ON	Regulator OFF / internal reset OFF
LQFP64 LQFP100 LQFP144 LQFP176	Yes	No	No
WLCSP 64+2	Yes REGOFF and IRROFF set to V_{SS}	Yes REGOFF set to V_{DD} and IRROFF set to V_{SS}	Yes REGOFF set to V_{SS} and IRROFF set to V_{DD}
UFBGA176	Yes REGOFF set to V_{SS}	Yes REGOFF set to V_{DD}	No

Table 12. Current characteristics

Symbol	Ratings	Max	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(1)	120	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	120	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	25	
$I_{INJ(PIN)}$ (2)	Injected current on five-volt tolerant I/O(3)	–5/+0	
	Injected current on any other pin(4)	±5	
$\Sigma I_{INJ(PIN)}$ (4)	Total injected current (sum of all I/O and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.20: 12-bit ADC characteristics*.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 11* for the values of the maximum allowed input voltage.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 11* for the values of the maximum allowed input voltage.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 13. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	125	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 14. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	120	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	30	
f_{PCLK2}	Internal APB2 clock frequency	-	0	60	

Table 14. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Standard operating voltage	-	1.8(1)	3.6	V
V_{DDA}(2)	Analog operating voltage (ADC limited to 1 M samples)	Must be the same potential as V_{DD}(3)	1.8(1)	3.6	
	Analog operating voltage (ADC limited to 2 M samples)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.65	3.6	
V_{IN}	Input voltage on RST and FT pins	2 V ≤ V_{DD} ≤ 3.6 V	–0.3	5.5	
		1.7 V ≤ V_{DD} ≤ 2 V	–0.3	5.2	
	Input voltage on TTa pins	-	–0.3	V_{DD}+0.3	
	Input voltage on BOOT0 pin	-	0	9	
V_{CAP1}	Internal core voltage to be supplied externally in REGOFF mode	-	1.1	1.3	
V_{CAP2}					
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(4)	LQFP64	-	444	mW
		WLCSP64+2	-	392	
		LQFP100	-	434	
		LQFP144	-	500	
		LQFP176	-	526	
		UFBGA176	-	513	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low-power dissipation(5)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low-power dissipation(5)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).
2. When the ADC is used, refer to *Table 66: ADC characteristics*.
3. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
5. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

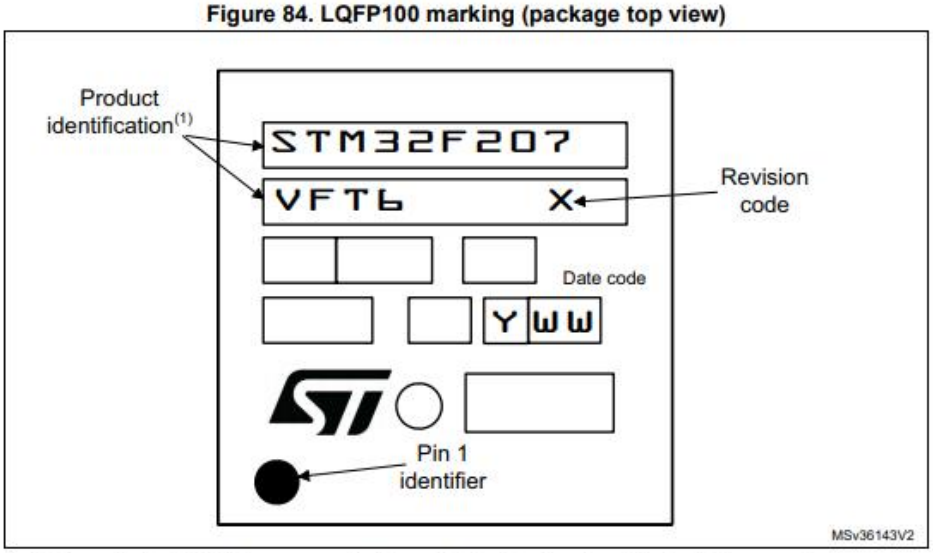
Device marking

The following figure gives an example of topside marking and pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 84. LQFP100 marking (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

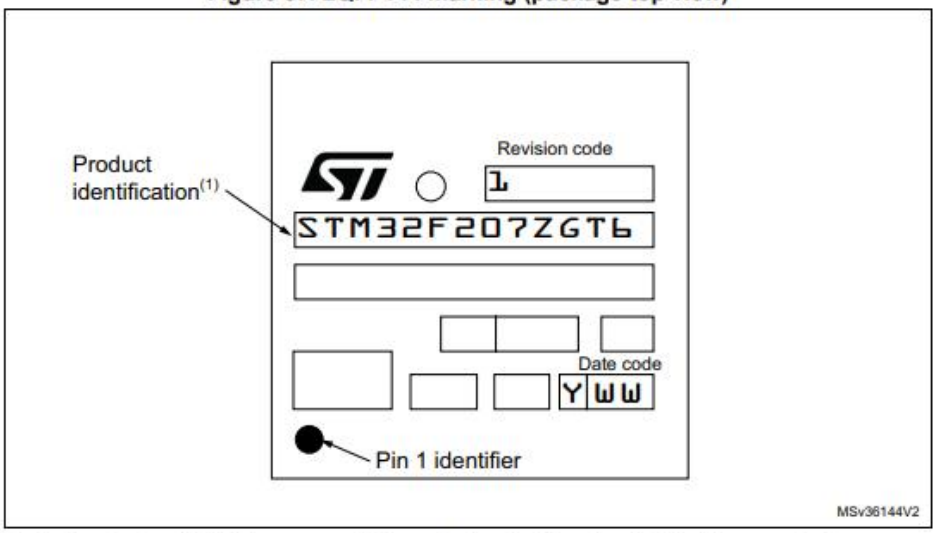
Device marking

The following figure gives an example of topside marking and pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 87. LQFP144 marking (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

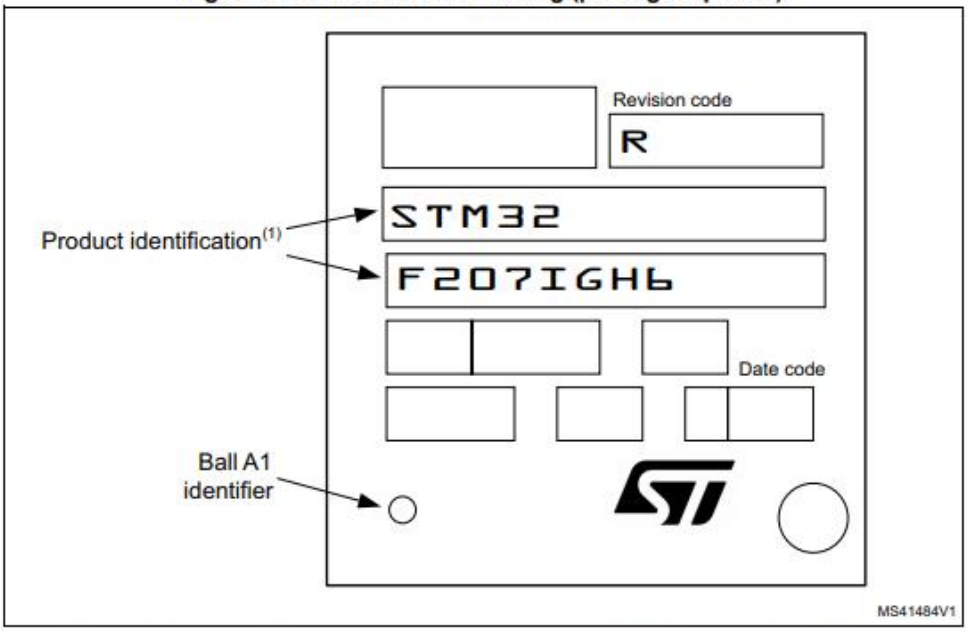
Device marking

The following figure gives an example of topside marking and ball A1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 92. UFBGA176+25 marking (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.