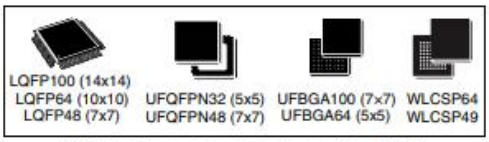
STM32L431xx

Ultra-low-power ARM® Cortex®-M4 32-bit MCU+FPU, 100DMIPS, up to 256KB Flash, 64KB SRAM, analog, audio

Datasheet - production data

Features

- Ultra-low-power with FlexPowerControl
  - 1.71 V to 3.6 V power supply
  - -40 °C to 85/105/125 °C temperature range
  - 200 nA in V_{BAT} mode: supply for RTC and 32x32-bit backup registers
  - 8 nA Shutdown mode (5 wakeup pins)
  - 28 nA Standby mode (5 wakeup pins)
  - 280 nA Standby mode with RTC
  - 1.0 µA Stop 2 mode, 1.28 µA Stop 2 with RTC
  - 84 µA/MHz run mode
  - Batch acquisition mode (BAM)
  - 4 µs wakeup from Stop mode
  - Brown out reset (BOR) in all modes except shutdown
  - Interconnect matrix
- Core: ARM® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait-state execution from Flash memory, frequency up to 80 MHz, MPU, 100DMIPS/1.25DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Performance Benchmark
  - 1.25 DMIPS/MHz (Drystone 2.1)
  - 273.55 Coremark® (3.42 Coremark/MHz @ 80 MHz)
- Energy Benchmark
  - 176.7 ULPBench® score
- Clock Sources
  - 4 to 48 MHz crystal oscillator
  - 32 kHz crystal oscillator for RTC (LSE)
  - Internal 16 MHz factory-trimmed RC (±1%)
  - Internal low-power 32 kHz RC (±5%)
  - Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than ±0.25 % accuracy)
  - Internal 48 MHz with clock recovery

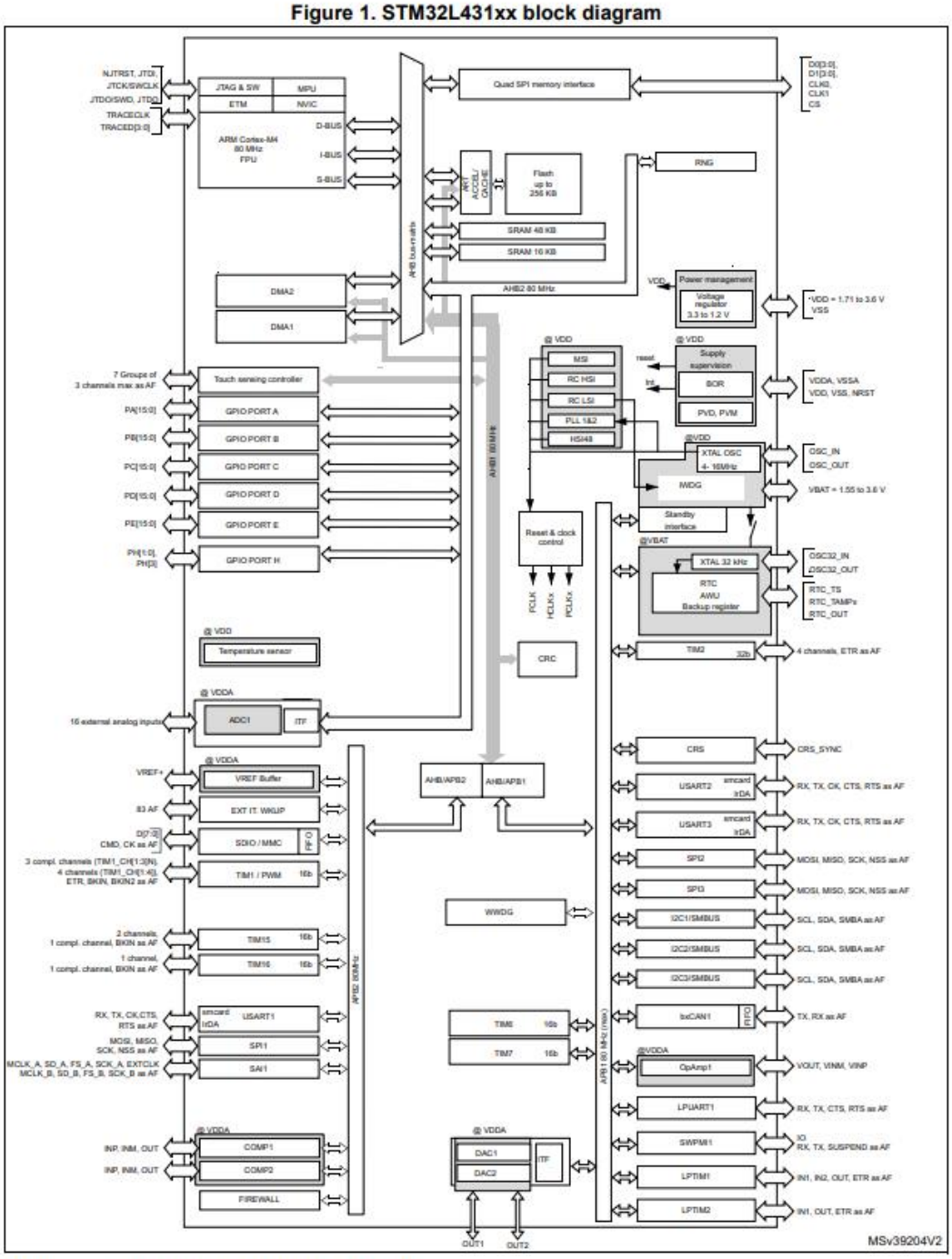


  - 2 PLLs for system clock, audio, ADC
- RTC with HW calendar, alarms and calibration
- Up to 21 capacitive sensing channels: support touchkey, linear and rotary touch sensors
- 11x timers: 1x 16-bit advanced motor-control, 1x 32-bit and 2x 16-bit general purpose, 2x 16-bit basic, 2x low-power 16-bit timers (available in Stop mode), 2x watchdogs, SysTick timer
- Up to 83 fast I/Os, most 5 V-tolerant
- Memories
  - Up to 256 KB single bank Flash, proprietary code readout protection
  - 64 KB of SRAM including 16 KB with hardware parity check
  - Quad SPI memory interface
- Rich analog peripherals (independent supply)
  - 1× 12-bit ADC 5 Msps, up to 16-bit with hardware oversampling, 200 µA/Msps
  - 2x 12-bit DAC, low-power sample and hold
  - 1x operational amplifier with built-in PGA
  - 2x ultra-low-power comparators
- 15x communication interfaces
  - 1x SAI (serial audio interface)
  - 3x I2C FM+(1 Mbit/s), SMBus/PMBus
  - 4x USARTs (ISO 7816, LIN, IrDA, modem)
  - 3x SPIs (4x SPIs with the Quad SPI)
  - CAN (2.0B Active) and SDMMC interface
  - SWPMI single wire protocol master I/F
  - IRTIM (Infrared interface)
- 14-channel DMA controller
- True random number generator
- CRC calculation unit, 96-bit unique ID
- Development support: serial wire debug (SWD), JTAG, Embedded Trace Macrocell™

Table 1. Device summary

Reference	Part numbers
STM32L431xx	STM32L431CC, STM32L431KC, STM32L431RC, STM32L431VC, STM32L431CB, STM32L431KB, STM32L431RB

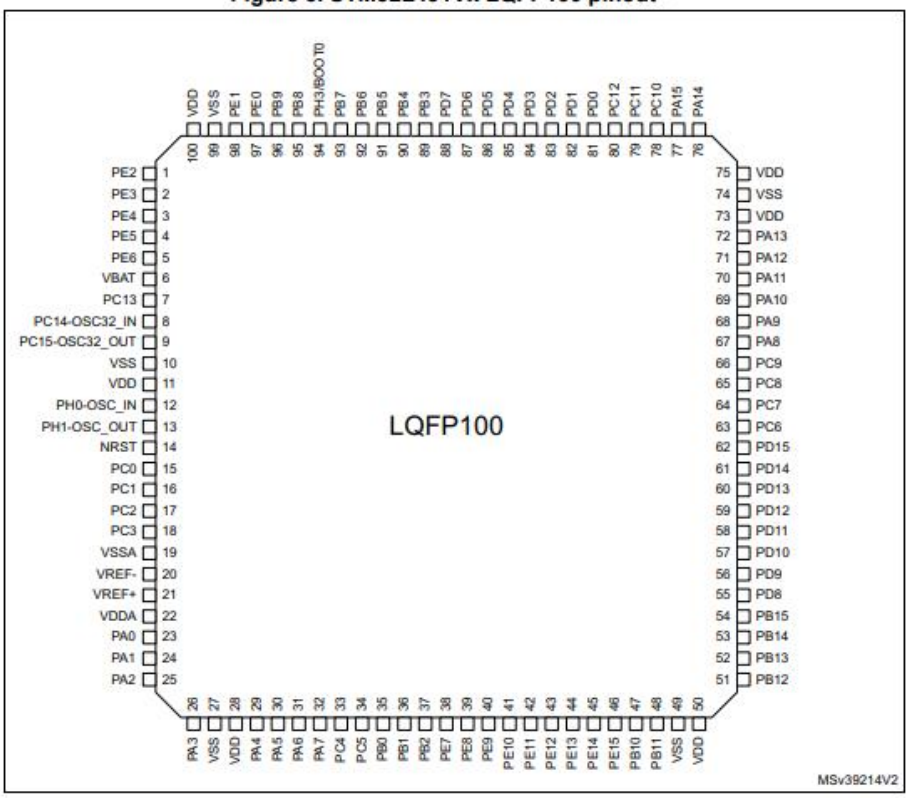
Figure 1. STM32L431xx block diagram



Note: AF: alternate function on I/O pins.

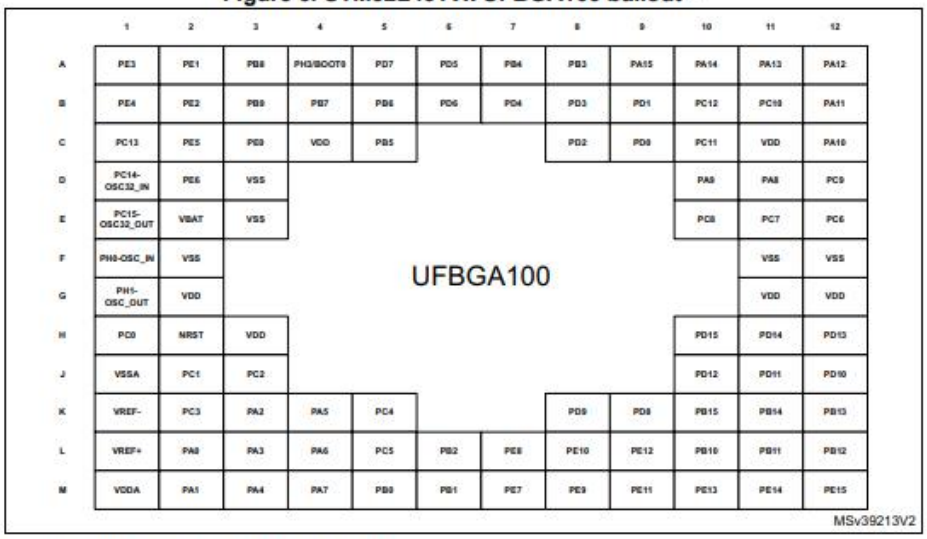
4 Pinouts and pin description

Figure 5. STM32L431Vx LQFP100 pinout(1)



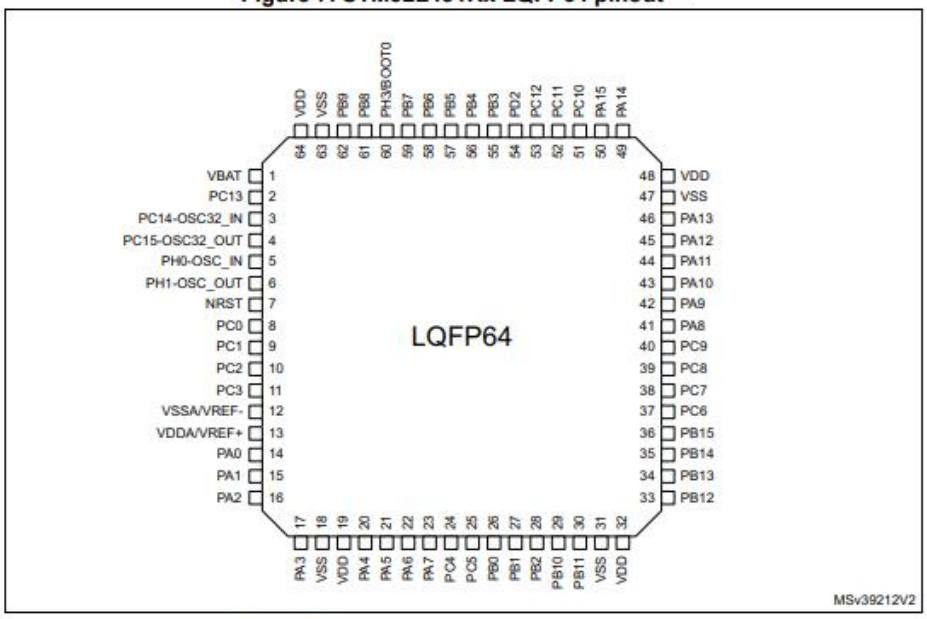
1. The above figure shows the package top view.

Figure 6. STM32L431Vx UFBGA100 ballout(1)



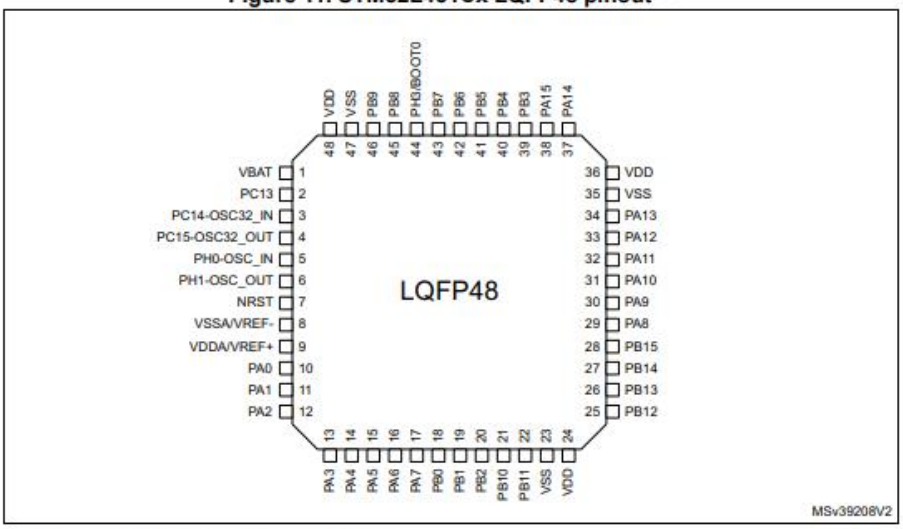
1. The above figure shows the package top view.

Figure 7. STM32L431Rx LQFP64 pinout(1)



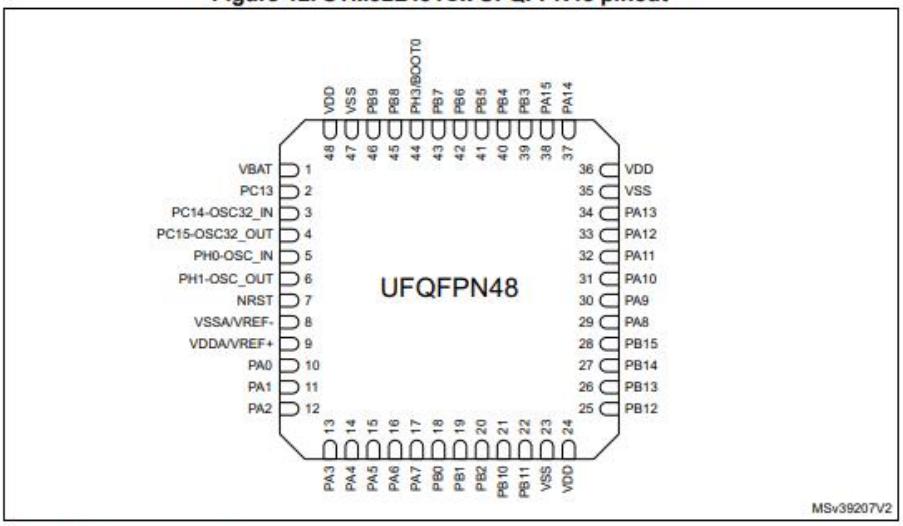
1. The above figure shows the package top view.

Figure 11. STM32L431Cx LQFP48 pinout(1)



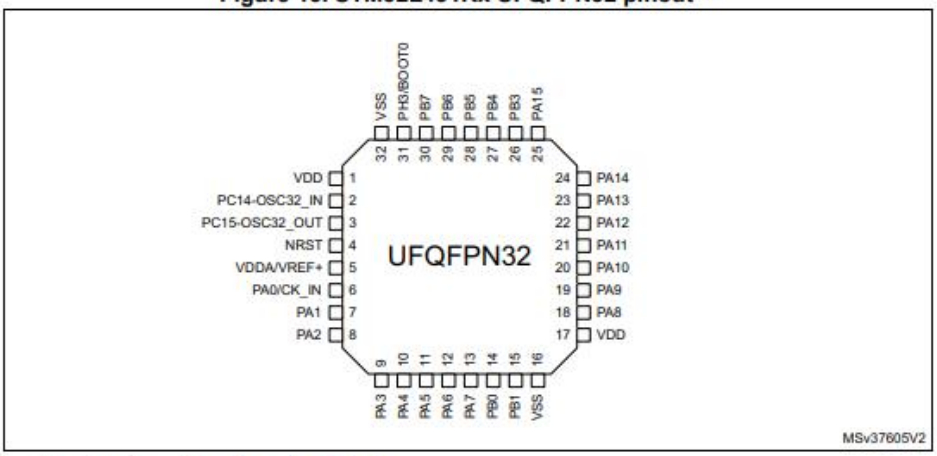
1. The above figure shows the package top view.

Figure 12. STM32L431Cx UFQFPN48 pinout(1)



1. The above figure shows the package top view.

Figure 13. STM32L431Kx UFQFPN32 pinout(1)



1. The above figure shows the package top view.

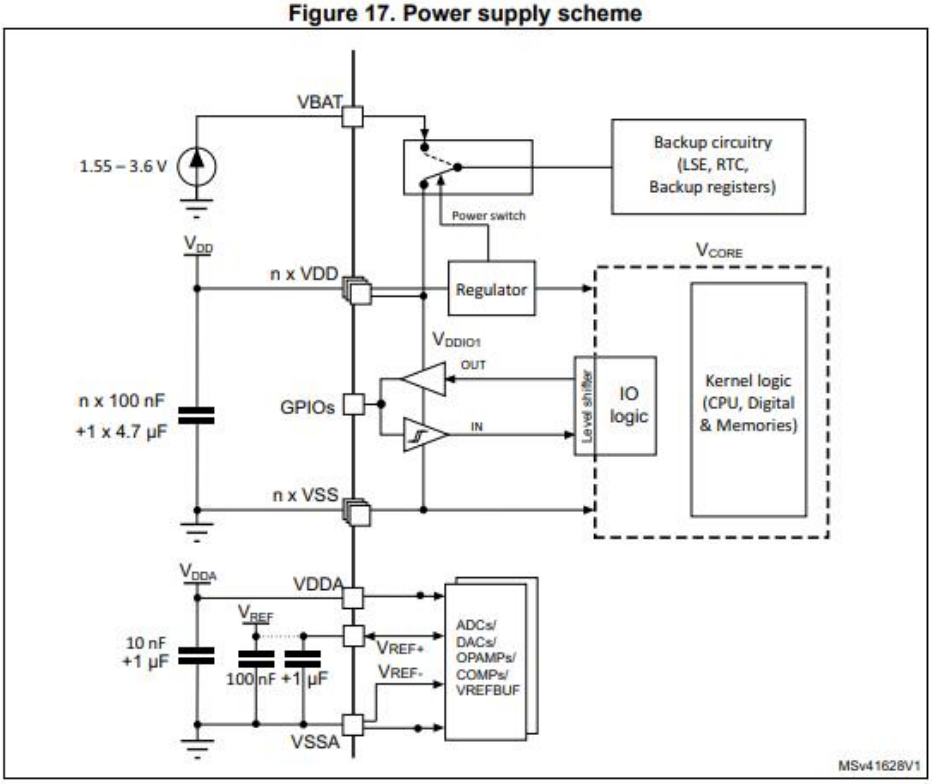
Table 13. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TT	3.6 V tolerant I/O
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Option for TT or FT I/Os	
		_f (1)	I/O, Fm+ capable
		_a (2)	I/O, with Analog switch function supplied by V_{DDA}
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures in *Table 14* are: FT_f, FT_fa.
2. The related I/O structures in *Table 14* are: FT_a, FT_fa, TT_a.

6.1.6 Power supply scheme

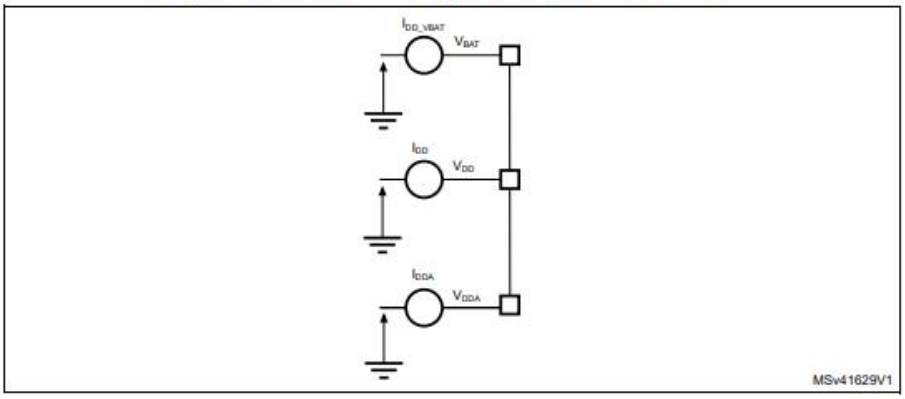
Figure 17. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.7 Current consumption measurement

Figure 18. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 18: Voltage characteristics*, *Table 19: Current characteristics* and *Table 20: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 18. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDA}, V_{BAT})	-0.3	4.0	V
V_{IN}(2)	Input voltage on FT_xxx pins	V_{SS}-0.3	min (V_{DD}, V_{DDA}) + 4.0(3)(4)	V
	Input voltage on TT_xx pins	V_{SS}-0.3	4.0	
	Input voltage on any other pins	V_{SS}-0.3	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins(5)	-	50	mV

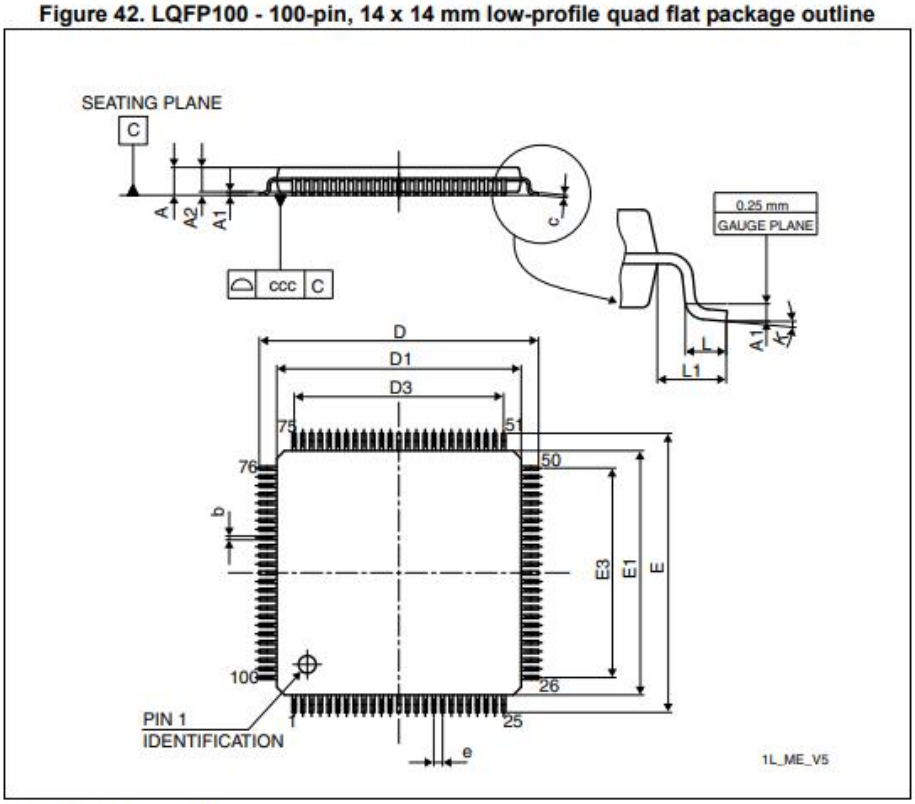
1. All main power (V_{DD}, V_{DDA}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 19: Current characteristics* for the maximum allowed injected current values.
3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.
4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 LQFP100 package information

Figure 42. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline

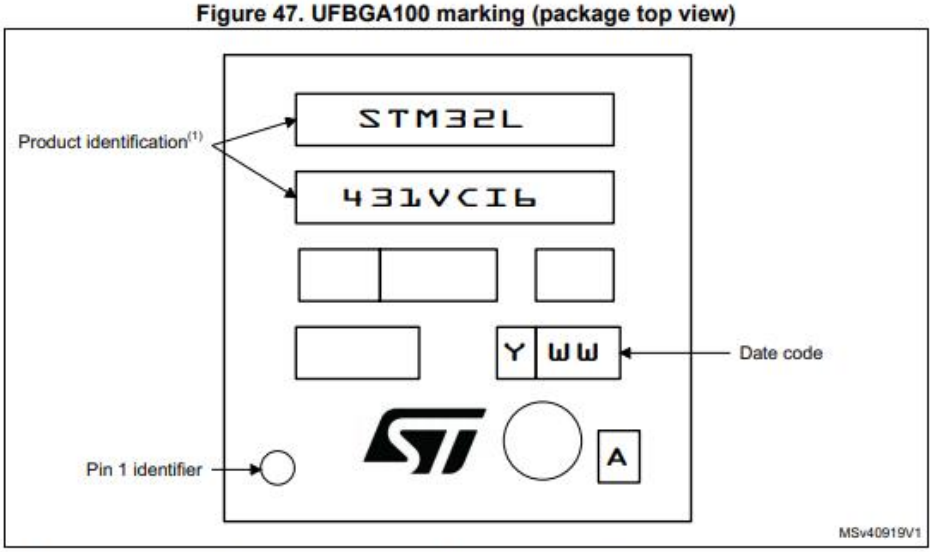


1. Drawing is not to scale.

Table 89. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

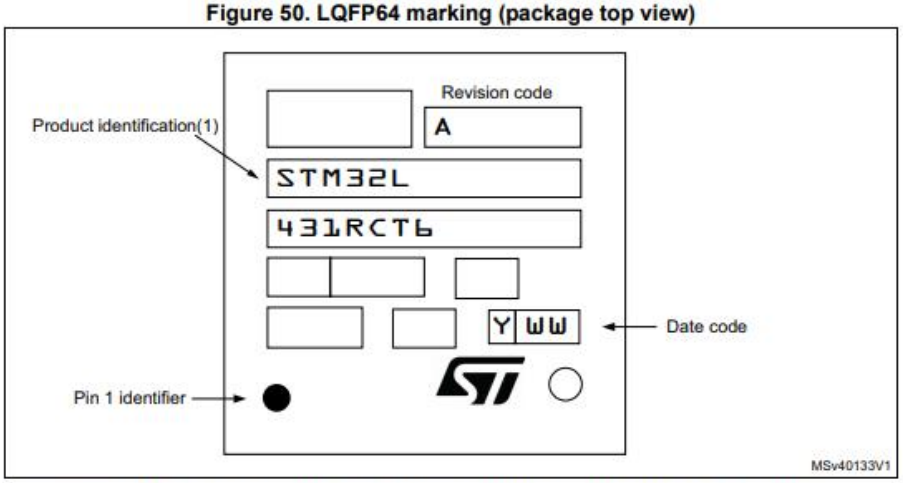
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059

Figure 47. UFBGA100 marking (package top view)



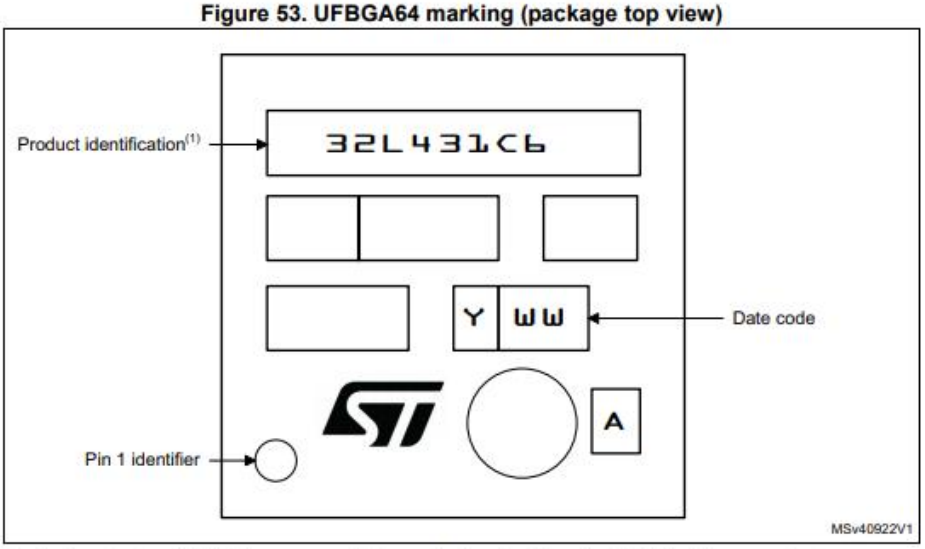
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Figure 50. LQFP64 marking (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Figure 53. UFBGA64 marking (package top view)

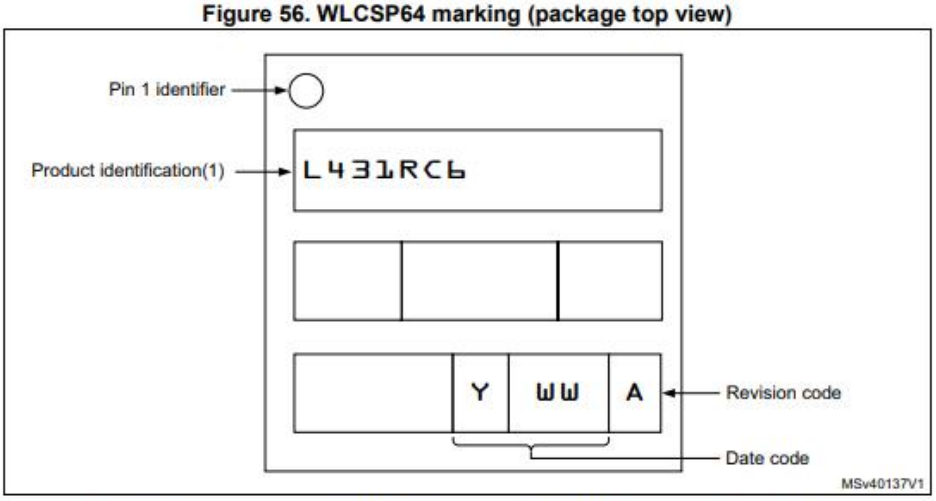


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 56. WLCSP64 marking (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

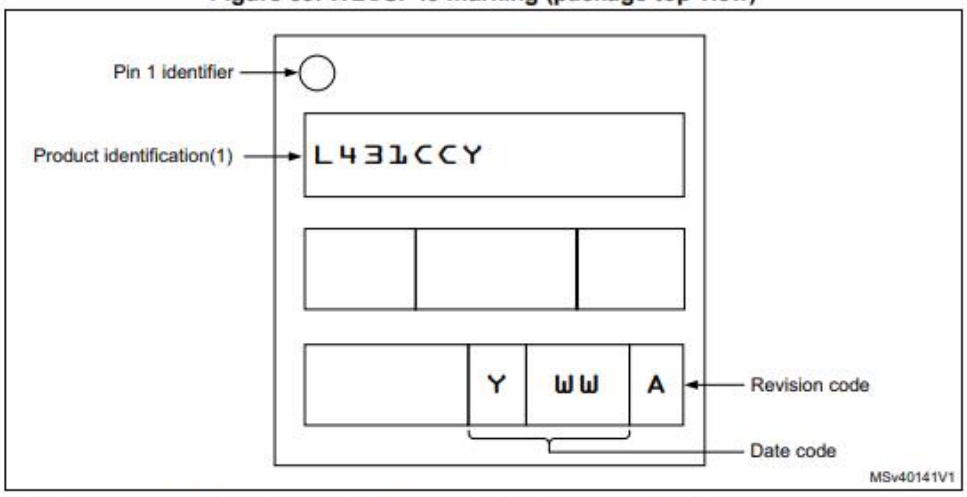
Table 98. WLCSP49 recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

Device marking

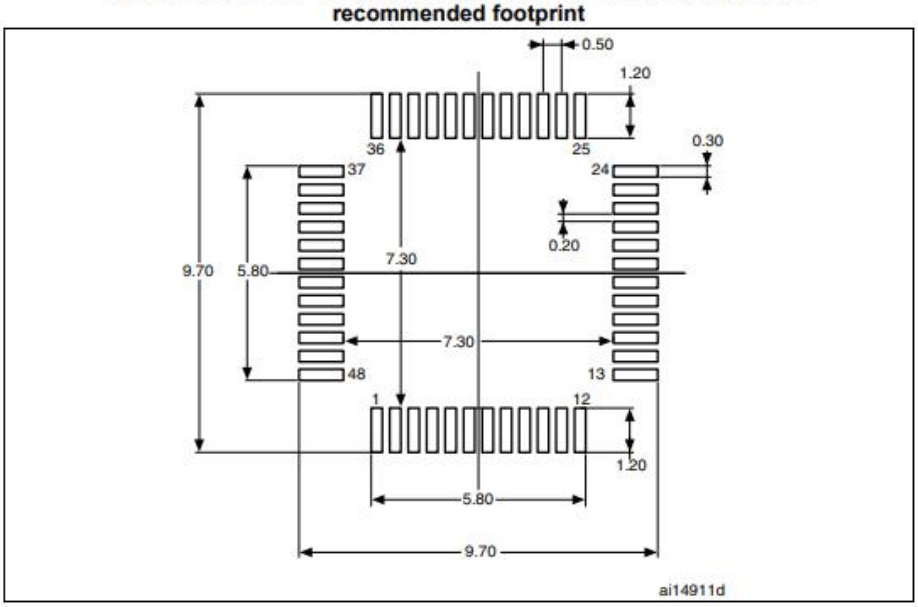
The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 59. WLCSP49 marking (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Figure 61. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint

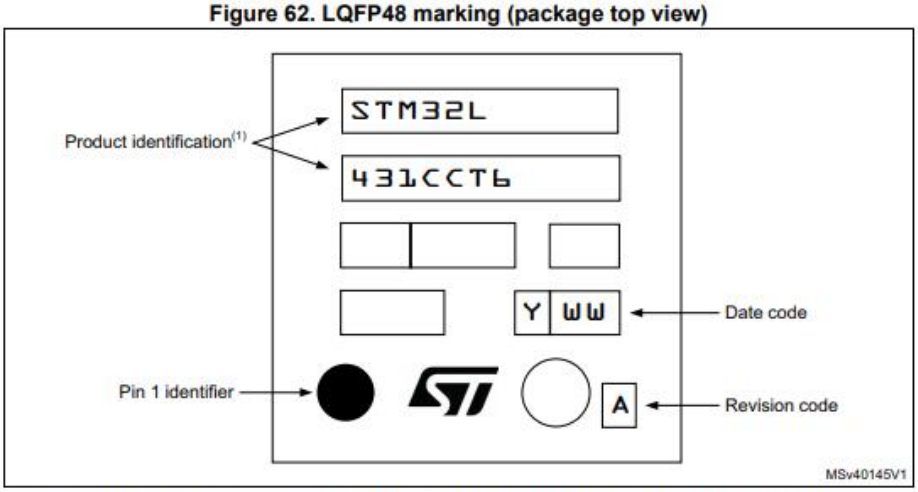


1. Dimensions are expressed in millimeters.

Device marking

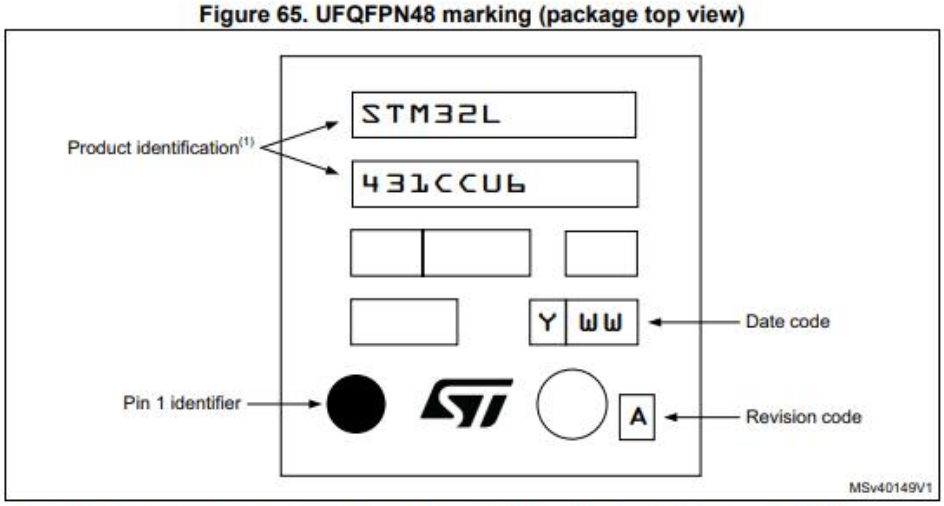
The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 62. LQFP48 marking (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Figure 65. UFQFPN48 marking (package top view)



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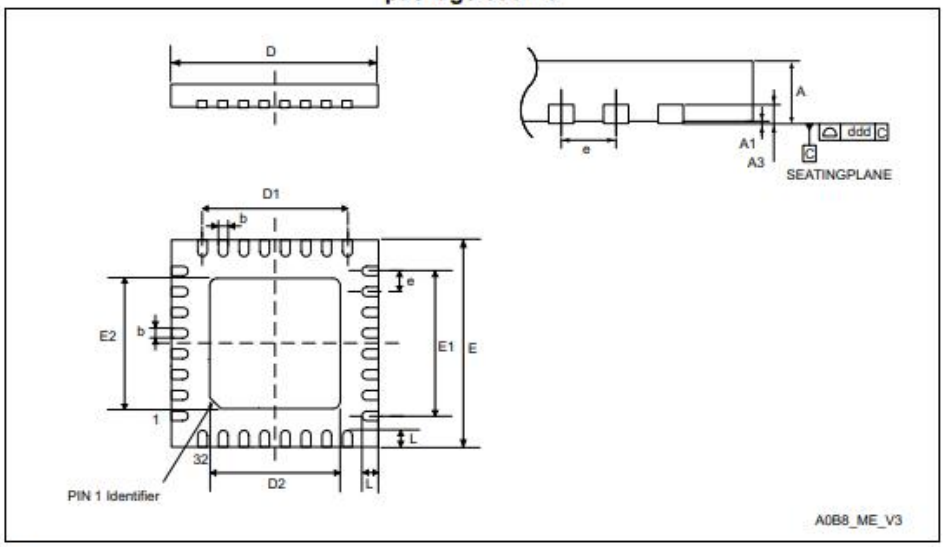
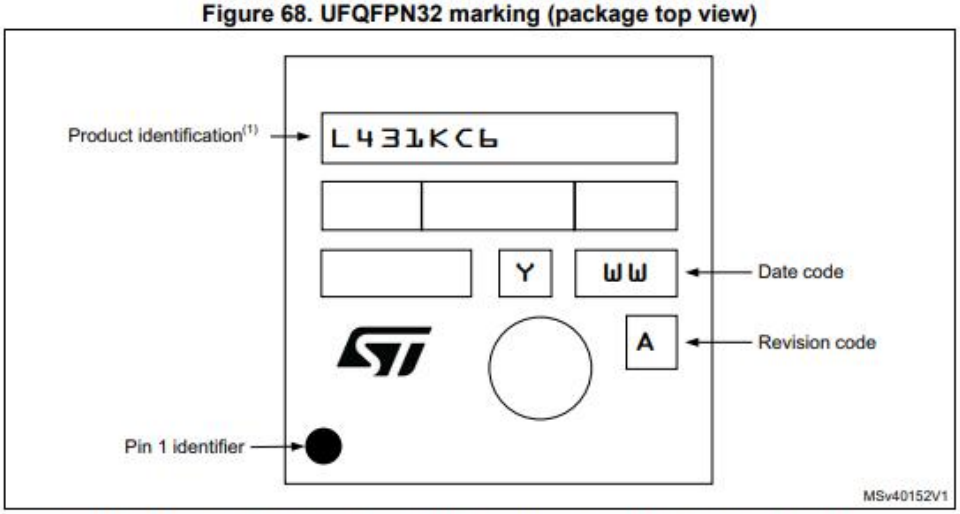
7.9 UFQFPN32 package information

Figure 66. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.
2. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this backside pad to PCB ground.

Figure 68. UFQFPN32 marking (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.