Silicon Image

PanelLink®

Technology

SiI 161B
PanelLink Receiver

Data Sheet

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Silicon Image, Inc.

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Application Information

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Revision History

Revision	Date	Comment
SiI-DS-0038-A	09/2001	Full release.
SiI-DS-0038-B	03/2002	Add design guidelines.
SiI-DS-0038-C	08/2002	Add Pb-free part number.

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General Description

The SiI 161B receiver uses PanelLink Digital technology to support high-resolution displays up to UXGA (25-165MHz). This receiver supports up to true color panels (24 bits per pixel, 16M colors) with both one and two pixels per clock.

All PanelLink products are designed on a scaleable CMOS architecture, ensuring support for future performance enhancements while maintaining the same logical interface. System designers can be assured that the interface will be stable through a number of technology and performance generations.

PanelLink Digital technology simplifies PC and display interface design by resolving many of the system level issues associated with high-speed mixed signal design, providing the system designer with a digital interface solution that is quicker to market and lower in cost.

Features

- Low Power Operation: 280mA max. current consumption at 3.3V core operation
- Time staggered data output for reduced ground bounce and lower EMI
- Sync Detect feature for Plug & Display
- Cable Distance Support: over 5m with twisted-pair, fiber-optics ready
- ESD tolerant to 5kV (HBM on all pins)
- Compliant with DVI 1.0 (DVI is backwards compatible with VESA® P&D™, FPDI-2™ and DFP)
- HSYNC de-jitter circuitry enables stable operation even when HSYNC contains jitter
- Low power standby mode
- Automatic entry into standby mode with clock detect circuitry
- Standard and Pb-free packages (see page 25).

SiI 161B Pin Diagram

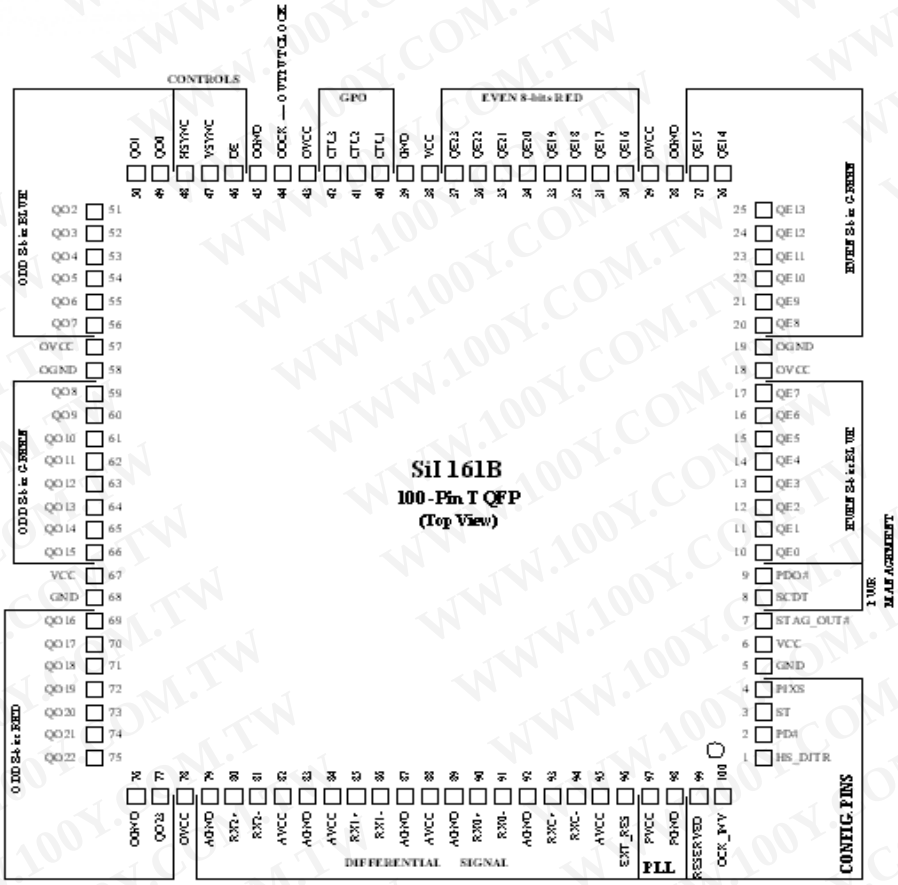


Figure 1. Pin Diagram for SiI 161B

Functional Description

The SiI 161B is a DVI 1.0 compliant PanelLink receiver in a compact package. It provides 48 bits for data output to allow for panel support up to UXGA. Figure 2 shows the functional blocks of the chip.

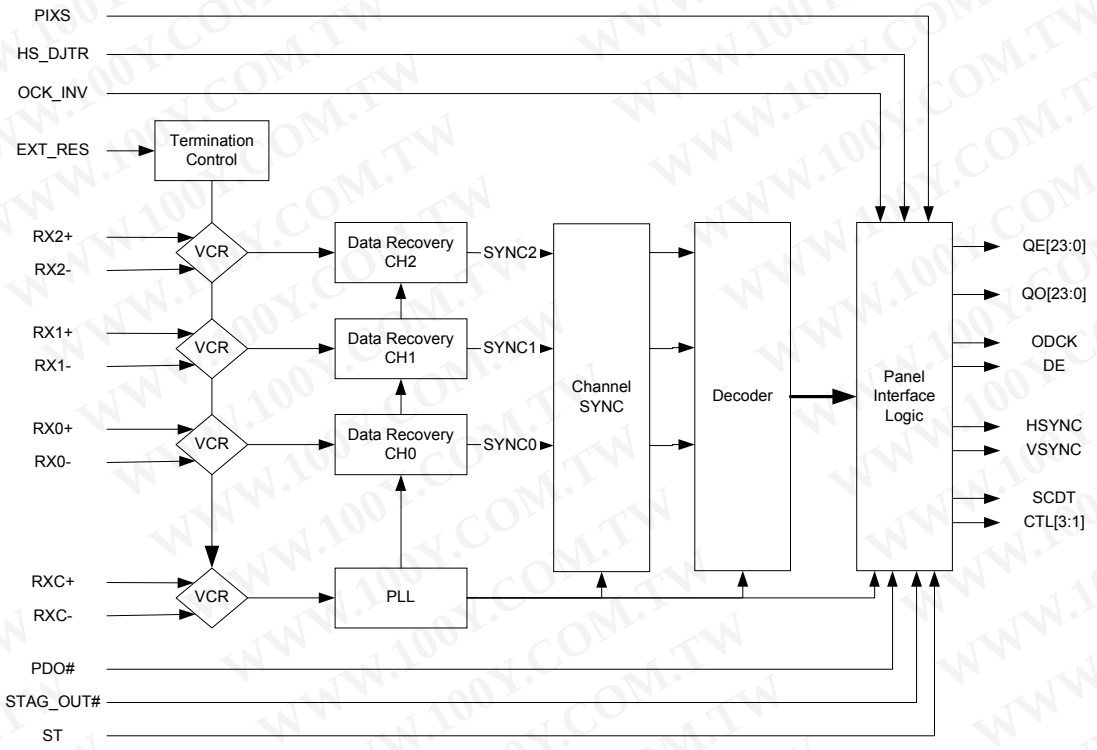


Figure 2. Functional Block Diagram

The PanelLink TMDS core accepts as inputs the three TMDS differential data lines and the differential clock. The core senses the signals on the link and properly decodes them providing accurate pixel data. The core outputs the necessary sync signals (HSYNC, VSYNC), clock (ODCK), and a DE signal that goes high when the active region of the video is present.

The SCDT signal is output when there is active video on the DVI link and the PLL in the TMDS has locked on to the video. SCDT can be used to trigger external circuitry, indicating that an active video signal is present or used to place the device in power down when no signal is present (by tying it to PD#). The EXT_RES component is used for impedance matching.

Electrical Specifications

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}[1]	Supply Voltage 3.3V	-0.3		4.0	V
V_I	Input Voltage	-0.3		V_{CC}+ 0.3	V
V_O[2]	Output Voltage	-0.3		V_{CC}+ 0.3	V
T_J	Junction Temperature			125	°C
T_{STG}	Storage Temperature	-65		150	°C

Notes
1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{CCN}	Supply Voltage Noise			100	mV_{P-P}
T_A	Ambient Temperature (with power applied)	0	25	70	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)			29	°C/W

Notes
1. Airflow at 0m/s. Package not soldered. With E-Pad soldered to landing pad θ_{JA} drops to 21°C/W.

Digital I/O Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		2			V
V_{IL}	Low-level Input Voltage				0.8	V
V_{OH}	High-level Output Voltage		2.4			V
V_{OL}	Low-level Output Voltage				0.4	V
V_{CINL}	Input Clamp Voltage[1]	I_{CL} = -18mA			GND -0.8	V
V_{CIPL}	Input Clamp Voltage[1]	I_{CL} = 18mA			IVCC + 0.8	V
V_{CONL}	Output Clamp Voltage[1]	I_{CL} = -18mA			GND -0.8	V
V_{COPL}	Output Clamp Voltage[1]	I_{CL} = 18mA			OVCC + 0.8	V
I_{OL}	Output Leakage Current	High Impedance	-10		10	µA

Note
1. Guaranteed by design. Voltage undershoot or overshoot cannot exceed absolute maximum conditions for a pulse of greater than 3 ns or one third of the clock cycle.

DC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OHD}	Output High Drive Data and Controls	V_{OUT} = 2.4 V; ST = 1 ST = 0	7.4 3.8	12.6 6.4	18.2 9.2	mA
I_{OLD}	Output Low Drive Data and Controls	V_{OUT} = 0.8 V; ST = 1 ST = 0	-11.1 -5.5	-12.6 -6.4	-13.6 -6.9	mA
		V_{OUT} = 0.4 V; ST = 1 ST = 0	-6.3 -3.2	-6.9 -3.5	-7.6 -3.8	mA
I_{OHC}	ODCK, DE High Drive	V_{OUT} = 2.4 V; ST = 1 ST = 0	14.7 7.5	23.8 11.5	34.3 17.6	mA
I_{OLC}	ODCK, DE Low Drive	V_{OUT} = 0.8V; ST = 1 ST = 0	-21.2 -11.1	-26.7 -12.5	-27.5 -13.9	mA
		V_{OUT} = 0.4 V; ST = 1 ST = 0	-12.3 -6.2	-13.6 -6.8	-15.9 -7.6	mA
V_{ID}	Differential Input Voltage Single Ended Amplitude		75		1000	mV
I_{PD}	Power-down Current	PD#=LOW, No RXC± input			1	mA
I_{CLKI}	Power-down Current	PD#=HIGH, No RXC± input			3	mA
I_{PDO}	Receiver Supply Current with Outputs Powered Down	ODCK=82.5MHz, Two pixel per clock mode C_{LOAD} = 10pF R_{EXT_SWING} = 510Ω PDO# = LOW			133	mA
I_{CCR}	Receiver Supply Current	ODCK=82.5MHz, Two pixel per clock mode C_{LOAD}= 10pF R_{EXT_SWING} = 510Ω Typical Pattern[1]			240	mA
		ODCK=82.5MHz, 0°C Two pixel per clock mode C_{LOAD} = 10pF R_{EXT_SWING} = 510Ω Worst Case Pattern[2]			280	mA

Notes

1. The Typical Pattern contains a gray scale area, checkerboard area, and text.
2. The Worst Case Pattern consists of a black and white checkerboard pattern; each checker is two pixels wide.
3. Asserting PD# to LOW disables all internal logic and outputs, including SCDT and clock detect functions.

AC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{DPS}	Intra-Pair (+ to -) Differential Input Skew[1]	165MHz			245	ps
T_{CCS}	Channel to Channel Differential Input Skew[1]	165MHz			4	ns
T_{IJIT}	Worst Case Differential Input Clock Jitter tolerance[2,3]	65 MHz			465	ps
		112 MHz			270	ps
		165 MHz			182	ps
D_{LHT}	Low-to-High Transition Time: Data and Controls (70°C, 82.5 MHz, two pixels per clock, PIXS=1)	C_L = 10pF; ST = 1			2.6	ns
		C_L = 5pF; ST = 0			2.7	ns
	Low-to-High Transition Time: Data and Controls (70°C, 165 MHz, one pixel per clock, PIXS=0)	C_L = 10pF; ST = 1			2.4	ns
		C_L = 5pF; ST = 0			3.0	ns
	Low-to-High Transition Time: ODCK (70°C, 82.5 MHz, two pixels per clock, PIXS=1)	C_L = 10pF; ST = 1			1.3	ns
		C_L = 5pF; ST = 0			1.7	ns
	Low-to-High Transition Time: ODCK (70°C, 165 MHz, one pixel per clock, PIXS=0)	C_L = 10pF; ST = 1			1.4	ns
		C_L = 5pF; ST = 0			1.7	ns
D_{HLT}	High-to-Low Transition Time: Data and Controls (70°C, 82.5 MHz, two pixels per clock, PIXS=1)	C_L = 10pF; ST = 1			2.8	ns
		C_L = 5pF; ST = 0			3.4	ns
	High-to-Low Transition Time: Data and Controls (70°C, 165 MHz, one pixel per clock, PIXS=0)	C_L = 10pF; ST = 1			2.3	ns
		C_L = 5pF; ST = 0			3.3	ns
	High-to-Low Transition Time: ODCK (70°C, 82.5 MHz, two pixels per clock, PIXS=1)	C_L = 10pF; ST = 1			1.1	ns
		C_L = 5pF; ST = 0			1.5	ns
	High-to-Low Transition Time: ODCK (70°C, 165 MHz, one pixel per clock, PIXS=0)	C_L = 10pF; ST = 1			1.2	ns
		C_L = 5pF; ST = 0			1.5	ns
T_{SETUP}	Data, DE, VSYNC, HSYNC, and CTL[3:1] Setup Time to ODCK falling edge (OCK_INV = 0) or to ODCK rising edge (OCK_INV = 1) at 165 MHz	C_L = 10pF; ST = 1	0.9 (1.4)[6]			ns
		C_L = 5pF; ST = 0	0.7 (0.5)[6]			ns
T_{HOLD}	Data, DE, VSYNC, HSYNC, and CTL[3:1] Hold Time from ODCK falling edge (OCK_INV = 0) or from ODCK rising edge (OCK_INV = 1) at 165 MHz	C_L = 10pF; ST = 1	2.7 (2.3)[6]			ns
		C_L = 5pF; ST = 0	3.0 (2.6)[6]			ns
R_{CIP}	ODCK Cycle Time[1] (one pixel per clock)		6.06		40	ns
F_{CIP}	ODCK Frequency[1] (one pixel per clock)		25		165	MHz
R_{CIP}	ODCK Cycle Time[1] (two pixels per clock)		12.1		80	ns
F_{CIP}	ODCK Frequency[1] (two pixels per clock)		12.5		82.5	MHz
R_{CIH}	ODCK High Time[4] 165 MHz, one pixel per clock, PIXS=0.	C_L = 10pF; ST = 1	1.7			ns
		C_L = 5pF; ST = 0	1.3			ns
R_{CIL}	ODCK Low Time[4]	C_L = 10pF; ST = 1	2.0			ns
		C_L = 5pF; ST = 0	1.4			ns
T_{PDL}	Delay from PD# / PDO# Low to high impedance outputs[1]				10	ns
T_{HSC}	Link disabled (DE inactive) to SCDT low[1]			100		ms
	Link disabled (Tx power down) to SCDT low[5]				250	ms
T_{FSC}	Link enabled (DE active) to SCDT high[1]			25	40	DE edges
T_{CLKPD}	Delay from RXC+ Inactive to high impedance outputs	RXC+ = 25MHz			10	µs
T_{CLKPU}	Delay from RXC+ active to data active	RXC+ = 25MHz			100	µs
T_{ST}	ODCK high to even data output[1]			0.25		R_{CIP}

Notes on previous table:

1. Guaranteed by design.
2. Jitter defined per DVI 1.0 Specification, Section 4.6 – Jitter Specification.
3. Jitter measured with Clock Recovery Unit per DVI 1.0 Specification, Section 4.7 – Electrical Measurement Procedures.
4. Output clock duty cycle is independent of the differential input clock duty cycle and the IDCK duty cycle.
5. Measured with transmitter powered down.
6. Value in parentheses is specified with OCK_INV=1.

Setup and Hold Timings for Data Rates other than 165 MHz

The measurements shown above are minimum setup and hold timings based on the maximum data rate of 165 MHz. To estimate the setup and hold times for slower data rates (for either different resolutions or two pixel per clock mode), the following formula can be used:

Time (at new frequency) = Time (165 MHz) + (Clock Period at new frequency – Clock Period at 165 MHz)/2

For the case of high strength output (ST=1) with a 10 pf load, and using the standard ODCK (OCK_INV = 0), Table 1 shows the minimum set up and hold times for other speeds as follows:

Table 1. Setup and Hold Times at Various Data Rates

Data Rate (MHz)	Clock (ns)	Setup (ns)	Hold (ns)	
112	8.9	2.3	4.1	SXGA one pixel per clock
56	17.9	6.8	8.6	SXGA two pixels per clock
135	7.4	1.6	3.4	SXGA+ one pixel per clock
67.5	14.8	5.3	7.1	SXGA+ two pixels per clock
82.5	12.1	3.9	5.7	UXGA two pixels per clock

Timing Diagrams

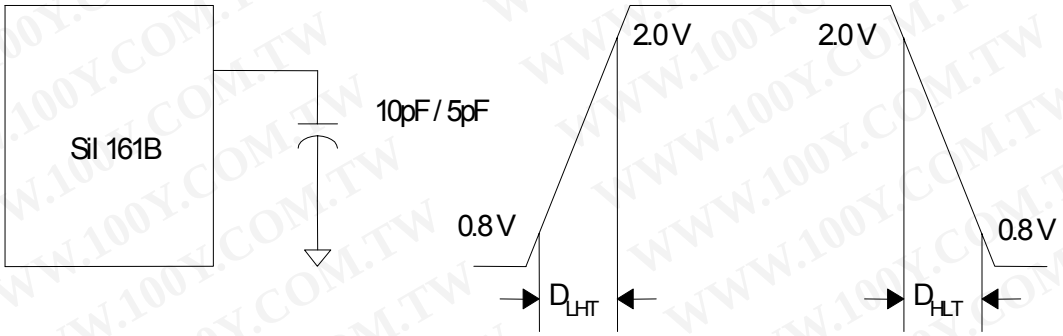


Figure 3. Digital Output Transition Times

Note:
1. 10pF loading used at ST=1 and 5pF loading using at ST=0

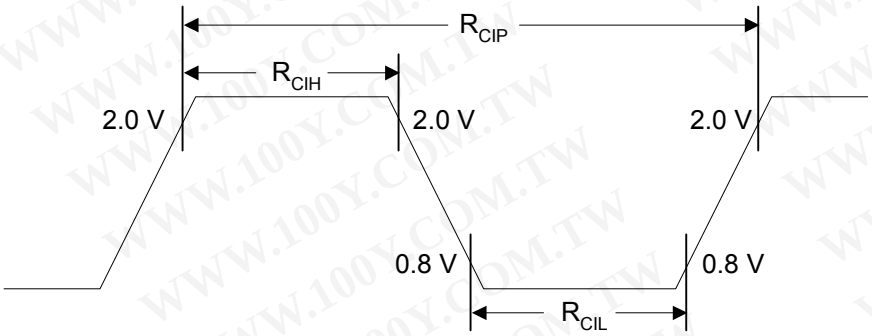


Figure 4. Receiver Clock Cycle/High/Low Times

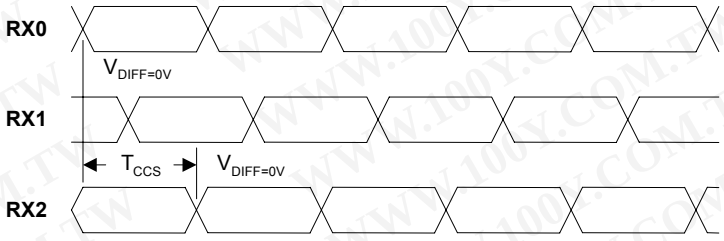


Figure 5. Channel-to-Channel Skew Timing

Output Timing

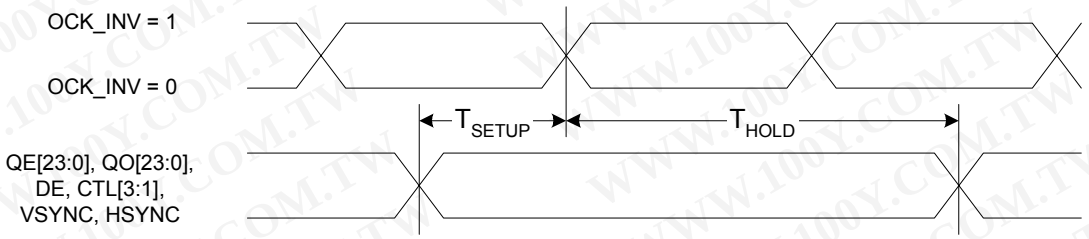


Figure 6. Output Setup/Hold Timings

Note
1. Output Data, DE and Control Signals Setup/Hold Times – to ODCK Falling Edge when OCK_INV = 0, or to ODCK Rising Edge when OCK_INV = 1

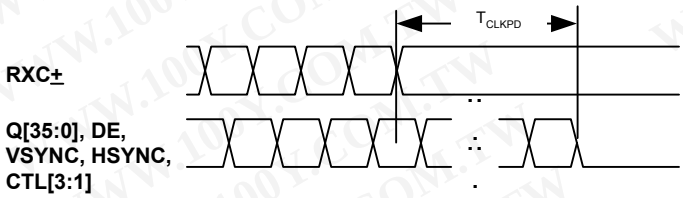


Figure 7. Output Signals Disabled Timing from Clock Inactive

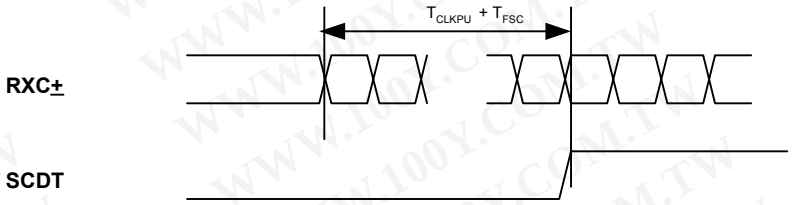


Figure 8. Wake-Up on Clock Detect

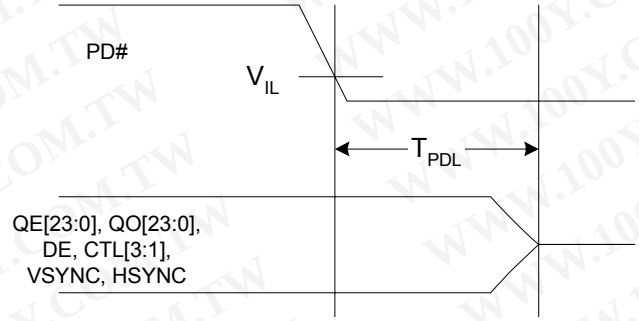


Figure 9. Output Signals Disabled Timing from PD# Active

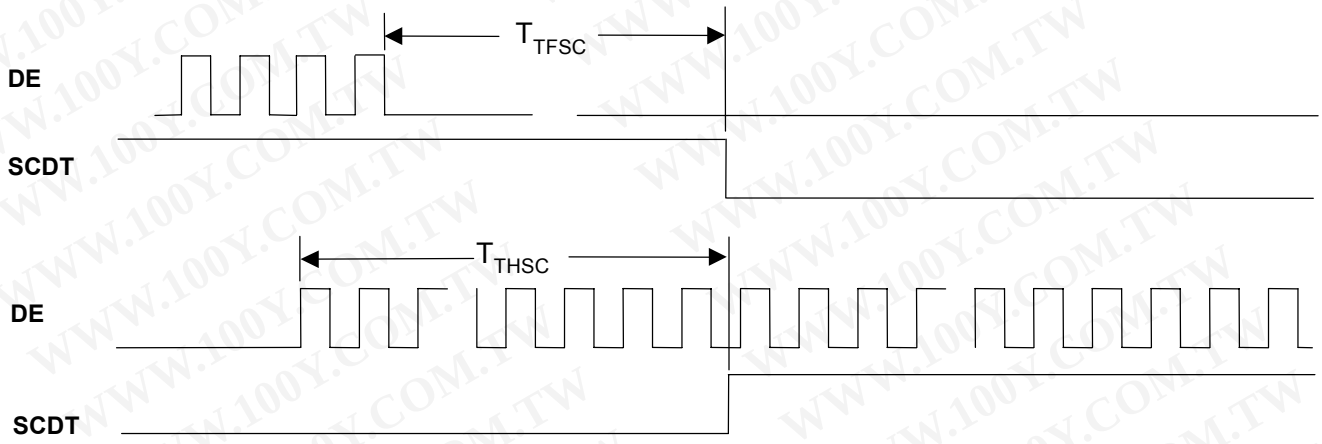


Figure 10. SCDT Timing from DE Inactive or Active

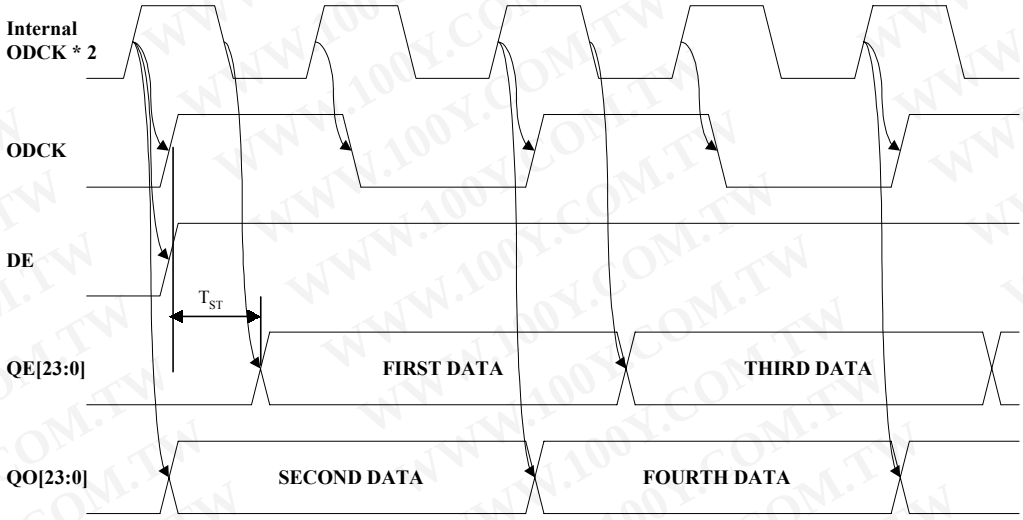


Figure 11. Two Pixels per Clock Staggered Output Timing Diagram

Pin Descriptions

Output Pins

Pin Name	Pin #	Type	Description
QE23-QE0	See SiI 161B Pin Diagram	Out	Output Even Data[23:0] corresponds to 24-bit pixel data for one pixel per clock input mode and to the first 24-bit pixel data for two pixels per clock mode. Output data is synchronized with output data clock (ODCK). Refer to the TFT Panel Data Mapping section, which tabulates the relationship between the input data to the transmitter and output data from the receiver. A low level on PD# or PDO# will put the output drivers into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground.
QO23-QO0	See SiI 161B Pin Diagram	Out	Output Odd Data[23:0] corresponds to the second 24-bit pixel data for two pixels per clock mode. During one pixel per clock mode, these outputs are driven low. Output data is synchronized with output data clock (ODCK). Refer to the TFT Panel Data Mapping section, which tabulates the relationship between the input data to the transmitter and output data from the receiver. A low level on PD# or PDO# will put the output drivers into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground.
ODCK	44	Out	Output Data Clock. This output can be inverted using the OCK_INV pin. A low level on PD# or PDO# will put the output driver into a high impedance (tri-state) mode. A weak internal pull-down device brings the output to ground.
DE	46	Out	Output Data Enable. This signal qualifies the active data area. A HIGH level signifies active display time and a LOW level signifies blanking time. This output signal is synchronized with the output data. A low level on PD# or PDO# will put the output driver into a high impedance (tri-state) mode. A weak internal pull-down device brings the output to ground.
HSYNC VSYNC CTL1 CTL2 CTL3	48 47 40 41 42	Out Out Out Out Out	Horizontal Sync output control signal. Vertical Sync output control signal. General output control signal 1. This output is **not** powered down by PDO#. General output control signal 2. General output control signal 3. A low level on PD# or PDO# will put the output drivers (except CTL1 by PDO#) into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground.

Configuration Pins

Pin Name	Pin #	Type	Description
OCK_INV	100	In	ODCK Polarity. A LOW level selects normal ODCK output. A HIGH level selects inverted ODCK output. All other output signals are unaffected by this pin. They will maintain the same timing no matter the setting of OCK_INV pin
PIXS	4	In	Pixel Select. A LOW level indicates one pixel (up to 24-bits) per clock mode using QE[23:0]. A HIGH level indicates two pixels (up to 48-bits) per clock mode using QE[23:0] for first pixel and QO[23:0] for second pixel.
STAG_OUT#	7	In	Staggered Output. A HIGH level selects normal simultaneous outputs on all odd and even data lines. A LOW level selects staggered output drive. This function is only available in two pixels per clock mode.
ST	3	In	Output Drive. A HIGH level selects HIGH output drive strength. A LOW level selects LOW output drive strength.
HS_DJTR	1	In	This pin enables/disable the HSYNC de-jitter function. To enable the HSYNC function this pin should be tied high. To disable the HSYNC de-jitter function and when using in a Single Link SiI 161A pin compatible application, this pin should be tied low.

Power Management Pins

Pin Name	Pin #	Type	Description
SCDT	8	Out	Sync Detect. A HIGH level is outputted when DE is actively toggling indicating that the link is alive. A LOW level is outputted when DE is inactive, indicating the link is down. Can be connected to PDO# to power down the outputs when DE is not detected. The SCDT output itself, however, remains in the active mode at all times.
PDO#	9	In	Output Driver Power Down (active LOW). A HIGH level indicates normal operation. A LOW level puts all the output drivers only (except SCDT and CTL1) into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground. PDO# is a sub-set of the PD# description. The chip is not in power-down mode with this pin. SCDT and CTL1 are not tri-stated by this pin.
PD#	2	In	Power Down (active LOW). A HIGH level indicates normal operation. A LOW level indicates power down mode. During power down mode, all the output drivers are put into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground. Additionally, all analog logic is powered down, and all inputs are disabled. Asserting PD# to LOW disables all internal logic and outputs, including SCDT and clock detect functions.

Differential Signal Data Pins

Pin Name	Pin #	Type	Description
RX0+ RX0- RX1+ RX1- RX2+ RX2-	90 91 85 86 80 81	Analog Analog Analog Analog Analog Analog	Receiver Differential Data Pins. TMDS Low Voltage Differential Signal input data pairs.
RXC+ RXC-	93 94	Analog Analog	Receiver Differential Clock Pins. TMDS Low Voltage Differential Signal input clock pair.
EXT_RES	96	Analog	Impedance Matching Control. An external 390Ω resistor must be connected between AVCC and this pin.

Reserved Pin

Pin Name	Pin #	Type	Description
RESERVED	99	In	Reserved Pin. Must be tied HIGH for normal operation.

Power and Ground Pins

Pin Name	Pin #	Type	Description
VCC	6,38,67	Power	Digital Core VCC, must be set to 3.3V.
GND	5,39,68	Ground	Digital Core GND.
OVCC	18,29,43,57,78	Power	Output VCC, must be set to 3.3V.
OGND	19,28,45,58,76	Ground	Output GND.
AVCC	82,84,88,95	Power	Analog VCC must be set to 3.3V.
AGND	79,83,87,89,92	Ground	Analog GND.
PVCC	97	Power	PLL Analog VCC must be set to 3.3V.
PGND	98	Ground	PLL Analog GND.

Feature Information

The SiI 161B is pin-compatible with the SiI 161A and shares many of the same features. It also includes two new features: HSYNC de-jitter and power down when the clock is inactive.

HSYNC De-jitter Function

HSYNC de-jitter enables the 161B to operate properly even when the HSYNC signal contains jitter. Pin 1 is used to enable or disable this circuit. Tying this pin high enables the HSYNC de-jitter circuitry while tying it low disables the circuitry. The HSYNC de-jitter circuitry operates normally with most VESA standard timings. In most modes, HSYNC and VSYNC total times and front and back porch times are multiples of four pixel times. If the timings are not a multiple of four, operation is not guaranteed and the HSYNC de-jitter circuitry should be turned off. When HSYNC de-jitter is enabled, the circuitry will introduce anywhere from 1 to 4 CLK delays in the HSYNC signal relative to the output data.

Clock Detect Function

The SiI 161B includes a new power saving feature: power down with clock detect circuit. The SiI 161B will go into a low power mode when there is no video clock coming from the transmitter. In this mode, the entire chip is powered down except the clock detect circuitry. During this mode, digital I/O are set to a high impedance (tri-state) mode. The SCDT pin is driven LOW. A weak internal pull-down device brings each output to ground. The device power down and wake-up times are shown in Figure 7 and Figure 8.

OCK_INV Function

OCK_INV affects only the phase of the clock output as indicated in Figure 12. OCK_INV does not change the timing for the internal data latching. This timing is shown in Figure 6.

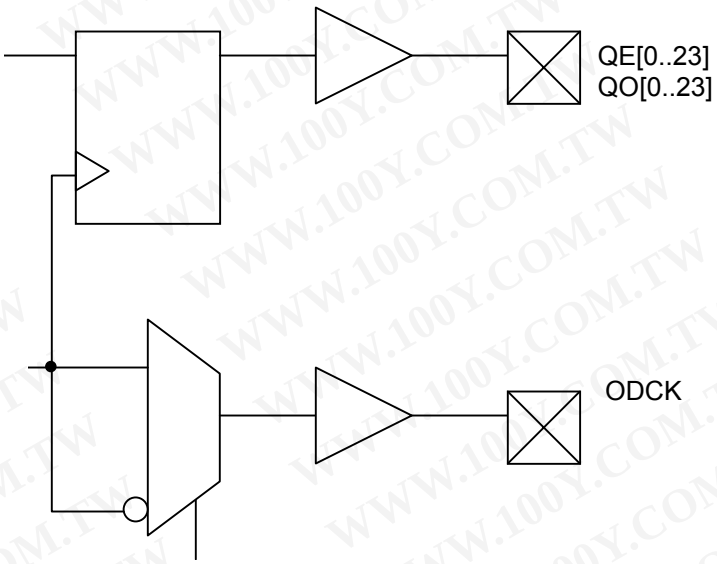


Figure 12. Block Diagram for OCK_INV

TFT Panel Data Mapping

Table 2 summarizes the output data mapping in one pixel per clock mode for the SiI 161B. This output data mapping is dependent upon the PanelLink transmitters having the exact same type of input data mappings.

Table 3 summarizes the output data mapping in two pixels per clock mode. More detailed mapping information is found on the following pages. Refer to application note SiI-AN-0007 for DSTN applications.

Note that the data configuration of the receiver is independent of the configuration of the transmitter. The data is always transmitted across the link in the same format, regardless of the selection of 12, 24 or 48 bit input format. Therefore, display-side designers do not need to know how the transmitter is configured. Receiver configuration is for compatibility with the display, not the transmitter.

Table 2. One Pixel per Clock Mode Data Mapping

DATA	SiI 161B	
	One Pixel per Clock Output	
	18bpp	24bpp
BLUE[7:0]	QE[7:2]	QE[7:0]
GREEN[7:0]	QE[15:10]	QE[15:8]
RED[7:0]	QE[23:18]	QE[23:16]

Table 3. Two Pixel per Clock Mode Data Mapping

DATA	SiI 161B	
	Two Pixel per Clock Output	
	18bpp	24bpp
BLUE[7:0] – 0	QE[7:2]	QE[7:0]
GREEN[7:0] – 0	QE[15:10]	QE[15:8]
RED[7:0] – 0	QE[23:18]	QE[23:16]
BLUE[7:0] – 1	QO[7:2]	QO[7:0]
GREEN[7:0] – 1	QO[15:10]	QO[15:8]
RED[7:0] – 1	QO[23:18]	QO[23:16]

Note: SiI143B, SiI151B, SiI153B and SiI 161B all have the same pinout. The pin assignments shown in the following tables should also be used for these other receivers.

Table 4. One Pixel per Clock Input/Output TFT Mode – VESA P&D and FPDI-2 Compliant

TFT VGA Output		Tx Input Data		Rx Output Data		TFT Panel Input	
24-bpp	18-bpp	160	164	161B	141B	24-bpp	18-bpp
B0		DIE0	D0	QE0	Q0	B0	
B1		DIE1	D1	QE1	Q1	B1	
B2	B0	DIE2	D2	QE2	Q2	B2	B0
B3	B1	DIE3	D3	QE3	Q3	B3	B1
B4	B2	DIE4	D4	QE4	Q4	B4	B2
B5	B3	DIE5	D5	QE5	Q5	B5	B3
B6	B4	DIE6	D6	QE6	Q6	B6	B4
B7	B5	DIE7	D7	QE7	Q7	B7	B5
G0		DIE8	D8	QE8	Q8	G0	
G1		DIE9	D9	QE9	Q9	G1	
G2	G0	DIE10	D10	QE10	Q10	G2	G0
G3	G1	DIE11	D11	QE11	Q11	G3	G1
G4	G2	DIE12	D12	QE12	Q12	G4	G2
G5	G3	DIE13	D13	QE13	Q13	G5	G3
G6	G4	DIE14	D14	QE14	Q14	G6	G4
G7	G5	DIE15	D15	QE15	Q15	G7	G5
R0		DIE16	D16	QE16	Q16	R0	
R1		DIE17	D17	QE17	Q17	R1	
R2	R0	DIE18	D18	QE18	Q18	R2	R0
R3	R1	DIE19	D19	QE19	Q19	R3	R1
R4	R2	DIE20	D20	QE20	Q20	R4	R2
R5	R3	DIE21	D21	QE21	Q21	R5	R3
R6	R4	DIE22	D22	QE22	Q22	R6	R4
R7	R5	DIE23	D23	QE23	Q23	R7	R5
Shift CLK	Shift CLK	IDCK	IDCK	ODCK	ODCK	Shift CLK	Shift CLK
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
DE	DE	DE	DE	DE	DE	DE	DE

For 18-bit mode, the Flat Panel Graphics Controller interfaces to the Transmitter exactly the same as in the 24-bit mode; however, 6 bits per channel (color) are used instead of 8. It is recommended that unused data bits be tied low. As can be seen from the above table, the data mapping for less than 24-bit per pixel interfaces are MSB justified. The data is sent during active display time while the control signals are sent during blank time. Note that the three data channels (CH0, CH1, CH2) are mapped to Blue, Green and Red data respectively.

Table 5. Two Pixels per Clock Input/Output TFT Mode

TFT VGA Output		Tx Input Data	Rx Output Data	TFT Panel Input	
24-bpp	18-bpp	160	161B	24-bpp	18-bpp
B0 – 0		DIE0	QE0	B0 – 0	
B1 – 0		DIE1	QE1	B1 – 0	
B2 – 0	B0 – 0	DIE2	QE2	B2 – 0	B0 – 0
B3 – 0	B1 – 0	DIE3	QE3	B3 – 0	B1 – 0
B4 – 0	B2 – 0	DIE4	QE4	B4 – 0	B2 – 0
B5 – 0	B3 – 0	DIE5	QE5	B5 – 0	B3 – 0
B6 – 0	B4 – 0	DIE6	QE6	B6 – 0	B4 – 0
B7 – 0	B5 – 0	DIE7	QE7	B7 – 0	B5 – 0
G0 – 0		DIE8	QE8	G0 – 0	
G1 – 0		DIE9	QE9	G1 – 0	
G2 – 0	G0 – 0	DIE10	QE10	G2 – 0	G0 – 0
G3 – 0	G1 – 0	DIE11	QE11	G3 – 0	G1 – 0
G4 – 0	G2 – 0	DIE12	QE12	G4 – 0	G2 – 0
G5 – 0	G3 – 0	DIE13	QE13	G5 – 0	G3 – 0
G6 – 0	G4 – 0	DIE14	QE14	G6 – 0	G4 – 0
G7 – 0	G5 – 0	DIE15	QE15	G7 – 0	G5 – 0
R0 – 0		DIE16	QE16	R0 – 0	
R1 – 0		DIE17	QE17	R1 – 0	
R2 – 0	R0 – 0	DIE18	QE18	R2 – 0	R0 – 0
R3 – 0	R1 – 0	DIE19	QE19	R3 – 0	R1 – 0
R4 – 0	R2 – 0	DIE20	QE20	R4 – 0	R2 – 0
R5 – 0	R3 – 0	DIE21	QE21	R5 – 0	R3 – 0
R6 – 0	R4 – 0	DIE22	QE22	R6 – 0	R4 – 0
R7 – 0	R5 – 0	DIE23	QE23	R7 – 0	R5 – 0
B0 – 1		DIO0	QO0	B0 – 1	
B1 – 1		DIO1	QO1	B1 – 1	
B2 – 1	B0 – 1	DIO2	QO2	B2 – 1	B0 – 1
B3 – 1	B1 – 1	DIO3	QO3	B3 – 1	B1 – 1
B4 – 1	B2 – 1	DIO4	QO4	B4 – 1	B2 – 1
B5 – 1	B3 – 1	DIO5	QO5	B5 – 1	B3 – 1
B6 – 1	B4 – 1	DIO6	QO6	B6 – 1	B4 – 1
B7 – 1	B5 – 1	DIO7	QO7	B7 – 1	B5 – 1
G0 – 1		DIO8	QO8	G0 – 1	
G1 – 1		DIO9	QO9	G1 – 1	
G2 – 1	G0 – 1	DIO10	QO10	G2 – 1	G0 – 1
G3 – 1	G1 – 1	DIO11	QO11	G3 – 1	G1 – 1
G4 – 1	G2 – 1	DIO12	QO12	G4 – 1	G2 – 1
G5 – 1	G3 – 1	DIO13	QO13	G5 – 1	G3 – 1
G6 – 1	G4 – 1	DIO14	QO14	G6 – 1	G4 – 1
G7 – 1	G5 – 1	DIO15	QO15	G7 – 1	G5 – 1
R0 – 1		DIO16	QO16	R0 – 1	
R1 – 1		DIO17	QO17	R1 – 1	
R2 – 1	R0 – 1	DIO18	QO18	R2 – 1	R0 – 1
R3 – 1	R1 – 1	DIO19	QO19	R3 – 1	R1 – 1
R4 – 1	R2 – 1	DIO20	QO20	R4 – 1	R2 – 1
R5 – 1	R3 – 1	DIO21	QO21	R5 – 1	R3 – 1
R6 – 1	R4 – 1	DIO22	QO22	R6 – 1	R4 – 1
R7 – 1	R5 – 1	DIO23	QO23	R7 – 1	R5 – 1
ShiftClk/2	ShiftClk/2	IDCK	ODCK	Shift CLK	Shift CLK
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
DE	DE	DE	DE	DE	DE

Table 6. 24-bit One Pixel per Clock Input with 24-bit Two Pixels per Clock Output TFT Mode

TFT VGA Output	Tx Input Data		Rx Output Data	TFT Panel Input
24-bpp	160	164	161B	24-bpp
B0	DIE0	D0	QE0	B0 – 0
B1	DIE1	D1	QE1	B1 – 0
B2	DIE2	D2	QE2	B2 – 0
B3	DIE3	D3	QE3	B3 – 0
B4	DIE4	D4	QE4	B4 – 0
B5	DIE5	D5	QE5	B5 – 0
B6	DIE6	D6	QE6	B6 – 0
B7	DIE7	D7	QE7	B7 – 0
G0	DIE8	D8	QE8	G0 – 0
G1	DIE9	D9	QE9	G1 – 0
G2	DIE10	D10	QE10	G2 – 0
G3	DIE11	D11	QE11	G3 – 0
G4	DIE12	D12	QE12	G4 – 0
G5	DIE13	D13	QE13	G5 – 0
G6	DIE14	D14	QE14	G6 – 0
G7	DIE15	D15	QE15	G7 – 0
R0	DIE16	D16	QE16	R0 – 0
R1	DIE17	D17	QE17	R1 – 0
R2	DIE18	D18	QE18	R2 – 0
R3	DIE19	D19	QE19	R3 – 0
R4	DIE20	D20	QE20	R4 – 0
R5	DIE21	D21	QE21	R5 – 0
R6	DIE22	D22	QE22	R6 – 0
R7	DIE23	D23	QE23	R7 – 0
			QO0	B0 – 1
			QO1	B1 – 1
			QO2	B2 – 1
			QO3	B3 – 1
			QO4	B4 – 1
			QO5	B5 – 1
			QO6	B6 – 1
			QO7	B7 – 1
			QO8	G0 – 1
			QO9	G1 – 1
			QO10	G2 – 1
			QO11	G3 – 1
			QO12	G4 – 1
			QO13	G5 – 1
			QO14	G6 – 1
			QO15	G7 – 1
			QO16	R0 – 1
			QO17	R1 – 1
			QO18	R2 – 1
			QO19	R3 – 1
			QO20	R4 – 1
			QO21	R5 – 1
			QO22	R6 – 1
			QO23	R7 – 1
Shift CLK	IDCK	IDCK	ODCK	Shift CLK/2
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
DE	DE	DE	DE	DE

Table 7. 18-bit One Pixel per Clock Input with 18-bit Two Pixels per Clock Output TFT Mode

TFT VGA Output	Tx Input Data		Tx Output Data		TFT Panel Input
18-bpp	160	164	161B	141B	18-bpp
	DIE0	D0	QE0		
	DIE1	D1	QE1		
B0	DIE2	D2	QE2	Q0	B0 – 0
B1	DIE3	D3	QE3	Q1	B1 – 0
B2	DIE4	D4	QE4	Q2	B2 – 0
B3	DIE5	D5	QE5	Q3	B3 – 0
B4	DIE6	D6	QE6	Q4	B4 – 0
B5	DIE7	D7	QE7	Q5	B5 – 0
	DIE8	D8	QE8		
	DIE9	D9	QE9		
G0	DIE10	D10	QE10	Q6	G0 – 0
G1	DIE11	D11	QE11	Q7	G1 – 0
G2	DIE12	D12	QE12	Q8	G2 – 0
G3	DIE13	D13	QE13	Q9	G3 – 0
G4	DIE14	D14	QE14	Q10	G4 – 0
G5	DIE15	D15	QE15	Q11	G5 – 0
	DIE16	D16	QE16		
	DIE17	D17	QE17		
R0	DIE18	D18	QE18	Q12	R0 – 0
R1	DIE19	D19	QE19	Q13	R1 – 0
R2	DIE20	D20	QE20	Q14	R2 – 0
R3	DIE21	D21	QE21	Q15	R3 – 0
R4	DIE22	D22	QE22	Q16	R4 – 0
R5	DIE23	D23	QE23	Q17	R5 – 0
			QO0		
			QO1		
			QO2	Q18	B0 – 1
			QO3	Q19	B1 – 1
			QO4	Q20	B2 – 1
			QO5	Q21	B3 – 1
			QO6	Q22	B4 – 1
			QO7	Q23	B5 – 1
			QO8		
			QO9		
			QO10	Q24	G0 – 1
			QO11	Q25	G1 – 1
			QO12	Q26	G2 – 1
			QO13	Q27	G3 – 1
			QO14	Q28	G4 – 1
			QO15	Q29	G5 – 1
			QO16		
			QO17		
			QO18	Q30	R0 – 1
			QO19	Q31	R1 – 1
			QO20	Q32	R2 – 1
			QO21	Q33	R3 – 1
			QO22	Q34	R4 – 1
			QO23	Q35	R5 – 1
Shift CLK	IDCK	IDCK	ODCK	Shift CLK/2	Shift CLK/2
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
DE	DE	DE	DE	DE	DE

Table 8. Two Pixels per Clock Input with One Pixel per Clock Output TFT Mode

TFT VGA Output		Tx Input Data	Rx Output Data		TFT Panel Input	
24-bpp	18-bpp	160	161B	141B	24-bpp	18-bpp
B0 – 0		DIE0	QE0	Q0	B0	
B1 – 0		DIE1	QE1	Q1	B1	
B2 – 0	B0 – 0	DIE2	QE2	Q2	B2	B0
B3 – 0	B1 – 0	DIE3	QE3	Q3	B3	B1
B4 – 0	B2 – 0	DIE4	QE4	Q4	B4	B2
B5 – 0	B3 – 0	DIE5	QE5	Q5	B5	B3
B6 – 0	B4 – 0	DIE6	QE6	Q6	B6	B4
B7 – 0	B5 – 0	DIE7	QE7	Q7	B7	B5
G0 – 0		DIE8	QE8	Q8	G0	
G1 – 0		DIE9	QE9	Q9	G1	
G2 – 0	G0 – 0	DIE10	QE10	Q10	G2	G0
G3 – 0	G1 – 0	DIE11	QE11	Q11	G3	G1
G4 – 0	G2 – 0	DIE12	QE12	Q12	G4	G2
G5 – 0	G3 – 0	DIE13	QE13	Q13	G5	G3
G6 – 0	G4 – 0	DIE14	QE14	Q14	G6	G4
G7 – 0	G5 – 0	DIE15	QE15	Q15	G7	G5
R0 – 0		DIE16	QE16	Q16	R0	
R1 – 0		DIE17	QE17	Q17	R1	
R2 – 0	R0 – 0	DIE18	QE18	Q18	R2	R0
R3 – 0	R1 – 0	DIE19	QE19	Q19	R3	R1
R4 – 0	R2 – 0	DIE20	QE20	Q20	R4	R2
R5 – 0	R3 – 0	DIE21	QE21	Q21	R5	R3
R6 – 0	R4 – 0	DIE22	QE22	Q22	R6	R4
R7 – 0	R5 – 0	DIE23	QE23	Q23	R7	R5
B0 – 1		DIO0				
B1 – 1		DIO1				
B2 – 1	B0 – 1	DIO2				
B3 – 1	B1 – 1	DIO3				
B4 – 1	B2 – 1	DIO4				
B5 – 1	B3 – 1	DIO5				
B6 – 1	B4 – 1	DIO6				
B7 – 1	B5 – 1	DIO7				
G0 – 1		DIO8				
G1 – 1		DIO9				
G2 – 1	G0 – 1	DIO10				
G3 – 1	G1 – 1	DIO11				
G4 – 1	G2 – 1	DIO12				
G5 – 1	G3 – 1	DIO13				
G6 – 1	G4 – 1	DIO14				
G7 – 1	G5 – 1	DIO15				
R0 – 1		DIO16				
R1 – 1		DIO17				
R2 – 1	R0 – 1	DIO18				
R3 – 1	R1 – 1	DIO19				
R4 – 1	R2 – 1	DIO20				
R5 – 1	R3 – 1	DIO21				
R6 – 1	R4 – 1	DIO22				
R7 – 1	R5 – 1	DIO23				
ShiftClk/2	ShiftClk/2	IDCK	ODCK	ODCK	ShiftClk	ShiftClk
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
DE	DE	DE	DE	DE	DE	DE

Table 9. Output Clock Configuration by Typical Application

DF0	PIX	OCK_INV	PANEL	ODCK (frequency/data latch edge/mode)
0	0	0	TFT/16-bit DSTN	divide by 1 / negative / free running
0	0	1	TFT/16-bit DSTN	divide by 1 / positive / free running
0	1	0	TFT	divide by 2 / negative / free running
0	1	1	TFT	divide by 2 /positive / free running
1	0	0	24-bit DSTN	divide by 1 / negative / blanked low
1	0	1	**NONE**	divide by 1 / negative / blanked high
1	1	0	24-bit DSTN	divide by 2 / negative / blanked low
1	1	1	24-bit DSTN	divide by 4 / negative / blanked low

Note: DF0 is a signal available only on the SiI141B receiver. DSTN panels may be supported with the SiI 161B by running the extra blanked clock through an unused data pin. This works only at one pixel per clock mode, and only when the 24 data bits are not already used for pixel data. Such a solution also requires that the transmitter board design input the shift clock (the blanked clock for DSTN) into the same unused data pin. By using the SiI141B, DSTN panels may be driven without requiring any special connections on the transmitter side.

Design Recommendations

The following sections describe recommendations for robust board design with this PanelLink receiver. Designers should include provision for these circuits in their design, and adjust the specific passive component values according to the characterization results.

Differences Between SiI 161A and SiI 161B

While the SiI 161B is pin to pin compatible with the SiI 161A, there are minor differences in functions and suggested external component value. When designing the SiI 161B into an existing design, note that the recommended external resistor (EXT_RES) value has changed from 560 ohms to 390 ohms to match the impedance of a 50 ohm cable.

Pin 1 of the SiI 161A functions as a selection between Single Link and Dual Link mode. The SiI 161B does not support Dual Link operation. Instead pin 1 is used to enable or disable the HSYNC De-jitter function. For dual-link applications, please refer to the SiI163B Data Sheet.

Table 10 lists the differences between SiI 161A and SiI 161B.

Table 10. SiI 161A vs. SiI 161B Pin Differences

Pin/Function	SiI 161A	SiI 161B
Pin 1	S_D: to select Single/Dual Link mode. Pull high to select Dual Link and Pull low for Single Link.	HS_DJTR added to enable HSYNC De-jitter circuitry. Pull high to enable. Pull low to disable.
Pin 4	PIXS/M_S	Pin 4 is for PIXS only, since M_S for dual-link is not supported. See SiI 163B .
Pin 7	STAG_OUT# / SYNCO	Pin 7 is for STAG_OUT# only, since SYNCO for dual-link is not supported. See SiI 163B .
EXT_RES Resistor Value	560 ohms	390 ohms
SCDT	When PDO# is asserted, a pull-up resistor is needed on SCDT to assure high-level.	SCDT continues to drive high or low when PDO# is asserted. No need for pull-up.
HSYNC, VSYNC, CTL[1..3]	Dejitter circuit adds one pixel clock time to time from DE fall to first edge of these signals. This affects front-porch time for HSYNC and VSYNC.	Dejitter circuit improved. The DE-low to first-edge time for these signals is identical to the timing input to the transmitter.
Improved Output Drive Strength	Refer to 161A Data Sheet for specifics.	Output drive strength improved for these signals. Refer to DC Specifications on page 4. This improves output waveforms when driving multiple loads. Some designs may be able to change from ST=1 to ST=0.
Clock Detect for Lower Standby Power.	Receiver powers down when PDO# is asserted. SCDT asserts only when the chip detects the lack of DE pulses.	Receiver detects when the differential input clock has stopped and powers down the internals of the chip. Refer to I_{CLKI} in DC Specifications on page 4.
PDO# Low-Power Mode Improved	PDO# assertion powers down most of the chip.	Improved design powers down more active circuitry, resulting in lower power when PDO# is asserted.
Differential Input Capacitance Reduced		Improved eye diagram over 161A.
PD#, PDO#, STAG_OUT#	Pins were named: PD, PDO, STAG_OUT.	No functional change was made. Names were changed to clarify their “active low” sense.

Voltage Ripple Regulation

The power supply to VCC pins is very important to the proper operation of the receiver chips. Two examples of regulators are shown in Figure 13 and Figure 14.

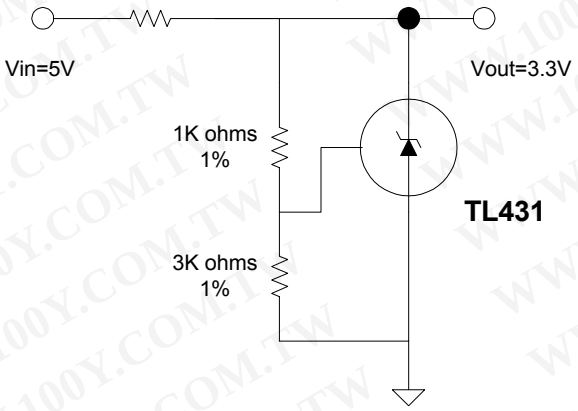


Figure 13. Voltage Regulation using TL431

Decoupling and bypass capacitors are also involved with power supply connections, as described in detail in Figure 16.

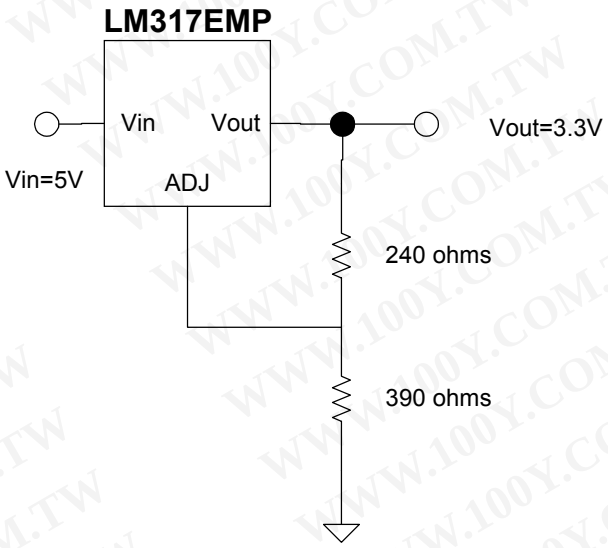


Figure 14. Voltage Regulation using LM317

Decoupling Capacitors

Designers should include decoupling and bypass capacitors at each power pin in the layout. These are shown schematically in Figure 16. Place these components as closely as possible to the PanelLink device pins, and avoid routing through vias if possible, as shown in Figure 15, which is representative of the various types of power pins on the receiver.

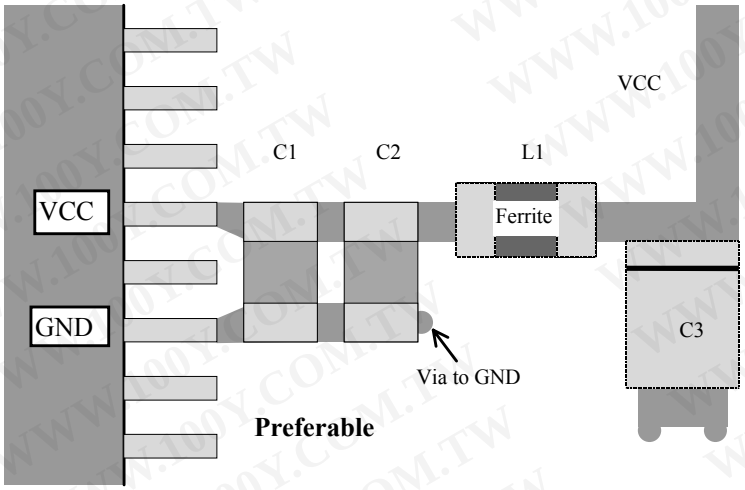


Figure 15. Decoupling and Bypass Capacitor Placement

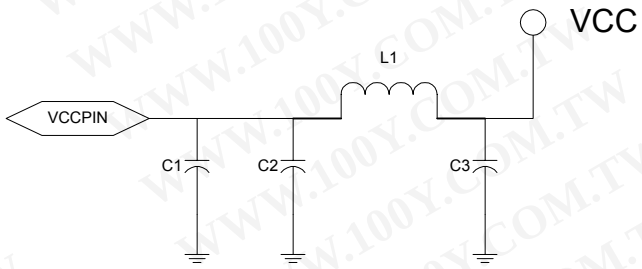


Figure 16. Decoupling and Bypass Schematic

Table 11. Recommended Components

C1	C2	C3	L1
100 – 300 pF	2.2 – 10 uF	10 uF	200+ ohms

The values shown in Table 11 are recommendations that should be adjusted according to the noise characteristics of the specific board-level design. Pins in one group (such as OVCC) may share L1 and C3, each pin having C1 placed as closely to the pin as possible.

Series Damping Resistors on Outputs

Series resistors are effective in lowering the data-related emissions and reducing reflections. Series resistors should be placed close to the output pins on the receiver chip, as shown in Figure 17.

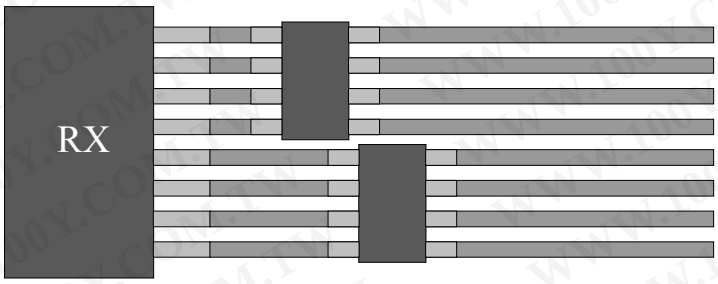


Figure 17. Receiver Output Series Damping Resistors

Receiver Layout

The receiver chip should be placed as closely as possible to the input connector which carries the TMDS signals. For a system using the industry-standard DVI connector (see http://www.ddwg.org), the differential lines should be routed as directly as possible from connector to receiver. PanelLink devices are tolerant of skews between differential pairs, so spiral skew compensation for path length differences is not required. Each differential pair should be routed together, minimizing the number of vias through which the signal lines are routed. An example of a DVI routing is shown in Figure 18.

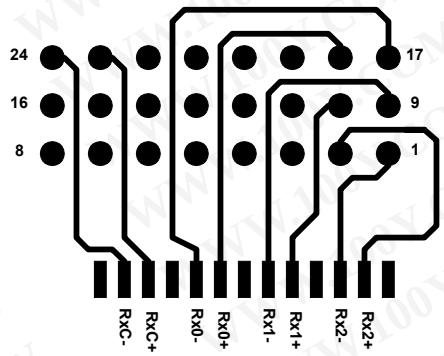


Figure 18. DVI to Receiver Routing - Top View

PCB Ground Planes

All ground pins on the device should be connected to the same, contiguous ground plane in the PCB. This helps to avoid ground loops and inductances from one ground plane segment to another. Such low-inductance ground paths are critical for return currents, which affect EMI performance. The entire ground plane surrounding the PanelLink receiver should be one piece, and include the ground vias for the DVI connector.

As defined in the DVI 1.0 Specification, the impedance of the traces between the connector and the receiver should be 100 ohms differentially, and close to 50 ohms single-ended. The 100 ohm requirement is to best match the differential impedance of the cable and connectors, to prevent reflections. The common mode currents are very small on the TMDS interface, so differential impedance is more important than single-ended.

Thermal Design Options

The SiI 161B is packaged in a thermally enhanced 100 pin TQFP with an exposed metal pad (7.5mm x 7.5 mm) on the package for improved thermal dissipation. With the minimal power consumption and heat dissipation of the SiI 161B, its exposed thermal pad does not require soldering to the PCB. Optionally, for improved thermal dissipation, the exposed thermal pad may be soldered to a thermal landing area on the PCB. Please refer to application note SiI-AN-0062-A, which includes information on the thermal characteristics of the SiI 161B.

Important: Do **not** place any vias or exposed signal traces beneath the exposed thermal metal pad of the SiI 161B on the PCB.

Staggered Outputs and Two Pixels per Clock

PanelLink receivers offer two features that can minimize the switching effects of the high-speed output data bus: two pixels per clock mode and staggered outputs.

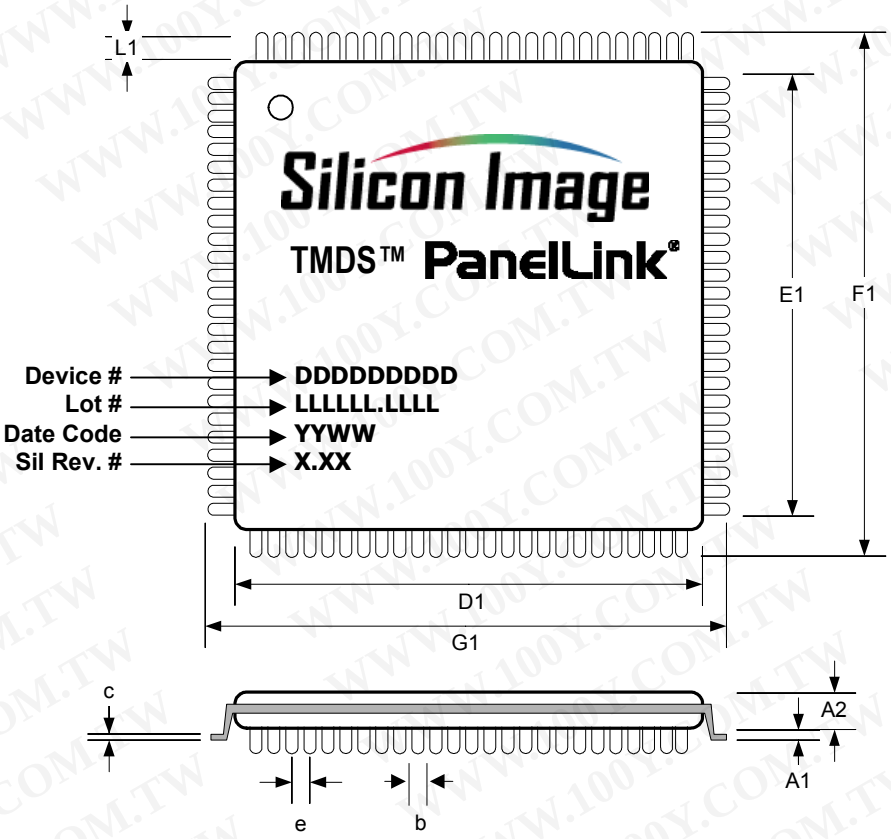
The receiver can output one or two pixels in each output clock cycle. By widening the bus to two pixels per clock whenever possible, the clock speed is halved and the switching period of the data signals themselves is twice as long as in one pixel per clock mode. Typically, SXGA-resolution and above LCD panels expect to be connected with a 36-bit or 48-bit bus, two pixels per clock. Most XGA-resolution and below LCD panels use an 18- to 24-bit one pixel per clock interface.

When in two pixel per clock mode, the STAG_OUT# pin on receivers provides an additional means of reducing simultaneous switching activity. When enabled (STAG_OUT# = Low), only half of the output data pins switch together. The other half are switched one quarter clock cycle later. Note that both pixel buses use the same clock. Therefore, the staggered bus will have one quarter clock cycle less setup time to the clock, and one quarter clock cycle more hold time. Board designers driving into another clocked chip should take this into account in their timing analysis.

Silicon Image recommends the use of STAG_OUT# and the two pixels per clock mode whenever possible.

Package

100-pin TQFP Package Dimensions and Marking Specification



JEDEC Package Code MS026-AED-HD

		typ	max
A	Thickness		1.20
A1	Stand-off		0.15
A2	Body Thickness	1.00	1.05
D1	Body Size	14.00	
E1	Body Size	12.00	
F1	Footprint	16.00	
G1	Footprint	16.00	
L1	Lead Length	1.00	
b	Lead Width	0.20	
c	Lead Thickness	0.20	
e	Lead Pitch	0.50	

Dimensions in millimeters.
Overall thickness A=A1+A2.

Device	Device Number DDDDDDDDD
Standard	SiI161BCT100
Pb-free	SiI161BCTG100

Legend	Description
LLLLLL.LLLL	Lot Number
YY	Year of Mfr
WW	Week of Mfr
X.XX	Revision Number

Figure 19. Package Diagram

Ordering Information

Standard Part Number: SiI161BCT100

Pb-Free Part Number: SiI161BCTG100 ('G' designates Pb-free packaging)

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