W78E65/W78E065A Data Sheet

Winbond Electronics Corp.

8-BIT MICROCONTROLLER

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1. GENERAL DESCRIPTION

The W78E65 is an 8-bit microcontroller which has an in-system programmable Flash EPROM for firmware updating. The instruction set of the W78E65 is fully compatible with the standard 8052. The W78E65 contains a 64K bytes of main ROM and a 4K bytes of auxiliary ROM which allows the contents of the 64KB main ROM to be updated by the loader program located at the 4KB auxiliary ROM; 256+1K bytes of on-chip RAM; four 8-bit bi-directional and bit-addressable I/O ports; an additional 4-bit port P4; three 16-bit timer/counters; a serial port. These peripherals are supported by a eight sources two-level interrupt capability. To facilitate programming and verification, the ROM inside the W78E65 allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

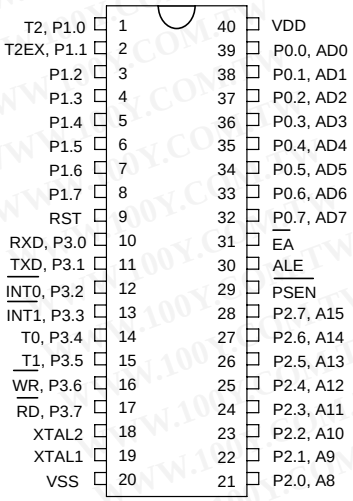
The W78E65 microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

2. FEATURES

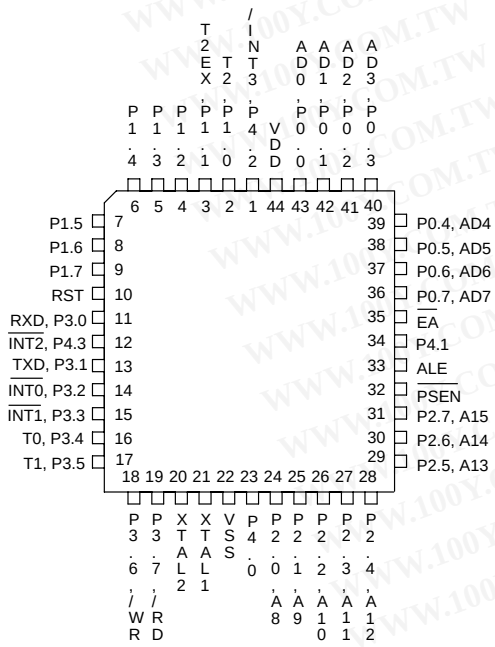
- Fully static design 8-bit CMOS microcontroller
- 64K bytes of in-system programmable Flash EPROM for Application Program (AP FLASH EPROM)
- 4K bytes of auxiliary ROM for Loader Program (LD FLASH EPROM)
- 256+1K bytes of on-chip RAM. (Including 1K bytes of AUX-RAM, software selectable)
- 64K bytes program memory address space and 64K bytes data memory address space
- ALE off software selectable.
- Four 8-bit bi-directional ports; Port 0 has internal pull-up resisters enabled by software
- One 4-bit multipurpose programmable port (I/O, interrupt, Chip select function)
- Three 16-bit timer/counters
- One full duplex serial port
- 5 channel PWM
- Watchdog timer
- Software Reset
- P1.0 T2 programmable clock out
- Eight-sources, two-level interrupt capability
- Built-in power management
- Code protection
- Packaged in
  - DIP 44: W78E65-40
  - PLCC 44: W78E65P-40
  - QFP 44: W78E65F-40
  - Lead Free(RoHS) PLCC 44: W78E065A40PL
  - Lead Free(RoHS) DIP 40: W78E065A40DL
  - Lead Free(RoHS) QFP 44: W78E065A40FL

3. PIN CONFIGURATIONS

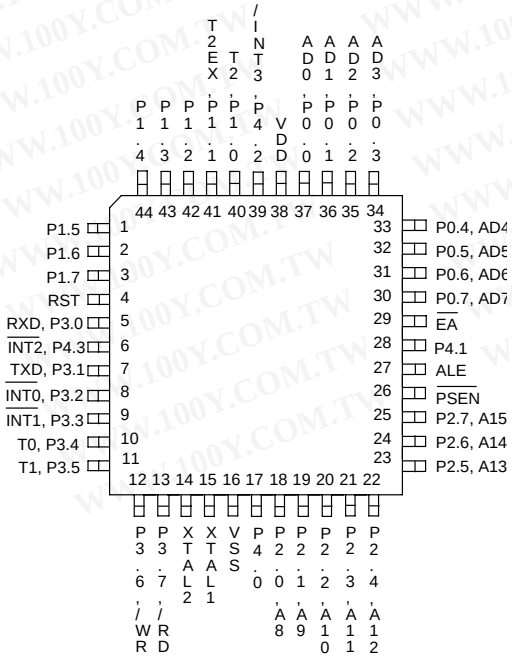
40-Pin DIP



44-Pin PLCC



44-Pin QFP

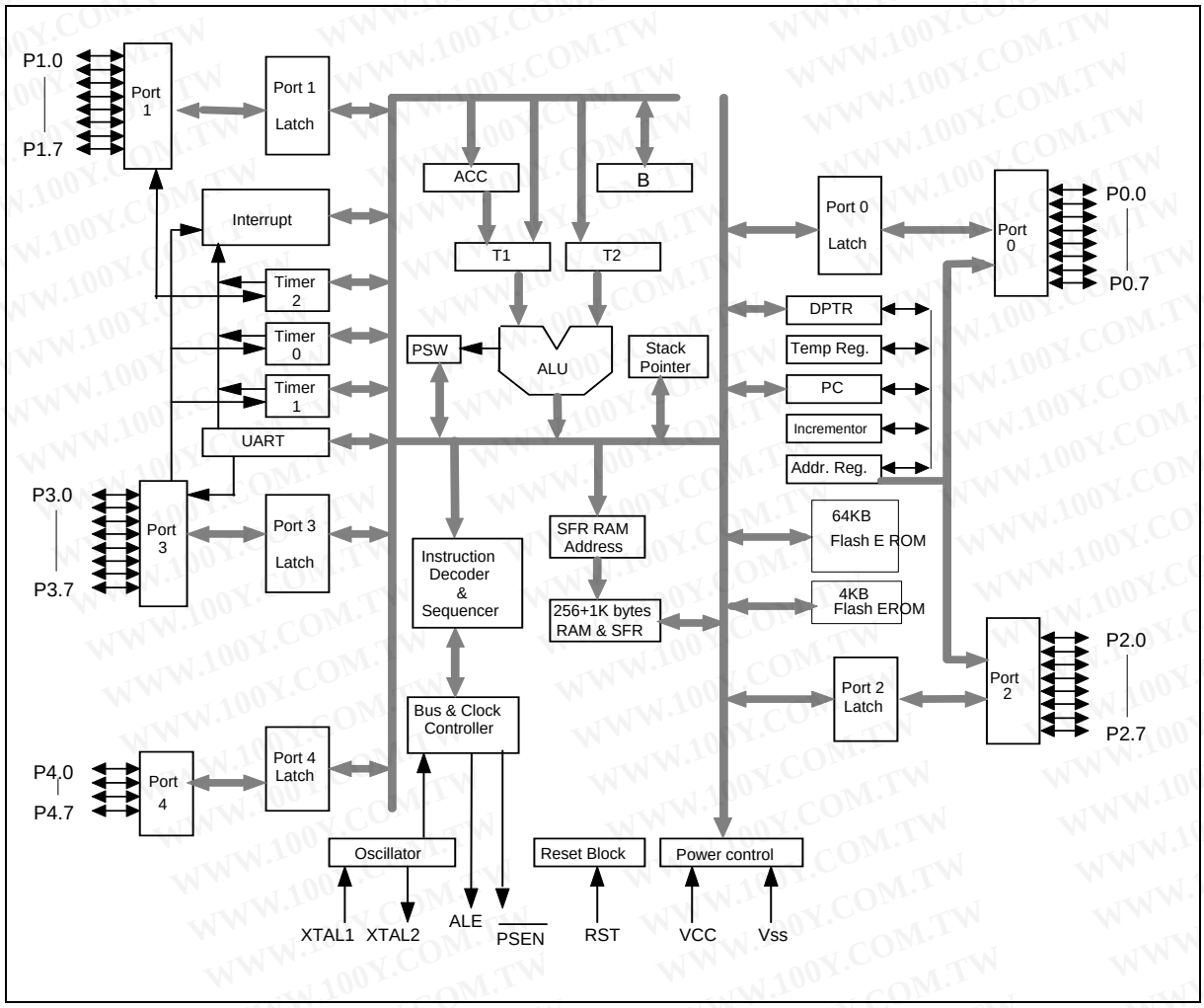


4. PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTIONS
$\overline{EA}$	I	EXTERNAL ACCESS ENABLE: This pin forces the processor to execute the external ROM. The ROM address and data will not be presented on the bus if the $\overline{EA}$ pin is high.
$\overline{PSEN}$	O H	PROGRAM STORE ENABLE: $\overline{PSEN}$ enables the external ROM data in the Port 0 address/data bus. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs originate from this pin.
ALE	O H	ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency.
RST	I L	RESET: A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	I	CRYSTAL 1: This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	O	CRYSTAL 2: This is the crystal oscillator output. It is the inversion of XTAL1.
V_{SS}	I	GROUND: ground potential.
V_{DD}	I	POWER SUPPLY: Supply voltage for operation.
P0.0–P0.7	I/O D	PORT 0: Function is the same as that of standard 8052. This port also provides a multiplexed low order address/data bus during accesses to external memory. Port 0 has internal pull-up resisters enabled by software.
P1.0–P1.7	I/O H	PORT 1: Function is the same as that of standard 8052.
P2.0–P2.7	I/O H	PORT 2: Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory. The P2.6 and P2.7 also provide the alternate function $\overline{REBOOT}$ which is H/W reboot from LD flash.
P3.0–P3.7	I/O H	PORT 3: Function is the same as that of the standard 8052.
P4.0–P4.3	I/O H	PORT 4: A bi-directional I/O. The P4.3 also provide the alternate function $\overline{REBOOT}$ which is H/W reboot from LD flash.

*** Note: TYPE** I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain

5. BLOCK DIAGRAM



6. FUNCTIONAL DESCRIPTION

The W78E65 architecture consists of a core controller surrounded by various registers, four general purpose I/O ports, one special purpose programmable 4-bits I/O port, 256+1K bytes of RAM, three timer/counters, a serial port. The processor supports 111 different opcodes and references both a 64K program address space and a 64K data storage space.

6.1 RAM

The internal data RAM in the W78E65 is 256+1K bytes. It is divided into two banks: 256 bytes of scratchpad RAM and 1K bytes of AUX-RAM. These RAMs are addressed by different ways.

- RAM 0H–7FH can be addressed directly and indirectly as the same as in 8051. Address pointers are R0 and R1 of the selected register bank.
- RAM 80H–FFH can only be addressed indirectly as the same as in 8051. Address pointers are R0, R1 of the selected registers bank.
- AUX-RAM 0H–3FFH is addressed indirectly as the same way to access external data memory with the MOVX instruction. Address pointer are R0 and R1 of the selected register bank and DPTR register. An access to external data memory locations higher than 3FFH will be performed with the MOVX instruction in the same way as in the 8051. The AUX-RAM is enable after a reset. Setting the bit 4 in CHPCON register will enable the access to AUX-RAM. When executing from internal program memory, an access to AUX-RAM will not affect the Ports P0, P2, $\overline{WR}$ and $\overline{RD}$.

Example,

```
CHPENR    REG     F6H
CHPCON    REG     BFH
XRAMAH    REG     A1H

MOV     CHPENR, #87H
MOV     CHPENR, #59H
ORL     CHPCON, #00010000B    ; enable AUX-RAM
MOV     CHPENR, #00H
MOV     XRAMAH, #01H          ; internal high address
MOV     R0, #23H
MOV     A, #55H
MOVX    @R0, A                ; Write 55h data to 0123h AUX-RAM address.
MOV     XRAMAH, #02H
MOV     R1, #FFH              ; Read data from 02FFh AUX-RAM address.
MOVX    A, @R1
MOV     DPTR, #0134H
MOV     A, #78H
MOVX    @DPTR, A              ; Write 78h data to 0134h AUX-RAM address.
MOV     DPTR, #7FFFH
MOVX    A, @DPRT              ; Read data from the external 7FFFh address SRAM
```

6.2 Timers 0, 1, and 2

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0, 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2. The operations of Timer 0 and Timer 1 are the same as in the W78C51. Timer 2 is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1.

6.2.1 Timer 2 Output

If Set T2OE(T2MOD.1) bit and clear C/T2 (T2CON.1) bit when CPU work at auto-reload mode and happen overflow, CPU will toggle P1.0 pin.

TIMER 2 Mode

Bit:	7	6	5	4	3	2	1	0
							T2OE	

Mnemonic: T2MOD Address: C9H

T2OE: Enable this bit to toggle P1.0 pin while Timer2 has been overflowed.

6.3 Clock

The W78E65 is designed with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used by default. This makes the W78E65 relatively insensitive to duty cycle variations in the clock.

6.3.1 Crystal Oscillator

The W78E65 incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground.

6.3.2 External Clock

An external clock should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator.

6.4 Power Management

6.4.1 Idle Mode

Setting the IDL bit in the PCON register enters the idle mode. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

6.4.2 Power-down Mode

When the PD bit in the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks are stopped, including the oscillator. To exit from power-down mode is by a hardware reset or external interrupts $\overline{INT0}$ to $\overline{INT1}$ when enabled and set to level triggered.

6.4.3 Reduce EMI Emission

The W78E65 allows user to diminish the gain of on-chip oscillator amplifier by using programmer to clear the B7 bit of security register. Once B7 is set to 0, a half of gain will be decreased. Care must be taken if user attempts to diminish the gain of oscillator amplifier, reducing a half of gain may affect the external crystal operating improperly at high frequency. The value of C1 and C2 may need some adjustment while running at lower gain.

ALE OFF Function

Auxiliary Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	ALEOFF

Mnemonic: AUXR Address: 8EH

ALEOFF: Set this bit to disable ALE output.

6.5 Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running. An internal trigger circuit in the reset line is used to deglitch the reset line when the W78E65 is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line. During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

6.5.1 W78E65 Special Function Registers (SFRs) and Reset Values

F8									FF
F0	+B 00000000						CHPENR 00000000		F7
E8									EF
E0	+ACC 00000000								E7
D8	+P4 11111111	PWMP 00000000	PWM0 00000000	PWM1 00000000	PWMCON1 00000000	PWM2 00000000	PWM3 00000000		DF
D0	+PSW 00000000								D7
C8	+T2CON 00000000	T2MOD 00000000	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000	PWMCON2 00000000	PWM4 00000000	CF
C0	+XICON 00000000		P4CONA 00000000	P4CONB 00000000	SFRAL 00000000	SFRAH 00000000	SFRFD 00000000	SFRCN 00000000	C7
B8	+IP 00000000							CHPCON 0xx00000	BF
B0	+P3 00000000				P43AL 00000000	P43AH 00000000			B7
A8	+IE 00000000				P42AL 00000000	P42AH 00000000	P4CSIN 00000000		AF
A0	+P2 11111111	XRAMAH 00000000							A7
98	+SCON 00000000	SBUF xxxxxxxx							9F
90	+P1 11111111				P41AL 00000000	P41AH 00000000			97
88	+TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR 00000000	WDTC 00000000	8F
80	+P0 11111111	SP 00000111	DPL 00000000	DPH 00000000	P40AL 00000000	P40AH 00000000	POR 00000000	PCON 00110000	87

Notes:

1. The SFRs marked with a plus sign(+) are both byte- and bit-addressable.
2. The text of SFR with bold type characters are extension function registers.

6.6 Port 4

Port 4, address D8H, is a 8-bit multipurpose programmable I/O port. Each bit can be configured individually by software. The Port 4 has four different operation modes.

Mode 0: P4.0–P4.3 is a bi-directional I/O port which is same as port 1. P4.2 and P4.3 also serve as external interrupt $\overline{INT3}$ and $\overline{INT2}$ if enabled.

Mode 1: P4.0–P4.3 are read strobe signals that are synchronized with $\overline{RD}$ signal at specified addresses. These signals can be used as chip-select signals for external peripherals.

Mode 2: P4.0–P4.3 are write strobe signals that are synchronized with $\overline{WR}$ signal at specified addresses. These signals can be used as chip-select signals for external peripherals.

Mode 3: P4.0–P4.3 are read/write strobe signals that are synchronized with $\overline{RD}$ or $\overline{WR}$ signal at specified addresses. These signals can be used as chip-select signals for external peripherals.

When Port 4 is configured with the feature of chip-select signals, the chip-select signal address range depends on the contents of the SFR P4xAH, P4xAL, P4CONA and P4CONB. The registers P4xAH and P4xAL contain the 16-bit base address of P4.x. The registers P4CONA and P4CONB contain the control bits to configure the Port 4 operation mode.

6.6.1 Port Options Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	P0UP

Mnemonic: POR Address: 86H

P0UP: Enable Port 0 weak up. The pins of Port 0 can be configured with either the open drain or standard port with internal pull-up. By the default, Port 0 is an open drain bi-directional I/O port. When the P0UP bit in the POR register is set, the pins of port 0 will perform a bi-directional I/O port with internal pull-up that is structurally the same Port2.

6.6.2 $\overline{INT2}$ / $\overline{INT3}$

Two additional external interrupts, $\overline{INT2}$ and $\overline{INT3}$, whose functions are similar to those of external interrupt 0 and 1 in the standard 80C52. The functions/status of these interrupts are determined/shown by the bits in the XICON (External Interrupt Control) register. The XICON register is bit-addressable but is not a standard register in the standard 80C52. Its address is at 0C0H. To set/clear bits in the XICON register, one can use the "SETB ($\overline{CLR}$) bit" instruction. For example, "SETB 0C2H" sets the EX2 bit of XICON.

XICON - external interrupt control (C0H)

PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

PX3: External interrupt 3 priority high if set

EX3: External interrupt 3 enable if set

IE3: If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced

IT3: External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software

PX2: External interrupt 2 priority high if set

EX2: External interrupt 2 enable if set

IE2: If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced

IT2: External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software

Eight-source interrupt information:

INTERRUPT SOURCE	VECTOR ADDRESS	POLLING SEQUENCE WITHIN PRIORITY LEVEL	ENABLE REQUIRED SETTINGS	INTERRUPT TYPE EDGE/LEVEL
External Interrupt 0	03H	0 (highest)	IE.0	TCON.0
Timer/Counter 0	0BH	1	IE.1	-
External Interrupt 1	13H	2	IE.2	TCON.2
Timer/Counter 1	1BH	3	IE.3	-
Serial Port	23H	4	IE.4	-
Timer/Counter 2	2BH	5	IE.5	-
External Interrupt 2	33H	6	XICON.2	XICON.0
External Interrupt 3	3BH	7 (lowest)	XICON.6	XICON.3

P4CONB (C3H)

BIT	NAME	FUNCTION
7, 6	P43FUN1 P43FUN0	00: Mode 0. P4.3 is a general purpose I/O port which is the same as Port1. 01: Mode 1. P4.3 is a Read Strobe signal for chip select purpose. The address range depends on the SFR P43AH, P43AL, P43CMP1 and P43CMP0. 10: Mode 2. P4.3 is a Write Strobe signal for chip select purpose. The address range depends on the SFR P43AH, P43AL, P43CMP1 and P43CMP0. 11: Mode 3. P4.3 is a Read/Write Strobe signal for chip select purpose. The address range depends on the SFR P43AH, P43AL, P43CMP1, and P43CMP0.
5, 4	P43CMP1 P43CMP0	Chip-select signals address comparison: 00: Compare the full address (16 bits length) with the base address register P43AH, P43AL. 01: Compare the 15 high bits (A15–A1) of address bus with the base address register P43AH, P43AL. 10: Compare the 14 high bits (A15–A2) of address bus with the base address register P43AH, P43AL. 11: Compare the 8 high bits (A15–A8) of address bus with the base address register P43AH, P43AL.

P4CONB (C3H), continued

BIT	NAME	FUNCTION
3, 2	P42FUN1 P42FUN0	The P4.2 function control bits which are the similar definition as P43FUN1, P43FUN0.
1, 0	P42CMP1 P42CMP0	The P4.2 address comparator length control bits which are the similar definition as P43CMP1, P43CMP0.

P4CONA (C2H)

BIT	NAME	FUNCTION
7, 6	P41FUN1 P41FUN0	The P4.1 function control bits which are the similar definition as P43FUN1, P43FUN0.
5, 4	P41CMP1 P41CMP0	The P4.1 address comparator length control bits which are the similar definition as P43CMP1, P43CMP0.
3, 2	P40FUN1 P40FUN0	The P4.0 function control bits which are the similar definition as P43FUN1, P43FUN0.
1, 0	P40CMP1 P40CMP0	The P4.0 address comparator length control bits which are the similar definition as P43CMP1, P43CMP0.

P4CSIN (AEH)

BIT	NAME	FUNCTION
7	P43CSINV	The active polarity of P4.3 when pin P4.3 is defined as read and/or write strobe signal. = 1: P4.3 is active high when pin P4.3 is defined as read and/or write strobe signal. = 0: P4.3 is active low when pin P4.3 is defined as read and/or write strobe signal.
6	P42CSINV	The similarity definition as P43SINV.
5	P41CSINV	The similarity definition as P43SINV.
4	P40CSINV	The similarity definition as P43SINV.
3	-	Reserve
2	-	Reserve
1	-	0
0	-	0

6.6.3 Port 4 Base Address Registers

P40AH, P40AL:

The Base address register for comparator of P4.0. P40AH contains the high-order byte of address, P40AL contains the low-order byte of address.

P41AH, P41AL:

The Base address register for comparator of P4.1. P41AH contains the high-order byte of address, P41AL contains the low-order byte of address.

P42AH, P42AL:

The Base address register for comparator of P4.2. P42AH contains the high-order byte of address, P42AL contains the low-order byte of address.

P43AH, P43AL:

The Base address register for comparator of P4.3. P43AH contains the high-order byte of address, P43AL contains the low-order byte of address.

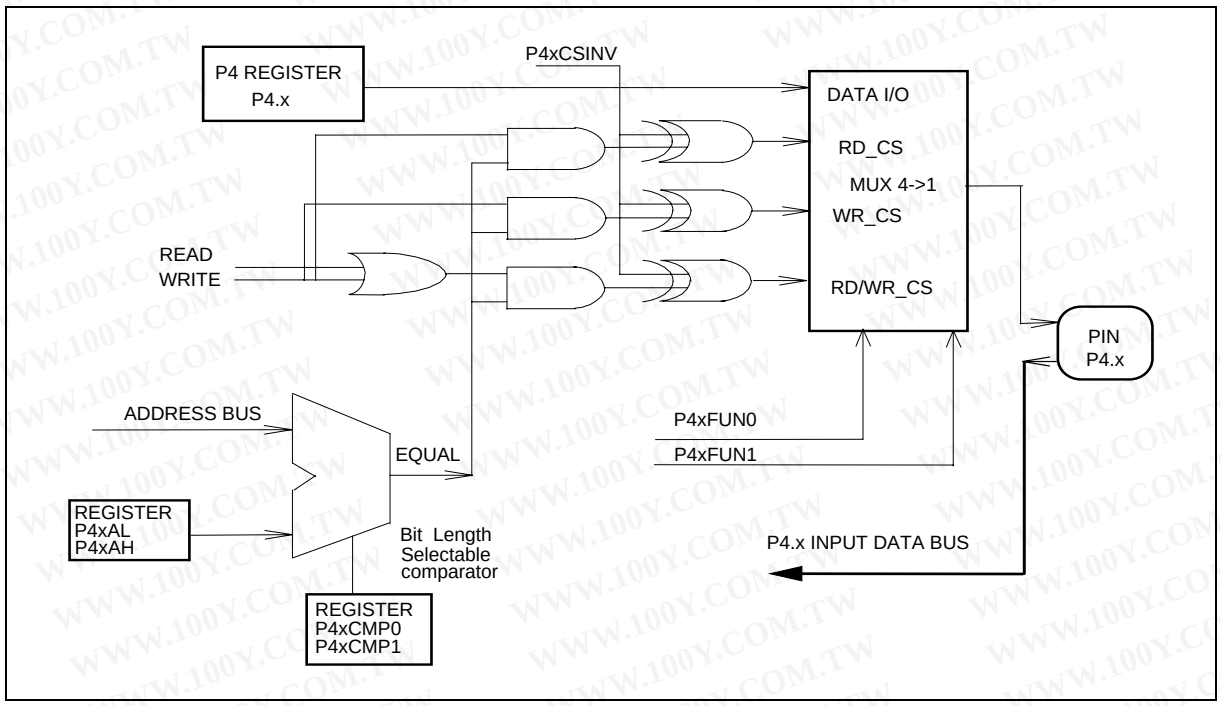
P4 (D8H)

BIT	NAME	FUNCTION
7	P47	I/O pin
6	P46	I/O pin.
5	P45	I/O pin.
4	P44	I/O pin.
3	P43	Port 4 Data bit which outputs to pin P4.3 at mode 0.
2	P42	Port 4 Data bit. which outputs to pin P4.2 at mode 0.
1	P41	Port 4 Data bit. which outputs to pin P4.1at mode 0.
0	P40	Port 4 Data bit which outputs to pin P4.0 at mode 0.

Here is an example to program the P4.0 as a write strobe signal at the I/O port address 1234H–1237H and positive polarity, and P4.1–P4.3 are used as general I/O ports.

```
MOV  P40AH, #12H
MOV  P40AL, #34H          ; Base I/O address 1234H for P4.0
MOV  P4CONA, #00001010B   ; P4.0 a write strobe signal and address line A0 and A1 are masked.
MOV  P4CONB, #00H         ; P4.1–P4.3 as general I/O port which are the same as PORT1
MOV  P2ECON, #10H         ; Write the P40SINV = 1 to inverse the P4.0 write strobe polarity
                          ; default is negative.
```

Then any instruction MOVX @DPTR, A (with DPTR = 1234H–1237H) will generate the positive polarity write strobe signal at pin P4.0. And the instruction MOV P4, #XX will output the bit3 to bit1 of data #XX to pin P4.3–P4.1.



6.7 Pulse Width Modulated Outputs (PWM)

There are five pulse width modulated output channels to generate pulses of programmable length and interval. The repedtition frequency is defined by an 8-bit prescaler PWMP, which supplies the clock for the counter. The prescaler and counter are common to both PWM channels. The 8-bit counter counts modular 255 (0–254). The value of the 8-bit counteris compared to the contents of five registers: PWM0, PWM1, PWM2, PWM3 and PWM4. Provided the contents of either of these registers is greater than the counter value, the corresponding PWM0, PWM1, PWM2, PWM3 or PWM4 output is set HIGH. If the contents of these registers are equal to, or less than the counter value, the output will be LOW. The pulse-width-ratio is thesefore defined by the contents of the registers PWM0, PWM1, PWM2, PWM3 and PWM4. The pulse-width-ratio is in the range of 0 to 1 and may be programmed in increments of 1/255. ENPWM0, ENPWM1, ENPWM2, ENPWM3 and ENPWM4 bit will enable or disable PWM output.

Buffered PWM outputs may be used to drive DC motors. The rotation speed of the motor would be proportional to the contents of PWM0/1/2/3/4. The repetition frequency f_{pwm}, at the PWM0/1/2/3/4 output is given by:

$$f_{pwm} = \frac{f_{osc}}{2 \times (1 + PWMP) \times 255}$$

Prescaler division factor = PWM + 1

PWMn high/low ratio of $\mathrm{PWMn} = \frac{(\mathrm{PWMn})}{255 - (\mathrm{PWMn})}$

This gives a repetition frequency range of 123 Hz to 31.4 KHz (f_{osc} = 16 MHz). By loading the PWM registers with either 00H or FFH, the PWM channels will output a constant HIGH or LOW level, respectively. Since the 8-bit counter counts modulo 255, it can never actually reach the value of the PWM registers when they are loaded with FFH.

When a compare register (PWM0, PWM1, PWM2, PWM3, PWM4) is loaded with a new value, the associated output updated immediately. It does not have to wait until the end of the current counter period. There is weakly pulled high on PWM output.

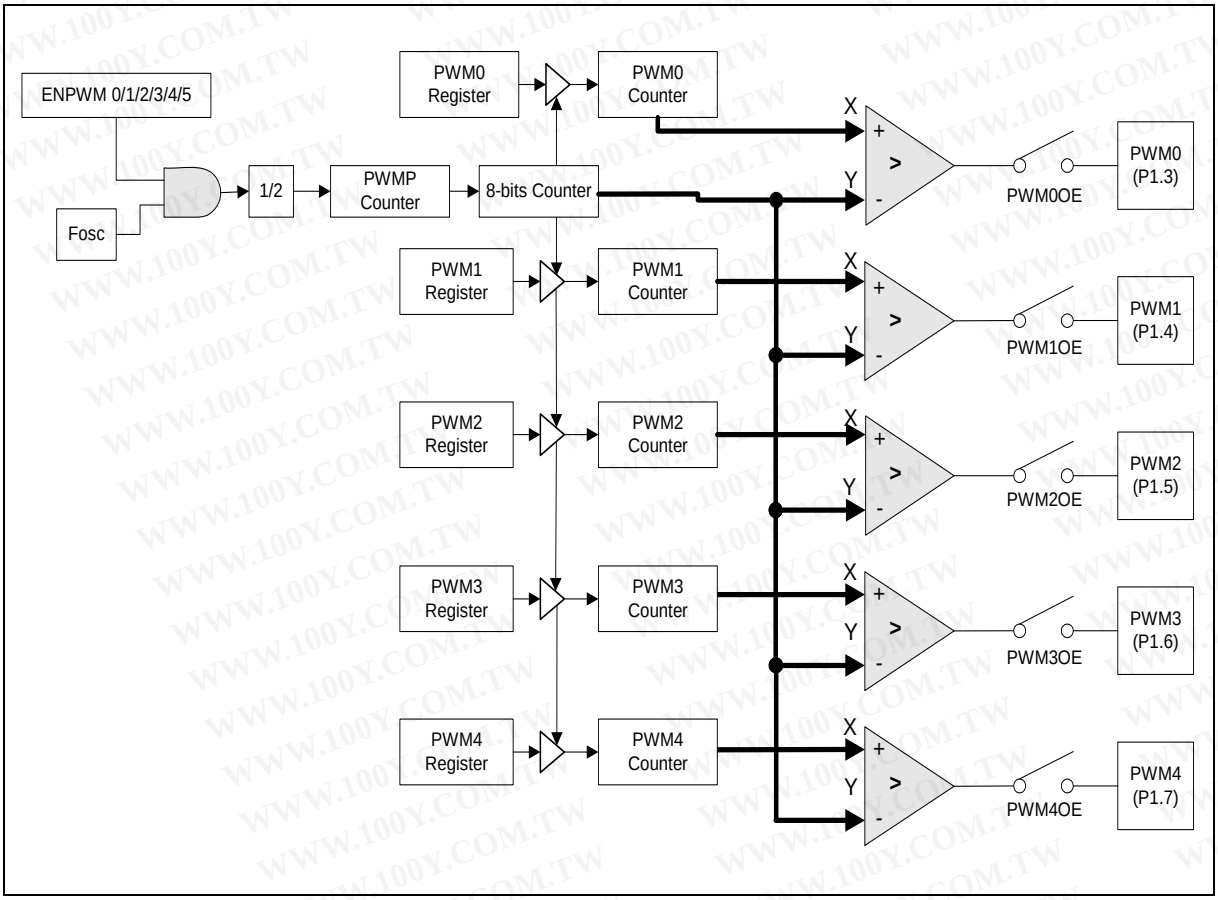


Figure 1 PWM diagram

Please refer as below code.

```
mov    pwmcon1, #00110011b      ; enable pwm3, 2, 1, 0
mov    pwmcon2, #00000101b      ; enable pwm4
mov    pwmp, #40h               ; Fpwm = XT/(2*(1+pwmp)*255)
jb     p1.3, $
mov    pwm0, #14h               ; duty cycle high/low = pwm0/(255-pmw0)
jb     p1.4, $
mov    pwm1, #18h
```

```
jb      p1.5, $
mov   pwm2, #20h
jb      p1.6, $
mov    pwm3, #b0h
jb      p1.7, $
mov    pwm4, #40h
mov    pwmcon1, #11111111b    ; output enable pwm3, 2, 1, 0
```

PWM3 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM3 Address: DEH

PWM2 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM2 Address: DDH

PWM CONTROL 1 Register

Bit:	7	6	5	4	3	2	1	0
	PWM3OE	PWM2OE	ENPWM3	ENPWM2	PWM1OE	PWM0OE	ENPWM1	ENWPM0

Mnemonic: PWMCON1 Address: DCH

PWM3OE: Output enable for PWM3
PWM2OE: Output enable for PWM2
ENPWM3: Enable PWM3
ENPWM2: Enable PWM2
PWM1OE: Output enable for PWM1
PWM0OE: Output enable for PWM0
ENPWM1: Enable PWM1
ENPWM0: Enable PWM0

PWM1 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM1 Address: DBH

PWM0 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM0 Address: DAH

PWMP Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWMP Address: D9H

PWM4 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM4 Address: CFH

PWM CONTROL 2 Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	PWM4OE	-	ENWPM4

Mnemonic: PWMCON2 Address: CEH

PWM4OE: Output enable for PWM4

ENPWM: Enable for PWM4

6.8 Watchdog Timer

The Watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs, a system reset can also be caused if it is enabled. The main use of the Watchdog timer is as a system monitor. This is important in real-time control applications. In case of power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. The watchdog time-out selection will result in different time-out values depending on the clock speed. The Watchdog timer will de disabled on reset. In general, software should restart the Watchdog timer to put it into a known state. The control bits that support the Watchdog timer are discussed below.

Watchdog Timer Control Register

Bit:	7	6	5	4	3	2	1	0
	ENW	CLRW	WIDL	-	-	PS2	PS1	PS0

Mnemonic: WDTC Address: 8FH

ENW : Enable watch-dog if set.

CLRW: Clear watch-dog timer and prescaler if set. This flag will be cleared automatically

WIDL : If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watch-dog is disabled under IDLE mode. Default is cleared.

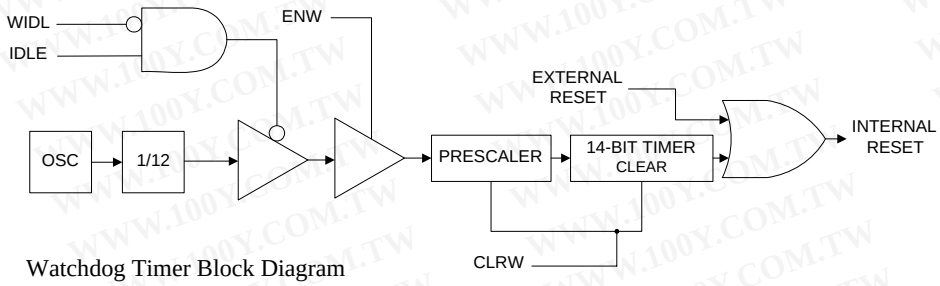
PS2, PS1, PS0: Watch-dog prescaler timer select. Prescaler is selected when set PS2–0 as follows:

PS2	PS1	PS0	PRESCALER SELECT
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

The time-out period is obtained using the following equation:

$$\frac{1}{\text{OSC}} \times 2^{14} \times \text{PRESCALER} \times 1000 \times 12 \text{ mS}$$

Before Watchdog time-out occurs, the program must clear the 14-bit timer by writing 1 to WDTC.6 (CLRW). After 1 is written to this bit, the 14-bit timer, prescaler and this bit will be reset on the next instruction cycle. The Watchdog timer is cleared on reset.



Watchdog Timer Block Diagram

Typical Watch-Dog time-out period when OSC = 20 MHz

PS2	PS1	PS0	WATCHDOG TIME-OUT PERIOD
0	0	0	19.66 mS
0	0	1	39.32 mS
0	1	0	78.64 mS
0	1	1	157.28 mS
1	0	0	314.57 mS
1	0	1	629.14 mS
1	1	0	1.25 S
1	1	1	2.50 S

6.9 In-System Programming (ISP) Mode

The W78E65 equips one 64K byte of main ROM bank for application program (called AP FLASH EPROM) and one 4K byte of auxiliary ROM bank for loader program (called LD FLASH EPROM). In the normal operation, the microcontroller executes the code in the AP FLASH EPROM. If the content of AP FLASH EPROM needs to be modified, the W78E65 allows user to activate the In-System Programming (ISP) mode by setting the CHPCON register. **The CHPCON is read-only by default, software must write two specific values 87H, then 59H sequentially to the CHPENR register to enable the CHPCON write attribute. Writing CHPENR register with the values except 87H and 59H will close CHPCON register write attribute.** The W78E65 achieves all in-system programming operations including enter/exit ISP Mode, program, erase, read ... etc, during device in the idle mode. Setting the bit CHPCON.0 the device will enter in-system programming mode after a wake-up from idle mode. Because device needs proper time to complete the ISP operations before awaken from idle mode, software may use timer interrupt to control the duration for device wake-up from idle mode. To perform ISP operation for revising contents of AP FLASH EPROM, software located at AP FLASH EPROM setting the CHPCON register then enter idle mode, after awaken from idle mode the device executes the corresponding interrupt service routine in LD FLASH EPROM. Because the device will clear the program counter while switching from AP FLASH EPROM to LD FLASH EPROM, the first execution of RETI instruction in interrupt service routine will jump to 00H at LD FLASH EPROM area. The device offers a software reset for switching back to AP FLASH EPROM while the content of AP FLASH EPROM has been updated completely. **Setting CHPCON register bit 0, 1 and 7 to logic-1 will result a software reset to reset the CPU**. The software reset serves as a external reset. This in-system programming feature makes the job easy and efficient in which the application needs to update firmware frequently. In some applications, the in-system programming feature make it possible to easily update the system firmware without opening the chassis.

SFRAH, SFRAL: The objective address of on-chip ROM in the in-system programming mode. SFRAH contains the high-order byte of address, SFRAL contains the low-order byte of address.

SFRFD: The programming data for on-chip ROM in programming mode.

SFRCN: The control byte of on-chip ROM programming mode.

SFRCN (C7)

BIT	NAME	FUNCTION
7	-	Reserve.
6	WFWIN	On-chip ROM bank select for in-system programming. = 0: 64K bytes ROM bank is selected as destination for re-programming. = 1: 4K bytes ROM bank is selected as destination for re-programming.
5	OEN	ROM output enable.
4	CEN	ROM chip enable.
3, 2, 1, 0	CTRL[3:0]	The flash control signals

MODE	WFWIN	CTRL<3:0>	OEN	CEN	SFRAH, SFRAL	SFRFD
Erase 64KB AP FLASH EPROM	0	0010	1	0	X	X
Program 64KB AP FLASH EPROM	0	0001	1	0	Address in	Data in
Read 64KB AP FLASH EPROM	0	0000	0	0	Address in	Data out
Erase 4KB LD FLASH EPROM	1	0010	1	0	X	X
Program 4KB LD FLASH EPROM	1	0001	1	0	Address in	Data in
Read 4KB LD FLASH EPROM	1	0000	0	0	Address in	Data out

6.9.1 In-System Programming Control Register (CHPCON)

CHPCON (BFH)

BIT	NAME	FUNCTION
7	SWRESET	When this bit is set to 1, and both FBOOTSL and FPROGEN are set to 1. It will enforce microcontroller reset to initial condition just like power on reset.
6	-	Reserve.
5	LD/AP	This bit is read only. 1: CPU is running LD FLASH EPROM program. 0: CPU is running AP FLASH EPROM program.
4	ENAUXRAM	1: Enable on-chip AUX-RAM. 0: Disable the on-chip AUX-RAM
3	1	Must be 1
2	-	Reserve.
1	FBOOTSL	When this bit is set to 1, and both SWRESET and FPROGEN are set to 1. It will enforce microcontroller reset to initial condition just like power on reset.
0	FPROGEN	When this bit is set to 1, and both SWRESET and FBOOTSL are set to 1. It will enforce microcontroller reset to initial condition just like power on reset.

This register is protected by CHPENR register. Please write as below procedures while you would like to write CHPCON register.

```
Mov  CHPENR, #87h
Mov CHPENR, #59h
Anl  CHPCON, #EFh;  Disable AUX-RAM
Mov CHPENR, #0h
```

6.10 Software Reset

Set CHPCON = 0X83, timer and enter IDLE mode. CPU will reset and restart from APFLASH after time out.

6.11 H/W Reboot Mode (Boot from LD FLASH EPROM)

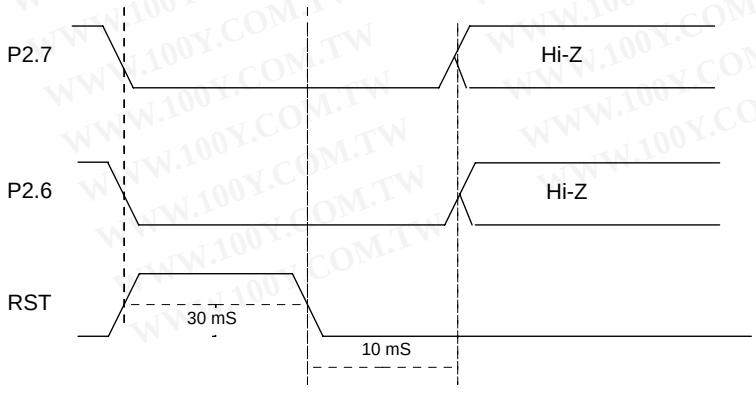
By default, the W78E65 boots from AP FLASH EPROM program after a power on reset. On some occasions, user can force the W78E65 to boot from the LD FLASH EPROM program via following settings. The possible situation that you need to enter H/W REBOOT mode when the AP FLASH EPROM program can not run properly and device can not jump back to LD FLASH EPROM to execute in-system programming function. Then you can use this H/W REBOOT mode to force the W78E65 jumps to LD FLASH EPROM and executes in-system programming procedure. When you design your system, you may reserve the pins P2.6, P2.7 to switches or jumpers. For example in a CD-ROM system, you can connect the P2.6 and P2.7 to PLAY and EJECT buttons on the panel. When the AP FLASH EPROM program fails to execute the normal application program. User can press both two buttons at the same time and then turn on the power of the personal computer to force the W78E65 to enter the H/W REBOOT mode. After power on of personal computer, you can release both buttons and finish the in-system programming procedure to update the AP FLASH EPROM code.

In application system design, user must take care of the P2, P3, ALE, $\overline{EA}$ and $\overline{PSEN}$ pin value at reset to prevent from accidentally activating the programming mode or H/W REBOOT mode. It is necessary to add 10K resistor on these P2.6, P2.7 and P4.3 pins.

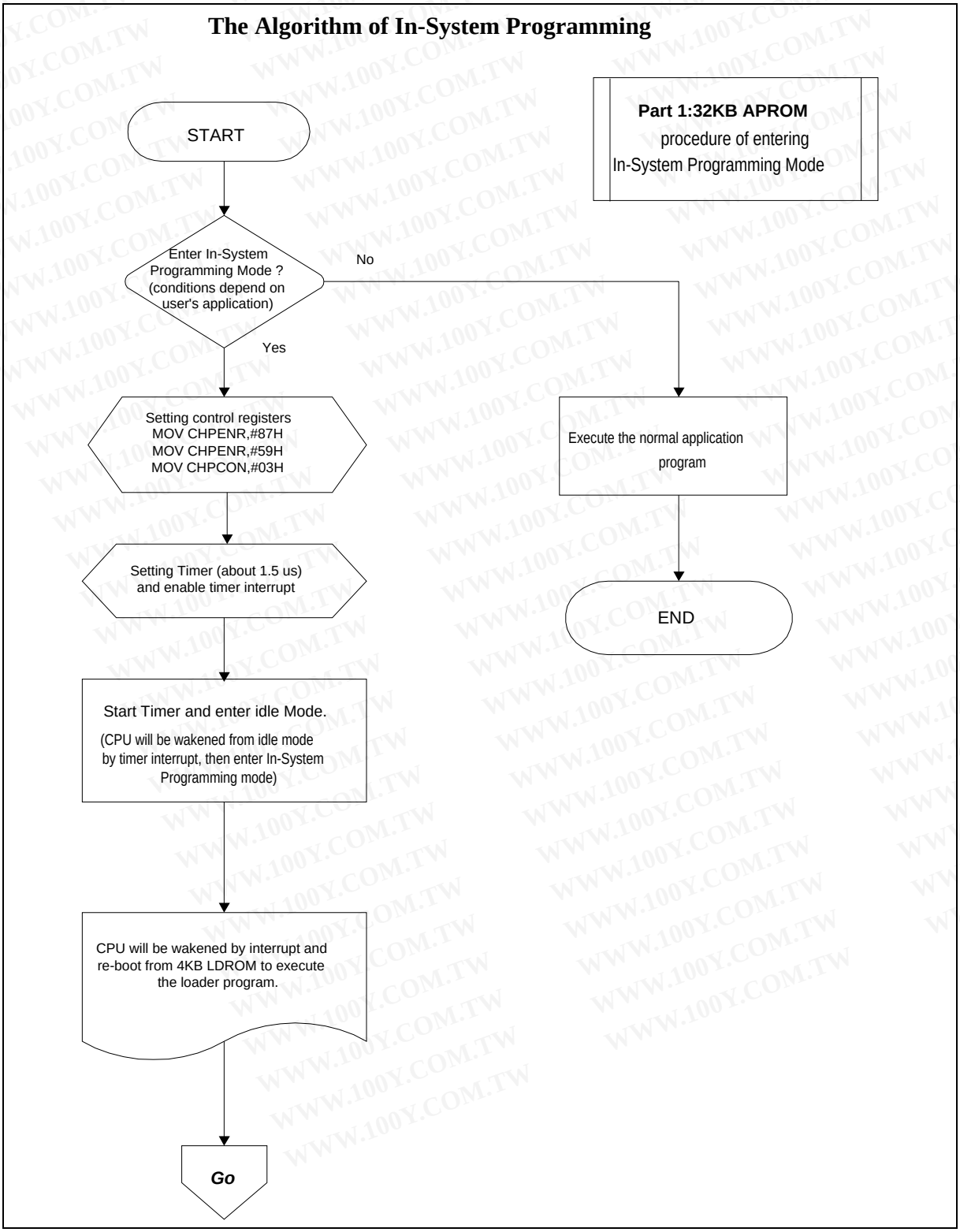
H/W Reboot Mode

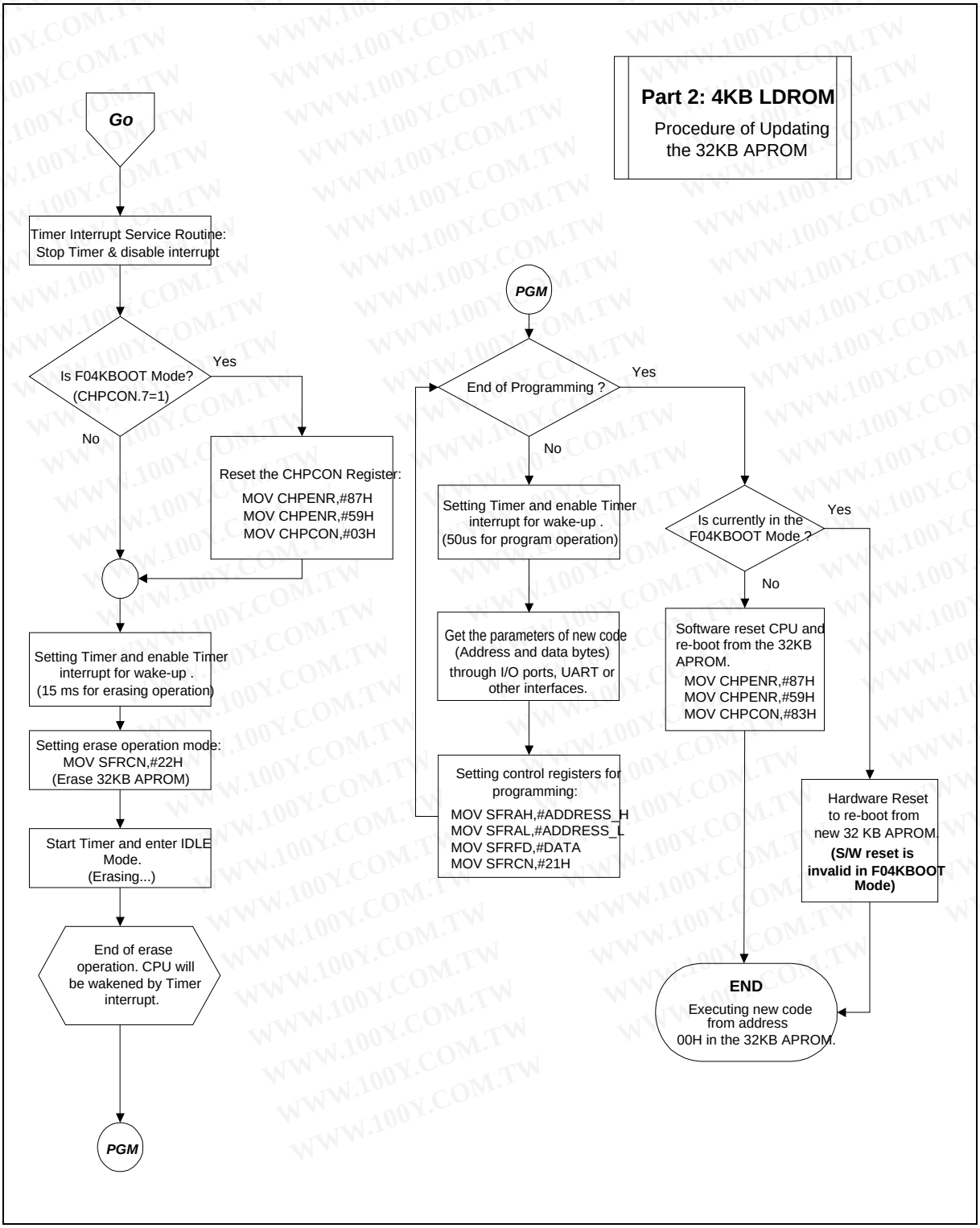
P4.3	P2.7	P2.6	MODE
X	L	L	REBOOT
L	X	X	REBOOT

The Reset Timing For Entering F04KBOOT Mode



The Algorithm of In-System Programming

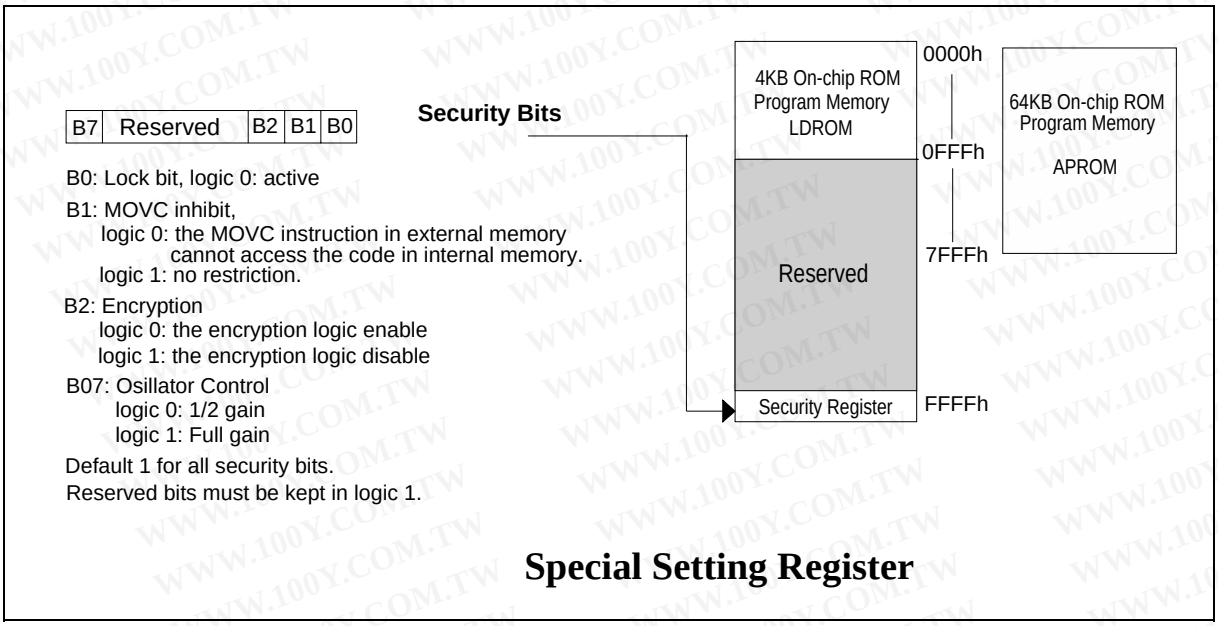




6.12 Security

During the on-chip ROM programming mode, the ROM can be programmed and verified repeatedly. Until the code inside the ROM is confirmed OK, the code can be protected. The protection of ROM and those operations on it are described below.

The W78E65 has a Security Register that can be accessed in programming mode. Those bits of the Security Registers can not be changed once they have been programmed from high to low. They can only be reset through erase-all operation. The Security Register is located at the 0FFFFH of the LD FLASH EPROM space.



Special Setting Register

Lock bit

This bit is used to protect the customer's program code in the W78E65. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the ROM data and Security Register can not be accessed again.

MOVC Inhibit

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

Encryption

This bit is used to enable/disable the encryption logic for code protection. Once encryption feature is enabled, the data presented on port 0 will be encoded via encryption logic. Only whole chip erase will reset this bit.

Oscillator Control

W78E65/E516 allow user to diminish the gain of on-chip oscillator amplifier by using programmer to set the bit B7 of security register. Once B7 is set to 0, a half of gain will be decreased. Care must be taken if user attempts to diminish the gain of oscillator amplifier, reducing a half of gain may improperly affect the external crystal operation at high frequency above 24 MHz. The value of R and C1, C2 may need some adjustment while running at lower gain.

7. ELETRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	V_{DD}–V_{SS}	-0.3	+6.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{ST}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

7.2 DC Characteristics

(V_{DD} – V_{SS}= 5V ±10%, T_A= 25°C, Fosc = 20MHz, unless otherwise specified.)

SYMBOL	PARAMETER	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
V_{DD}	Operating Voltage	4.5	5.5	V	RST = 1, P0 = V_{DD}
I_{DD}	Operating Current	-	20	mA	No load V_{DD} = 5.5V
I_{IDLE}	Idle Current	-	6	mA	Idle mode V_{DD} = 5.5V
I_{PWDN}	Power Down Current	-	10	µA	Power-down mode V_{DD} = 5.5V
I_{IN1}	Input Current P1, P2, P3, P4	-50	+10	µA	V_{DD} = 5.5V V_{IN} = 0V or V_{DD}
I_{IN2}	Input Current RST	-10	+300	µA	V_{DD} = 5.5V 0<V_{IN}<V_{DD}
I_{LK}	Input Leakage Current P0, $\overline{EA}$	-10	+10	µA	V_{DD} = 5.5V 0V<V_{IN}<V_{DD}
I_{TL}[*4]	Logic 1 to 0 Transition Current P1, P2, P3, P4	-500	-	µA	V_{DD} = 5.5V V_{IN} =2.0V

DC Characteristics, continued

SYMBOL	PARAMETER	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
V_{IL1}	Input Low Voltage P0, P1, P2, P3, P4, $\overline{EA}$	0	0.8	V	V_{DD} = 4.5V
V_{IL2}	Input Low Voltage RST	0	0.8	V	V_{DD} = 4.5V
V_{IL3}	Input Low Voltage XTAL1[*4]	0	0.8	V	V_{DD} = 4.5V
V_{IH1}	Input High Voltage P0, P1, P2, P3, P4, $\overline{EA}$	2.4	V_{DD} +0.2	V	V_{DD} = 5.5V
V_{IH2}	Input High Voltage RST	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
V_{IH3}	Input High Voltage XTAL1[*4]	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
V_{OL1}	Output Low Voltage P1, P2, P3, P4	-	0.45	V	V_{DD} = 4.5V I_{OL} = +2 mA
V_{OL2}	Output Low Voltage P0, ALE, $\overline{PSEN}$ [*3]	-	0.45	V	V_{DD} = 4.5V I_{OL} = +4 mA
Isk1	Sink current P1, P3, P4	4	12	mA	V_{DD} = 4.5V VOL = 0.45V
Isk2	Sink current P0, P2, ALE, $\overline{PSEN}$	10	20	mA	V_{DD} = 4.5V VOL = 0.45V
V_{OH1}	Output High Voltage P1, P2, P3, P4	2.4	-	V	V_{DD} = 4.5V I_{OH} = -100 μA
V_{OH2}	Output High Voltage P0, ALE, $\overline{PSEN}$ [*3]	2.4	-	V	V_{DD} = 4.5V I_{OH} = -400 μA
Isr1	Source current P1, P2, P3, P4	-120	-250	uA	V_{DD} = 4.5V VOH = 2.4V
Isr2	Source current P0, P2, ALE, $\overline{PSEN}$	-8	-20	mA	V_{DD} = 4.5V VOH = 2.4V

Notes:

*1. RST pin is a Schmitt trigger input.

*2. P0, ALE and $\overline{PSEN}$ are tested in the external access mode.

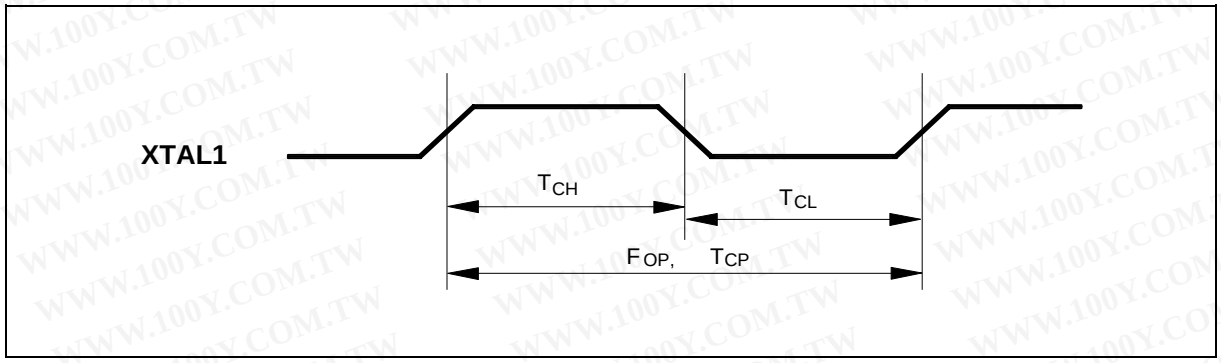
*3. XTAL1 is a CMOS input.

*4. Pins of P1, P2, P3, P4 can source a transition current when they are being externally driven from 1 to 0.

7.3 AC Characteristics

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (T_{CP}), and actual parts will usually experience less than a ±20 nS variation.

Clock Input Waveform



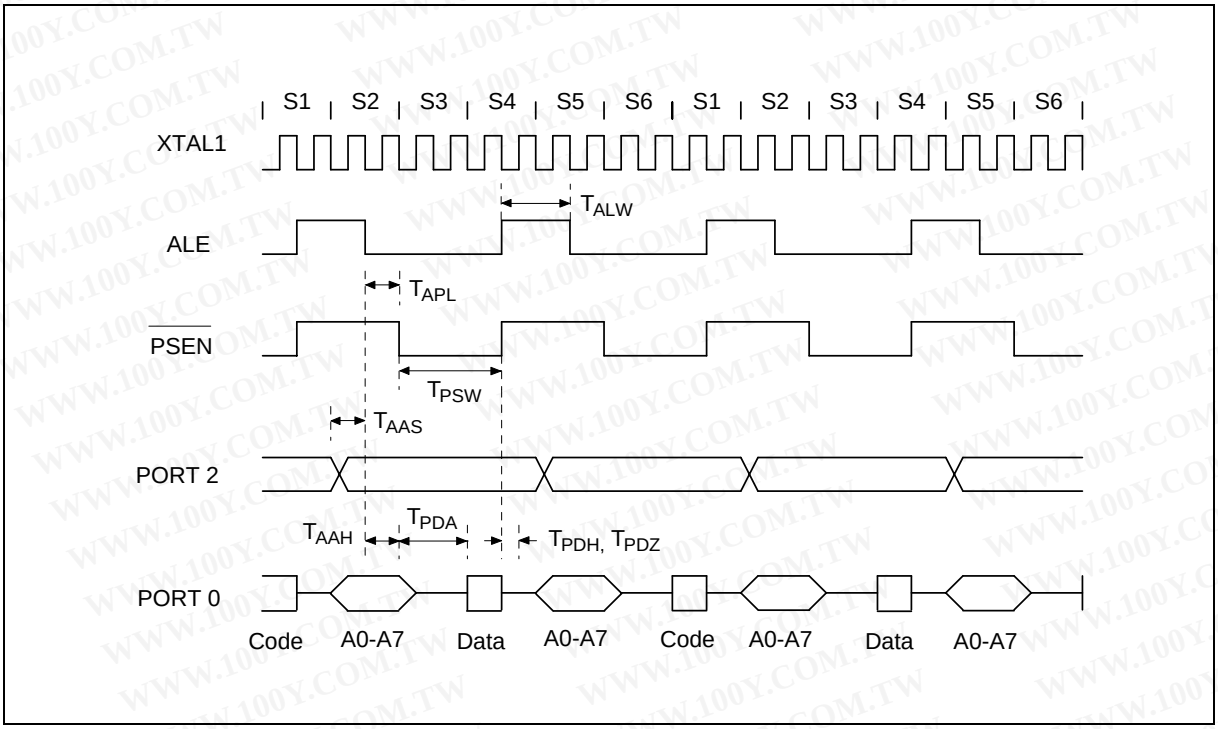
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	F_{OP}	0	-	40	MHz	1
Clock Period	T_{CP}	41.7	-	-	nS	2
Clock High	T_{CH}	20	-	-	nS	3
Clock Low	T_{CL}	20	-	-	nS	3

Notes:

1. The clock may be stopped indefinitely in either state.
2. The T_{CP} specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

8. TIMING WAVEFORMS

8.1 Program Fetch Cycle



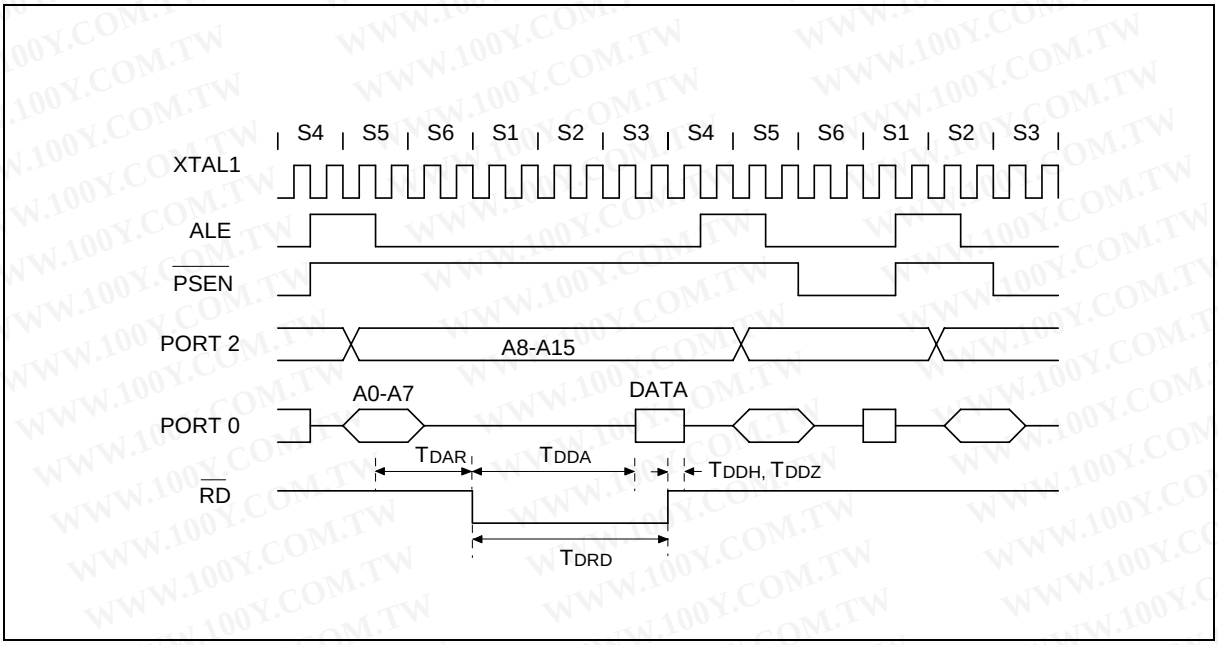
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	T_{AAS}	1 T_{CP}-Δ	-	-	nS	4
Address Hold from ALE Low	T_{AAH}	1 T_{CP}-Δ	-	-	nS	1, 4
ALE Low to $\overline{PSEN}$ Low	T_{APL}	1 T_{CP}-Δ	-	-	nS	4
$\overline{PSEN}$ Low to Data Valid	T_{PDA}	-	-	2 T_{CP}	nS	2
Data Hold after $\overline{PSEN}$ High	T_{PDH}	0	-	1 T_{CP}	nS	3
Data Float after $\overline{PSEN}$ High	T_{PDZ}	0	-	1 T_{CP}	nS	
ALE Pulse Width	T_{ALW}	2 T_{CP}-Δ	2 T_{CP}	-	nS	4
$\overline{PSEN}$ Pulse Width	T_{PSW}	3 T_{CP}-Δ	3 T_{CP}	-	nS	4

Notes:

1. P0.0–P0.7, P2.0–P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 T_{CP}.
3. Data have been latched internally prior to $\overline{PSEN}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Timing Waveforms, continued

8.2 Data Read Cycle



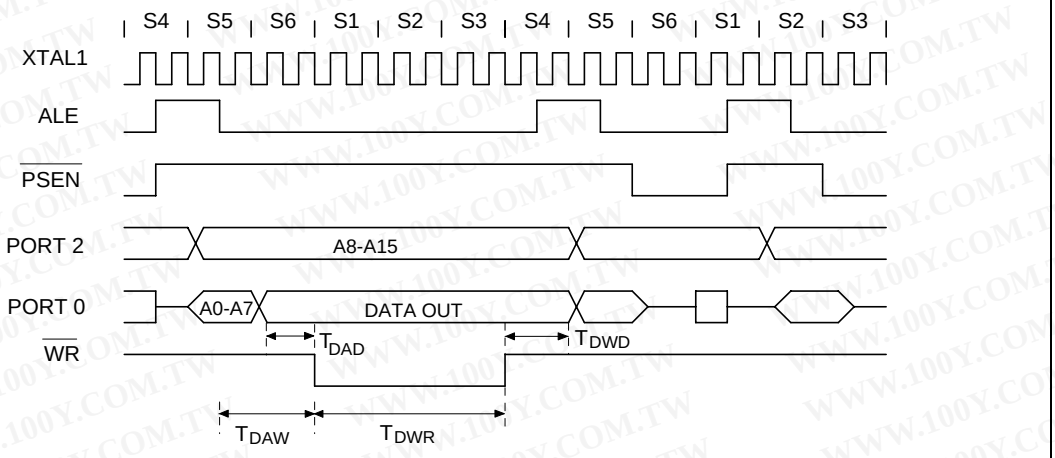
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to $\overline{RD}$ Low	T_{DAR}	3 T_{CP}-Δ	-	3 T_{CP} +Δ	nS	1, 2
$\overline{RD}$ Low to Data Valid	T_{DDA}	-	-	4 T_{CP}	nS	1
Data Hold from $\overline{RD}$ High	T_{DDH}	0	-	2 T_{CP}	nS	
Data Float from $\overline{RD}$ High	T_{DDZ}	0	-	2 T_{CP}	nS	
$\overline{RD}$ Pulse Width	T_{DRD}	6 T_{CP}-Δ	6 T_{CP}	-	nS	2

Notes:

1. Data memory access time is 8 T_{CP}.
2. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Timing Waveforms, continued

8.3 Data Write Cycle

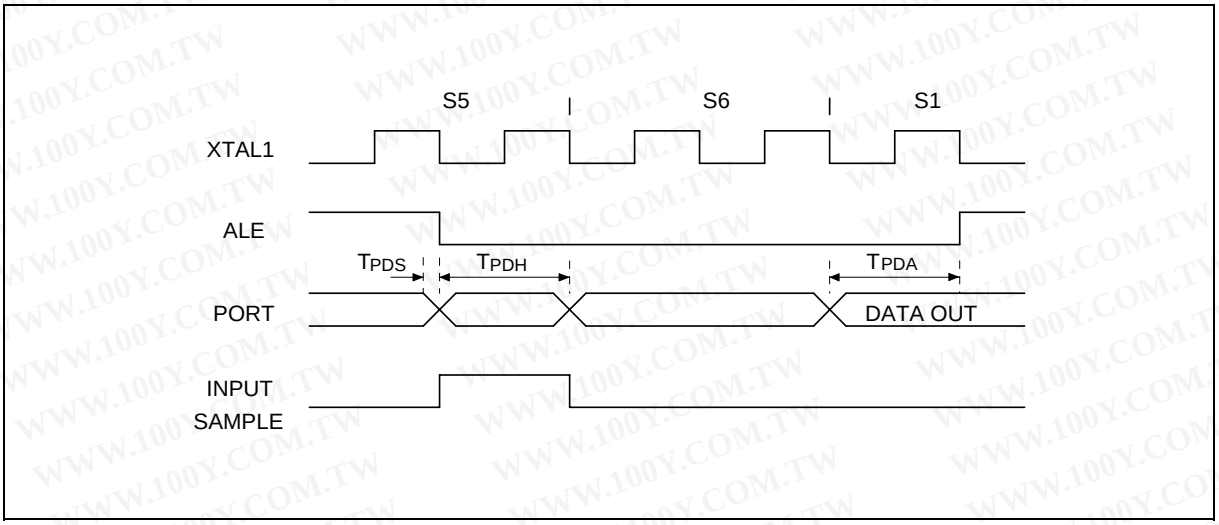


PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{WR}$ Low	TDAW	3 TCP-Δ	-	3 TCP+Δ	nS
Data Valid to $\overline{WR}$ Low	TDAD	1 TCP-Δ	-	-	nS
Data Hold from $\overline{WR}$ High	TDWD	1 TCP-Δ	-	-	nS
$\overline{WR}$ Pulse Width	TDWR	6 TCP-Δ	6 TCP	-	nS

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Timing Waveforms, continued

8.4 Port Access Cycle



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	T_{PDS}	1 T_{CP}	-	-	nS
Port Input Hold from ALE Low	T_{PDH}	0	-	-	nS
Port Output to ALE	T_{PDA}	1 T_{CP}	-	-	nS

Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

9. TYPICAL APPLICATION CIRCUIT

9.1 External Program Memory and Crystal

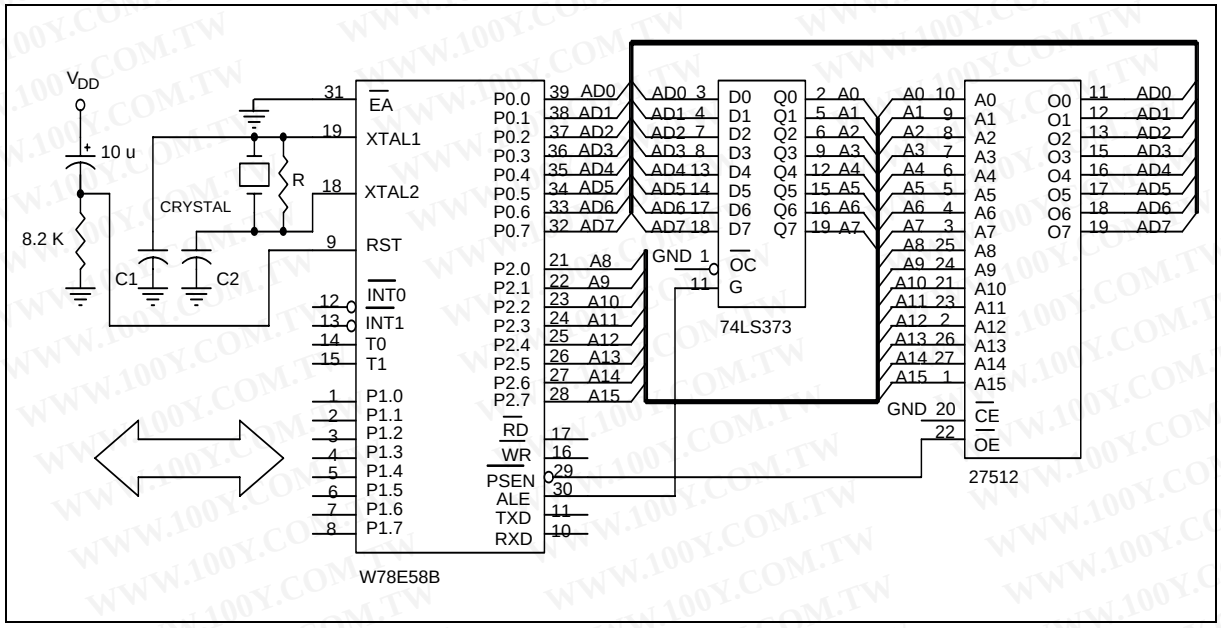


Figure A

CRYSTAL	C1	C2	R
6 MHz	47P	47P	-
16 MHz	30P	30P	-
24 MHz	15P	15P	-
32 MHz	10P	10P	6.8K
40 MHz	5P	5P	4.7K

Above table shows the reference values for crystal applications.

Notes:

1. C1, C2, R components refer to Figure A
2. Crystal layout must get close to XTAL1 and XTAL2 pins on user's application board.

Typical Application Circuit, continued

9.2 Expanded External Data Memory and Oscillator

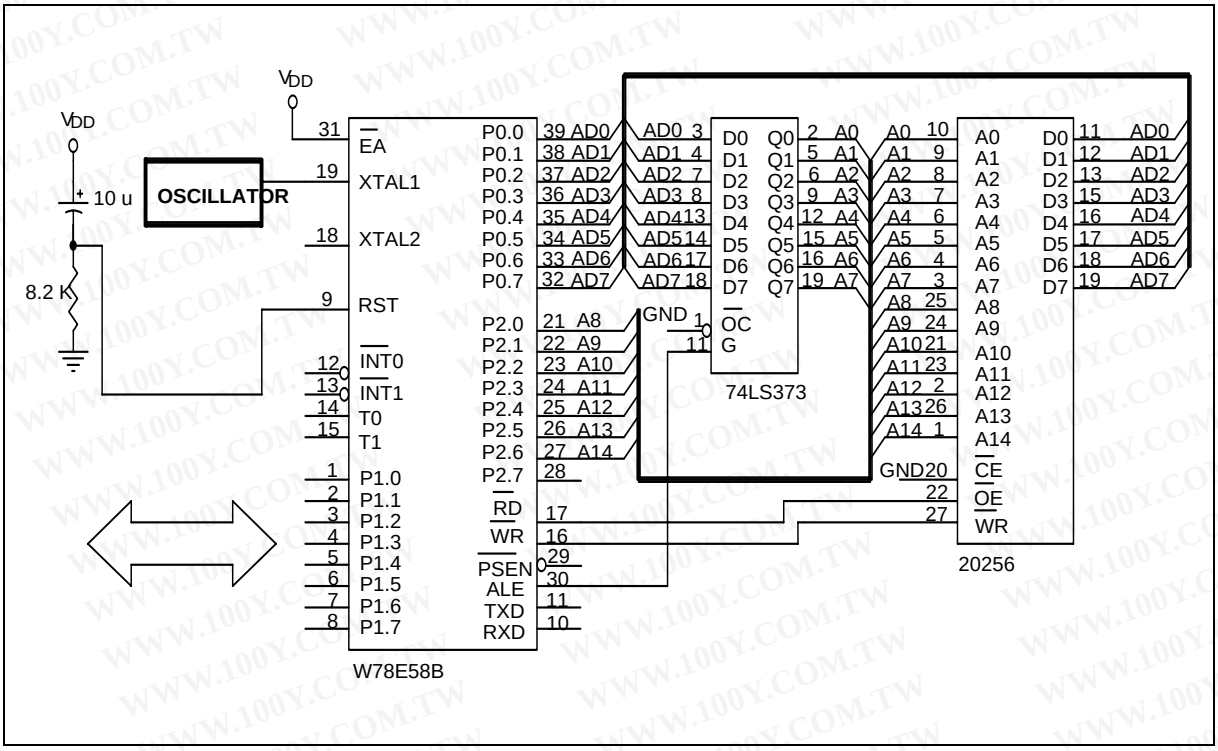
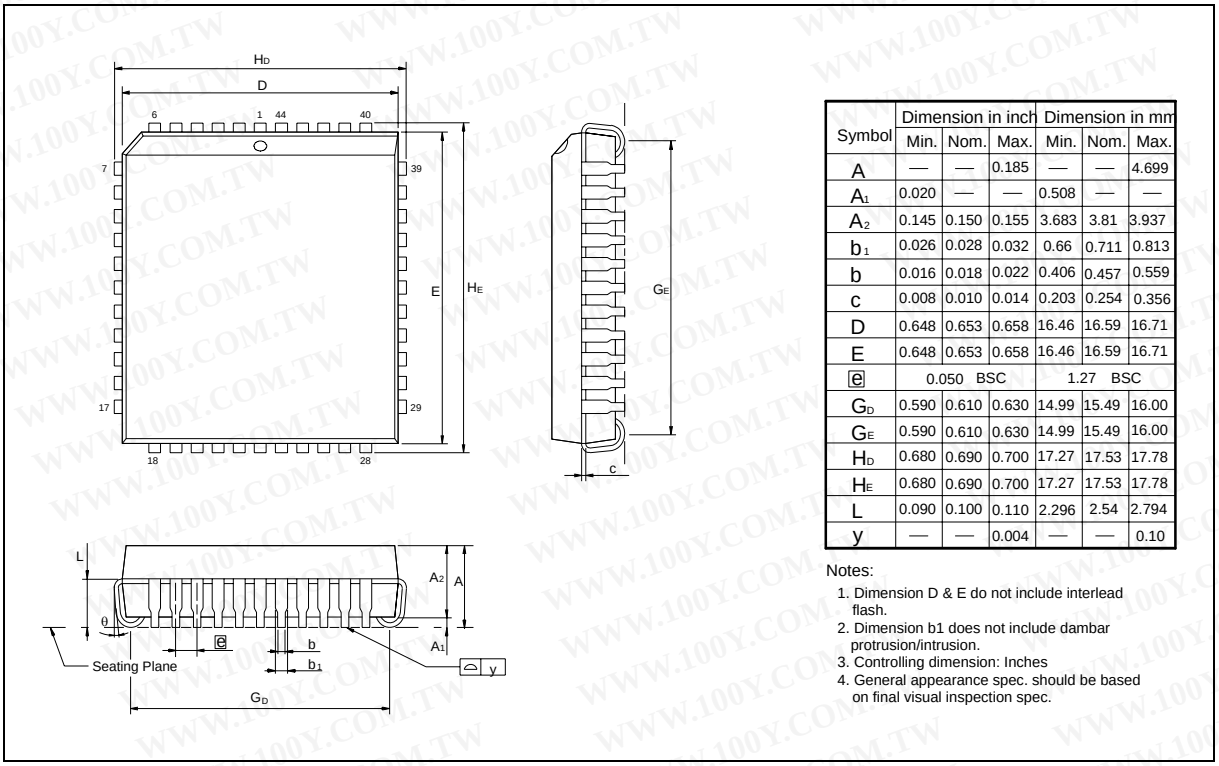


Figure B

10. PACKAGE DIMENSIONS

10.1 44-pin PLCC



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

11. APPLICATION NOTE

11.1 In-system Programming Software Examples

This application note illustrates the in-system programmability of the Winbond W78E65 ROM microcontroller. In this example, microcontroller will boot from 64KB AP FLASH EPROM bank and waiting for a key to enter in-system programming mode for re-programming the contents of 64KB AP FLASH EPROM. While entering in-system programming mode, microcontroller executes the loader program in 4KB LD FLASH EPROM bank. The loader program erases the 64KB AP FLASH EPROM then reads the new code data from external SRAM buffer (or through other interfaces) to update the 64KB AP FLASH EPROM.

EXAMPLE 1:

```
;*****************************************************************************************************************
;* Example of 64K AP FLASH EPROM program: Program will scan the P1.0. If P1.0 = 0, enters in-system
;* programming mode for updating the content of AP FLASH EPROM code else executes the current ROM code.
;* XTAL = 16 MHz
;*****************************************************************************************************************
        .chip 8052
        .RAMCHK OFF
        .symbols

        CHPCON    EQU     BFH
        CHPENR    EQU     F6H
        SFRAL     EQU     C4H
        SFRAH     EQU     C5H
        SFRFD     EQU     C6H
        SFRCN     EQU     C7H

        ORG     0H
        LJMP    100H                    ; JUMP TO MAIN PROGRAM
    ;*********************************************************************
    ;*  TIMER0 SERVICE VECTOR ORG = 000BH
    ;*********************************************************************
        ORG     00BH
        CLR     TR0                     ; TR0 = 0, STOP TIMER0
        MOV     TL0, R6
        MOV     TH0, R7
        RETI
    ;*********************************************************************
    ;*  64K AP FLASH EPROM MAIN PROGRAM
    ;*********************************************************************
      ORG100H

MAIN_64K:
        MOV A, P1                       ; SCAN P1.0
        ANL A, #01H
        CJNE A, #01H, PROGRAM_64K; IF P1.0 = 0, ENTER IN-SYSTEM PROGRAMMING MODE
        JMP NORMAL_MODE

PROGRAM_64K:
        MOV CHPENR, #87H                ; CHPENR = 87H, CHPCON REGISTER WRTE ENABLE
```

```
        MOV CHPENR, #59H            ; CHPENR = 59H, CHPCON REGISTER WRITE ENABLE
        MOV CHPCON, #03H            ; CHPCON = 03H, ENTER IN-SYSTEM PROGRAMMING MODE
        MOV TCON, #00H              ; TR = 0 TIMER0 STOP
        MOV IP, #00H                ; IP = 00H
        MOV IE, #82H                ; TIMER0 INTERRUPT ENABLE FOR WAKE-UP FROM IDLE MODE
        MOV R6, #F0H                ; TL0 = F0H
        MOV R7, #FFH                ; TH0 = FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV TMOD, #01H              ; TMOD = 01H, SET TIMER0 A 16-BIT TIMER
        MOV TCON, #10H              ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H              ; ENTER IDLE MODE FOR LAUNCHING THE IN-SYSTEM
                                    ; PROGRAMMING
;*****************************************************************************
;* Normal mode 64KB AP FLASH EPROM program: depending user's application
;*****************************************************************************
NORMAL_MODE:
            .                       ; User's application program
            .
            .
            .
```

EXAMPLE 2:

```
;*************************************************************************************************************************
Example of 4 KB LD FLASH EPROM program: This loader program will erase the 64KB AP FLASH EPROM first, then reads the new ;* code from external SRAM and program them into 32 KB AP FLASH EPROM bank. XTAL = 16 MHz
;*************************************************************************************************************************
    .chip 8052
    .RAMCHK OFF
    .symbols

    CHPCON    EQU    BFH
    CHPENR    EQU    F6H
    SFRAL     EQU    C4H
    SFRAH     EQU    C5H
    SFRFD     EQU    C6H
    SFRCN     EQU    C7H

        ORG    000H
        LJMP   100H                 ; JUMP TO MAIN PROGRAM
  ;*************************************************************************
  ;* 1. TIMER0 SERVICE VECTOR ORG = 0BH
  ;*************************************************************************
        ORG 000BH
        CLR  TR0                    ; TR0 = 0, STOP TIMER0
        MOV TL0, R6
        MOV TH0, R7
        RETI
  ;*************************************************************************
  ;*  4KB LD FLASH EPROM MAIN PROGRAM
  ;*************************************************************************
```

```
        ORG 100H
MAIN_4K:
        MOV SP, #C0H
        MOV CHPENR, #87H          ; CHPENR = 87H, CHPCON WRITE ENABLE.
        MOV CHPENR, #59H          ; CHPENR = 59H, CHPCON WRITE ENABLE.
        MOV CHPCON, #03H          ; CHPCON = 03H, ENABLE IN-SYSTEM PROGRAMMING.
        MOV CHPENR, #00H          ; DISABLE CHPCON WRITE ATTRIBUTE

        MOV TCON, #00H            ; TCON = 00H, TR = 0 TIMER0 STOP
        MOV TMOD, #01H            ; TMOD = 01H, SET TIMER0 A 16BIT TIMER
        MOV IP, #00H              ; IP = 00H
        MOV IE, #82H              ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV R6, #F0H
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV TCON, #10H            ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H            ; ENTER IDLE MODE

 UPDATE_64K:
        MOV TCON, #00H            ; TCON = 00H, TR = 0 TIM0 STOP
        MOV IP, #00H              ; IP = 00H
        MOV IE, #82H              ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV TMOD, #01H            ; TMOD = 01H, MODE1
        MOV R6, #E0H              ; SET WAKE-UP TIME FOR ERASE OPERATION, ABOUT 15 mS.
        DEPENDING
                                  ; ON USER'S SYSTEM CLOCK RATE.
        MOV R7, #B1H
        MOV TL0, R6
        MOV TH0, R7

ERASE_P_4K:
        MOV SFRCN, #22H           ; SFRCN (C7H) = 22H ERASE 64K
        MOV TCON, #10H            ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H            ; ENTER IDLE MODE (FOR ERASE OPERATION)

;*********************************************************************
;* BLANK CHECK
;*********************************************************************
        MOV SFRCN, #0H            ; READ 64KB AP FLASH EPROM MODE
        MOV SFRAH, #0H            ; START ADDRESS = 0H
        MOV SFRAL,  #0H
        MOV R6, #FEH              ; SET TIMER FOR READ OPERATION, ABOUT 1.5 µS.
        MOV R7,  #FFH
        MOV TL0,R6
        MOV TH0,   R7

BLANK_CHECK_LOOP:
        SETB TR0                  ; ENABLE TIMER 0
        MOV PCON, #01H            ; ENTER IDLE MODE
        MOV A, SFRFD              ; READ ONE BYTE
        CJNE A, #FFH, BLANK_CHECK_ERROR
        INC SFRAL                 ; NEXT ADDRESS
        MOV A, SFRAL
        JNZ BLANK_CHECK_LOOP
        INC SFRAH
```

```
        MOV A, SFRAH
        CJNE A, #80H, BLANK_CHECK_LOOP   ; END ADDRESS = 7FFFH
        JMP PROGRAM_64KROM

BLANK_CHECK_ERROR:
        MOV P1, #F0H
        MOV P3, #F0H
        JMP $

;*******************************************************************************
;* RE-PROGRAMMING 64KB AP FLASH EPROM BANK
;*******************************************************************************
PROGRAM_64KROM:
        MOV DPTR, #0H       ; THE ADDRESS OF NEW ROM CODE
        MOV R2, #00H        ; TARGET LOW BYTE ADDRESS
        MOV R1, #00H        ; TARGET HIGH BYTE ADDRESS
        MOV DPTR, #0H       ; EXTERNAL SRAM BUFFER ADDRESS
        MOV SFRAH, R1       ; SFRAH, TARGET HIGH ADDRESS
        MOV SFRCN, #21H     ; SFRCN (C7H) = 21 (PROGRAM 64K)
        MOV R6, #BEH        ; SET TIMER FOR PROGRAMMING, ABOUT 50 μS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7

PROG_D_64K:
        MOV SFRAL, R2           ; SFRAL (C4H) = LOW BYTE ADDRESS
        MOVX A, @DPTR           ; READ DATA FROM EXTERNAL SRAM BUFFER. BY ACCORDING USER?
                                ; CIRCUIT, USER MUST MODIFY THIS INSTRUCTION TO FETCH CODE
        MOV SFRFD, A            ; SFRFD (C6H) = DATA IN
        MOV TCON, #10H          ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H          ; ENTER IDLE MODE (PRORGAMMING)
        INC DPTR
        INC R2
        CJNE R2, #0H, PROG_D_64K
        INC  R1
        MOV SFRAH, R1
        CJNE R1, #80H, PROG_D_64K

;*******************************************************************************
; * VERIFY 64KB AP FLASH EPROM BANK
;*******************************************************************************
        MOV R4, #03H            ; ERROR COUNTER
        MOV R6, #FEH            ; SET TIMER FOR READ VERIFY, ABOUT 1.5 μS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV DPTR, #0H           ; The start address of sample code
        MOV R2, #0H             ; Target low byte address
        MOV R1, #0H             ; Target high byte address
        MOV SFRAH, R1           ; SFRAH, Target high address
        MOV SFRCN, #00H         ; SFRCN = 00 (Read ROM CODE)

READ_VERIFY_64K:
        MOV SFRAL,  R2          ; SFRAL (C4H) = LOW ADDRESS
```

```
        MOV TCON,   #10H        ; TCON = 10H, TR0 = 1, GO
        MOV PCON,   #01H
        INC R2
        MOVX A, @DPTR
        INC DPTR
        CJNE A, SFRFD, ERROR_64K
        CJNE R2, #0H, READ_VERIFY_64K
        INC R1
        MOV SFRAH, R1
        CJNE R1, #80H, READ_VERIFY_64K

;*****************************************************************************
;* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU
;*****************************************************************************
        MOV CHPENR, #87H        ; CHPENR = 87H
        MOV CHPENR, #59H        ; CHPENR = 59H
        MOV CHPCON, #83H        ; CHPCON = 83H, SOFTWARE RESET.

ERROR_64K:
        DJNZ R4, UPDATE_64K     ; IF ERROR OCCURS, REPEAT 3 TIMES.
        .                       ; IN-SYSTEM PROGRAMMING FAIL, USER'S PROCESS TO DEAL WITH IT.
        .
        .
        .
```

12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	May 14, 2003	-	Initial Issued
A2	Dec. 30, 2004	2	Add Lead Free package
A3	Feb. 14, 2005	2	Add Lead Free DIP
		5	Remove P4.4 ~ P4.7
A4	April 20, 2005	38	Add Important Notice
A5	June 22, 2005	27	Correct operating speed from 20Mhz to 40Mhz
		32	Add 32M/40Mhz items in the table
A6	Aug. 25, 2005	3, 5	Add Port 0 pull-up resisters information
A7	Jan. 9, 2006	3	Add W78E65F-40 and W78E065A40FL

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