SECTION 5—BiMOS SMART POWER INTERFACE DRIVERS

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SELECTION GUIDE

Description	I_{OUT}	V_{OUT}	Device Type	Page
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8-Bit	350 mA	80 V	UCN-5822A	5-55
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8-Bit	−25 mA	80 V	UCN-5815A-1	5-46
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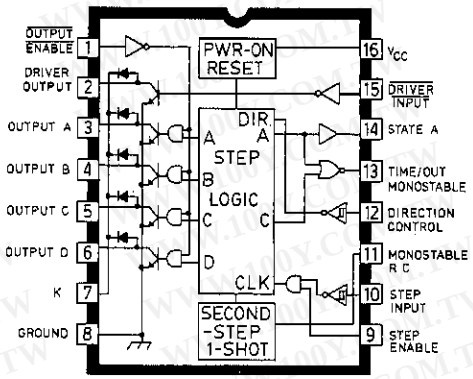
8 of 32-Bit AC Plasma Display Drivers	±15 mA	100 V	UCN-5857/59A/EP	5-103

Current ratings shown are maximum tested condition; voltage ratings are maximum allowable.
†Internal transient-suppression diodes included for inductive-load protection.
*New product, contact factory for information.

UCN-4202A AND UCN-4203A
STEPPER-MOTOR TRANSLATORS AND DRIVERS

FEATURES

- 600 mA Output Current
- Full-Step or Double-Step Operation
- Single-Input Direction Control
- Power-On Reset
- Internal Transient Suppression
- Schmitt Trigger Inputs



DWG. NO. A-11,184

DESIGNED TO DRIVE permanent-magnet stepper motors with current ratings of up to 500 mA, these integrated circuits employ a full-step, double-pulse drive scheme that allows use of up to 90 percent of available motor torque. The two devices differ only in output-voltage ratings: Type UCN-4202A has a 20 V breakdown-voltage rating and a 15 V sustaining voltage rating; Type UCN-4203A has a 50 V breakdown-voltage rating and a 35 V sustaining voltage rating.

Both drivers are bipolar I^2L designs containing approximately 100 logic gates, TTL-compatible input/output circuitry, and 600 mA outputs with internal transient suppressors. The devices operate with a minimum of external components.

The four-phase stepper-motor load is controlled by step-logic functions. To step the load from one position to the next, STEP INPUT is pulled down to a logic low for at least 1 μs, then allowed to return to a logic high. The step logic is activated on the positive-going edge, which in turn activates one of the four current-sink outputs. DIRECTION CONTROL determines the sequence of states (A-B-C-D or A-D-C-B).

In the full-step mode, the MONOSTABLE RC timing pin is tied to V_{CC}, making states B and D stationary. A separate input pulse is required to move through each of the four output states.

In the double-step mode, states B and D are transition states with duration determined by MONOSTABLE RC timing. Improved motor torque is obtained at double the nominal motor step angle, and motor stability is improved for high step rates.

Higher current ratings, or bipolar operation, can be obtained by using Type UCN-4202A or UCN-4203A as a logic translator to drive integrated motor drivers (Sprague UDN-2950Z, UDN-2953B, or UDN-2954W) or discrete high-power transistors.

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ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

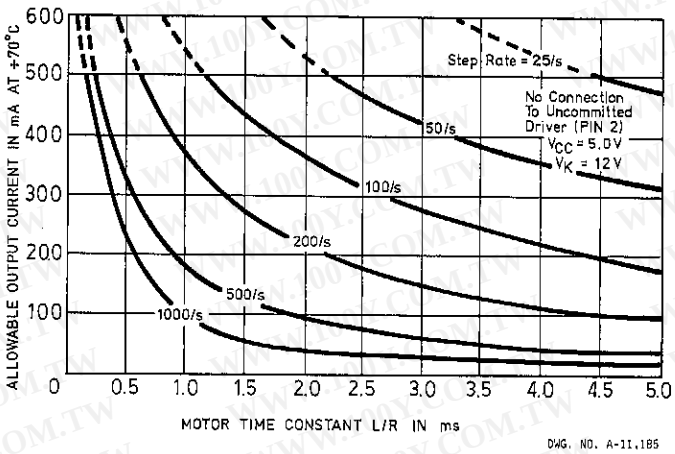
Supply Voltage, V_{CC}	7.0 V
V_K (UCN-4202A)	20 V
(UCN-4203A)	50 V
Output Voltage, V_{OUT} (UCN-4202A)	20 V
(UCN-4203A)	50 V
Input Voltage, V_{IN}	7.0 V
Output Sink Current, I_{OUT}	600 mA
Power Dissipation, P_D (One Driver)	0.8 W
(Total Package)	2.0 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

*Derate at the rate of 16.6 mW/°C above +25°C.

RECOMMENDED OPERATING CONDITIONS

Characteristic	UCN-4202A			UCN-4203A			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage, V_{CC}	4.5	5.0	5.5	4.5	5.0	5.5	V
V_K	—	12	13.5	—	30	35	V
Output Voltage, V_{CE}	—	—	13.5	—	—	35	V
Output Sink Current, I_{OUT}	—	—	500	—	—	500	mA
Operating Temperature, T_A	0	25	70	0	25	70	°C

MAXIMUM COLLECTOR CURRENT AS A FUNCTION OF MOTOR TIME CONSTANT



Notes: 1. Values shown take into account static d-c losses ($V_{SAT}I_{OUT}$ and $V_{CC}I_{CC}$) as well as switching losses induced by inductive flyback through the clamp diodes at V_K = 12 V. Maximum package power dissipation is assumed to be 1.33 W at +70°C. Higher package power dissipation may be obtained at lower operating temperatures.

2. Use of external discrete flyback diodes will eliminate power dissipation resulting from switching losses and will allow the full 500 mA output capability (Output A, B, C, or D and the Driver Output) under all conditions.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = +5.0$ V (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Max.	Units
Supply Current	I_{CC}	All	2 Drivers ON	—	85	mA
TTL Inputs (Pins 1, 9, and 15), TTL Outputs (Pins 13 and 14)						
Input Voltage	$V_{IN(1)}$	All	$V_{CC} = 4.5$ V	2.0	—	V
	$V_{IN(0)}$	All	$V_{CC} = 5.5$ V	—	0.8	V
Input Current	$I_{IN(1)}$	All	$V_{CC} = 5.5$ V, $V_{IN} = 2.4$ V	—	40	μA
	$I_{IN(0)}$	All	$V_{CC} = 5.5$ V, $V_{IN} = 0.4$ V	—	−1.6	mA
Input Clamp Voltage	V_{IK}	All	$I_{IN} = -12$ mA	—	−1.5	V
Output Voltage	$V_{OUT(1)}$	All	$V_{CC} = 4.5$ V, $I_{OUT} = 80$ μA	2.4	—	V
	$V_{OUT(0)}$	UCN-4202A	$V_{CC} = 4.5$ V, $I_{OUT} = 3.2$ mA	—	0.4	V
		UCN-4203A	$V_{CC} = 4.5$ V, $I_{OUT} = 1.5$ mA	—	0.4	V
Output Current	$I_{OUT(SC)}$	All	$V_{CC} = 5.5$ V, $V_{OUT} = 0$	—	38	mA
Second-Step Monostable RC Input (Pin 11)						
Time Constant	t_{RC}	All		0.95	1.3	s/RC
Reset Voltage	V_{MR}	All	$R = 200$ kΩ, $I_{IN} = 25$ μA	—	50	mV
Reset Current	I_{MR}	All	$V_{IN} = 2.0$ V	40	—	μA
Schmitt Trigger Inputs (Pins 10 and 12)						
Threshold Voltage	V_{T+}	All		1.3	2.1	V
	V_{T-}	All		0.6	1.1	V
Hysteresis	ΔV_T	All		0.2	—	V
Input Current	$I_{IN(1)}$	All	$V_{CC} = 4.5$ V, $V_{IN} = 2.4$ V, $T_A = 25°C$	—	5.0	μA
		All	$V_{CC} = 4.5$ V, $V_{IN} = 2.4$ V, $T_A = 70°C$	—	40	μA
	$I_{IN(0)}$	All	$V_{CC} = 5.5$ V, $V_{IN} = 0.4$ V	—	−1.6	mA
Input Clamp Voltage	V_{IK}	All	$I_{IN} = -12$ mA	—	−1.5	V
Open Collector Outputs (Pins 2, 3, 4, 5, and 6)						
Output Leakage Current	I_{CEX}	UCN-4202A	$V_{CC} = 5.5$ V, K = Open, $V_{OUT} = 20$ V	—	500	μA
		UCN-4203A	$V_{CC} = 5.5$ V, K = Open, $V_{OUT} = 50$ V	—	500	μA
Output Saturation Voltage	$V_{CE(SAT)}$	UCN-4202A	$V_{CC} = 4.5$ V, $I_{OUT} = 300$ mA	—	500	mV
			$V_{CC} = 4.5$ V, $I_{OUT} = 400$ mA	—	750	mV
			$V_{CC} = 4.5$ V, $I_{OUT} = 500$ mA	—	900	mV
		UCN-4203A	$V_{CC} = 4.5$ V, $I_{OUT} = 300$ mA	—	850	mV
			$V_{CC} = 4.5$ V, $I_{OUT} = 400$ mA	—	1100	mV
			$V_{CC} = 4.5$ V, $I_{OUT} = 500$ mA	—	1350	mV
Output Sustaining Voltage	$V_{CE(SUS)}$	UCN-4202A	$I_{OUT} = 30$ mA, $t_p \leq 300$ μs, Duty Cycle ≤ 2%	15	—	V
		UCN-4203A	$I_{OUT} = 30$ mA, $t_p \leq 300$ μs, Duty Cycle ≤ 2%	35	—	V
Turn-On Delay	t_{pd0}	All	0.5 E_{in} (Pin 10) to 0.5 E_{out}	—	10	μs
Turn-Off Delay	t_{pd1}	All	0.5 E_{in} (Pin 10) to 0.5 E_{out}	—	10	μs
Clamp Diode Leakage Current	I_R	UCN-4202A	$V_R = 20$ V	—	50	μA
		UCN-4203A	$V_R = 50$ V	—	50	μA
Clamp Diode Forward Voltage	V_F	All	$I_F = 500$ mA	—	3.0	V

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FUNCTIONAL DESCRIPTION

Power-On Reset

An internal RS flip-flop sets the Output A "ON" with the initial application of power. This state occurs approximately 30 μs after the logic supply voltage reaches 4 V with supply rise times of up to 10 ms/V. Once reset, the circuit functions according to the logic input conditions.

Step Enable

Pin 9 (STEP ENABLE) must be held high to enable the step pulses for advancing the motor to reach the translator logic clock circuits. Pulling this pin low inhibits the translator logic.

Step Input

Pin 10 (STEP INPUT) is normally high. The logic will advance one position on the positive transition after the input has been pulled low for at least 1 μs. The STEP INPUT current specification is compatible with NMOS and CMOS.

Direction Control

The direction of output rotation is determined by the logic level at pin 12. If the input is held high the rotation is A-D-C-B; if pulled low the rotation is A-B-C-D. This input is also NMOS and CMOS compatible.

Output Enable

Outputs A through D are inhibited (all outputs OFF) when pin 1 (OUTPUT ENABLE) is at high level. This condition creates a potential for wired-OR device outputs, or other potential control functions such as chopping or bi-level drive.

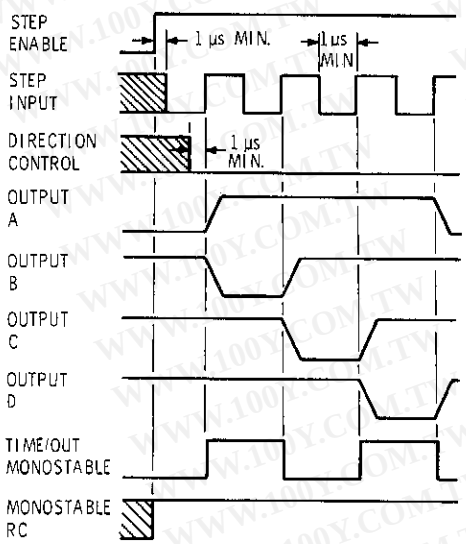
Transient Suppression

All five power outputs are diode protected against inductive transients. Zener diode or resistor "flyback" transient suppression is often used, provided the peak output voltage does not exceed the sustaining voltage rating of the device (15 V for Type UCN-4202A or 35 V for Type UCN-4203A).

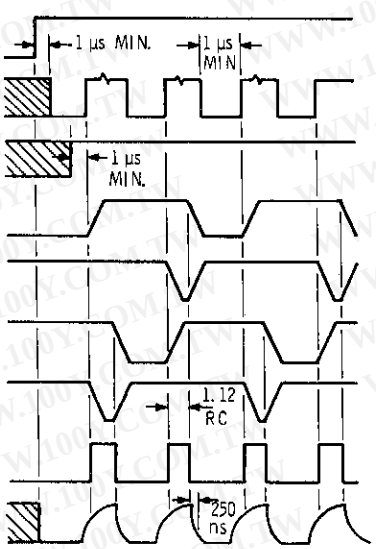
Full-Step/Double-Step

Full-step operation is the most commonly used drive technique. The devices are capable of unipolar drive without external active devices, either in a full-step mode (pin 11, Monostable RC, tied high), or in a double-step mode (pin 11 connected to RC timing). The double-step mode provides improved torque characteristics, while the specified angular increment is doubled.

FULL-STEP MODE



DOUBLE-STEP MODE



Dwg. No. A-11,844

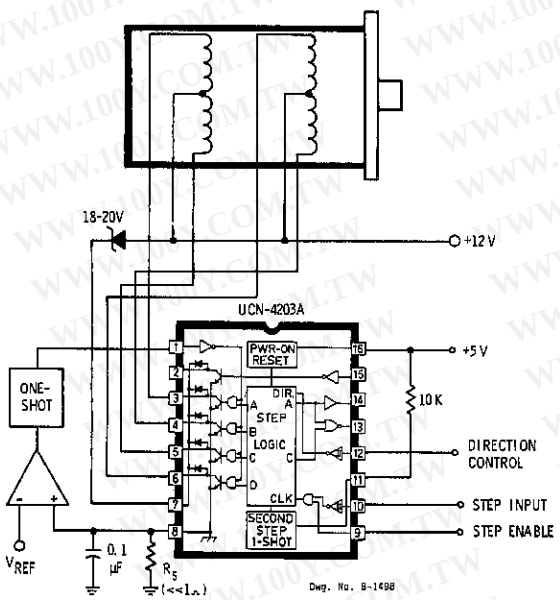
STEPPER MOTORS

(Representative List)

Manufacturer	Model	L/R	Typ. Ratings	Step
Eastern Air Devices	LA23ACK-2	1.4 ms	440 mA, 12 V	1.8°
	LA23ACK-3	1.25 ms	220 mA, 24 V	1.8°
	LA23ACY-1	1.2 ms	440 mA, 12 V	7.5°
	LA34ADK-6	2.6 ms	530 mA, 14 V	1.8°
IMC Hanson	S-114	1.6 ms	340 mA, 12 V	7.5°
	S-115	1.9 ms	130 mA, 12 V	7.5°
	S-382	1.6 ms	171 mA, 24 V	7.5°
	S-406	4.3 ms	280 mA, 24 V	15°
	S-451	3.9 ms	280 mA, 24 V	7.5°
North American Phillips	K82701-P2	1.5 ms	330 mA, 12 V	7.5°
	K83701-P2	1.5 ms	330 mA, 12 V	15°
Septor	S-0912A	1.5 ms	340 mA, 12 V	9°
Superior Electric	M061-FD-301	0.8 ms	440 mA, 12 V	1.8°
	M061-FD-311	1.5 ms	220 mA, 20 V	1.8°

TYPICAL APPLICATIONS

CHOPPER DRIVE CIRCUIT
Used to Drive a 12 V, 500 mA Unipolar Stepper Motor



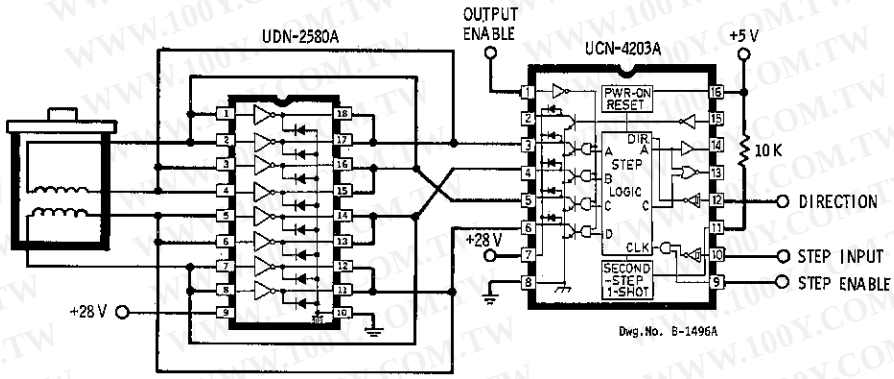
DISC DRIVE APPLICATIONS

These stepper-motor translator/drivers provide additional special-purpose logic for use in disc drive applications. Pin 14 (STATE A) is high with OUTPUT A activated and is used with other drive logic in determining Track 0 Position on the disc. Pin 13 (TIME/OUT MONOSTABLE) in disc drive applications is called ON TRACK and is low with either OUTPUT A or OUTPUT C activated. It is used as a WRITE ENABLE condition with other drive logic.

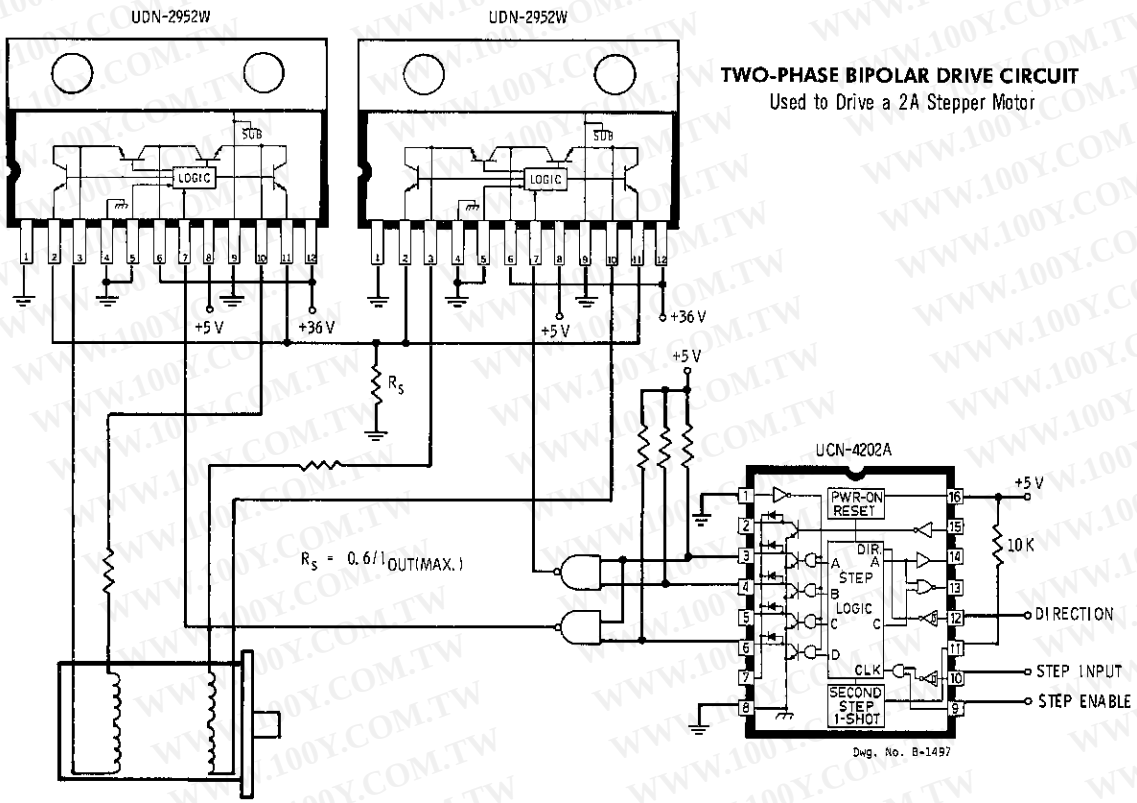
An independent driver (pins 2 and 15) is used to control the head load solenoid.

TYPICAL APPLICATIONS

BIPOLAR DRIVE CIRCUIT
Used to Drive a 500 mA Stepper Motor

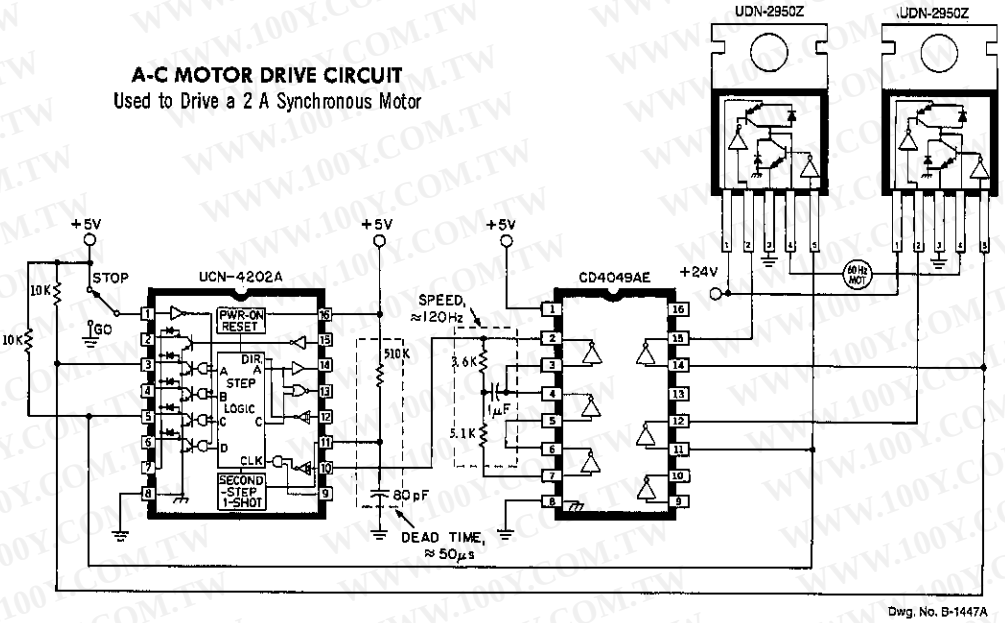


TWO-PHASE BIPOLAR DRIVE CIRCUIT
Used to Drive a 2A Stepper Motor



TYPICAL APPLICATIONS

A-C MOTOR DRIVE CIRCUIT
Used to Drive a 2 A Synchronous Motor



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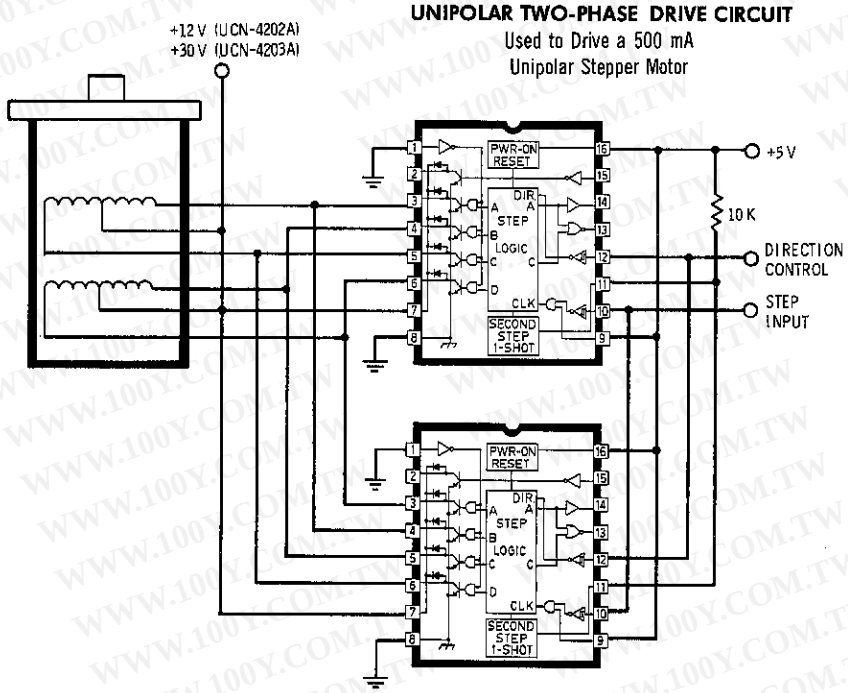
UNIPOLAR TWO-PHASE DRIVE CIRCUIT
Used to Drive a 500 mA
Unipolar Stepper Motor



Dwg. No. B-1499

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UCN-4204B AND UCN-4205B-2
STEPPER-MOTOR TRANSLATORS/DRIVERS

FEATURES

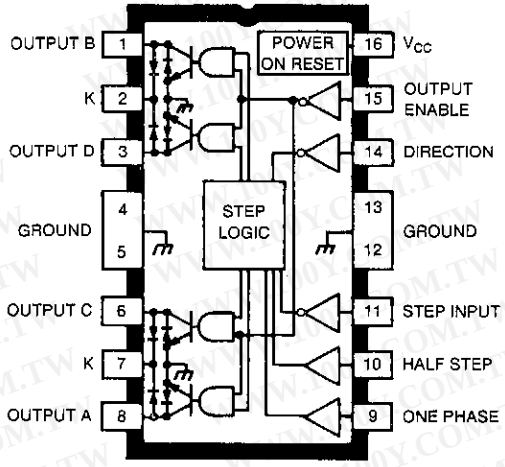
- 1.5 A Max. Output Current
- Wave Drive, Two-Phase, and Half-Step
- Internal Clamp Diodes
- Output Enable
- Internal Thermal Shutdown
- Power-ON Reset

Providing control and direct drive to unipolar four-phase stepper motors, UCN-4204B and UCN-4205B-2 integrated circuits are rated up to 1.5 A per phase and will sustain inductive loads to 15 V or 25 V, respectively. In other respects, the UCN-4204B and UCN-4205B-2 are identical. Both devices feature on-chip I^2L logic to provide direction and OUTPUT ENABLE control functions, thermal shutdown, and power-ON reset, as well as externally selectable one-phase (wave drive), two-phase, and half-step drive formats.

The one-phase or wave-drive format consists of energizing one motor phase at a time in an A-B-C-D (or D-C-B-A) sequence. This excitation mode consumes the least power and assures positional accuracy regardless of any winding imbalance in the motor. Devices with 500 mA output current ratings, using this drive format, are available as Sprague UCN-4202A and UCN-4203A.

Two-phase drive energizes two adjacent phases in each detent position (AB-BC-CD-DA). This mode offers an improved torque-speed product, greater detent torque, and is less susceptible to motor resonance.

Half-step excitation alternates between the one-phase and two-phase modes (A-AB-B-BC-C-CD-D-DA), providing an eight-step sequence.



Dwg. No. W-109

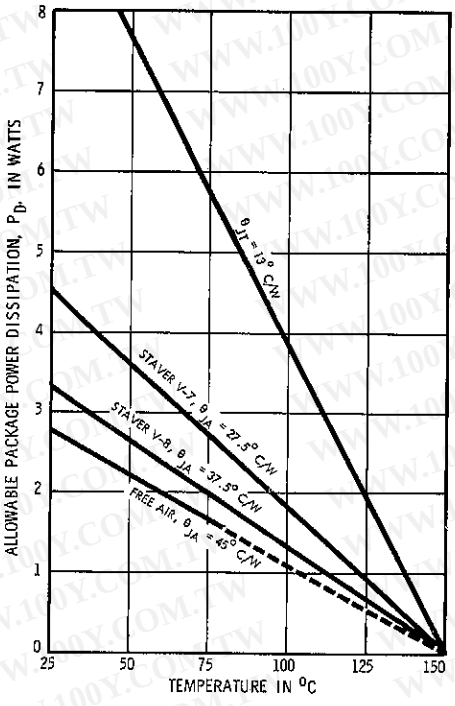
Both devices are supplied in 16-pin dual in-line plastic batwing packages with heat-sinkable tabs and copper lead frames for improved thermal characteristics.

ABSOLUTE MAXIMUM RATINGS
at $T_A = +25°C$

Output Voltage, V_{CE}
(UCN-4204B) ..... 20 V
(UCN-4205B-2) ..... 30 V
Output Sink Current, I_{OUT} ..... 1.5 A
Logic Supply Voltage, V_{CC} ..... 7.0 V
Input Voltage, V_{IN} ..... 7.0 V
Package Power Dissipation, P_D ..... See Graph
Operating Temperature Range, T_A .... −20°C to +85°C
Storage Temperature Range, T_S .... −55°C to +150°C

Output current rating will be limited by ambient temperature, heat sinking, air flow, duty cycle, and number of outputs conducting. Under any set of conditions, do not exceed a 1.5 A peak output current or a junction temperature of +150°C.

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



Dwg. No. A-11, 793A

WAVE-DRIVE SEQUENCE

←DIRECTION = L

Half Step = L, One Phase = H				
Step	A	B	C	D
POR	ON	OFF	OFF	OFF
1	ON	OFF	OFF	OFF
2	OFF	ON	OFF	OFF
3	OFF	OFF	ON	OFF
4	OFF	OFF	OFF	ON

→DIRECTION = H

TWO-PHASE DRIVE SEQUENCE

←DIRECTION = L

Half Step = L, One Phase = L				
Step	A	B	C	D
POR	ON	OFF	OFF	ON
1	ON	OFF	OFF	ON
2	ON	ON	OFF	OFF
3	OFF	ON	ON	OFF
4	OFF	OFF	ON	ON

→DIRECTION = H

HALF-STEP DRIVE SEQUENCE

←DIRECTION = L

Half Step = H, One Phase = L				
Step	A	B	C	D
POR	ON	OFF	OFF	OFF
1	ON	OFF	OFF	OFF
2	ON	ON	OFF	OFF
3	OFF	ON	OFF	OFF
4	OFF	ON	ON	OFF
5	OFF	OFF	ON	OFF
6	OFF	OFF	ON	ON
7	OFF	OFF	OFF	ON
8	ON	OFF	OFF	ON

→DIRECTION = H

5

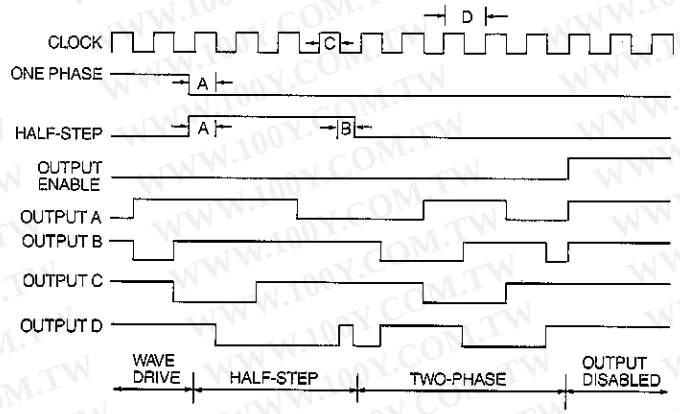
TRUTH TABLE

	PIN 9	PIN 10
TWO-PHASE	L	L
ONE-PHASE	H	L
HALF-STEP	L	H
STEP-INHIBIT	H	H

TIMING CONDITIONS

A. Minimum data set-up time ..... 1 µs
B. Minimum data hold time ..... 1 µs
C. Minimum data pulse width ..... 1 µs
D. Minimum clock period ..... 200 µs

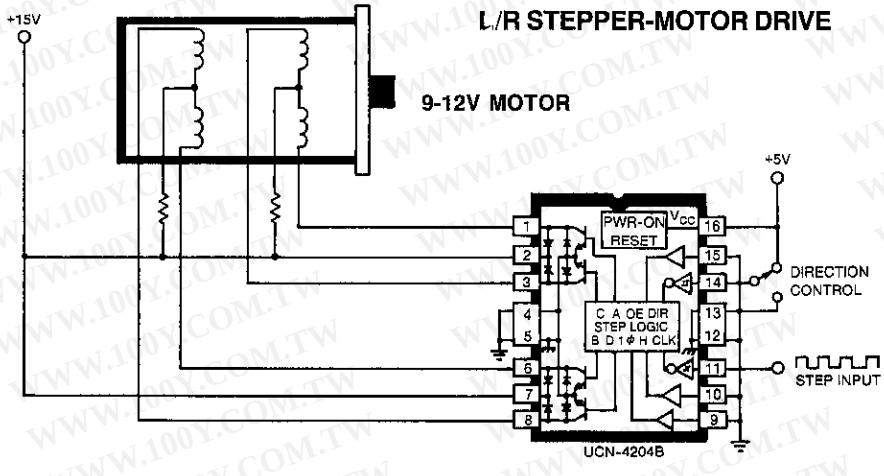
Note: Clock must be in low state when changing state of ONE PHASE, HALF-STEP, or DIRECTION or unwanted stepping may occur.



Dwg. No. W-110

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $T_{TAB} \leq +70°C$, $V_{CC} = 5\,V$

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	UCN-4204B	$V_{CC} = 5.5\,V$, K = Open, $V_{OUT} = 20\,V$	—	50	µA
		UCN-4205B-2	$V_{CC} = 5.5\,V$, K = Open, $V_{OUT} = 30\,V$	—	50	µA
Output Sustaining Voltage	$V_{CE(sus)}$	UCN-4204B	$I_{OUT} = 1.25\,A$, L = 3 mH	15	—	V
		UCN-4205B-2	$I_{OUT} = 1.0\,A$, L = 3 mH	25	—	V
Output Saturation Voltage	$V_{CE(sat)}$	UCN-4204B	$V_{CC} = 4.5\,V$, $I_{OUT} = 700\,mA$	—	0.5	V
			$V_{CC} = 4.5\,V$, $I_{OUT} = 1.0\,A$	—	0.7	V
			$V_{CC} = 4.5\,V$, $I_{OUT} = 1.25\,A$	—	1.0	V
		UCN-4205B-2	$V_{CC} = 4.5\,V$, $I_{OUT} = 700\,mA$	—	0.8	V
			$V_{CC} = 4.5\,V$, $I_{OUT} = 1.0\,A$	—	1.25	V
Clamp Diode Leakage Current	I_R	UCN-4204B	$V_R = 20\,V$	—	50	µA
		UCN-4205B-2	$V_R = 30\,V$	—	50	µA
Clamp Diode Forward Voltage	V_F	Both	$I_F = 1.5\,A$	—	3.0	V
Input Current	$I_{IN(1)}$	Both	$V_{CC} = 4.5\,V$, $V_{IN} = 2.0\,V$, $T_A = 25°C$	—	5.0	µA
		Both	$V_{CC} = 4.5\,V$, $V_{In} = 2.0\,V$, $T_A = 70°C$	—	40	µA
	$I_{IN(0)}$	Both	$V_{CC} = 5.5\,V$, $V_{IN} = 0.8\,V$	—	−1.6	mA
Input Voltage	$V_{IN(1)}$	Both	$V_{CC} = 4.5\,V$	2.0	—	V
	$V_{IN(0)}$	Both	$V_{CC} = 5.5\,V$	—	0.8	V
Input Clamp Voltage	V_{IN}	Both	$I_{UB} = -12\,mA$	—	−1.5	V
Supply Current	I_{CC}	Both	2 Drivers ON	—	90	mA
Turn-ON Delay	t_{on}	Both	0.5 E_{in} (Pin 11) to 0.5 E_{out}	—	10	µs
Turn-OFF Delay	t_{off}	Both	0.5 E_{in} (Pin 11) to 0.5 E_{out}	—	10	µs



UCN-4805A
BiMOS LATCHED DECODER/DRIVER

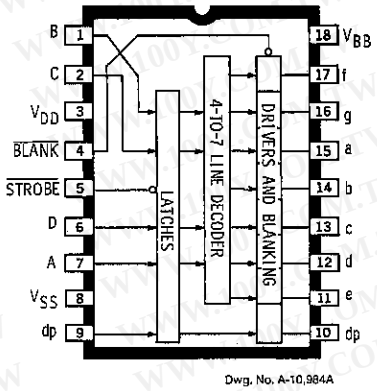
FEATURES

- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Latches
- Hexadecimal Decoding
- Internal Pull-Up/Pull-Down Resistors
- Wide Supply Voltage Range

DESIGNED for use in high-voltage vacuum fluorescent display driver applications, the UCN-4805A latched decoder/driver combines CMOS logic with bipolar source outputs. The device consists of eight high-voltage bipolar sourcing outputs, with internal pull-down resistors and CMOS input latches, hexadecimal decoder, and control circuitry (strobe and blanking).

Type UCN-4805A is intended to serve as the segment driver with standard 7-segment displays incorporating a colon or decimal point. The integrated circuit uses hexadecimal decoding to display 0-9, A, b, C, d, E, and F.

This BiMOS latched decoder/driver has sufficient speed to permit operation with most microprocessor/LSI-based systems. The CMOS input latches provide operation over the supply voltage range of 5 to 15 V with minimum logic loading. Internal output pull-down resistors eliminate the need for external components usually required for fluorescent display applications. When used with standard TTL or low-speed TTL logic, the device may require employment of input pull-up resistors to insure a proper input logic high.



Dwg. No. A-10,984A

UCN-4805A

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ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature and V_{SS} = 0 V

Output Voltage, V_{OUT}	60 V
Logic Supply Voltage Range, V_{DD}	4.5 V to 18 V
Driver Supply Voltage Range, V_{BB}	5.0 V to 60 V
Input Voltage Range, V_{IN}	−0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT}	−40 mA
Package Power Dissipation, P_D	1.82 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +125°C

*Derate at the rate of 18.18 mW/°C above T_A = 25°C.

Caution: Sprague CMOS devices feature input static protection but are still susceptible to damage when exposed to extremely high static electrical charges.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{BB} = 60 V, V_{DD} = 4.75 V to 15.75 V, V_{SS} = 0 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		I_{OUT} = − 25 mA	57.5	—	V
Output Pull-Down Current	I_{OUT}	V_{OUT} = V_{BB}	400	850	μA
Output Leakage Current		T_A = 70°C	—	−15	μA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	5.3	V
		V_{DD} = 15 V	13.5	15.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = 5.0 V	—	100	μA
		V_{DD} = 15 V	—	300	μA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	50	—	kΩ
Supply Current	I_{BB}	Display "8"	—	9.1	mA
		All outputs OFF	—	100	μA
	I_{DD}	V_{DD} = I/O = STROBE = 5.0 V, All other inputs = 0 V	—	200	μA
		V_{DD} = I/O = STROBE = 15 V, All other inputs = 0 V	—	500	μA
		V_{DD} = STROBE = BLANK = 5.0 V, Data latched, Display "8"	—	7.0	mA
		V_{DD} = STROBE = BLANK = 15 V, Data latched, Display "8"	—	21	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

MAXIMUM ALLOWABLE DUTY CYCLE

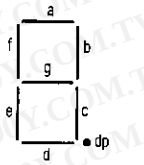
Number of Outputs ON (I_{OUT} = −25 mA)	Max. Allowable Duty Cycle at Ambient Temperature of 50°C	60°C	70°C
8	100%	92%	78%
7	↑	100%	89%
6	↕	↑	100%
↕		↕	↕
1	100%	100%	100%

Caution: Sprague CMOS devices feature input static protection but are still susceptible to damage when exposed to extremely high static electrical charges.

UCN-4805A TRUTH TABLE

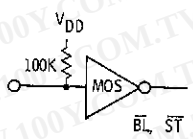
Inputs								Outputs							
D	C	B	A	dp	$\overline{BL}$	$\overline{ST}$	Character	a	b	c	d	e	f	g	dp
0	0	0	0	0	1	0	Zero	1	1	1	1	1	1	0	0
0	0	0	1	0	1	0	One	0	1	1	0	0	0	0	0
0	0	1	0	0	1	0	Two	1	1	0	1	1	0	1	0
0	0	1	1	0	1	0	Three	1	1	1	1	0	0	1	0
0	1	0	0	0	1	0	Four	0	1	1	0	0	1	1	0
0	1	0	1	0	1	0	Five	1	0	1	1	0	1	1	0
0	1	1	0	0	1	0	Six	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	Seven	1	1	1	0	0	0	0	0
1	0	0	0	0	1	0	Eight	1	1	1	1	1	1	1	0
1	0	0	1	0	1	0	Nine	1	1	1	0	0	1	1	0
1	0	1	0	0	1	0	A	1	1	1	0	1	1	1	0
1	0	1	1	0	1	0	b	0	0	1	1	1	1	1	0
1	1	0	0	0	1	0	C	1	0	0	1	1	1	0	0
1	1	0	1	0	1	0	d	0	1	1	1	1	0	1	0
1	1	1	0	0	1	0	E	1	0	0	1	1	1	1	0
1	1	1	1	0	1	0	F	1	0	0	0	1	1	1	0
X	X	X	X	1	1	0	dp	X	X	X	X	X	X	X	1
X	X	X	X	X	0	X	blank	0	0	0	0	0	0	0	0

X = irrelevant

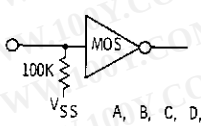


Dwg. No. A-10,985

TYPICAL INPUT CIRCUITS

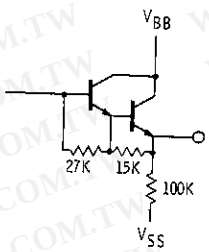


Dwg. No. A-10,979A



Dwg. No. A-10,980

TYPICAL OUTPUT DRIVER



Dwg. No. A-10,981

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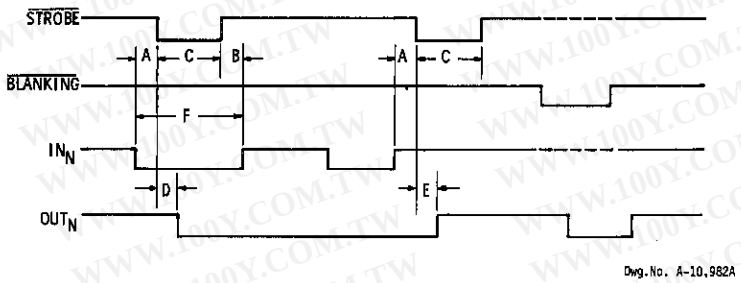
TIMING CONDITIONS

(Logic Levels are V_{DD} and V_{SS})



Dwg. No. A-10,982A

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) ..... 100 ns
B. Minimum Data Active Time After Strobe Disabled (Data Hold Time) ..... 100 ns
C. Minimum Strobe Pulse Width ..... 300 ns
D. Typical Time Between Strobe Activation and Output On to Off Transition ..... 1.0 μs
E. Typical Time Between Strobe Activation and Output Off to On Transition ..... 1.0 μs
F. Minimum Data Pulse Width ..... 500 ns

Information present at an input is transferred to its latch when the STROBE (ST) is low. The latches will continue to accept new data as long as the STROBE is held low. Applications where the latches are bypassed (STROBE tied low) ordinarily require that the BLANKING input be low between digit selection because of possible non-synchronous decoding.

When the BLANKING (BL) input is low, all of the output buffers are disabled (OFF) without affecting the information stored in the latches. With the BLANKING input high, the outputs are controlled by the latch/decoder circuitry.

UCN-4807A AND UCN-4808A
BiMOS ADDRESSABLE LATCHED DRIVERS

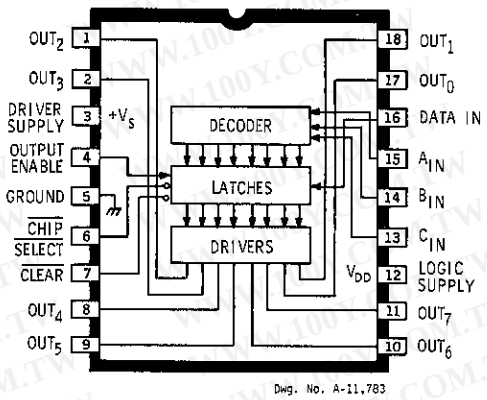
FEATURES

- Addressable Data Entry
- 50 V Current-Sink Outputs
- CMOS, PMOS, NMOS, TTL Compatible
- Low-Power CMOS Logic and Latches
- Wide Supply-Voltage Range

THESE 8-BIT, ADDRESSABLE, latched drivers are used in a wide variety of power demultiplexer applications. They can drive all types of common peripheral power loads, including lamps, relays, solenoids, LEDs, printer heads, heaters, and stepper motors. They can also be used as DMUX drivers for higher power loads requiring discrete power semiconductors.

Type UCN-4807A and UCN-4808A drivers are identical except for output current ratings. The former is rated for a maximum of 200 mA per output while the latter is capable of sinking up to 600 mA per output. The 50 V outputs are bipolar NPN saturated switches with first stage driver currents optimized for each version.

Each MSI array is comprised of a 3-bit to 8-line decoder, 8 type D latches, 8 open-collector output drivers, and MOS control circuitry for $\overline{\text{CHIP SELECT}}$, $\overline{\text{CLEAR}}$, and OUTPUT ENABLE functions. Any of the eight power loads can be addressed individually and can be turned ON or OFF independently of the other loads.



Dwg. No. A-11,783

Under normal operating conditions, all outputs of Type UCN-4807A can sustain 150 mA over the operating temperature range without derating. Type UCN-4808A will sustain 500 mA per output at 30°C and a duty cycle of 33%. Other combinations of number of outputs conducting and duty cycle are shown in the specifications.

These devices are supplied in 18-pin dual in-line plastic packages for operation over the temperature range of −20°C to +85°C.

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UCN-4808A DERATING

Number of Outputs ON (I_{OUT} = 500 mA)	Max. Duty Cycle (with V_{DD} = 5 V) at Ambient Temperature of				
	30°C	40°C	50°C	60°C	70°C
8	33%	29%	25%	21%	17%
7	37%	33%	29%	24%	20%
6	44%	39%	33%	28%	23%
5	52%	46%	40%	34%	28%
4	65%	58%	50%	42%	35%
3	87%	77%	67%	57%	46%
2	100%	100%	100%	85%	70%
1	100%	100%	100%	100%	100%

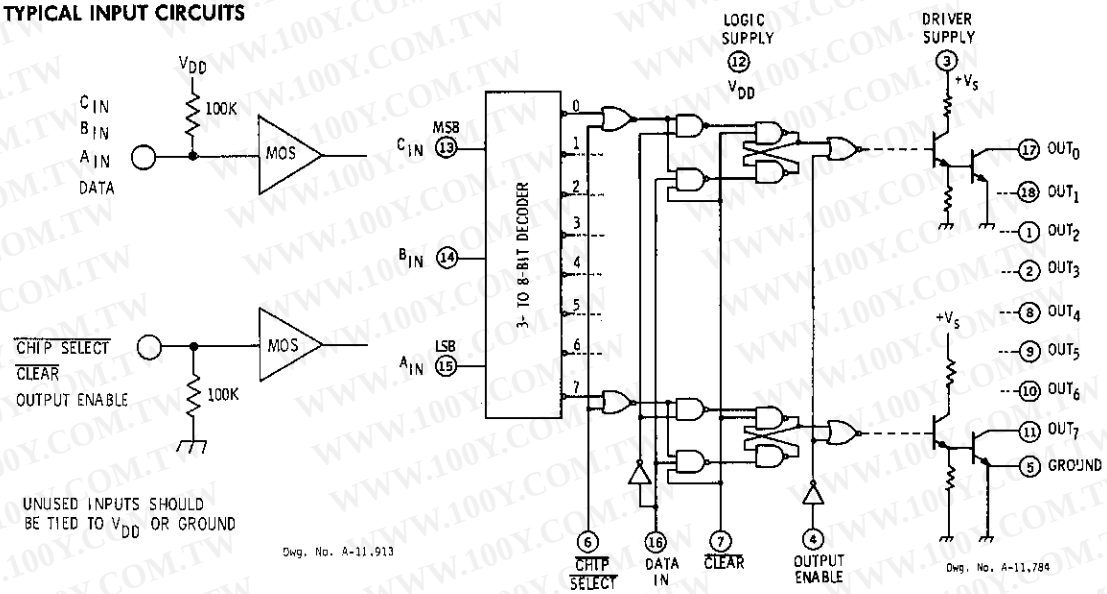
ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature

Output Voltage, V_{OUT} . . . . . 50 V
Logic Supply Voltage Range, V_{DD} . . . . . 4.5 V to 18 V
Driver Supply Voltage Range, V_S . . . . . 4.5 V to 5.5 V
Input Voltage Range, V_{IN} . . . . . −0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT} (UCN-4807A) . . . . . 200 mA
(UCN-4808A) . . . . . 600 mA
Package Power Dissipation, P_D . . . . . 1.82 W*
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +125°C

*Derate at the rate of 18.18 mW/°C above T_A = +25°C.

FUNCTIONAL BLOCK DIAGRAM

TYPICAL INPUT CIRCUITS



Terminal Designation	Function
ADDRESS	A 3-bit binary address on these pins defines which one of the 8 latches is to receive the data. C_{IN} is the most-significant bit; A_{IN} is least significant.
$\overline{\text{CHIP SELECT}}$	When this input is low, the addressed output latch will accept data. When $\overline{\text{CHIP SELECT}}$ is high, the latches will retain their existing state, regardless of ADDRESS or DATA input conditions. This input should be held high while ADDRESS is being changed. $\overline{\text{CHIP SELECT}}$ also allows an additional level of address decoding.
DATA INPUT	When $\overline{\text{CHIP SELECT}}$ is low, the data bit present here is transferred to the addressed latch and output such that (when OUTPUT ENABLE is high) "1" turns the output ON and "0" turns the output OFF.
$\overline{\text{CLEAR}}$	When $\overline{\text{CLEAR}}$ goes from high to low, all latches are reset and outputs are turned OFF.
OUTPUT ENABLE	When this input is high, the outputs are controlled by their respective latches. When OUTPUT ENABLE is low, all outputs are OFF.
OUTPUTS	These are the 8 open-collector NPN outputs.
DRIVER SUPPLY	This is the supply voltage for the first stage of the bipolar output drivers. The nominal supply is 5.0 V.
LOGIC SUPPLY	This is the CMOS logic supply voltage input. Typically it is between 4.75 V and 15.75 V.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5$ V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	UCN-4807A Min.	UCN-4807A Max.	UCN-4808A Min.	UCN-4808A Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 50$ V	—	50	—	50	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 50$ mA	—	0.2	—	—	V
		$I_{OUT} = 100$ mA	—	0.3	—	—	V
		$I_{OUT} = 150$ mA	—	0.4	—	—	V
		$I_{OUT} = 200$ mA	—	—	—	0.5	V
		$I_{OUT} = 350$ mA	—	—	—	0.7	V
		$I_{OUT} = 500$ mA	—	—	—	1.0	V
Input Voltage	$V_{IN(0)}$		—	0.8	—	0.8	V
	$V_{IN(1)}$	$V_{DD} = 15$ V	13.5	—	13.5	—	V
		$V_{DD} = 5$ V	3.5	—	3.5	—	V
Input Current	$I_{IN(1)}$	$V_{IN} = V_{DD} = 15$ V	—	300	—	300	µA
		$V_{IN} = V_{DD} = 5$ V	—	100	—	100	µA
Input Resistance	R_{IN}		50	—	50	—	kΩ
Supply Current	$I_{DD(ON)}$	One Driver ON, $V_{DD} = 15$ V	—	5.0	—	5.0	mA
		One Driver ON, $V_{DD} = 5$ V	—	1.0	—	1.0	mA
	$I_{DD(OFF)}$	CLEAR = 0 V, SELECT = $V_{DD} = 15$ V	—	300	—	300	µA
		CLEAR = 0 V, SELECT = $V_{DD} = 5$ V	—	100	—	100	µA
	$I_{S(ON)}$	One Driver ON, $V_S = 5$ V	—	5.5	—	50	mA
		All Drivers ON, $V_S = 5$ V	—	45	—	160	mA
	$I_{S(OFF)}$	ENABLE = 0 V, $V_S = 5$ V	—	0.1	—	35	mA

Note: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure the minimum logic "I".

CAUTION: Sprague CMOS devices have input static protection but are still susceptible to damage when exposed to extremely high static electrical charges.

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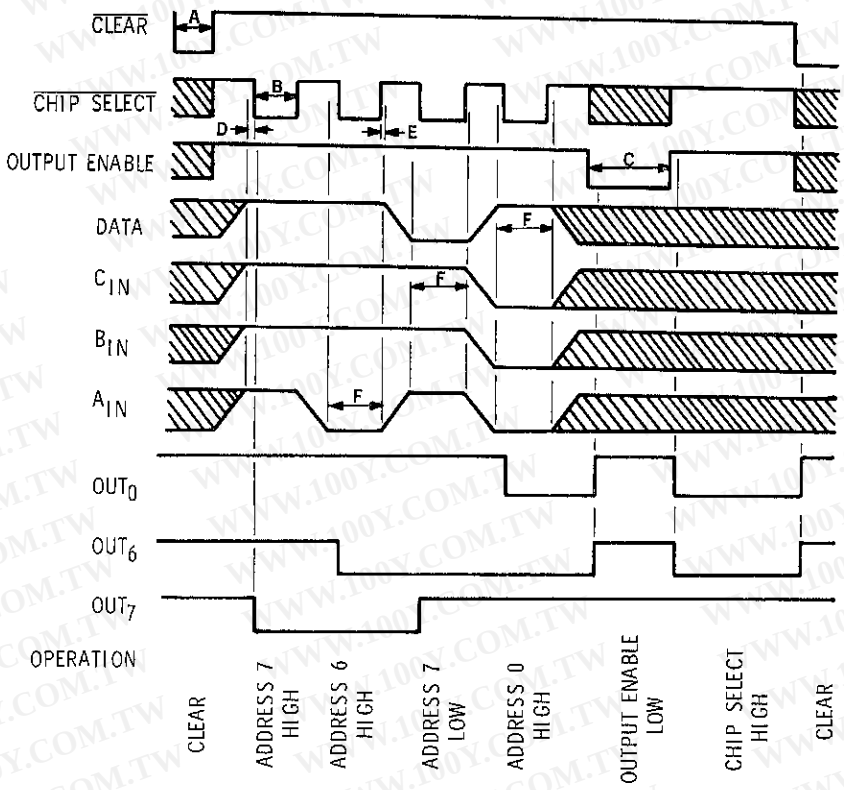
TRUTH TABLE

$\overline{\text{CHIP SELECT}}$	$\overline{\text{CLEAR}}$	DATA	C_{IN}	B_{IN}	A_{IN}	OUTPUT ENABLE	OUT_7	OUT_6	OUT_5	OUT_4	OUT_3	OUT_2	OUT_1	OUT_0	
X	L	X	X	X	X	X	H	H	H	H	H	H	H	H	Clear
H	H	X	X	X	X	H	R	R	R	R	R	R	R	R	Memory
L	H	D	L	L	L	H	R	R	R	R	R	R	$\overline{D}$	D	Address Latch 0
L	H	D	L	L	H	H	R	R	R	R	R	$\overline{D}$	D	R	Address Latch 1
L	H	D	L	H	L	H	R	R	R	R	$\overline{D}$	D	R	R	Address Latch 2
L	H	D	L	H	H	H	R	R	R	$\overline{D}$	D	R	R	R	Address Latch 3
L	H	D	H	L	L	H	R	R	$\overline{D}$	D	R	R	R	R	Address Latch 4
L	H	D	H	L	H	H	R	$\overline{D}$	D	R	R	R	R	R	Address Latch 5
L	H	D	H	H	L	H	$\overline{D}$	D	R	R	R	R	R	R	Address Latch 6
L	H	D	H	H	H	H	$\overline{D}$	R	R	R	R	R	R	R	Address Latch 7
X	X	X	X	X	X	L	H	H	H	H	H	H	H	H	Blanking
X	X	X	X	X	X	H	R	R	R	R	R	R	R	R	

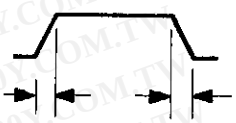
L = Low Logic Level
H = High Logic Level
D = Data (High or Low)
X = Irrelevant
R = Previous State

I/O WAVEFORMS



Dwg. No. A-11,785

Logic Level Irrelevant



Allowable Transition Time

TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

A.	Minimum $\overline{\text{CLEAR}}$ Pulse Width	300 ns
B.	Minimum $\overline{\text{CHIP SELECT}}$ Pulse Width	500 ns
C.	Typical OUTPUT ENABLE (Blanking) Pulse Width	5.0 µs
D.	Minimum DATA or ADDRESS Setup Time	100 ns
E.	Minimum DATA or ADDRESS Hold Time	100 ns
F.	Minimum DATA or ADDRESS Pulse Width	700 ns

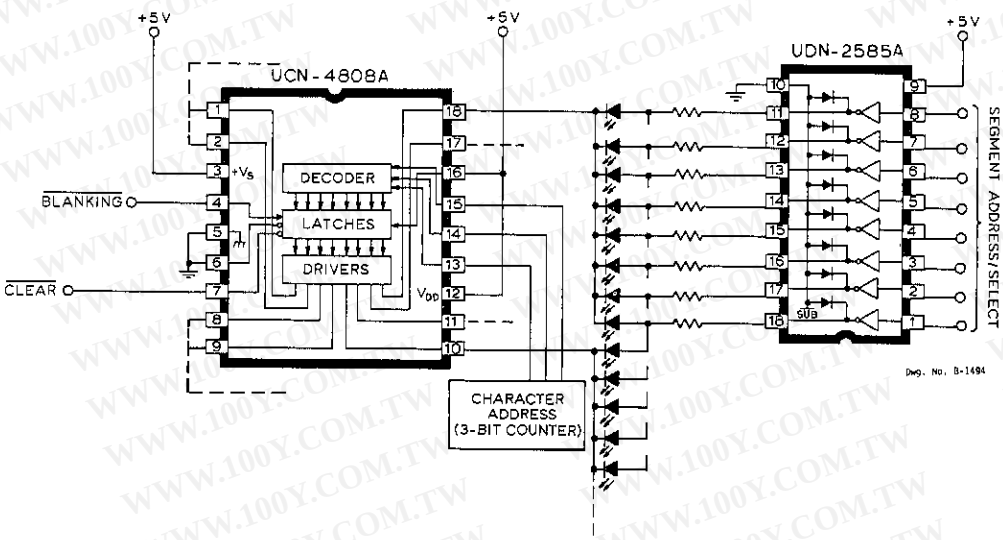
TYPICAL APPLICATIONS

A typical application for Type UCN-4808A, driving a common-cathode LED display, is shown below. Many multi-character LED displays can make use of the high-current capability of this device. With the DATA input held high, the proper address code may be furnished by a 3-bit counter. Note that with DATA held constant and the ADDRESS sequenced through the binary code, setup and hold times associated with CHIP SELECT may be ignored.

The second application illustrates the use of Type UCN-4807A or UCN-4808A as a multiplexed power driver. A wide variety of peripheral loads including lamps, relays, solenoids, LEDs, and stepper motors can be accommodated. Inductive loads require external transient suppression.

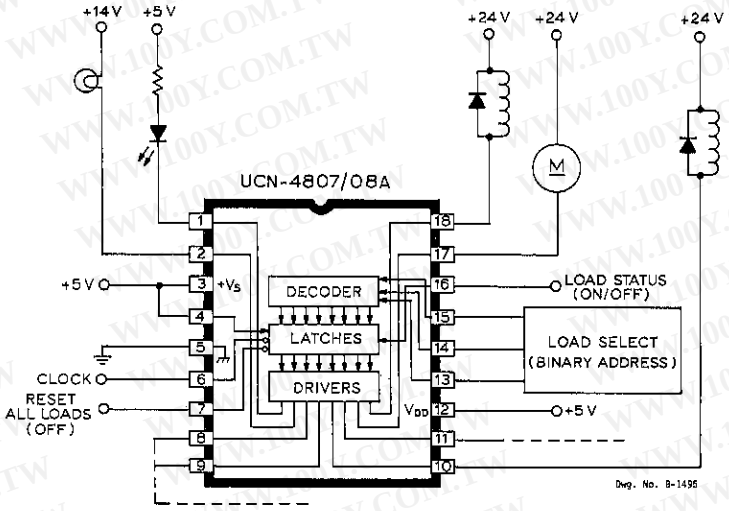
These devices can also be employed as multi-channel drivers for discrete high-current or high-voltage semiconductors.

Common-Cathode LED Display Driver

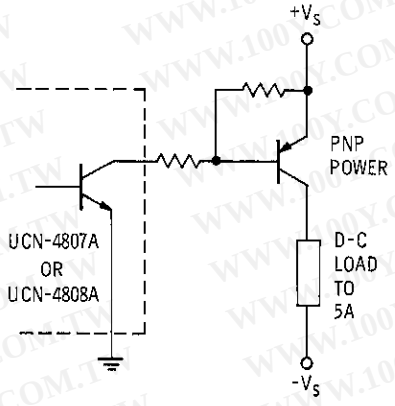


TYPICAL APPLICATIONS (Continued)

Multiplexed Power Driver



Multichannel Driver for Discrete Power Semiconductors



Dwg. No. A-11,786

UCN-5800A AND UCN-5801A
BiMOS II LATCHED DRIVERS

FEATURES

- 4.4 MHz Minimum Data Input Rate
- High-Voltage, High-Current Outputs
- Output Transient Protection
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches

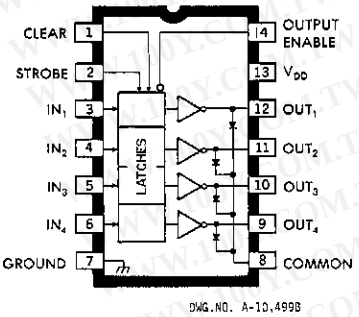
THE UCN-5800A and UCN-5801A latched drivers are high-voltage, high-current integrated circuits comprised of four or eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions.

The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility. Type UCN-5800A contains four latched drivers; Type UCN-5801A contains eight latched drivers.

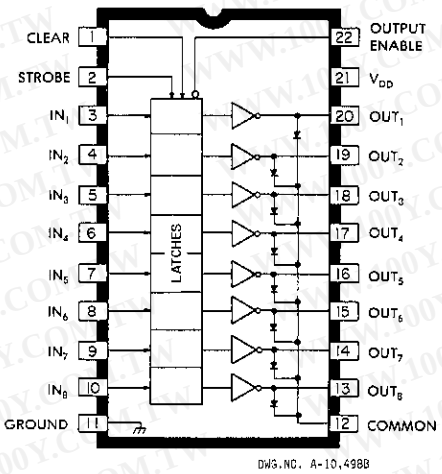
BiMOS II devices have much faster data input rates than the original BiMOS circuits. With a 5 V supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power loads.

Both units have open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 500 mA and will sustain at least 50 V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.



UCN-5800A

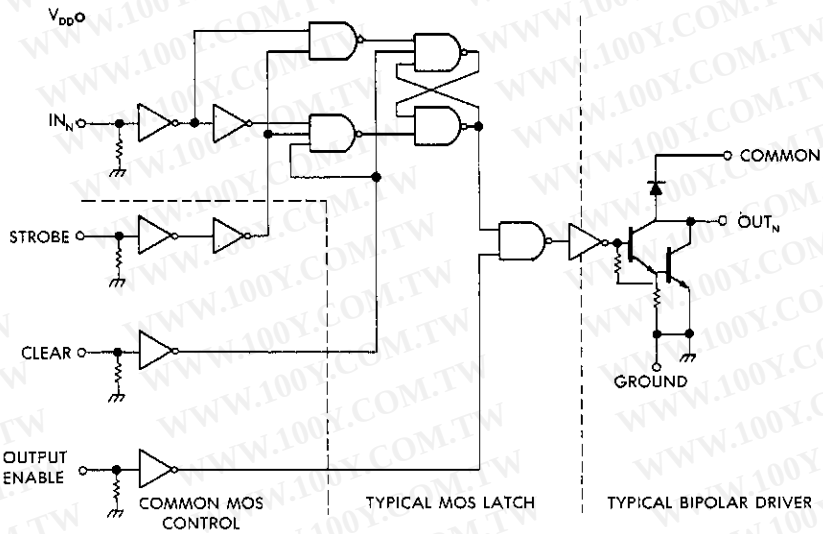


UCN-5801A

UCN-5800A, the 4-latch device, is furnished in a standard 14-pin dual in-line plastic package. UCN-5801A, the 8-latch device, is supplied in a 22-pin dual in-line plastic package with lead spacing on 0.400" (10.16 mm) centers. To simplify circuit board layout, all outputs are opposite their respective inputs.

5

FUNCTIONAL BLOCK DIAGRAM



DWG.NO. A-10,495A

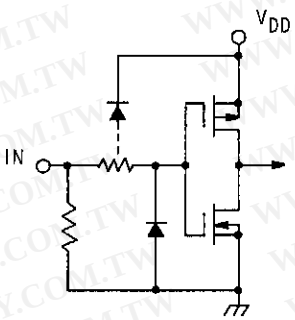
ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Output Voltage, V_{CE} . . . . . 50 V
Supply Voltage, V_{DD} . . . . . 15 V
Input Voltage Range, V_{IN} . . . . . −0.3 V to V_{DD} + 0.3 V
Continuous Collector Current, I_C . . . . . 500 mA
Package Power Dissipation, P_D
(UCN-5800A) . . . . . 1.6 W*
(UCN-5801A) . . . . . 2.0 W**
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +125°C

*Derate at the rate of 16.7 mW/°C above T_A = +25°C.
**Derate at the rate of 20 mW/°C above T_A = +25°C.

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

TYPICAL INPUT CIRCUIT



Dwg.No. A-12,520

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5\ V$ (unless otherwise noted)

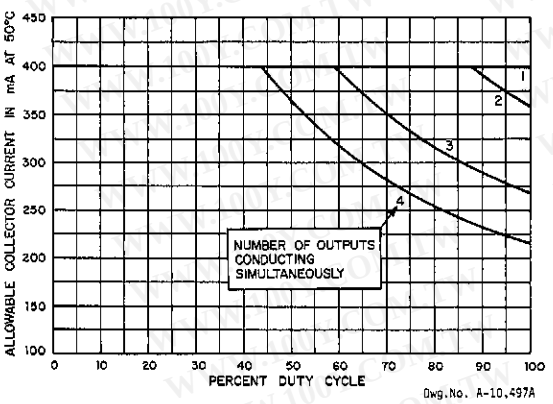
Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	$V_{CE} = 50\ V$, $T_A = +25°C$	—	—	50	µA
		$V_{CE} = 50\ V$, $T_A = +70°C$	—	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100\ mA$	—	0.9	1.1	V
		$I_C = 200\ mA$	—	1.1	1.3	V
		$I_C = 350\ mA$, $V_{DD} = 7.0\ V$	—	1.3	1.6	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	$V_{DD} = 12\ V$	10.5	—	—	V
		$V_{DD} = 10\ V$	8.5	—	—	V
		$V_{DD} = 5.0\ V$ (See Note)	3.5	—	—	V
Input Resistance	R_{IN}	$V_{DD} = 12\ V$	50	200	—	kΩ
		$V_{DD} = 10\ V$	50	300	—	kΩ
		$V_{DD} = 5.0\ V$	50	600	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	$V_{DD} = 12\ V$, Outputs Open	—	1.0	2.0	mA
		$V_{DD} = 10\ V$, Outputs Open	—	0.9	1.7	mA
		$V_{DD} = 5.0\ V$, Outputs Open	—	0.7	1.0	mA
	$I_{DD(OFF)}$ (Total)	$V_{DD} = 12\ V$, Outputs Open, Inputs = 0 V	—	—	200	µA
		$V_{DD} = 5.0\ V$, Outputs Open, Inputs = 0 V	—	50	100	µA
Clamp Diode Leakage Current	I_R	$V_R = 50\ V$, $T_A = +25°C$	—	—	50	µA
		$V_R = 50\ V$, $T_A = +70°C$	—	—	100	µA
Clamp Diode Forward Voltage	V_F	$I_F = 350\ mA$	—	1.7	2.0	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".

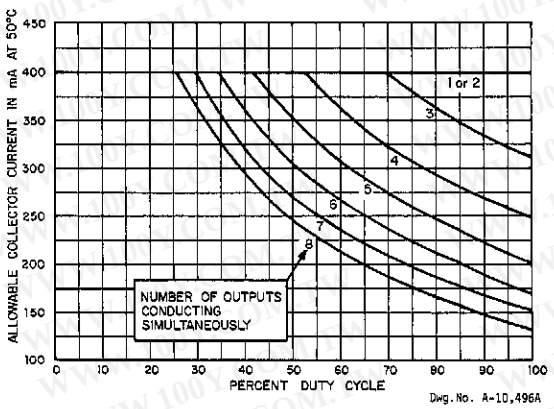
5

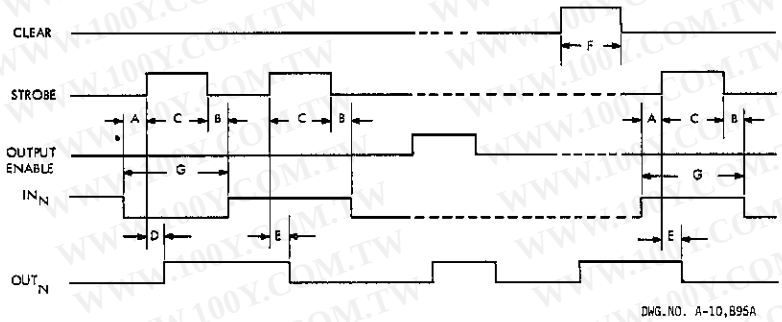
ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE

UCN-5800A



UCN-5801A





DWG.NO. A-10,895A

TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

A.	Minimum data active time before strobe enabled (data set-up time)	50 ns
B.	Minimum data active time after strobe disabled (data hold time)	50 ns
C.	Minimum strobe pulse width	125 ns
D.	Typical time between strobe activation and output on to off transition	500 ns
E.	Typical time between strobe activation and output off to on transition	500 ns
F.	Minimum clear pulse width	300 ns
G.	Minimum data pulse width	225 ns

TRUTH TABLE

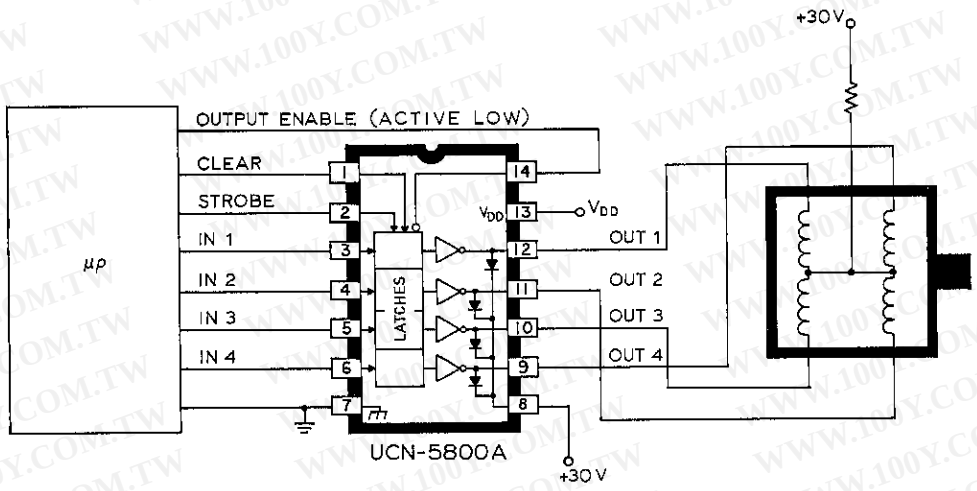
IN_N	STROBE	CLEAR	OUTPUT ENABLE	OUT_N t-1	OUT_N t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = irrelevant.
t-1 = previous output state.
t = present output state.

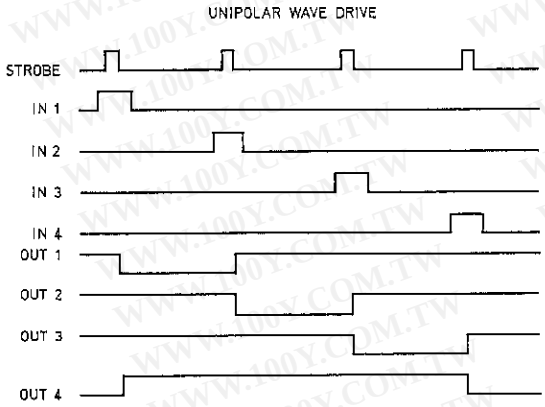
Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

TYPICAL APPLICATION

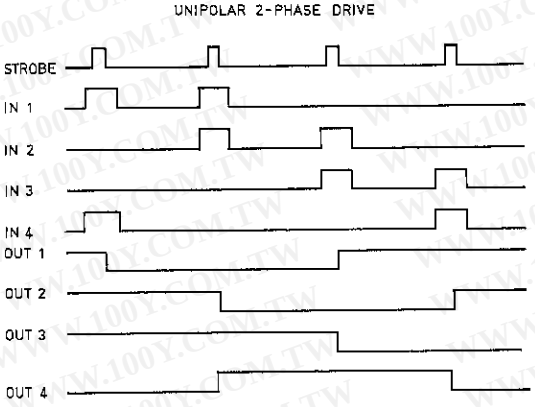
UNIPOLAR STEPPER-MOTOR DRIVE



Dwg. No. B-1537



DWG.NO. A-11,446



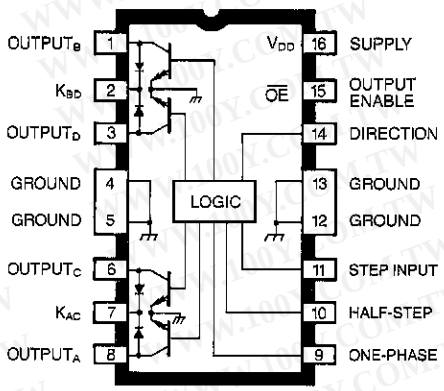
DWG.NO. A-11,447

5

UCN-5804B
BiMOS II TRANSLATOR/DRIVER

FEATURES

- 1.5 A Maximum Output Current
- 35 V Output Sustaining Voltage
- Wave-Drive, Two-Phase, and Half-Step Drive Formats
- Internal Clamp Diodes
- Output Enable and Direction Control
- Power-ON Reset
- Internal Thermal Shutdown Circuitry



Dwg. No. W-194

Combining low-power CMOS logic with high-current and high-voltage bipolar outputs, the UCN-5804B BiMOS II translator/driver provides complete control and drive for a four-phase unipolar stepper-motor with continuous output current ratings to 1.25 A per phase (1.5 A startup) and 35 V.

The CMOS logic section provides the sequencing logic, DIRECTION and OUTPUT ENABLE control, and a power-ON reset function. Three stepper-motor drive formats, wave-drive (one-phase), two-phase, and half-step are externally selectable. The inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or LSTTL may require the use of appropriate pull-up resistors to insure a proper input-logic high.

The wave-drive format consists of energizing one motor phase at a time in an A-B-C-D (or D-C-B-A) sequence. This excitation mode consumes the least power and assures positional accuracy regardless of any winding inbalance in the motor. Two-phase drive energizes two adjacent phases in each detent position (AB-BC-CD-DA). This sequence mode offers an improved torque-speed product, greater detent torque, and is less susceptible to motor resonance. Half-step excitation alternates between the one-phase and two-phase modes (A-AB-B-BC-C-CD-D-DA), providing an eight-step sequence.

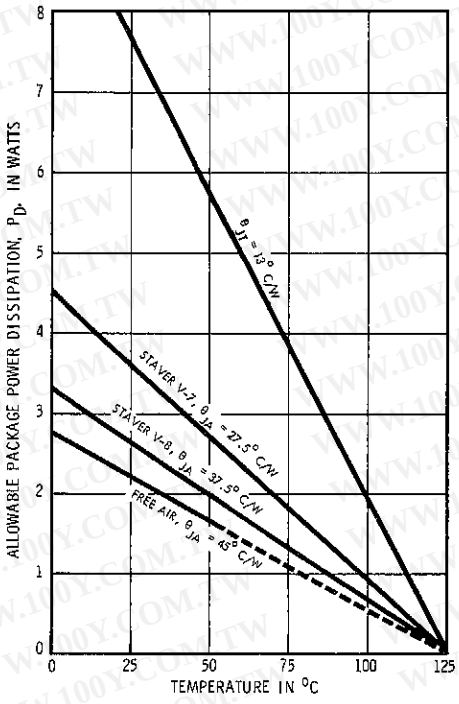
The bipolar outputs are capable of sinking up to 1.5 A and withstanding 50 V in the OFF state (sustaining voltages up to 35 V). Ground clamp and flyback diodes provide protection against inductive transients. Thermal protection circuitry disables the outputs when the chip temperature is excessive.

The UCN-5804B is rated for operation over the temperature range of −20°C to +85°C. It is supplied in a 16-pin dual in-line plastic batwing package with a copper lead frame and heat-sinkable tabs for improved power dissipation capabilities.

ABSOLUTE MAXIMUM RATINGS

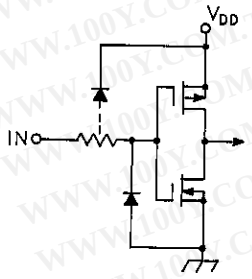
Output Voltage, V_{CE}	50 V
Output Sustaining Voltage, $V_{CE(sus)}$	35 V
Output Sink Current, I_{OUT}	1.5 A
Logic Supply Voltage, V_{DD}	7.0 V
Input Voltage, V_{IN}	7.0 V
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +125°C

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



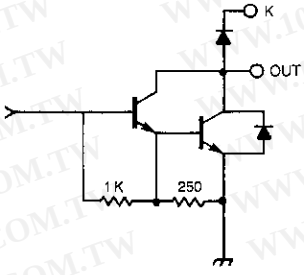
Dwg. No. W-195

TYPICAL INPUT CIRCUIT



Dwg. No. A-13,035

TYPICAL OUTPUT DRIVER



Dwg. No. D-196

5

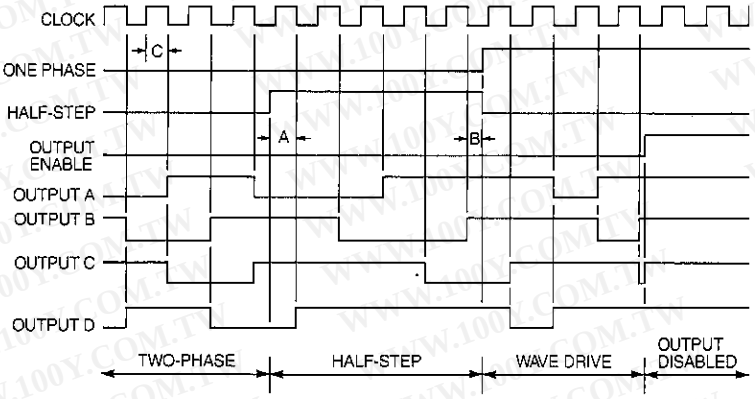
TRUTH TABLE

	PIN 9	PIN 10
TWO-PHASE	L	L
ONE-PHASE	H	L
HALF-STEP	L	H
STEP-INHIBIT	H	H

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $T_{TAB} \leq 70°C$, $V_{DD} = 4.5\ V$ to $5.5\ V$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	$V_{OUT} = 50\ V$	—	10	50	µA
Output Sustaining Voltage	$V_{CE(sus)}$	$I_{OUT} = 1.25\ A$, $L = 3\ mH$	35	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 700\ mA$	—	1.0	1.2	V
		$I_{OUT} = 1\ A$	—	1.1	1.4	V
		$I_{OUT} = 1.25\ A$	—	1.2	1.5	V
Clamp Diode Leakage Current	I_R	$V_R = 50\ V$	—	10	50	µA
Clamp Diode Forward Voltage	V_F	$I_F = 1.25\ A$	—	—	3.0	V
Input Current	$I_{IN(1)}$	$V_{IN} = V_{DD}$	—	0.5	5.0	µA
	$I_{IN(0)}$	$V_{IN} = 0.8\ V$	—	−0.5	−5.0	µA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5\ V$	3.5	—	5.3	V
	$V_{IN(0)}$		−0.3	—	0.8	V
Supply Current	I_{DD}	2 Outputs ON	—	20	30	mA
Turn-Off Delay	t_{ON}	50% Step Inputs to 50% Output	—	—	10	µs
Turn-On Delay	t_{OFF}	50% Step Inputs to 50% Output	—	—	10	µs
Thermal Shutdown Temperature	T_j		—	165	—	°C

TIMING CONDITIONS



Dwg. No. W-110A

A. Minimum data set up time..... 100 ns
B. Minimum data hold time ..... 100 ns
C. Minimum step input pulse width ..... 500 ns

APPLICATIONS INFORMATION

Internal power-ON reset (POR) circuitry resets $OUTPUT_A$ (and $OUTPUT_D$ in the two-phase drive format) to the ON state with initial application of the logic supply voltage. After reset, the circuit then steps according to the tables shown below.

The outputs will advance one sequence position on the high-to-low transition of the STEP INPUT pulse. Logic levels on the HALF-STEP and ONE-PHASE inputs will determine the drive format (one-phase, two-phase, or half-step). The DIRECTION pin determines the rotation sequence of the outputs. Note that the STEP INPUT must be in the low state when changing the state of ONE-PHASE, HALF-STEP, or DIRECTION to prevent erroneous stepping.

All outputs are disabled (OFF) when OUTPUT ENABLE is at a logic high. That input can be used for chopping applications without affecting the stepping logic. If the function is not required, OUTPUT ENABLE should be tied low. In that condition, all outputs depend only on the state of the step logic.

Internal thermal protection circuitry disables all outputs when the junction temperature reaches approximately 165°C. The outputs are enabled again when the junction cools down to approximately 145°C.

WAVE-DRIVE SEQUENCE

←DIRECTION = L	Half Step = L, One Phase = H				→DIRECTION = H
Step	A	B	C	D	
POR	ON	OFF	OFF	OFF	
1	ON	OFF	OFF	OFF	
2	OFF	ON	OFF	OFF	
3	OFF	OFF	ON	OFF	
4	OFF	OFF	OFF	ON	

TWO-PHASE DRIVE SEQUENCE

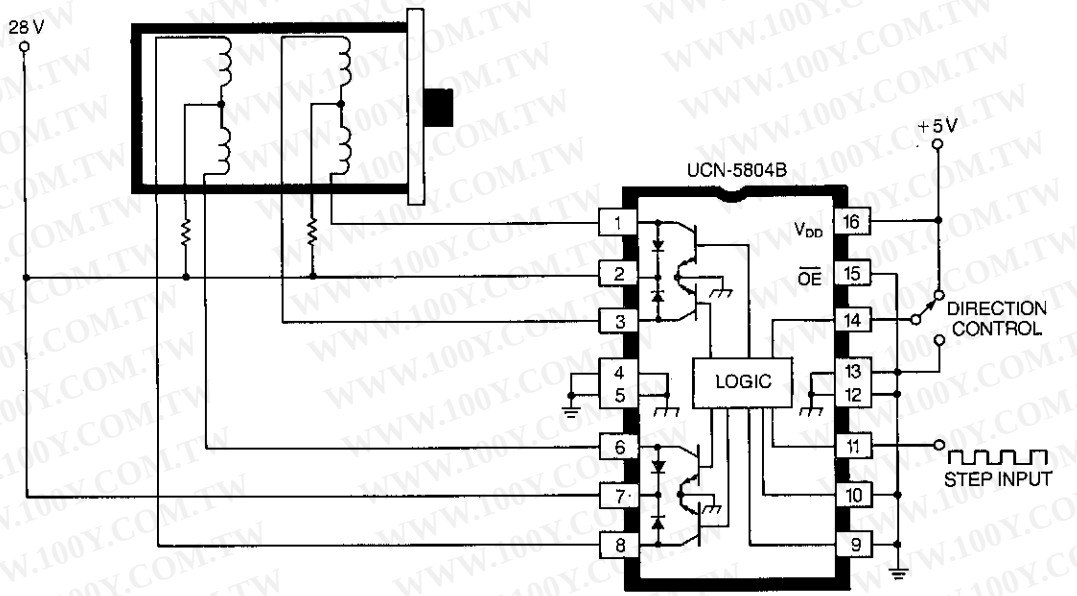
←DIRECTION = L	Half Step = L, One Phase = L				→DIRECTION = H
Step	A	B	C	D	
POR	ON	OFF	OFF	ON	
1	ON	OFF	OFF	ON	
2	ON	ON	OFF	OFF	
3	OFF	ON	ON	OFF	
4	OFF	OFF	ON	ON	

HALF-STEP DRIVE SEQUENCE

←DIRECTION = L	Half Step = H, One Phase = L				→DIRECTION = H
Step	A	B	C	D	
POR	ON	OFF	OFF	OFF	
1	ON	OFF	OFF	OFF	
2	ON	ON	OFF	OFF	
3	OFF	ON	OFF	OFF	
4	OFF	ON	ON	OFF	
5	OFF	OFF	ON	OFF	
6	OFF	OFF	ON	ON	
7	OFF	OFF	OFF	ON	
8	ON	OFF	OFF	ON	

TYPICAL APPLICATION

L/R STEPPER-MOTOR DRIVE



Dwg. No. D-197

UCN-5810A, UCN-5812A, AND UCN-5818A BiMOS II SERIAL-INPUT, LATCHED DRIVERS —10, 20, and 32 Bits

FEATURES

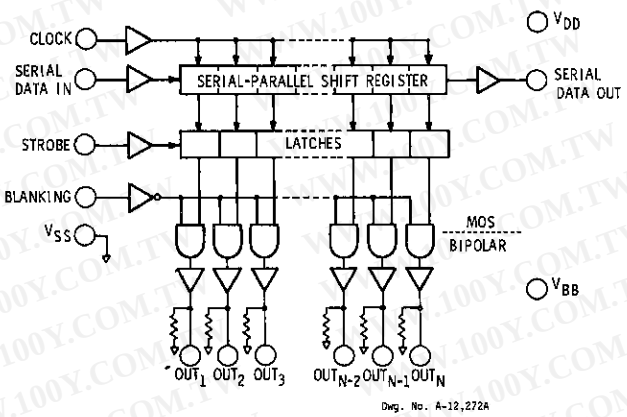
- 5 MHz Typical Data Input Rate
- Low-Power CMOS Logic and Latches
- 60 V or 80 V Source Outputs
- Internal Pull-Down Resistors

DESIGNED for use as segment or digit drivers in high-voltage, vacuum-fluorescent display applications, Type UCN-5810A, UCN-5812A, and UCN-5818A combine a CMOS register (10, 20, or 32 bits, respectively), associated latches, and control circuitry (strobe and blanking) with 60 V bipolar source outputs. The BiMOS drivers can also be used with non-multiplexed LED displays within their output limitation of 40 mA per driver.

Selected devices (suffix −1) have maximum ratings of 80 V and 40 mA per driver. In all other respects, the basic part and the part with the "−1" suffix are identical.

BiMOS II devices have much faster input data rates than the original BiMOS circuits. With a 5 V supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

The CMOS inputs cause minimal loading and are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors to insure a proper input-logic high. A CMOS serial-data output allows cascading these devices in multiple drive-line



FUNCTIONAL BLOCK DIAGRAM

applications required by many dot matrix, alphanumeric, and bar graph displays.

Type UCN-5810A, a 10-bit driver, is furnished in an 18-pin dual in-line plastic package. It is a high-speed, pin-compatible version of the UCN-4810A driver.

Type UCN-5812A, a 20-bit driver, is furnished in a 28-pin dual in-line plastic package with 0.600" (15.24 mm) row spacing. Type UCN-5818A, a 32-bit driver, is supplied in a 40-pin dual in-line plastic package with 0.600" row spacing.

All devices are rated for continuous operation over the temperature range of −20°C to +85°C. Because of limitations on package power dissipation, simultaneous operation of all drivers may require a reduction in duty cycle. The devices are also available with an extended operating temperature range (prefix UCQ-) and ceramic/glass cer-DIP hermetic packages (suffix R).

5

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature and V_{SS} = 0 V

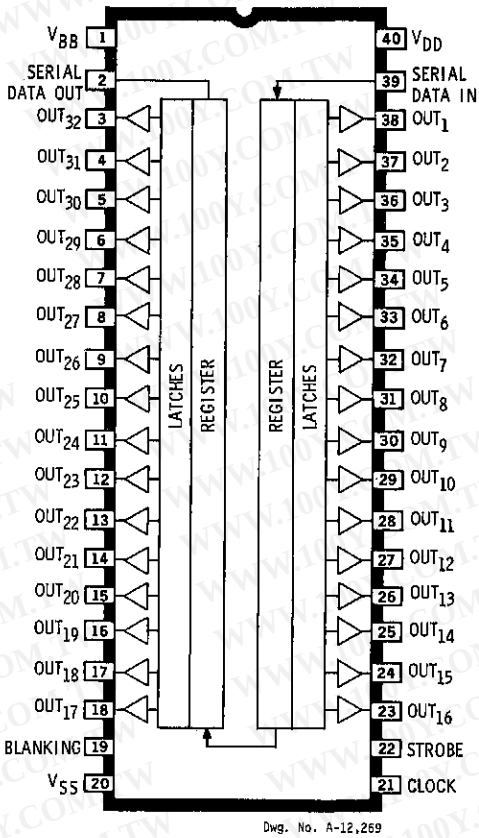
Output Voltage, V_{OUT} . . . . . 60 V
(Suffix −1) . . . . . 80 V
Logic Supply Voltage Range, V_{DD} . . . . . 4.5 V to 15 V
Driver Supply Voltage Range, V_{BB} . . . . . 5.0 V to 60 V
(Suffix −1) . . . . . 5.0 V to 80 V
Input Voltage Range, V_{IN} . . . . . −0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT} . . . . . −40 mA
Allowable Package Power Dissipation, P_D
(UCN-5810A) . . . . . 1.82 W*
(UCN-5812A) . . . . . 2.5 W*
(UCN-5818A) . . . . . 2.8 W*
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +125°C

*Derate linearly to 0 W at T_A = +125°C.

Part Number	Max. Allowable Duty Cycle With All Outputs ON (I_{OUT} = −25 mA) at T_A = +25°C	+40°C	+50°C	+60°C	+70°C
UCN-5810A	100%	97%	85%	73%	62%
UCN-5812A	100%	85%	75%	65%	55%
UCN-5818A	72%	61%	54%	43%	39%

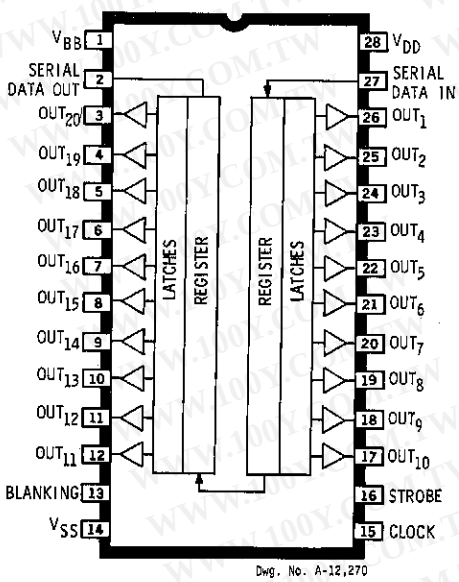
Caution: Sprague Electric CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

UCN-5818A



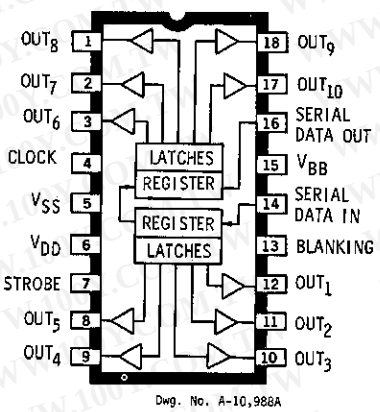
Dwg. No. A-12,269

UCN-5812A



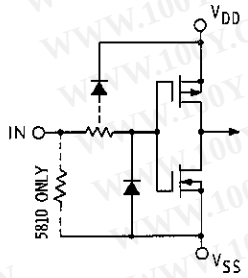
Dwg. No. A-12,270

UCN-5810A



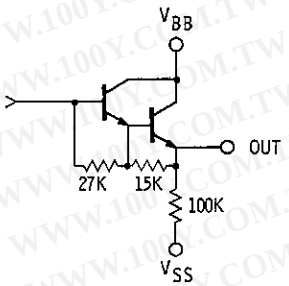
Dwg. No. A-10,988A

TYPICAL INPUT CIRCUIT



Dwg. No. A-12,304A

TYPICAL OUTPUT DRIVER

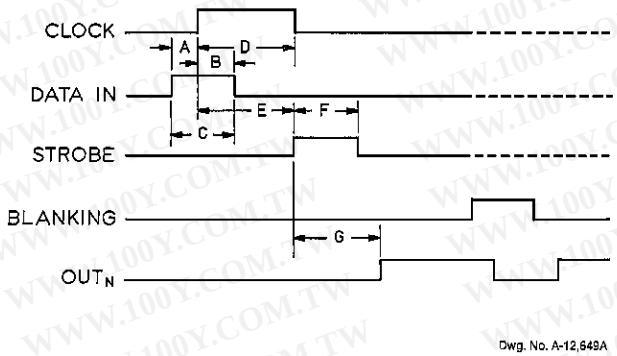


Dwg. No. A-10,981B

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{BB} = 60$ V, $V_{DD} = 5$ V to 12 V, $V_{SS} = 0$ V (unless otherwise noted)

Characteristic	Symbol	Applicable Devices*	Test Conditions	Limits Min.	Limits Max.	Units
Output OFF Voltage	V_{OUT}	All		—	1.0	V
Output ON Voltage	V_{OUT}	All	$I_{OUT} = -25$ mA, $V_{BB} = 60$ V	57.5	—	V
		Suffix −1	$I_{OUT} = -25$ mA, $V_{BB} = 80$ V	77.5	—	V
Output Pull-Down Current	I_{OUT}	All	$V_{OUT} = 60$ V	400	850	µA
		Suffix −1	$V_{OUT} = 80$ V $= V_{BB}$	550	1150	µA
Output Leakage Current	I_{OUT}	All	$T_A = +70°C$	—	−15	µA
Input Voltage	$V_{IN(1)}$	All	$V_{DD} = 5.0$ V	3.5	5.3	V
			$V_{DD} = 12$ V	10.5	12.3	V
	$V_{IN(0)}$	All	$V_{DD} = 5$ V to 12 V	−0.3	+0.8	V
Input Current	$I_{IN(1)}$	UCN-5810A	$V_{DD} = V_{IN} = 5.0$ V	—	100	µA
			$V_{DD} = V_{IN} = 12$ V	—	240	µA
		UCN-5812/18A	$V_{DD} = V_{IN} = 5.0$ V	—	0.5	µA
			$V_{DD} = V_{IN} = 12$ V		1.0	µA
	$I_{IN(0)}$	UCN-5812/18A	$V_{DD} = 12$ V, $V_{IN} = 0.8$ V	—	−1.0	µA
Input Impedance	Z_{IN}	UCN-5810A	$V_{DD} = 5.0$ V	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	All	$V_{DD} = 5.0$ V	—	20	kΩ
			$V_{DD} = 12$ V	—	6.0	kΩ
Supply Current	I_{BB}	UCN-5810A	All outputs ON, All outputs open	—	13	mA
		UCN-5812A	All outputs ON, All outputs open	—	22	mA
		UCN-5818A	All outputs ON, All outputs open	—	35	mA
		UCN-5810A	All outputs OFF, All outputs open	—	200	µA
		UCN-5812/18A	All outputs OFF, All outputs open	—	500	µA
	I_{DD}	All	$V_{DD} = 5.0$ V, All outputs OFF, Inputs = 0 V	—	100	µA
			$V_{DD} = 12$ V, All outputs OFF, Inputs = 0 V	—	200	µA
		UCN-5810A	$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	1.0	mA
			$V_{DD} = 12$ V, One output ON, All inputs = 0 V	—	3.0	mA
		UCN-5812/18A	$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	0.5	mA
			$V_{DD} = 12$ V, One output ON, All inputs = 0 V	—	1.2	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.
*"Suffix −1" indicates UCN-5810A-1, UCN-5812A-1 and UCN-5818A-1 only; "UCN-5810A," etc., indicates basic device and same part number with −1 suffix.



Dwg. No. A-12,649A

TIMING CONDITIONS

(Logic Levels are V_{DD} and V_{SS})

		V_{DD} = 5.0 V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C.	Minimum Data Pulse Width	150 ns
D.	Minimum Clock Pulse Width	150 ns
E.	Minimum Time Between Clock Activation and Strobe	300 ns
F.	Minimum Strobe Pulse Width	100 ns
G.	Typical Time Between Strobe Activation and Output Transition	500 ns

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the BLANKING input low, the outputs are controlled by the state of the latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents $I_1\ I_2\ I_3\ \ldots\ I_{N-1}\ I_N$	Serial Data Output	Strobe Input	Latch Contents $I_1\ I_2\ I_3\ \ldots\ I_{N-1}\ I_N$	Blanking Input	Output Contents $I_1\ I_2\ I_3\ \ldots\ I_{N-1}\ I_N$
H	↑	H $R_1\ R_2\ \ldots\ R_{N-2}\ R_{N-1}$	R_{N-1}				
L	↑	L $R_1\ R_2\ \ldots\ R_{N-2}\ R_{N-1}$	R_{N-1}				
X	↓	$R_1\ R_2\ R_3\ \ldots\ R_{N-1}\ R_N$	R_N				
		X X X ... X X	X	L	$R_1\ R_2\ R_3\ \ldots\ R_{N-1}\ R_N$		
		$P_1\ P_2\ P_3\ \ldots\ P_{N-1}\ P_N$	P_N	H	$P_1\ P_2\ P_3\ \ldots\ P_{N-1}\ P_N$	L	$P_1\ P_2\ P_3\ \ldots\ P_{N-1}\ P_N$
					X X X ... X X	H	L L L ... L L

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

UCN-5811A AND UCN-5811A-1
12-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS

FEATURES

- 3.3 MHz Guaranteed Data Input Rate
- Low-Power CMOS Logic and Latches
- High-Speed Source Drivers
- Active Pull-Downs
- Low-Output Saturation Voltages
- Improved Replacement for SN75512B

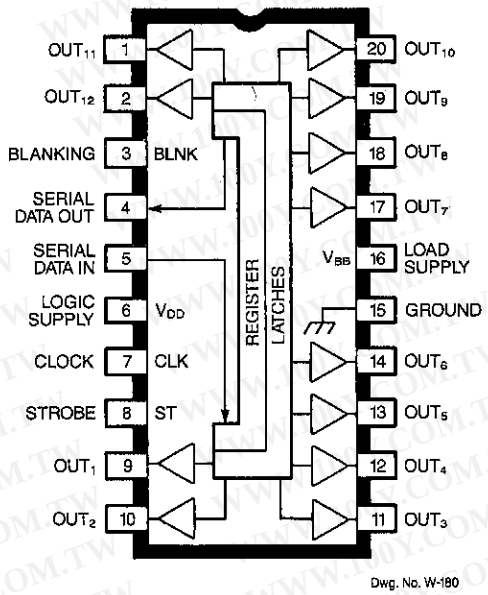
Designed primarily for use with vacuum-fluorescent displays, the UCN-5811A and UCN-5811A-1 Smart Power BiMOS II drivers feature low-output saturation voltages and high output switching speed. These devices contain CMOS shift registers, data latches, and control circuitry, and bipolar high-speed sourcing outputs with DMOS active pull-down circuitry. The high-speed shift register and data latches allow direct interface with microprocessor LSI-based systems. A CMOS serial data output enables cascade connections in applications requiring additional drive lines.

The UCN-5811A features 60 V and −40 mA output ratings, allowing it to be used in many other peripheral power driver applications. Selected devices (UCN-5811A-1) have maximum output ratings of 80 V. In all other respects, the UCN-5811A and UCN-5811A-1 are identical.

The UCN-5811A can be used as an improved replacement for the SN75512B. The Sprague devices do not require special power-up sequencing.

The UCN-5811A and UCN-5811A-1 have been designed with BiMOS II logic for improved data entry rates. With a 5 V supply, they will typically operate above 5 MHz. At 12 V, significantly higher speeds are obtained. Use of these devices with TTL may require the use of appropriate pull-up resistors to ensure an input logic high.

Both devices are supplied in 20-pin plastic dual in-line packages. They can be operated over the ambient temperature range of −20°C to +85°C. Copper lead frames and low output saturation voltages allow all outputs to be operated at 25 mA continuously at ambient temperatures of up to 62°C.

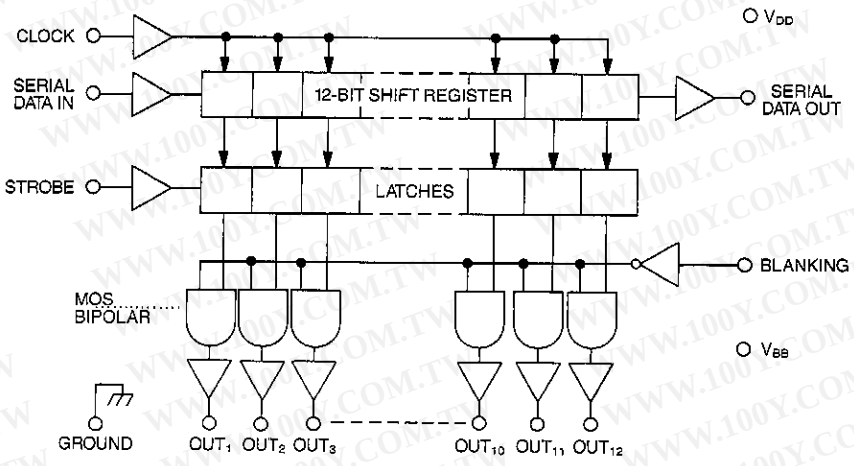


Dwg. No. W-180

ABSOLUTE MAXIMUM RATINGS
at T_A = 25°C

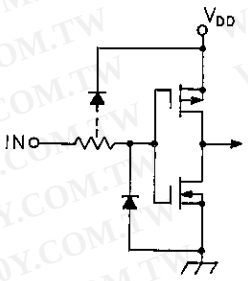
Logic Supply Voltage, V_{DD} ..... 15 V
Driver Supply Voltage, V_{BB} (UCN-5811A) ..... 60 V
(UCN-5811A-1) ..... 80 V
Continuous Output Current, I_{OUT} ..... −40 to +25 mA
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} +0.3 V
Package Power Dissipation, P_D ..... See Graph
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +125°C

FUNCTIONAL BLOCK DIAGRAM



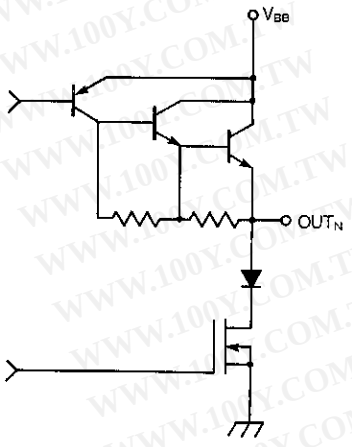
Dwg. No. W-181

TYPICAL INPUT CIRCUIT



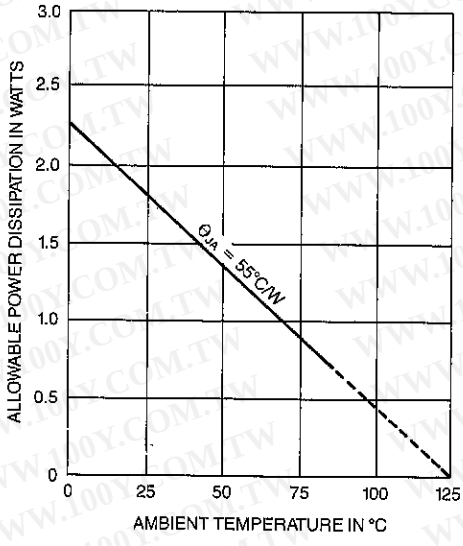
Dwg. No. A-13,035

TYPICAL OUTPUT DRIVER



Dwg. No. W-182

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



Dwg. No. W-183

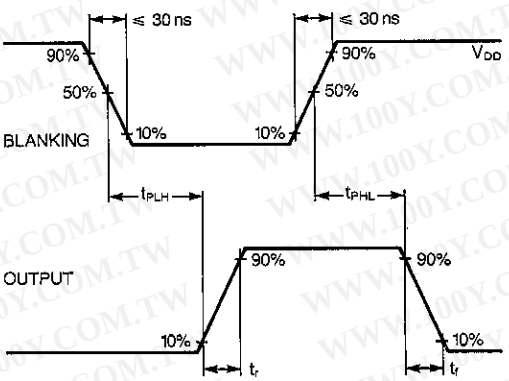
ELECTRICAL CHARACTERISTICS AT $T_A = +25°C$, $V_{BB} = 60$ V (UCN-5811A) or 80 V (UCN-5811A-1), unless otherwise noted.

Characteristic	Symbol	Test Conditions	Limits @ $V_{DD} = 5V$			Limits @ $V_{DD} = 12V$			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	$V_{OUT} = 0V, T_A = +70°C$	—	−5.0	−15	—	−5.0	−15	μA
Output Voltage	$V_{OUT(H)}$	$I_{OUT} = -25mA, V_{BB} = 60V$	58	58.5	—	58	58.5	—	V
		$I_{OUT} = -25mA, V_{BB} = 80V$*	78	78.5	—	78	78.5	—	V
	$V_{OUT(L)}$	$I_{OUT} = 1mA$	—	2.0	3.0	—	—	—	V
		$I_{OUT} = 2mA$	—	—	—	—	2.0	3.0	V
Output Pull-Down Current	$I_{OUT(L)}$	$V_{OUT} = 10V$ to V_{BB}	2.5	4.0	—	—	—	—	mA
		$V_{OUT} = 40V$ to V_{BB}	—	—	—	15	18	—	mA
Input Voltage	$V_{IN(1)}$		3.5	—	5.3	10.5	—	12.3	V
	$V_{IN(0)}$		−0.3	—	+0.8	−0.3	—	+0.8	V
Input Current	$I_{IN(1)}$	$V_{IN} = V_{DD}$	—	0.05	0.5	—	0.1	1.0	μA
	$I_{IN(0)}$	$V_{IN} = 0.8V$	—	−0.05	−0.5	—	−1.0	−1.0	μA
Serial Data Output Voltage	$V_{OUT(H)}$	$I_{OUT} = -200\mu A$	4.5	4.7	—	11.7	11.8	—	V
	$V_{OUT(L)}$	$I_{OUT} = 200\mu A$	—	200	250	—	100	200	mV
Maximum Clock Frequency	f_{clk}		3.3	5.0	—	—	7.5	—	MHz
Supply Current	$I_{DD(H)}$	All Outputs High	—	3.0	5.0	—	15	20	mA
	$I_{DD(L)}$	All Outputs Low	—	2.5	4.0	—	7.0	10	mA
	$I_{BB(H)}$	Outputs High, No Load	—	7.5	12	—	7.5	12	mA
	$I_{BB(L)}$	Outputs Low	—	10	100	—	10	100	μA
Blanking to Output Delay	t_{PHL}	$C_L = 30pF$	—	300	550	—	125	150	ns
	t_{PLH}	$C_L = 30pF$	—	250	450	—	170	200	ns
Output Fall Time	t_f	$C_L = 30pF$	—	1000	1250	—	250	300	ns
Output Rise Time	t_r	$C_L = 30pF$	—	150	170	—	150	170	ns

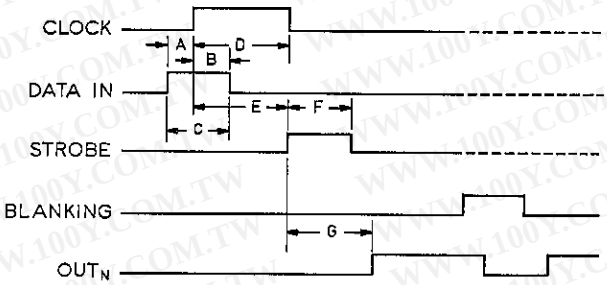
Negative current is defined as coming out of (sourcing) the specified device pin.
**UCN-5811A-1 only.*

5

TIMING WAVESHAPES



Dwg. No. W-184



Dwg. No. 12,649A

TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and Ground)

		V_{DD} = 5.0V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75ns
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	75ns
C.	Minimum Data Pulse Width	150ns
D.	Minimum Clock Pulse Width	150ns
E.	Minimum Time Between Clock Activation and Strobe	300ns
F.	Minimum Strobe Pulse Width	100ns
G.	Typical Time Between Strobe Activation and Output Transition	500ns

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information toward the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Blanking	Output Contents
		I_1 I_2 I_3 . . . I_{N-1} I_N			I_1 I_2 I_3 . . . I_{N-1} I_N		I_1 I_2 I_3 . . . I_{N-1} I_N
H	⎍	H R_1 R_2 . . . R_{N-2} R_{N-1}	R_{N-1}				
L	⎍	L R_1 R_2 . . . R_{N-2} R_{N-1}	R_{N-1}				
X	⎍	R_1 R_2 R_3 . . . R_{N-1} R_N	R_N				
		X X X . . . X X	X	L	R_1 R_2 R_3 . . . R_{N-1} R_N		
		P_1 P_2 P_3 . . . P_{N-1} P_N	P_N	H	P_1 P_2 P_3 . . . P_{N-1} P_N	L	P_1 P_2 P_3 . . . P_{N-1} P_N
					X X X . . . X X	H	L L L . . . L L

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

UCN-5813B AND UCN-5814B
BiMOS II 4-BIT LATCHED HIGH-CURRENT DRIVERS

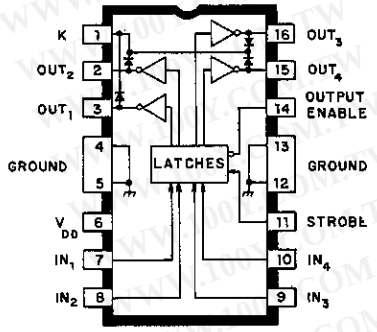
FEATURES

- 4.4 MHz Minimum Data Input Rate
- High-Voltage, High-Current Bipolar Outputs
- Output Loads to 480 Watts
- Transient-Protected Outputs
- Low-Power CMOS Logic and Latches
- Internal Input Pull-Down Resistors
- Plastic Dual In-Line Packages

Smart power integrated circuits, combining low-power CMOS latches with high-current bipolar Darlington power drivers, are available as the UCN-5813B and UCN-5814B. Each device consists of four CMOS latches, common STROBE and OUTPUT ENABLE functions, and four open-collector NPN bipolar drivers with output transient-suppression diodes. The UCN-5814B contains the additional functions of INPUT ENABLE and CLEAR for easier μP interface. The INPUT ENABLE can be used as a chip address/select function to control the drive lines to several packages in a simple multiplex scheme.

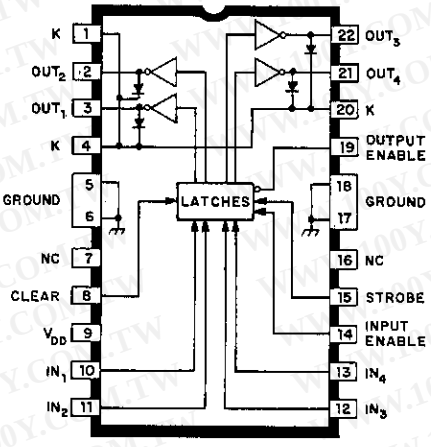
The CMOS inputs are compatible with CMOS, PMOS and NMOS logic families. TTL applications may require pull-up resistors to insure a proper logic "1" level. The bipolar outputs are rated at 50 V in the OFF state and can sustain 35 V and 1.0 A when driving inductive loads. Selected devices (-1 suffix) have maximum ratings of 80 V and 50 V sustaining. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. The outputs may be paralleled for higher load current capability.

BiMOS II devices have much improved data input rates. With a 5 V supply, they will typically operate at data input rates better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained.



UCN-5813B

DWG. NO. SG-101



UCN-5814B

DWG. NO. SG-102

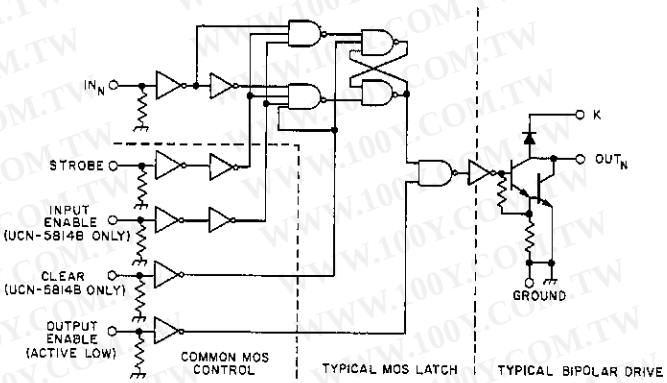
These devices are highly recommended for microprocessor-based application with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power loads. A similar 4-bit latched driver, for use with loads to 50 V (inductive loads to 35 V) and 350 mA, is the UCN-5800A. High-voltage devices, for operation to 150 V, are furnished as UCN-5900A.

Continued next page

5

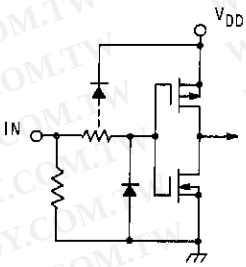
The UCN-5813B is furnished in a 16-pin dual in-line plastic package with 0.300" row centers while the UCN-5814B device is furnished in a 22-pin package with 0.400" row centers. Both packages feature a heat-sinkable tab for improved thermal characteristics. The lead configurations allow easy attachment of a heat sink while fitting standard integrated circuit sockets or printed wiring board layout.

FUNCTIONAL BLOCK DIAGRAM



DWG. NO. SG-103

TYPICAL INPUT CIRCUIT



DWG. NO. A-12,520

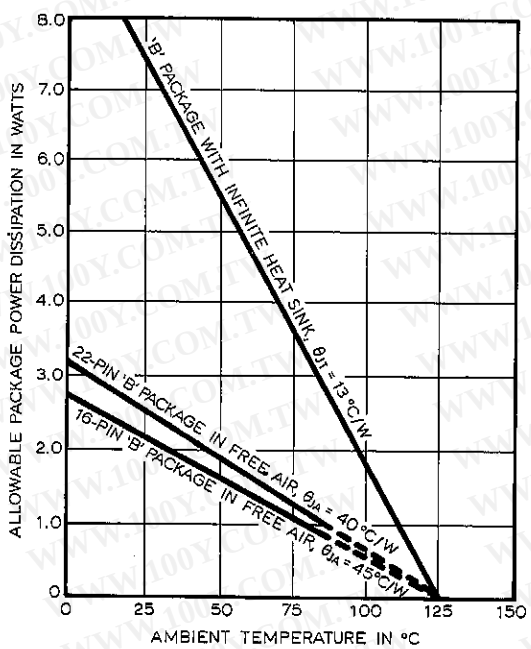
ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Output Voltage, V_{CE}
- UCN-5183B and UCN-5814B ..... 50 V
- UCN-5813B-1 and UCN-5814B-1 ..... 80 V

Output Sustaining Voltage, $V_{CE(sus)}$
- UCN-5813B and UCN-5814B ..... 35 V
- UCN-5813B-1 and UCN-5814B-1 ..... 50 V

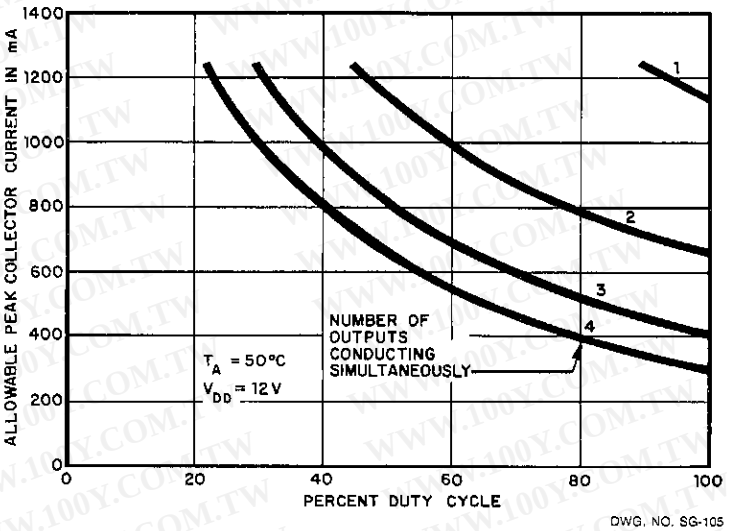
Output Current, I_{OUT} ..... 1.5 A
Logic Supply Voltage, V_{DD} ..... 15 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} +0.3 V
Package Power Dissipation, P_D ..... See Graph
Operating Temperature Range, T_A ... −20°C to +85°C
Storage Temperature Range, T_S ... −55°C to +125°C

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



DWG. NO. SG-104

ALLOWABLE PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE

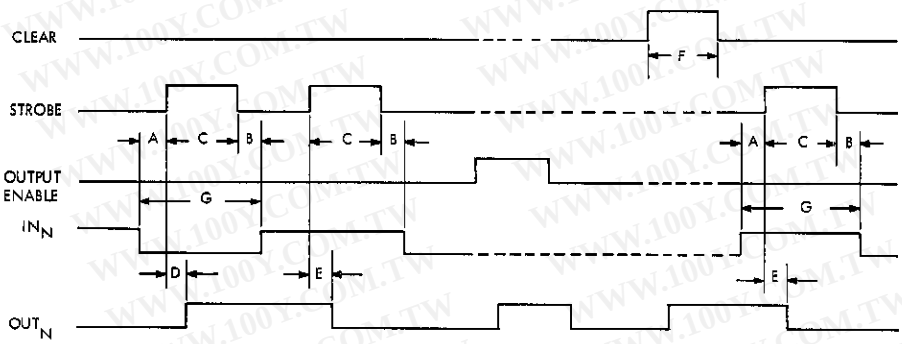


DWG. NO. SG-105

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $T_{TAB} = +70°C$, $V_{DD} = 5.0$ V (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Limits Units
Output Leakage Current	I_{CEX}	All	V_{OUT} = 50 V	—	100	μA
		Suffix -1	V_{OUT} = 80 V	—	100	μA
Output Sustaining Voltage	$V_{CE(sus)}$	All	I_{OUT} = 1.0 A, L = 2 mH	35	—	V
		Suffix -1	I_{OUT} = 1.0 A, L = 2 mH	50	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	All	I_{OUT} = 1.0 A	—	1.25	V
			I_{OUT} = 1.25 A	—	1.4	V
Clamp Diode Leakage Current	I_R	All	V_R = 50 V	—	100	μA
		Suffix -1	V_R = 80 V	—	100	μA
Clamp Diode Forward Voltage	V_F	All	I_F = 1.0 A	—	2.0	V
Input Voltage	$V_{IN(0)}$	All	V_{DD} = 5.0 V	−0.3	0.8	V
	$V_{IN(1)}$	All	V_{DD} = 5.0 V	3.5	5.3	V
			V_{DD} = 12 V	10.5	12.3	V
Input Resistance	R_{IN}	All	V_{DD} = 5.0 V, Except 5813B/13B-1 STROBE Input	100	—	kΩ
		5813B/13B-1	V_{DD} = 5.0 V, STROBE Input	50	—	kΩ
		All	V_{DD} = 12 V, Except 5813B/13B-1 STROBE Input	50	—	kΩ
		5813B/13B-1	V_{DD} = 12 V, STROBE Input	25	—	kΩ
Supply Current	$I_{DD(OFF)}$	All	V_{DD} = 5.0 V, All Outputs OFF, All Inputs = 0 V	—	100	μA
			V_{DD} = 12 V, All Outputs OFF, All Inputs = 0 V	—	200	μA
	$I_{DD(ON)}$	All	V_{DD} = 5.0 V, One Output ON, All Inputs = 0 V	—	5.0	mA
			V_{DD} = 12 V, One Output ON, All Inputs = 0 V	—	10	mA

5



DWG. NO. A-10,895A

TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

A. Minimum data active time before strobe enabled (data set-up time) ..... 50 ns
B. Minimum data active time after strobe disabled (data hold time) ..... 50 ns
C. Minimum strobe pulse width ..... 125 ns
D. Typical time between strobe activation and output on to off transition ..... 500 ns
E. Typical time between strobe activation and output off to on transition ..... 500 ns
F. Minimum clear pulse width (UCN-5814B only) ..... 300 ns
G. Minimum data pulse width ..... 225 ns

TRUTH TABLE

DATA IN	INPUT ENABLE	STROBE	CLEAR	OUTPUT ENABLE	LATCH CONTENTS	OUTPUT
UCN-5813B						
X	—	X	—	1	X	OFF
X	—	0	—	0	n-1	n-1
0	—	1	—	0	0	OFF
1	—	1	—	0	1	ON
UCN-5814B						
X	X	X	X	1	X	OFF
X	X	X	1	X	0	OFF
X	X	0	0	0	n-1	n-1
X	0	X	0	0	n-1	n-1
0	1	1	0	0	0	OFF
1	1	1	0	0	1	ON

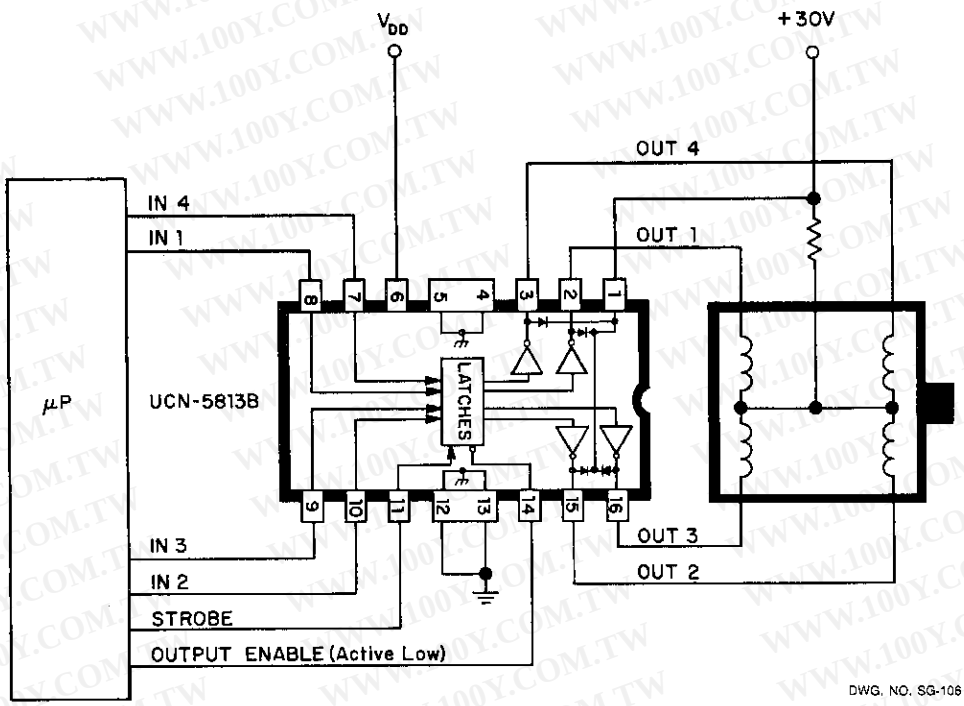
X = irrelevant
n-1 = previous output state

Information present at an input is transferred to its latch when the STROBE is high. A high OUTPUT ENABLE will force all outputs to the OFF condition, but does not affect the state of the latches. When OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

For the UCN-5814B, data is entered only when both STROBE and INPUT ENABLE are high. A high CLEAR input will set all latches to the output OFF condition, regardless of input data, INPUT ENABLE, or STROBE conditions.

TYPICAL APPLICATION

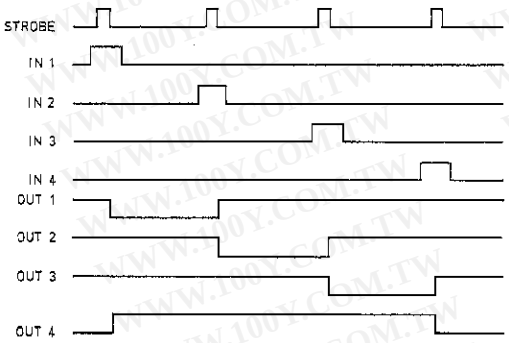
UNIPOLAR STEPPER-MOTOR DRIVE



DWG. NO. SG-106

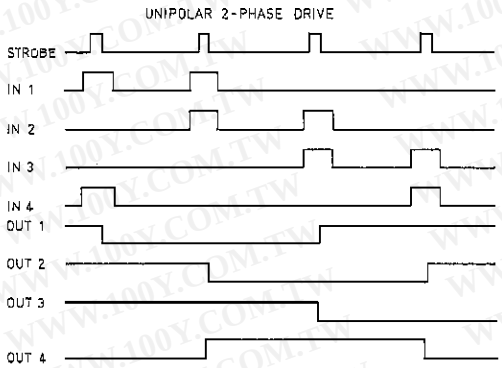
5

UNIPOLAR WAVE DRIVE



DWG. NO. A-11,446

UNIPOLAR 2-PHASE DRIVE

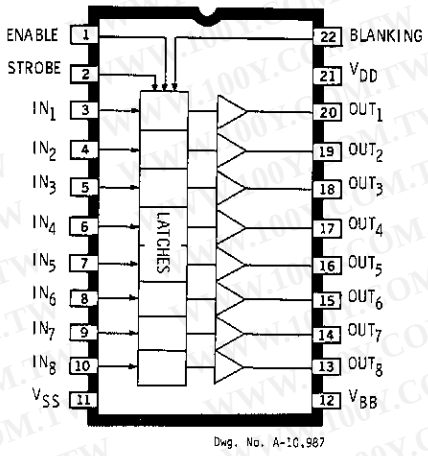


DWG. NO. A-11,447

UCN-5815A
BiMOS II 8-BIT LATCHED SOURCE DRIVER

FEATURES

- 4.4 MHz Minimum Date-Input Rate
- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Latches
- Internal Pull-Down Resistors
- Wide Supply-Voltage Range



Dwg. No. A-10,987

DESIGNED primarily for use with high-voltage vacuum-fluorescent displays, the UCN-5815A BiMOSII integrated circuit consists of eight NPN Darlington source drivers with pull-down resistors, a CMOS latch for each driver, and common STROBE, BLANKING, and ENABLE functions.

Selected devices (UCN-5815A-1) have maximum output ratings of 80 V and 40 mA per driver. In all other respects, the UCN-5815A-1 is identical to the 60 V UCN-5815A.

BiMOS II devices have considerably better data input rates than the original BiMOS circuits. With a 5 V supply, they typically operate above 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

The CMOS inputs cause minimal loading and are compatible with standard CMOS, PMOS, and NMOS logic commonly found in microprocessor designs. The use of CMOS latches also allows operation over a supply voltage range of 5 V to 12 V. When employed with either standard TTL or low-speed TTL logic, the UCN-5815A may require the use of appropriate pull-up resistors.

The bipolar outputs may be used as segment, dot (matrix), bar, or digit drivers in vacuum-fluorescent displays. All eight outputs can be activated simultaneously at ambient temperatures up to 60°C. To simplify circuit board layout, output pins are opposite input pins.

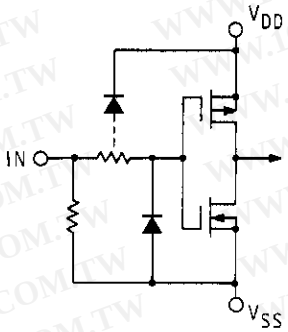
A minimum component display subsystem, requiring few or no discrete components, can be assembled using the UCN-5815A with the UCN-5810A, UCN-5812A or UCN-5818A serial-to-parallel latched driver.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature and V_{SS} = 0 V

Output Voltage, V_{OUT} (UCN-5815A) . . . . . 60 V
(UCN-5815A-1) . . . . . 80 V
Logic Supply Voltage Range, V_{DD} . . . . . 4.5 V to 15 V
Driver Supply Voltage Range, V_{BB}
(UCN-5815A) . . . . . 5.0 V to 60 V
(UCN-5815A-1) . . . . . 5.0 V to 80 V
Input Voltage Range, V_{IN} . . . . . −0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT} . . . . . −40 mA
Package Power Dissipation, P_D . . . . . 2.0 W*
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +125°C

*Derate at the rate of 20 mW/°C above T_A = +25°C.

TYPICAL INPUT CIRCUIT



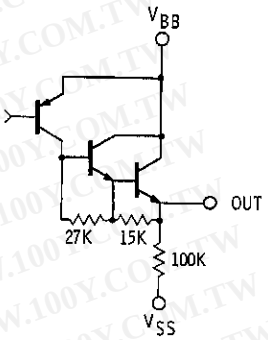
Dwg. No. A-12,517

MAXIMUM DUTY CYCLE

Number of Outputs ON (I_{OUT} = −25 mA)	Max. Allowable Duty Cycle at Ambient Temperature of +50°C	+60°C	+70°C
8	100%	100%	86%
7	100%	100%	98%
6	100%	100%	100%
1	100%	100%	100%

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

TYPICAL OUTPUT DRIVER



Dwg. No. A-12,546

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 60 V, V_{DD} = 4.5 V to 12 V, V_{SS} = 0 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage	V_{OUT}	I_{OUT} = −25 mA, V_{BB} = 60 V	57.5	—	V
		I_{OUT} = −25 mA, V_{BB} = 80 V, UCN-5815A-1 only	77.5	—	V
Output Pull-Down Current	I_{OUT}	V_{OUT} = V_{BB}	400	850	µA
		V_{BB} = V_{OUT} = 80 V, UCN-5815A-1 only	550	1150	µA
Output Leakage Current	I_{OUT}	T_A = 70°C	—	−15	µA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	5.3	V
		V_{DD} = 12 V	10.5	12.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = V_{IN} = 5.0 V	—	100	µA
		V_{DD} = V_{IN} = 12 V	—	240	µA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	50	—	kΩ
Supply Current	I_{BB}	All outputs ON, All outputs open	—	10.5	mA
		All outputs OFF, All outputs open	—	100	µA
	I_{DD}	V_{DD} = 5.0 V, All outputs OFF, All inputs = 0 V	—	100	µA
		V_{DD} = 12 V, All outputs OFF, All inputs = 0 V	—	200	µA
		V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 12 V, One output ON, All inputs = 0 V	—	3.0	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

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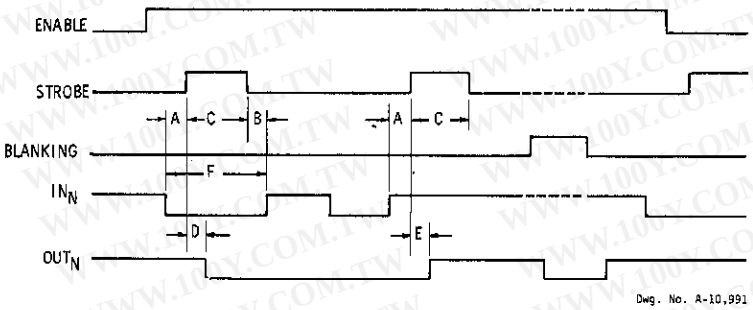


TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS})

		V_{DD} = 5.0 V
A.	Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time)	50 ns
B.	Minimum Data Active Time After Strobe Disabled (Data Hold Time)	50 ns
C.	Minimum Strobe Pulse Width	125 ns
D.	Typical Time Between Strobe Activation and Output ON to OFF Transition	5.0 µs
E.	Typical Time Between Strobe Activation and Output OFF to ON Transition	500 ns
F.	Minimum Data Pulse Width	225 ns

Information present at an input is transferred to its latch when the STROBE and ENABLE are high. The latches will continue to accept new data as long as both STROBE and ENABLE are held high. With either STROBE or ENABLE in the low state, no information can be loaded into the latches.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches. With the BLANKING input low, the outputs are controlled by the state of the latches.

The timing conditions shown above guarantee a 4.4 MHz, minimum data input rate with a 5 V supply. Typically, input rates above 5 MHz are permitted. With a 12 V supply, rates in excess of 10 MHz are possible.

UCN-5815A TRUTH TABLE

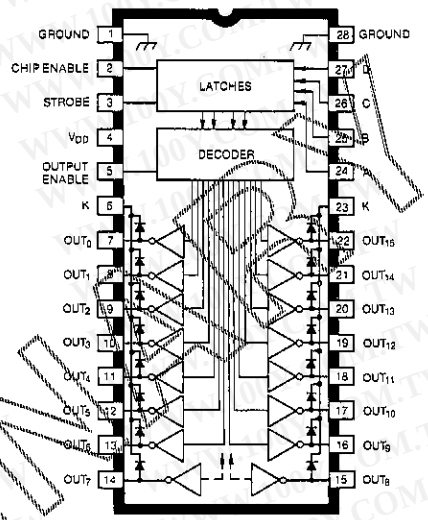
Inputs				OUT_N	
IN_N	STROBE	ENABLE	BLANK	T-1	T
0	1	1	0	X	0
1	1	1	0	X	1
X	X	X	1	X	0
X	0	X	0	1	1
X	0	X	0	0	0
X	X	0	0	1	1
X	X	0	0	0	0

X = irrelevant
T-1 = previous output state
T = present output state

UCN-5816A
DECODER/LATCH/SINK DRIVER

FEATURES

- Addressable Data Entry
- 60 V Output Voltage
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Logic and Latches
- Output Transient Protection
- STROBE, CHIP ENABLE, OUTPUT ENABLE* Functions



Dwg. No. A-14,320

This sixteen-bit, addressable, latched driver is used in a wide variety of power applications. The UCN-5816A can drive all types of common peripheral power loads, including lamps, relays, solenoids, LED's, printer heads, heaters, and stepper motors. It can also be used as a decoder driver for higher power loads requiring discrete power semiconductors.

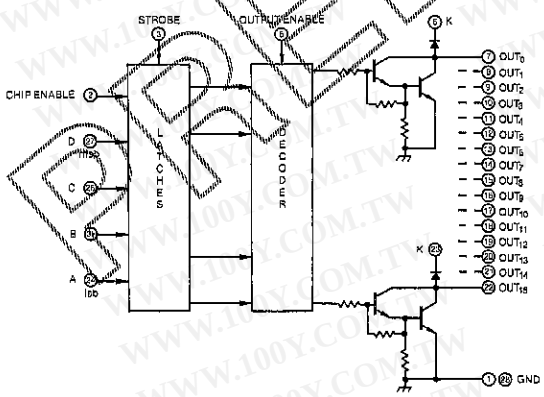
The UCN-5816A is capable of maintaining an output OFF voltage of 60 V and an output ON current of 500 mA.

The logic for this device is all new and is divided into sixteen latches, quadrant select, four 2-line to 4-line decoders, sixteen open-collector output drivers, and MOS control circuitry for CHIP ENABLE, OUTPUT ENABLE*, and STROBE functions. Any of the sixteen power loads can be addressed individually and can be turned ON or OFF independent of the other loads.

This device is supplied in a 28-pin dual in-line plastic package for operation over the temperature range of −20°C to +85°C.

*Output Enable—Active Low

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-14,319

ABSOLUTE MAXIMUM RATINGS
at T_A = 25°C

Output Voltage, V_{CE} . . . . . 60 V
Logic Supply Voltage, V_{DD} . . . . . 15 V
Input Voltage, V_{IN} . . . . . −0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT} . . . . . 500 mA
Package Power Dissipation, P_D . . . . . 2.5 W*
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +125°C

*Derate at the rate of 25 mW/°C above T_A = 25°C.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V_{DD} = 5\,V$, $V_{SS} = 0\,V$ (unless otherwise specified)

Characteristic	Symbol	Applicable Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{CE} = 60\,V$, $T_A = +25°C$	—	—	50	µA
		$V_{CE} = 60\,V$, $T_A = +70°C$	—	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100$ ma	—	0.9	1.1	V
		$I_C = 200$ mA	—	1.1	1.3	V
		$I_C = 350$ mA, $V_{DD} = 7.0\,V$	—	1.3	1.6	V
Input Voltage	$V_{IN(0)}$		−0.3	—	0.8	V
	$V_{IN(1)}$	$V_{DD} = 12\,V$	10.5	—	—	V
		$V_{DD} = 5.0\,V$ (See note)	3.5	—	5.3	V
Input Resistance	R_{IN}	$V_{DD} = 12\,V$	50	200	—	kΩ
		$V_{DD} = 5.0\,V$	100	600	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	$V_{DD} = 12\,V$, Outputs Open	—	2.0	3.0	mA
		$V_{DD} = 5.0\,V$, Outputs Open	—	1.0	1.5	mA
	$I_{DD(OFF)}$	All Drivers OFF, All Inputs = 0 V, $\overline{OE} = V_{DD} = 5\,V$	—	—	100	µA
		All Drivers OFF, All Inputs = 0 V, $\overline{OE} = V_{DD} = 12\,V$	—	—	200	µA
Clamp Diode Leakage Current	I_R	$V_R = 60\,V$, $T_A = +25°C$	—	—	50	µA
		$V_R = 60\,V$, $T_A = +70°C$	—	—	100	µA
Clamp Diode Forward Voltage	V_F	$I_F = 350$ mA	—	1.5	2.0	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure the minimum logic "1".
For Timing Conditions, see UCN-5800/01A.

TRUTH TABLE

	INPUTS																		
STR	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	X	1
$\overline{OE}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X
CE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	X	0
D	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	X	X	X
C	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	X	X	X
B	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	X	X	X
A	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	X	X	X

OUTPUTS (all outputs OFF unless otherwise specified)

0	ON																	
1		ON																
2			ON															
3				ON														
4					ON													
5						ON												
6							ON										↑	↑
7								ON									Q_o	ALL
8									ON									OFF
9										ON							↓	↓
10											ON							
11												ON						
12													ON					
13														ON				
14															ON			
15																ON		

NOTE: Q_o = The Output Conditions before the 1 to 0 transition of the STROBE pin.
1 = High Logic Level 0 = Low Logic Level X = Irrelevant

UCN-5818AF AND UCN-5818EPF BiMOS II 32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS

With Active DMOS Pulldowns

FEATURES

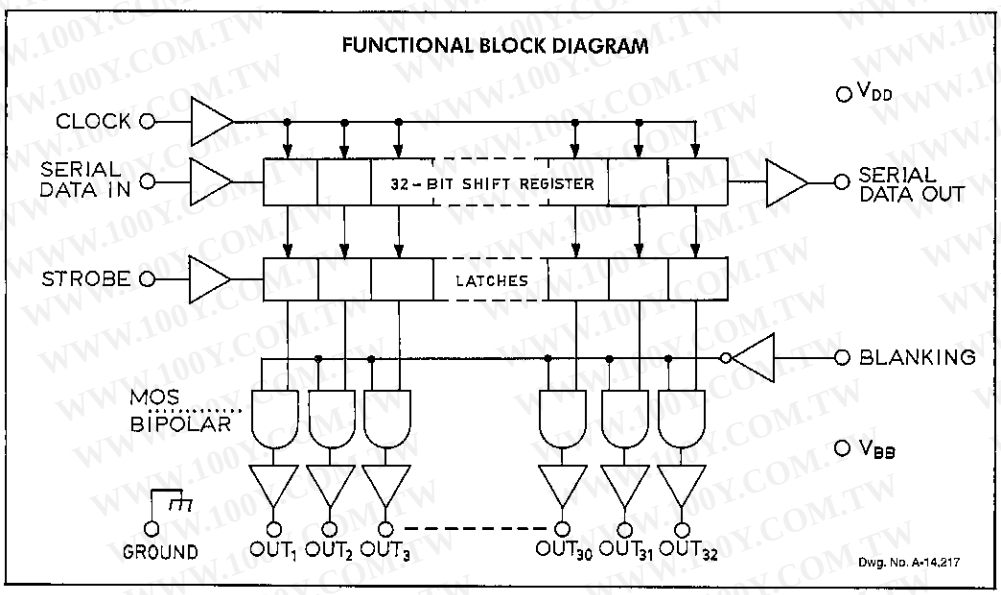
- 60 V or 80 V Source Outputs
- High-Speed Source Drivers
- Active DMOS Pull-Downs
- Low-Output Saturation Voltages
- Low-Power CMOS Logic and Latches
- 3.3 MHz Minimum Data Input Rate
- Reduced Supply Current Requirements
- Improved Replacements for SN75518N/FN

DESIGNED primarily for use with vacuum-fluorescent displays, the UCN-5818AF and UCN-5818EPF smart power BiMOS II drivers combine CMOS shift registers, data latches, and control circuitry, with bipolar high-speed sourcing outputs and DMOS active pull-down circuitry. The high-speed shift register and data latches allow direct interface with microprocessor LSI-based systems. A CMOS serial data output enables cascade connections in applications requiring additional drive lines. Both devices feature 60 V and −40 mA output ratings, allowing them to be used in many other peripheral power driver applications. Selected devices suffix "-1") have maximum output ratings of 80 V. In all other respects, devices with and without the "-1" suffix are identical.

These smart power drivers have been designed with BiMOS II logic for improved data entry rates. With a 5 V supply, they will typically operate above 5 MHz. At 12 V, significantly higher speeds are obtained. Use of these devices with TTL may require the use of appropriate pull-up resistors to ensure an input logic high. All devices can be operated over the ambient temperature range of −20°C to +85°C.

Continued

FUNCTIONAL BLOCK DIAGRAM



The UCN-5818AF is supplied in a 40-pin plastic dual in-line package with 0.600" (15.24 mm) row spacing. A copper lead frame, reduced supply current requirements, and low output saturation voltage permits operation with minimum junction temperature rise. The "A" package allows all 32 outputs to be operated at −25 mA continuously at ambient temperature up to 60°C.

For high-density packaging applications, the UCN-5818EPF is furnished in a 44-lead plastic chip carrier (quad pack) for surface moutning on solder lands with 0.050" (1.27 mm) centers. The PLCC allows −25 mA continuous operation of up to 21 outputs simultaneously at ambient temperatures to 60°C.

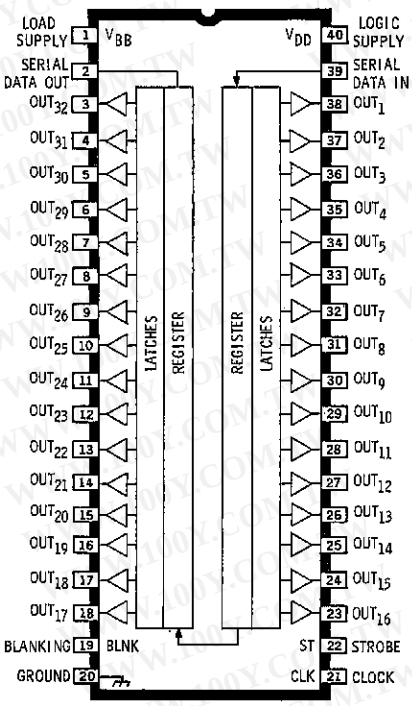
ABSOLUTE MAXIMUM RATINGS at T_A = 20l°C

Logic Supply Voltage, V_{DD} ..... 15 V
Driver Supply Voltage, V_{BB} ..... 60 V
(Suffix "-1") ..... 80 V
Continuous Output Current, I_{OUT} ..... −40 to +15 mA
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} +0.3 V
Package Power Dissipation, P_D (UCN-5818AF) ..... 2.8 W*
(UCN-5818EPF) ..... 2.0 W†
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +125°C

*Derate at rate of 28 mW/°C above T_A = +25°C
†Derate at rate of 20 mW/°C above T_A = +25°C

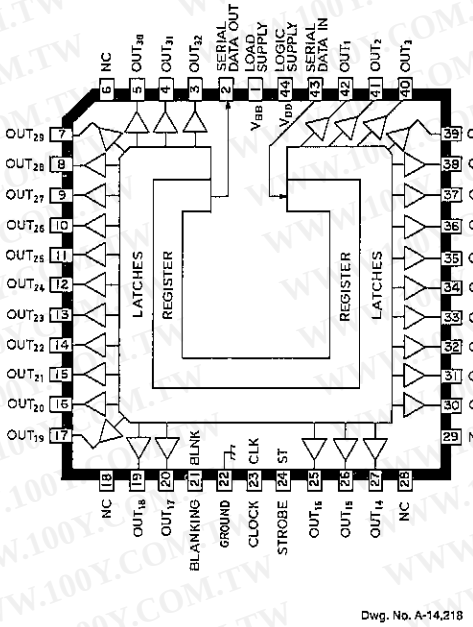
Caution: Sprague Electric CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

UCN-5818AF



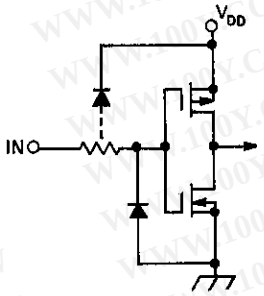
DWG. NO A-14,313

UCN-5818EPF



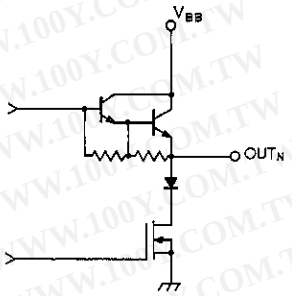
Dwg. No. A-14,218

TYPICAL INPUT CIRCUIT



Dwg. No. A-13,035

TYPICAL OUTPUT DRIVER

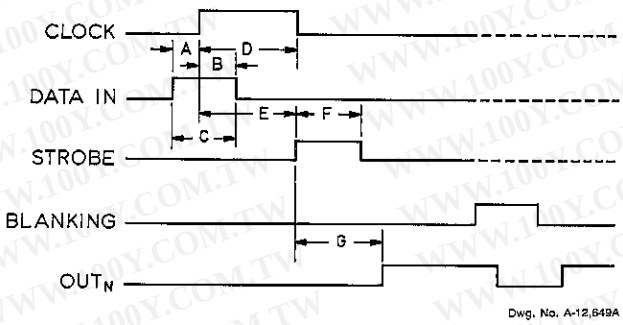


Dwg. No. A-14,219

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{BB} = 60$ V (UCN-5818AF/EPF) or 80 V (suffix '-1') unless otherwise noted

Characteristic	Symbol	Test Conditions	Limits at $V_{DD} = 5$ V			Limits at $V_{DD} = 12$ V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	$V_{OUT} = 0$ V, $T_A = +70°C$	—	−5.0	−15	—	−5.0	−15	µA
Output Voltage	$V_{OUT(1)}$	$I_{OUT} = -25$ mA, $V_{BB} = 60$ V	58	58.5	—	58	58.5	—	V
		$I_{OUT} = -25$ mA, $V_{BB} = 80$ V*	78	78.5	—	78	78.5	—	V
	$V_{OUT(0)}$	$I_{OUT} = 1$ mA	—	2.0	3.0	—	—	—	V
		$I_{OUT} = 2$ mA	—	—	—	—	2.0	3.0	V
Output Pull-Down Current	$I_{OUT(0)}$	$V_{OUT} = 5$ V to V_{BB}	2.0	3.5	—	—	—	—	mA
		$V_{OUT} = 20$ V to V_{BB}	—	—	—	8.0	13	—	mA
Input Voltage	$V_{IN(1)}$		3.5	—	5.3	10.5	—	12.3	V
	$V_{IN(0)}$		−0.3	—	+0.8	−0.3	—	+0.8	V
Input Current	$I_{IN(1)}$	$V_{IN} = V_{DD}$	—	0.05	0.5	—	0.1	1.0	µA
	$I_{IN(0)}$	$V_{IN} = 0.8$ V	—	−0.05	−0.5	—	−1.0	−1.0	µA
Serial Data Output Voltage	$V_{OUT(1)}$	$I_{OUT} = -200$ µA	4.5	4.7	—	11.7	11.8	—	V
	$V_{OUT(0)}$	$I_{OUT} = 200$ µA	—	200	250	—	100	200	mV
Maximum Clock Frequency	f_{clk}		3.3	5.0	—	—	7.5	—	MHz
Supply Current	$I_{DD(1)}$	All Outputs High	—	100	200	—	200	400	µA
	$I_{DD(0)}$	All Outputs Low	—	100	200	—	200	400	µA
	$I_{BB(1)}$	Outputs High, No Load	—	1.5	3.0	—	1.5	3.0	mA
	$I_{BB(0)}$	Outputs Low	—	10	100	—	10	100	µA
Blanking to Output Delay	t_{PHL}	$C_L = 30$ pF	—	300	550	—	125	150	ns
	t_{PLH}	$C_L = 30$ pF	—	250	450	—	170	200	ns
Output Fall Time	t_f	$C_L = 30$ pF	—	1000	1250	—	250	300	ns
Output Rise Time	t_r	$C_L = 30$ pF	—	150	170	—	150	170	ns

Negative current is defined as coming out of (sourcing) the specified device pin.
*UCN-5818AF-1 and UCN-5818EPF-1 only.



Dwg. No. A-12,649A

TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and Ground)

	V_{DD} = 5.0 V
A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C. Minimum Data Pulse Width	150 ns
D. Minimum Clock Pulse Width	150 ns
E. Minimum Time Between Clock Activation and Strobe	300 ns
F. Minimum Strobe Pulse Width	100 ns
G. Typical Time Between Strobe Activation and Output Transition	500 ns

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents $I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$	Serial Data Output	Strobe Input	Latch Contents $I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$	Blanking	Output Contents $I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$
H	⎍	H $R_1\ R_2\ \ldots R_{N-2}\ R_{N-1}$	R_{N-1}				
L	⎍	L $R_1\ R_2\ \ldots R_{N-2}\ R_{N-1}$	R_{N-1}				
X	⎍	$R_1\ R_2\ R_3\ \ldots R_{N-1}\ R_N$	R_N				
		X X X ... X X	X	L	$R_1\ R_2\ R_3\ \ldots R_{N-1}\ R_N$		
		$P_1\ P_2\ P_3\ \ldots P_{N-1}\ P_N$	P_N	H	$P_1\ P_2\ P_3\ \ldots P_{N-1}\ P_N$	L	$P_1\ P_2\ P_3\ \ldots P_{N-1}\ P_N$
					X X X ... X X	H	L L L ... L L

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

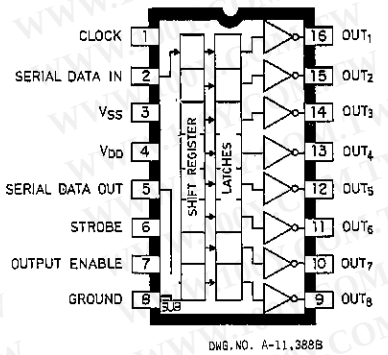
SERIES UCN-5820A
BiMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVERS

FEATURES

- 3.3 MHz Minimum Data Input Rate
- CMOS, PMOS, NMOS, TTL Compatible
- Internal Pull-Down Resistors
- Low-Power CMOS Logic & Latches
- High-Voltage Current-Sink Outputs
- 16-Pin Dual In-Line Plastic Package

A COMBINATION of bipolar and MOS technology gives the Series UCN-5820A an interface flexibility beyond the reach of standard logic buffers and power driver arrays. The three devices in this series each have an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sink Darlington output drivers. Except for maximum driver output voltage ratings, the UCN-5821A, UCN-5822A, and UCN-5823A are identical.

BiMOS II devices have much higher data-input rates than the original BiMOS circuits. With a 5 V logic supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL and DTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.



DWG. NO. A-11,388B

ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature and V_{SS} = 0 V

Output Voltage, V_{OUT} (UCN-5821A) ..... 50 V
(UCN-5822A) ..... 80 V
(UCN-5823A) ..... 100 V
Logic Supply Voltage, V_{DD} ..... 15 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT} ..... 500 mA
Package Power Dissipation, P_D ..... 1.67 W*
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +125°C

*Derate at the rate of 16.7 mW/°C above T_A = +25°C

Number of Outputs ON (I_{OUT} = 200 mA V_{DD} = 12 V)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	73%	62%	55%	47%	40%
7	83%	71%	62%	54%	46%
6	97%	82%	72%	63%	53%
5	100%	98%	87%	75%	63%
4	100%	100%	100%	93%	79%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

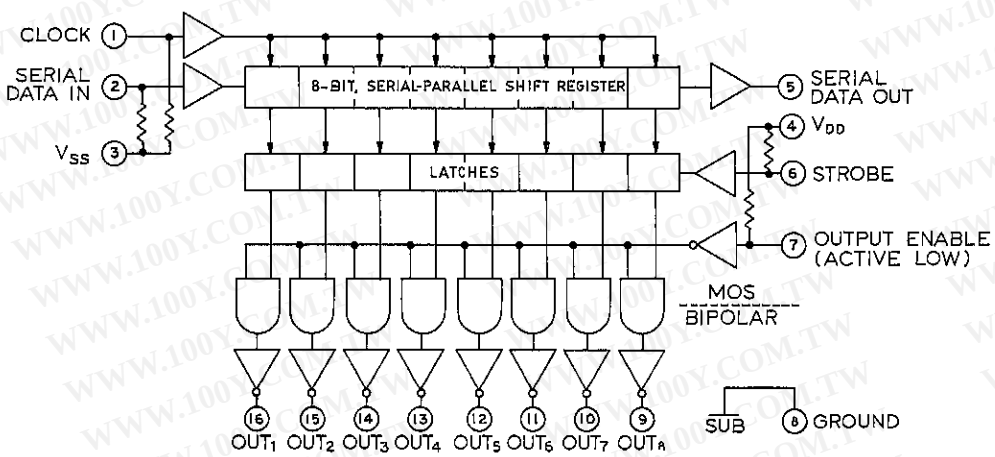
5

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5\ V$, $V_{SS} = 0\ V$ (unless otherwise specified)

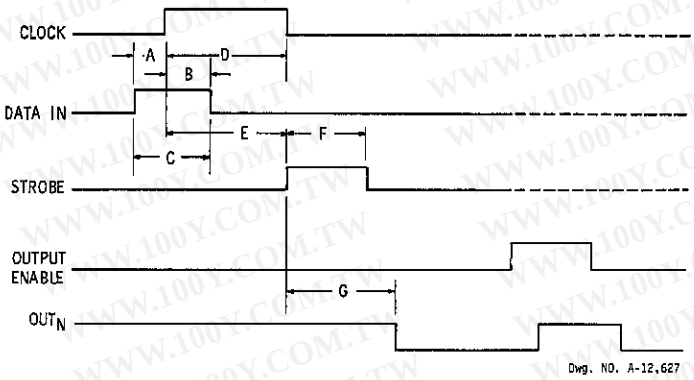
Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	UCN-5821A	$V_{OUT} = 50\ V$	—	50	µA
			$V_{OUT} = 50\ V$, $= +70°C$	—	100	µA
		UCN-5822A	$V_{OUT} = 80\ V$	—	50	µA
			$V_{OUT} = 80\ V$, $T_A = +70°C$	—	100	µA
		UCN-5823A	$V_{OUT} = 100\ V$	—	50	µA
			$V_{OUT} = 100\ V$, $T_A = +70°C$	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	$I_{OUT} = 100\ mA$	—	1.1	V
			$I_{OUT} = 200\ mA$	—	1.3	V
			$I_{OUT} = 350\ mA$, $V_{DD} = 7.0\ V$	—	1.6	V
Input Voltage	$V_{IN(0)}$	ALL		—	0.8	V
	$V_{IN(1)}$	ALL	$V_{DD} = 12\ V$	10.5	—	V
			$V_{DD} = 10\ V$	8.5	—	V
			$V_{DD} = 5.0\ V$	3.5	—	V
Input Resistance	R_{IN}	ALL	$V_{DD} = 12\ V$	50	—	kΩ
			$V_{DD} = 10\ V$	50	—	kΩ
			$V_{DD} = 5.0\ V$	50	—	kΩ
Supply Current	$I_{DD(ON)}$	ALL	One Driver ON, $V_{DD} = 12\ V$	—	4.5	mA
			One Driver ON, $V_{DD} = 10\ V$	—	3.9	mA
			One Driver ON, $V_{DD} = 5.0\ V$	—	2.4	mA
	$I_{DD(OFF)}$	ALL	$V_{DD} = 5.0\ V$, All Drivers OFF, All Inputs = 0 V	—	1.6	mA
			$V_{DD} = 12\ V$, All Drivers OFF, All Inputs = 0 V	—	2.9	mA

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-11,391D



TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS})

		V_{DD} = 5.0 V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C.	Minimum Data Pulse Width	150 ns
D.	Minimum Clock Pulse Width	150 ns
E.	Minimum Time Between Clock Activation and Strobe	300 ns
F.	Minimum Strobe Pulse Width	100 ns
G.	Typical Time Between Strobe Activation and Output Transition	500 ns

5

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial data entry.

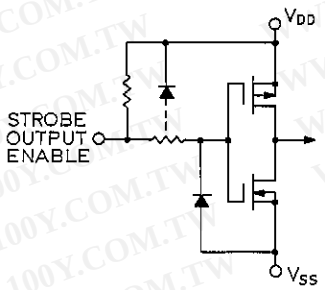
When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

SERIES UCN-5820A TRUTH TABLE

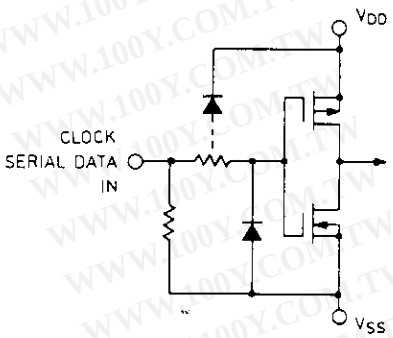
Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 ..... I_8	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 ..... I_8	Output Enable	Output Contents I_1 I_2 I_3 ..... I_8
H	⎍	H R_1 R_2 ..... R_7	R_7				
L	⎍	L R_1 R_2 ..... R_7	R_7				
X	⎎	R_1 R_2 R_3 ..... R_8	R_8				
		X X X X	X	L	R_1 R_2 R_3 ..... R_8		
		P_1 P_2 P_3 ..... P_8	P_8	H	P_1 P_2 P_3 ..... P_8	L	P_1 P_2 P_3 ..... P_8
					X X X X	H	H H H ..... H

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

TYPICAL INPUT CIRCUITS

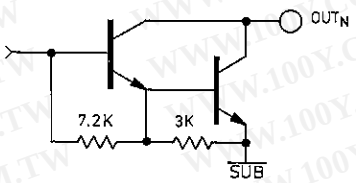


Dwg. No. A-12,658



Dwg. No. A-12,659

TYPICAL OUTPUT DRIVER

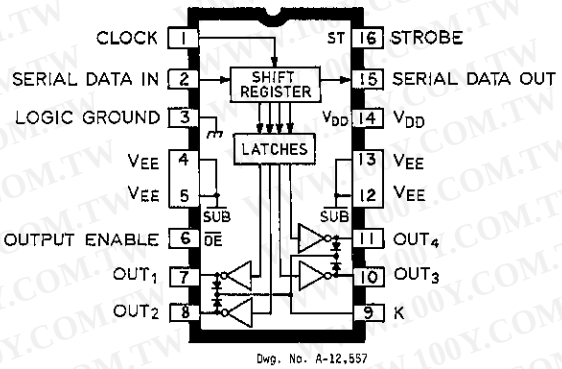


Dwg. No. A-14,314

UCN-5825B AND UCN-5826B
BiMOS II HIGH-CURRENT, SERIAL-INPUT, LATCHED DRIVERS

FEATURES

- 2 A Open Collector Outputs
- 60 V or 80 V Minimum Output Breakdown
- 35 V or 60 V Sustaining Voltage
- Output-Transient Protection
- Low-Power CMOS Logic and Latches
- Typical Data Input Rate > 5 MHz
- Internal Pull-Down Resistors
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Thermal Shutdown Circuitry



UCN-5825B and UCN-5826B BiMOS II integrated circuits combine a 4-bit CMOS shift register, associated latches, control circuitry, and level shifting, with bipolar Darlington outputs and transient-suppression diodes for inductive load applications.

The high-current, serial-input, latched drivers can be used with relays, solenoids, stepper motors, LED displays, incandescent displays, and other high-power loads. Control circuitry for both devices includes STROBE and OUTPUT ENABLE functions, and an internal latch that disables outputs at power-up and provides thermal shutdown protection.

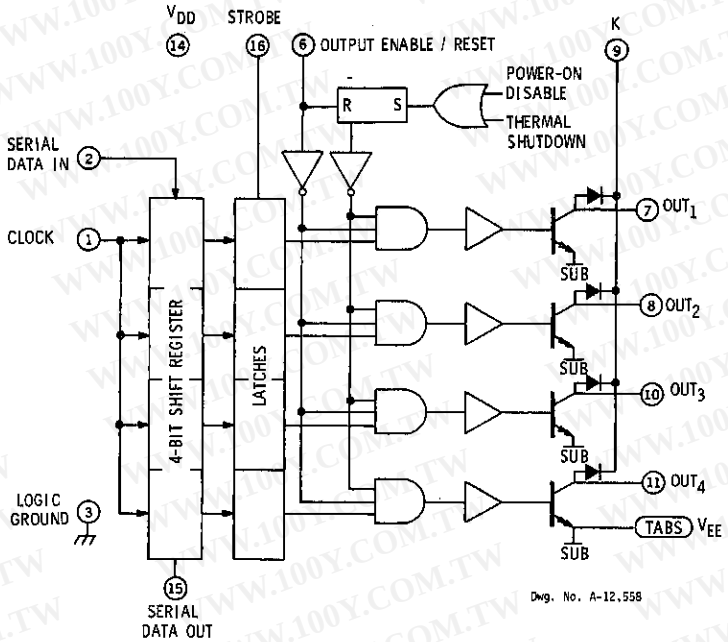
Except for output-voltage ratings, the UCN-5825B and UCN-5826B drivers are identical. The former is rated for operation to 60 V (35 V sustaining); the latter has a minimum output breakdown rating of 80 V (60 V sustaining).

The CMOS inputs cause minimum loading and are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors to insure a proper input-logic high level. A CMOS serial data output enables cascade connections in applications requiring additional drive lines. With a 5 V supply, BiMOS II devices typically operate at data-input rates above 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

Monolithic construction and a 16-pin dual in-line package with copper heat-sink contact tabs enable cost-effective and reliable systems designs supported by excellent package power dissipation rating, minimum size, and ease of installation. The package configuration is suitable for automatic insertion, allows easy attachment of an inexpensive heat sink, and fits a standard IC socket or printed wiring board layout.

Both devices are rated for continuous operation over the temperature range of −20°C to +85°C. Because of limitations on package power dissipation, simultaneous operation of all drivers may require a reduction in duty cycle.

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-12,558

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

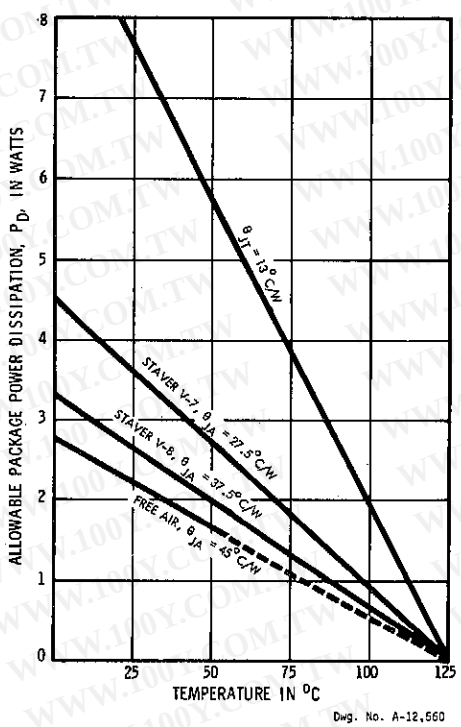
Output Voltage, V_{CE}
(UCN-5825B) ..... 60 V
(UCN-5826B) ..... 80 V
Output Voltage, $V_{CE(sus)}$
(UCN-5825B) ..... 35 V*
(UCN-5826B) ..... 60 V*
Logic Supply Voltage Range, V_{DD} ..... 4.5 V to 15 V
V_{DD} with reference to V_{EE} ..... 25 V
Emitter Supply Voltage, V_{EE} ..... −20 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT} ..... 2 A
Allowable Package Power Dissipation, P_D ..... See Graph
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +125°C

*For inductive load applications: The sum of the load supply voltage and clamping voltage(s).

Note: Output-current rating may be limited by duty cycle, ambient temperature, heat sinking, and a number of outputs conducting. Under any combination of conditions, do not exceed the specified maximum current rating and a junction temperature of +125°C.

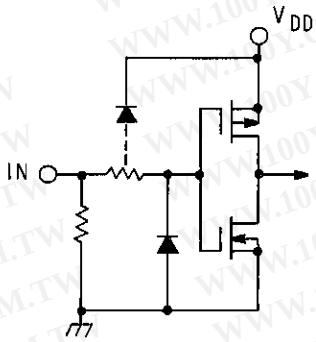
Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



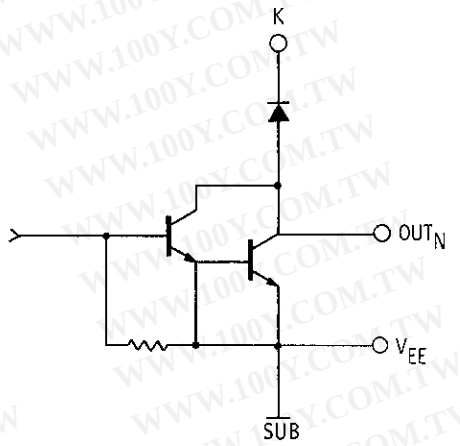
Dwg. No. A-12,560

TYPICAL INPUT CIRCUIT



Dwg. No. A-12,559

TYPICAL OUTPUT DRIVER



Dwg. No. A-12,561A

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = 60$ V, $V_{DD} = 5$ V to 12 V, $V_{EE} = 0$ V (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Limits Units
Output Leakage Current	I_{CEX}	UCN-5825B	$T_A = +25°C$	—	100	µA
			$T_A = +70°C$	—	500	µA
		UCN-5826B	$V_{CC} = 80$ V, $T_A = +25°C$	—	100	µA
			$V_{CC} = 80$ V, $T_A = +70°C$	—	500	µA
Output Saturation Voltage	$V_{CE(SAT)}$	Both	$I_{OUT} = 1.75$ A	—	1.75	V
Output Sustaining Voltage	$V_{CE(SAT)}$	UCN-5825B	$I_{OUT} = 1.75$ A, L = 2 mH	35	—	V
		UCN-5826B	$I_{OUT} = 1.75$ A, L = 2 mH	60	—	V
Clamp Diode Leakage Current	I_R	UCN-5825B	$V_R = 60$ V	—	100	µA
		UCN-5826B	$V_R = 80$ V	—	100	µA
Clamp Diode Forward Voltage	V_F	Both	$I_F = 1.75$ A	—	2.0	V
Input Voltage	$V_{IN(1)}$	Both	$V_{DD} = 5.0$ V	3.5	5.3	V
			$V_{DD} = 12$ V	10.5	12.3	V
	$V_{IN(0)}$	Both	$V_{DD} = 5$ V to 12 V	−0.3	+0.8	V
Input Resistance	R_{IN}	Both	$V_{DD} = 5.0$ V	100	—	kΩ
			$V_{DD} = 12$ V	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	Both	$V_{DD} = 5.0$ V	—	20	kΩ
			$V_{DD} = 12$ V	—	6.0	kΩ
Supply Current	I_{DD}	Both	All outputs OFF	—	3.0	mA
			All outputs ON	—	20	mA
Maximum Clock Frequency	f_C	Both		3.3	—	MHz
Turn-ON Delay	t_{PHL}	Both	0.5 E_{OE} to 0.5 E_{out}	—	1.0	µs
Turn-OFF Delay	t_{PLH}	Both	0.5 E_{OE} to 0.5 E_{out}	—	2.0	µs
Propagation Delay	t_{PD}	Both	0.5 E_{OE} to 0.5 E_{out}	—	100	ns

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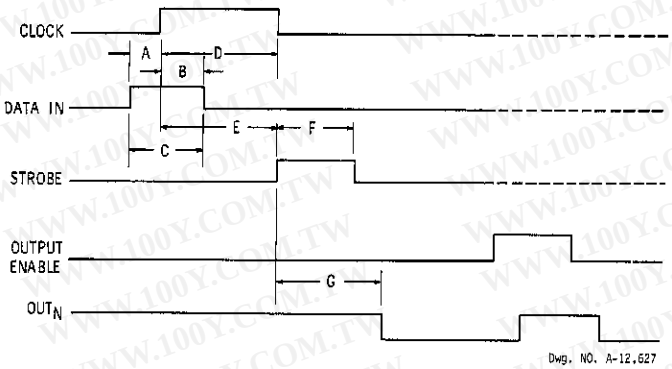


TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

		V_{DD} = 5.0 V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C.	Minimum Data Pulse Width	150 ns
D.	Minimum Clock Pulse Width	150 ns
E.	Minimum Time Between Clock Activation and Strobe	300 ns
F.	Minimum Strobe Pulse Width	100 ns
G.	Typical Time Between Strobe Activation and Output Transition	500 ns

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input low, the outputs are controlled by the state of the latches.

Two additional functions serve to protect the system and the device. Either power-up or overheating will set an internal latch that disables the outputs. With the latch set, data can be shifted and latched while the outputs are disabled. To resume normal operation, the latch must be reset by toggling OUTPUT ENABLE a minimum of 500 ns.

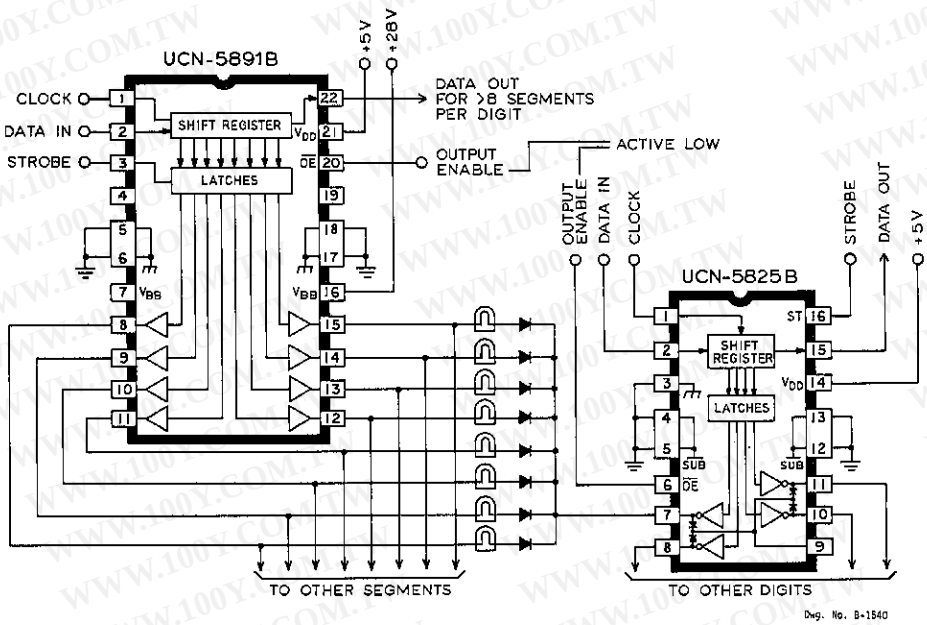
TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents I_1	I_2	I_3	I_4	Serial Data Output	Strobe Input	Latch Contents I_1	I_2	I_3	I_4	Output Enable	Output Contents I_1	I_2	I_3	I_4
H	↑	H	R_1	R_2	R_3	R_3										
L	↑	L	R_1	R_2	R_3	R_3										
X	↓	R_1	R_2	R_3	R_4	R_4										
		X	X	X	X	X	L	R_1	R_2	R_3	R_4					
		P_1	P_2	P_3	P_4	P_4	H	P_1	P_2	P_3	P_4	L	P_1	P_2	P_3	P_4
								X	X	X	X	H	H	H	H	H

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

TYPICAL APPLICATION

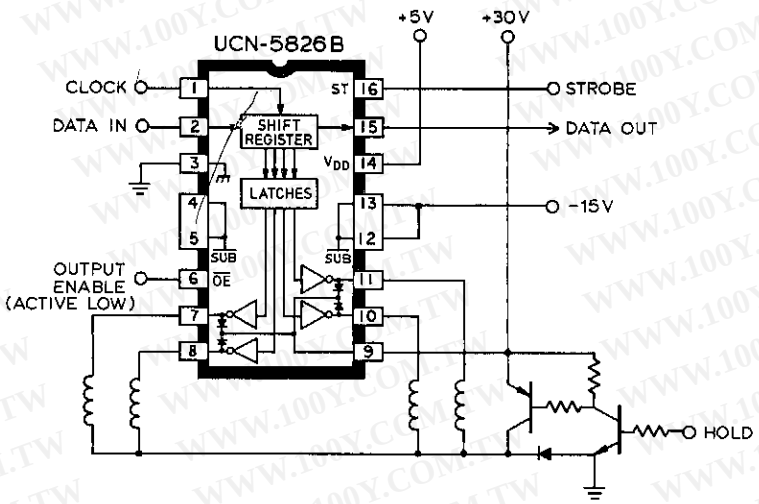
MULTIPLEXED INCANDESCENT LAMP DRIVE



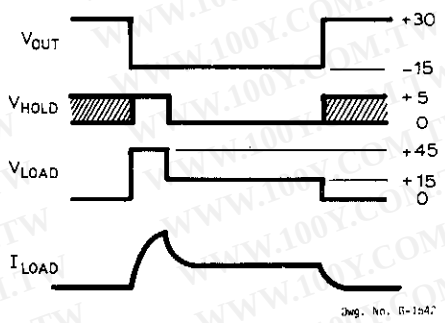
*Active Low

TYPICAL APPLICATION

BILEVEL HAMMER DRIVE



*Active Low



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UCN-5832A AND UCN-5832C
BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVERS

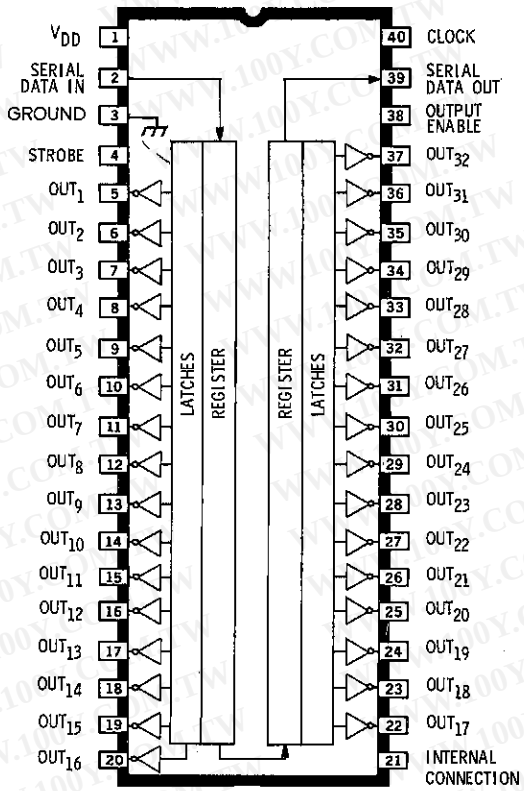
FEATURES

- 5 MHz Typical Data Input Rate
- Low-Power CMOS Logic and Latches
- 40 V Current Sink Outputs
- Low Saturation Voltage

INTENDED PRIMARILY to drive thermal printheads, Types UCN-5832A and UCN-5832C have been optimized for low output-saturation voltage, high-speed operation, and pin/pad configurations most convenient for the tight space requirements of high-resolution printheads. The integrated circuits can also be used to drive multiplexed LED displays or incandescent lamps at up to 150 mA peak current. A combination of bipolar and MOS technologies gives BiMOS II arrays an interface flexibility beyond the reach of standard buffers and power driver circuits.

The devices each have 32 bipolar open-collector saturated drivers, a CMOS data latch for each of the drivers, two 16-bit CMOS shift registers, and CMOS control circuitry. The high-speed CMOS shift registers and latches allow operation with most microprocessor/LSI-based systems. Use of these drivers with TTL may require input pull-up resistors to ensure an input logic high.

Type UCN-5832A is supplied in a 40-pin dual in-line plastic package with 0.600" (15.24 mm) row spacing. Under normal operating conditions, all outputs of the packaged device will sustain 100 mA continuously without derating. Type UCN-5832C is an unpackaged, passivated, bare-back device in chip form. In this version, the shift register is divided into two 16-bit blocks for maximum flexibility. For either device, MOS serial outputs permit cascading for interface applications requiring additional drive lines.



Dwg. No. A-12,377A

A similar 32-bit serial-input latched source driver is available as UCN-5818A. High-voltage, high-current 8-bit devices are available in Series UCN-5820A.

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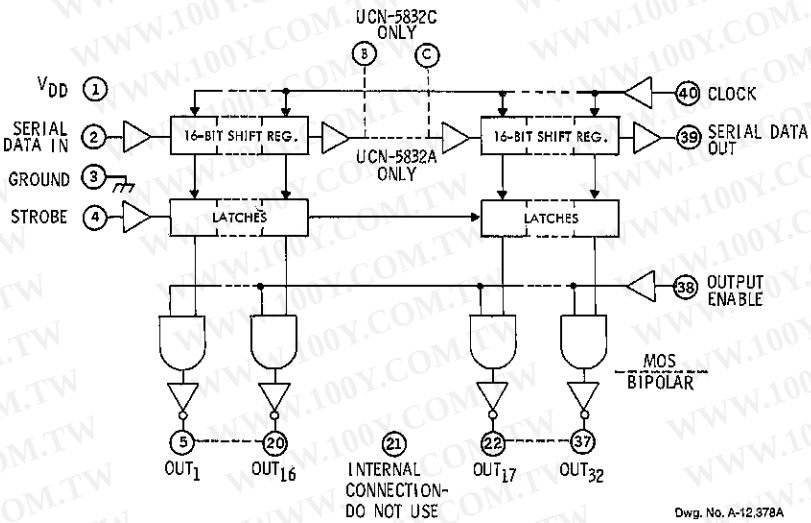
FUNCTIONAL BLOCK DIAGRAM



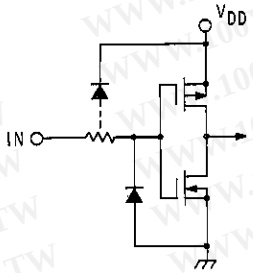
ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Output Voltage, V_{OUT} ..... 40 V
Logic Supply Voltage, V_{DD} ..... 15 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT} ..... 150 mA
Package Power Dissipation, P_D (UCN-5832A) ..... 2.8 W*
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +125°C

*Derate at the rate of 28 mW/°C above T_A = +25°C

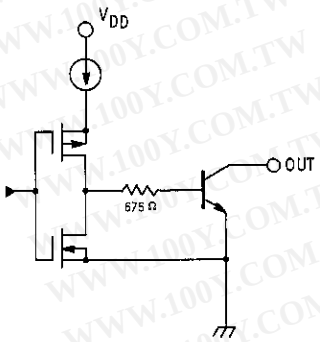
Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

TYPICAL INPUT CIRCUIT



Dwg. No. A-12,379A

TYPICAL OUTPUT DRIVER



Dwg. No. A-12,380A

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5$ V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 40$ V, $T_A = 70°C$	—	10	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 50$ mA	—	275	mV
		$I_{OUT} = 100$ mA	250	550	mV
Input Voltage	$V_{IN(1)}$		3.5	5.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{IN} = 3.5$ V	—	1.0	µA
	$I_{IN(0)}$	$V_{IN} = 0.8$ V	—	−1.0	µA
Input Impedance	Z_{IN}	$V_{IN} = 3.5$ V	3.5	—	MΩ
Serial Data/Output Resistance	R_{OUT}		—	20	kΩ
Supply Current	I_{DD}	One output ON, $I_{OUT} = 100$ mA	—	5.0	mA
		All outputs OFF	—	50	µA
Output Rise Time	t_r	$I_{OUT} = 100$ mA, 10% to 90%	—	1.0	µs
Output Fall Time	t_f	$I_{OUT} = 100$ mA, 90% to 10%	—	1.0	µs

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

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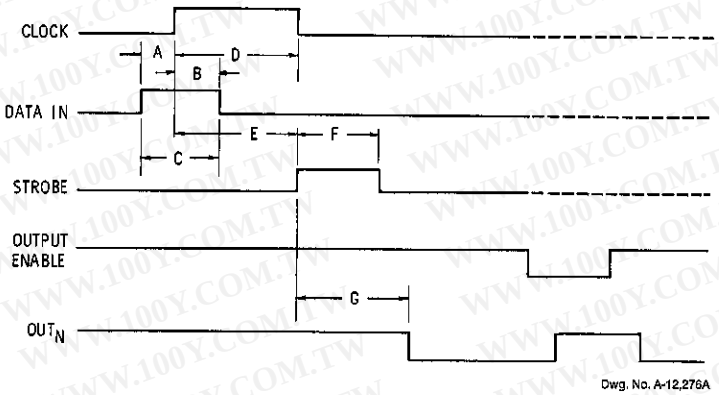


Dwg. No. A-12,276A

TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

		V_{DD} = 5.0 V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C.	Minimum Data Pulse Width	150 ns
D.	Minimum Clock Pulse Width	150 ns
E.	Minimum Time Between Clock Activation and Strobe	300 ns
F.	Minimum Strobe Pulse Width	100 ns
G.	Typical Time Between Strobe Activation and Output Transition	500 ns

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be low during serial data entry.

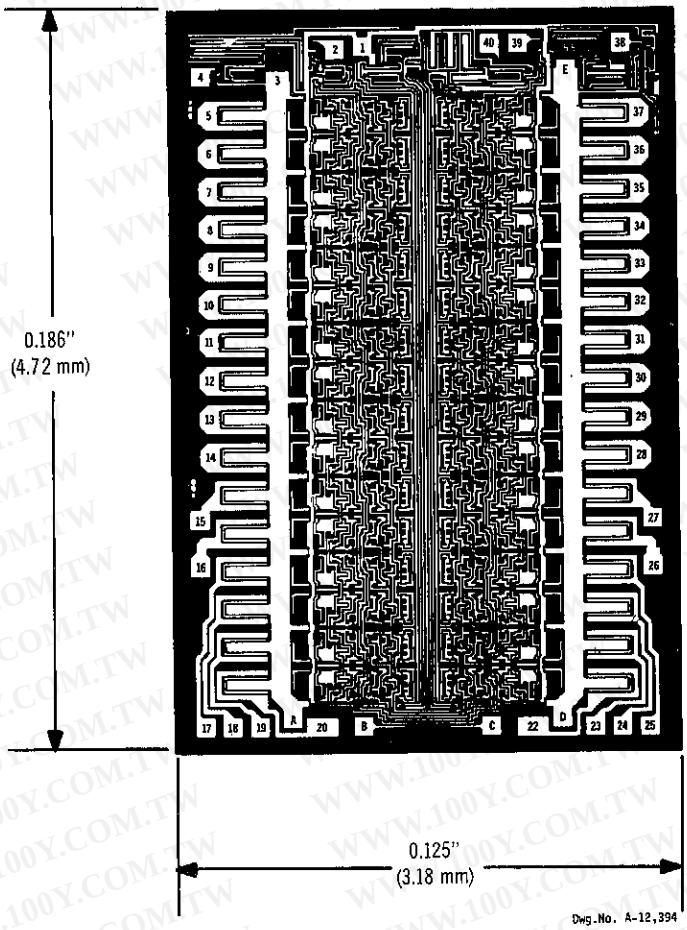
When the OUTPUT ENABLE input is low, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input high, the outputs are controlled by the state of the latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Output Enable Input	Output Contents
		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$			$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$
H	⎍	$H\ R_1\ R_2\ \ldots R_{N-2} R_{N-1}$	R_{N-1}				
L	⎍	$L\ R_1\ R_2\ \ldots R_{N-2} R_{N-1}$	R_{N-1}				
X	⎎	$R_1\ R_2\ R_3\ \ldots R_{N-1} R_N$	R_N				
		$X\ X\ X\ \ldots X\ X$	X	L	$R_1\ R_2\ R_3\ \ldots R_{N-1} R_N$		
		$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$	P_N	H	$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$	H	$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$
					$X\ X\ X\ \ldots X\ X$	L	$H\ H\ H\ \ldots H\ H$

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

UCN-5832C



UCN-5832 chips are of silicon planar epitaxial construction. They are identical to those used for packaged devices. When assembled correctly, they should lead to a high final test yield. All chips are visually inspected for masking, diffusion, and scribing defects. Conformance to electrical parameters can be guaranteed (at additional charge) by performing measurements on packaged units assembled from a random sample taken from the lot.

The preferred method of sale for unpackaged die is in wafer form. These are identified as UCN-5832C*W* and are supplied in 4" (100 mm) wafers that have been tested (probed) in wafer form. Electrically defective devices are identified by ink dots during this operation. Wafers do not include visual die inspection. Orders for UCN-5832C*W* will be accepted only for complete wafers.

Because Sprague Electric Company does not control the customer packaging of UCN-5832C chips or UCN-5832C*W* wafers, Sprague Electric company assumes no liability for final electrical and reliability parameters.

	PAD DESIGNATIONS	
PAD	UCN-5832A	UCN-5832C
1	V_{DD}	V_{DD}
2	SERIAL DATA IN	SERIAL DATA IN_1
3	GROUND	GROUND*
4	STROBE	STROBE
5	OUT_1	OUT_1
6	OUT_2	OUT_2
7	OUT_3	OUT_3
8	OUT_4	OUT_4
9	OUT_5	OUT_5
10	OUT_6	OUT_6
11	OUT_7	OUT_7
12	OUT_8	OUT_8
13	OUT_9	OUT_9
14	OUT_{10}	OUT_{10}
15	OUT_{11}	OUT_{11}
16	OUT_{12}	OUT_{12}
17	OUT_{13}	OUT_{13}
18	OUT_{14}	OUT_{14}
19	OUT_{15}	OUT_{15}
A	—	GROUND*
20	OUT_{16}	OUT_{16}
B	—	SERIAL DATA OUT_{16}
21	INTERNAL CONNECTION—DO NOT USE	—
C	—	SERIAL DATA IN_{17}
22	OUT_{17}	OUT_{17}
D	—	GROUND*
23	OUT_{18}	OUT_{18}
24	OUT_{19}	OUT_{19}
25	OUT_{20}	OUT_{20}
26	OUT_{21}	OUT_{21}
27	OUT_{22}	OUT_{22}
28	OUT_{23}	OUT_{23}
29	OUT_{24}	OUT_{24}
30	OUT_{25}	OUT_{25}
31	OUT_{26}	OUT_{26}
32	OUT_{27}	OUT_{27}
33	OUT_{28}	OUT_{28}
34	OUT_{29}	OUT_{29}
35	OUT_{30}	OUT_{30}
36	OUT_{31}	OUT_{31}
37	OUT_{32}	OUT_{32}
38	OUTPUT ENABLE	OUTPUT ENABLE
E	—	GROUND*
39	SERIAL DATA OUT	SERIAL DATA OUT_{32}
40	CLOCK	CLOCK

*Bonding pads *A* or *3* and *D* or *E* must be connected to the substrate. For maximum output current capability, pads *A, D, E,* and *3* must all be bonded to the substrate.

UCN-5832EP
BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVER

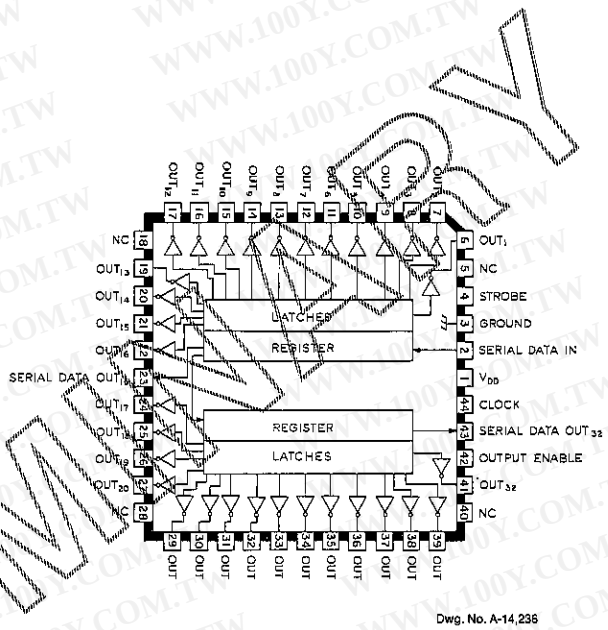
FEATURES

- 5 MHz Typical Data Input Rate
- Low-Power CMOS Logic and Latches
- 40 V Current-Sink Outputs
- Low Saturation Voltage

Intended primarily to drive thermal printheads, the UCN-5832EP has been optimized for low output-saturation voltage, high-speed operation, and a pin configuration most convenient for the tight space requirements of high-resolution printheads.

The device has 32 bipolar open-collector saturated drivers, a CMOS data latch for each of the drivers, two 16-bit CMOS shift registers, and CMOS control circuitry. The high-speed CMOS shift registers and latches allow operation with most microprocessor/LSI-based systems. Use of the driver with TTL may require input pull-up resistors to ensure an input logic high.

UCN-5832EP is packaged in a 44-pin plastic leaded chip carrier (quad) with 50-mil lead spacing.



Dwg. No. A-14,236

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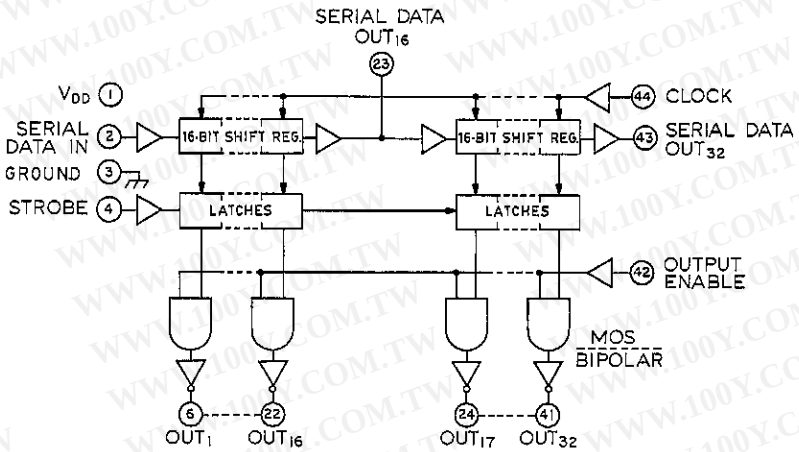
ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Output Voltage, V_{OUT}	40 V
Logic Supply Voltage, V_{DD}	15 V
Input Voltage Range, V_{IN}	−0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT}	150 mA
Package Power Dissipation, P_D	2.0 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +125°C

*Derate at the rate of 20 mW/°C above T_A = +25°C

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

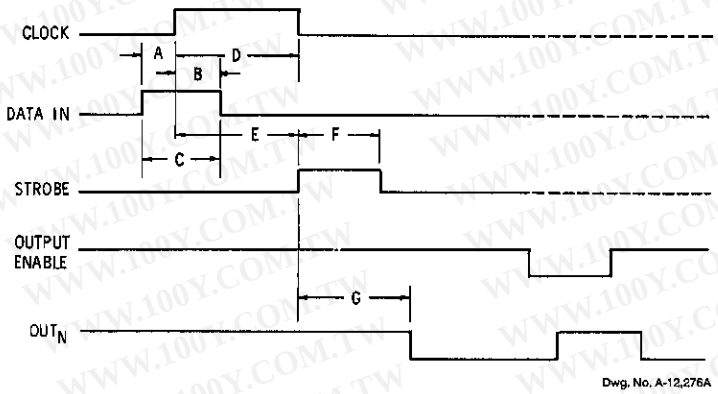


Dwg. No. A-14,237

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5$ V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 40$ V, $T_A = 70°C$	—	10	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 50$ mA	—	275	mV
		$I_{OUT} = 100$ mA	250	550	mV
Input Voltage	$V_{IN(1)}$		3.5	5.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{IN} = 3.5$ V	—	1.0	µA
	$I_{IN(0)}$	$V_{IN} = 0.8$ V	—	−1.0	µA
Input Impedance	Z_{IN}	$V_{IN} = 3.5$ V	3.5	—	MΩ
Serial Data/Output Resistance	R_{OUT}		—	20	kΩ
Supply Current	I_{DD}	One output ON, $I_{OUT} = 100$ mA	—	5.0	mA
		All outputs OFF	—	50	µA
Output Rise Time	t_r	$I_{OUT} = 100$ mA, 10% to 90%	—	1.0	µs
Output Fall Time	t_f	$I_{OUT} = 100$ mA, 90% to 10%	—	1.0	µs

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.



Dwg. No. A-12,276A

TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

		V_{DD} = 5.0 V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C.	Minimum Data Pulse Width	150 ns
D.	Minimum Clock Pulse Width	150 ns
E.	Minimum Time Between Clock Activation and Strobe	300 ns
F.	Minimum Strobe Pulse Width	100 ns
G.	Typical Time Between Strobe Activation and Output Transition	500 ns

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be low during serial data entry.

When the OUTPUT ENABLE input is low, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input high, the outputs are controlled by the state of the latches.

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TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents $I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$	Serial Data Output	Strobe Input	Latch Contents $I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$	Output Enable Input	Output Contents $I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$
H	⎍	H $R_1\ R_2\ \ldots R_{N-2} R_{N-1}$	R_{N-1}				
L	⎍	L $R_1\ R_2\ \ldots R_{N-2} R_{N-1}$	R_{N-1}				
X	⎎	$R_1\ R_2\ R_3\ \ldots R_{N-1} R_N$	R_N				
		X X X ...X X	X	L	$R_1\ R_2\ R_3\ \ldots R_{N-1} R_N$		
		$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$	P_N	H	$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$	H	$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$
					X X X ...X X	L	H H H ...H H

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

UCN-5833A, UCN-5833C, UCN-5833EP
BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVERS

FEATURES

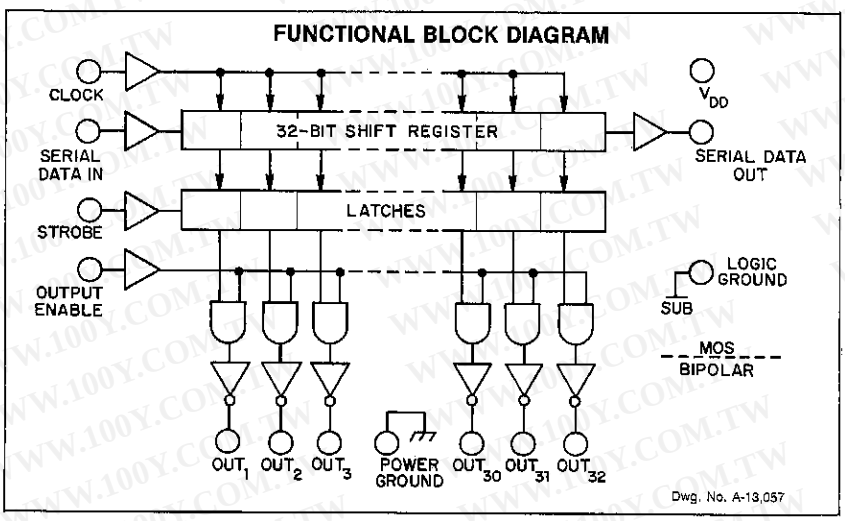
- 5 MHz Typical Data Input Rate
- 30 V Min. Output Breakdown
- Darlington Current-Sink Outputs
- Low-Power CMOS Logic and Latches
- Minimum Chip Size (UCN-5833C)

Designed primarily to reduce logic supply current, chip size and associated cost, the UCN-5833A/C/EP integrated circuits offer high-speed operation for thermal printers. These devices can also be used to drive multiplexed LED displays or incandescent lamps within their 125 mA peak output current rating. The combination of bipolar and MOS technologies gives BiMOS II smart power ICs an interface flexibility beyond the reach of standard buffers and power driver circuits. The unpackaged UCN-5833C features minimum size and pad configurations most convenient for the tighter space requirements of high-resolution thermal printheads.

These 32-bit drivers have bipolar open-collector Darlington outputs, a CMOS data latch for each of the drivers, a 32-bit CMOS shift register, and CMOS control circuitry. The high-speed CMOS shift registers and latches allow operation with most microprocessor/LSI-based systems at data input rates above 3.3 MHz. Use of these drivers with TTL may require input pull-up resistors to ensure an input logic high.

The UCN-5833A is supplied in a 40-pin dual in-line plastic package with 0.600″ (15.24 mm) row spacing. At an ambient temperature of +50°C, all outputs of the DIP-packaged device will sustain 50 mA continuously. The UCN-5833C is an unpackaged, passivated, bare-back device in chip form. For high-density applications, the UCN-5833EP is available. This 44-lead plastic chip carrier (quad pack) is intended for surface-mounting on solder lands with 0.050″ (1.27 mm) centers. CMOS serial data outputs permit cascading for applications requiring additional drive lines.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

at +25°C Free-Air Temperature

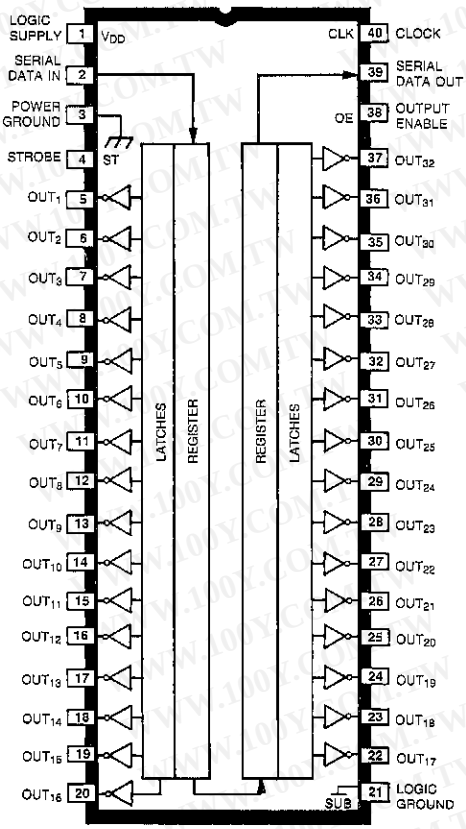
Output Voltage, V_{OUT}	30 V
Logic Supply Voltage, V_{DD}	7.0 V
Input Voltage Range, V_{IN}	−0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT} (each output)	125 mA
Package Power Dissipation, P_D (UCN-5833A)	2.8 W*
(UCN-5833EP)	2.0 W†
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +125°C

*Derate at the rate of 28 mW/°C above T_A = +25°C.

†Derate at the rate of 20 mW/°C above T_A = +25°C.

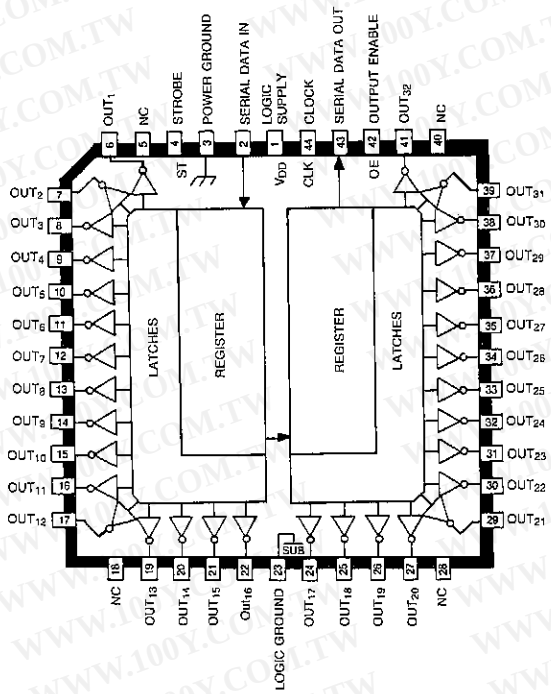
Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

UCN-5833A



Dwg. No. A-13,048

UCN-5833EP



Dwg. No. A-13,049

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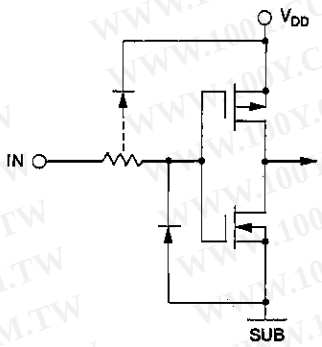
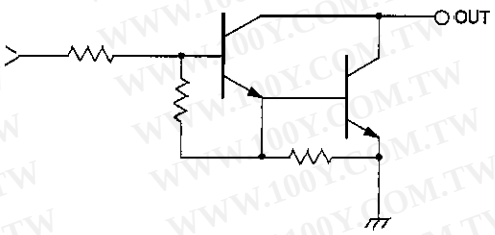
TYPICAL INPUT CIRCUIT



Dwg. No. A-13,050

TYPICAL OUTPUT DRIVER

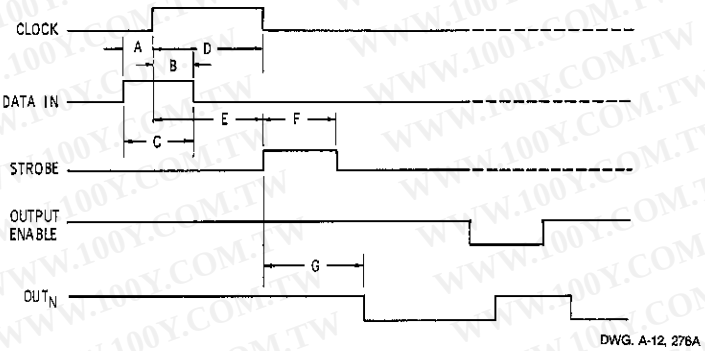


Dwg. No. A-13,051

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 30 V, T_A = 70°C	—	10	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 50 mA	—	1.2	V
		I_{OUT} = 100 mA	—	1.7	V
Input Voltage	$V_{IN(1)}$		3.5	5.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = 5.0 V	—	1.0	μA
	$I_{IN(0)}$	V_{IN} = 0 V	—	−1.0	μA
Serial Output Voltage	$V_{OUT(1)}$	I_{OUT} = −200 μA	4.5	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 μA	—	0.3	V
Supply Current	I_{DD}	One output ON, I_{out} = 100 mA	—	1.0	mA
		All outputs OFF	—	50	μA
Output Rise Time	t_r	I_{OUT} = 100 mA, 10% to 90%	—	500	ns
Output Fall Time	t_f	I_{OUT} = 100 mA, 90% to 10%	—	500	ns

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.



DWG. A-12, 276A

TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

		V_{DD} = 5.0V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C.	Minimum Data Pulse Width	150 ns
D.	Minimum Clock Pulse Width	150 ns
E.	Minimum Time Between Clock Activation and Strobe	300 ns
F.	Minimum Strobe Pulse Width	100 ns
G.	Typical Time Between Strobe Activation and Output Transition	500 ns

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are by-passed (STROBE tied high) will require that the OUTPUT ENABLE input be low during serial data entry.

When the OUTPUT ENABLE input is low, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input high, the outputs are controlled by the state of the latches.

5

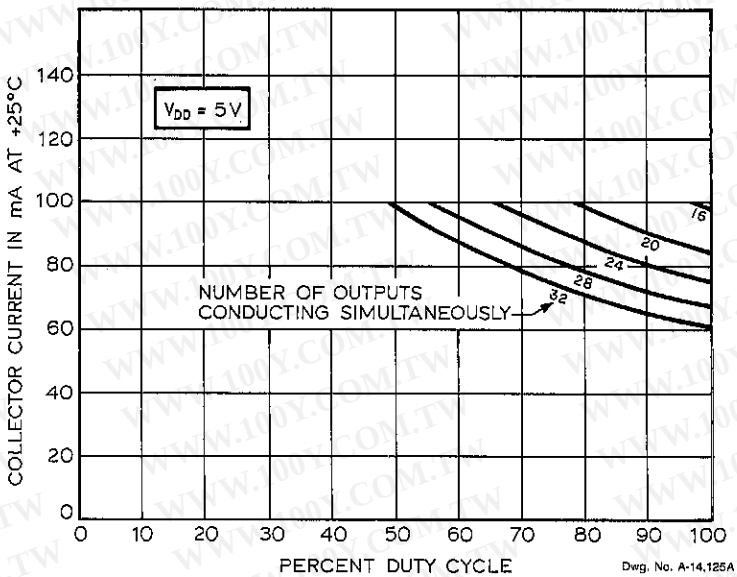
TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents $I_1\ I_2\ I_3 \ldots I_{N-1}\ I_N$	Serial Data Output	Strobe Input	Latch Contents $I_1\ I_2\ I_3 \ldots I_{N-1}\ I_N$	Output Enable Input	Output Contents $I_1\ I_2\ I_3 \ldots I_{N-1}\ I_N$
H	⎍	H $R_1\ R_2 \ldots R_{N-2}\ R_{N-1}$	R_{N-1}				
L	⎍	L $R_1\ R_2 \ldots R_{N-2}\ R_{N-1}$	R_{N-1}				
X	⎎	$R_1\ R_2\ R_3 \ldots R_{N-1}\ R_N$	R_N				
		X X X . . . X X	X	L	$R_1\ R_2\ R_3 \ldots R_{N-1}\ R_N$		
		$P_1\ P_2\ P_3 \ldots P_{N-1}\ P_N$	P_N	H	$P_1\ P_2\ P_3 \ldots P_{N-1}\ P_N$	H	$P_1\ P_2\ P_3 \ldots P_{N-1}\ P_N$
					X X X . . . X X	L	H H H . . . H H

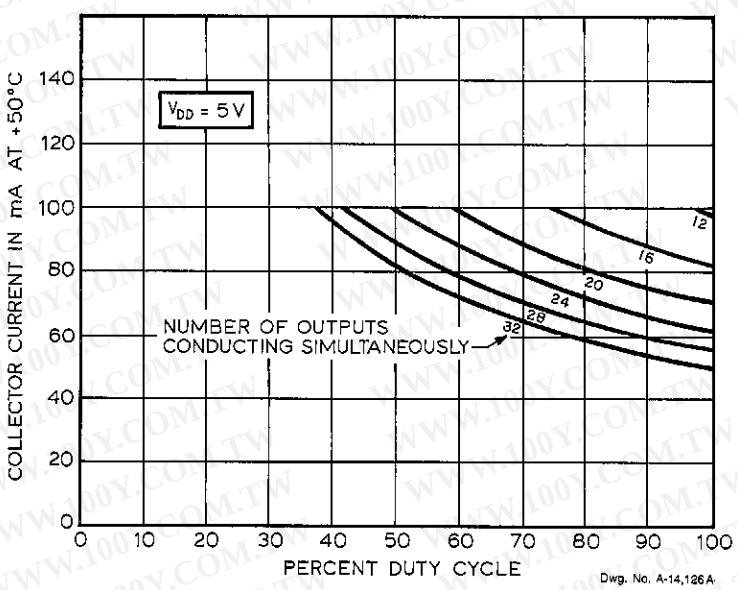
L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

UCN-5833A

ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +25°C

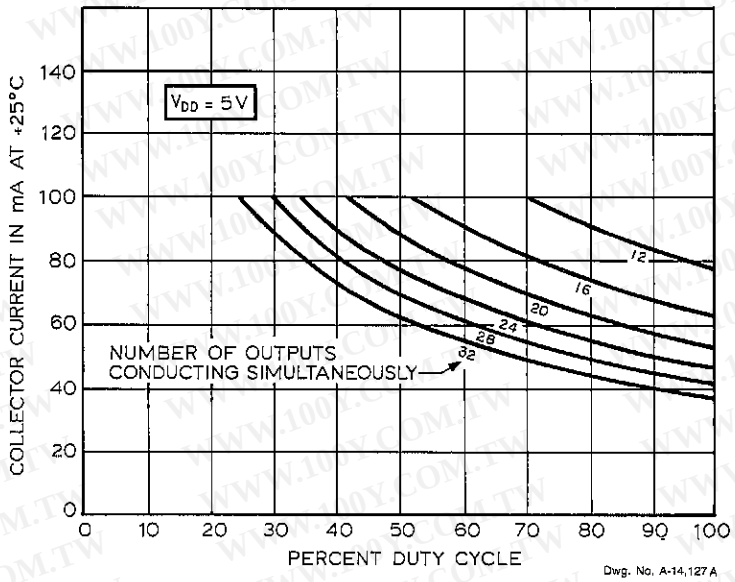


ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +50°C

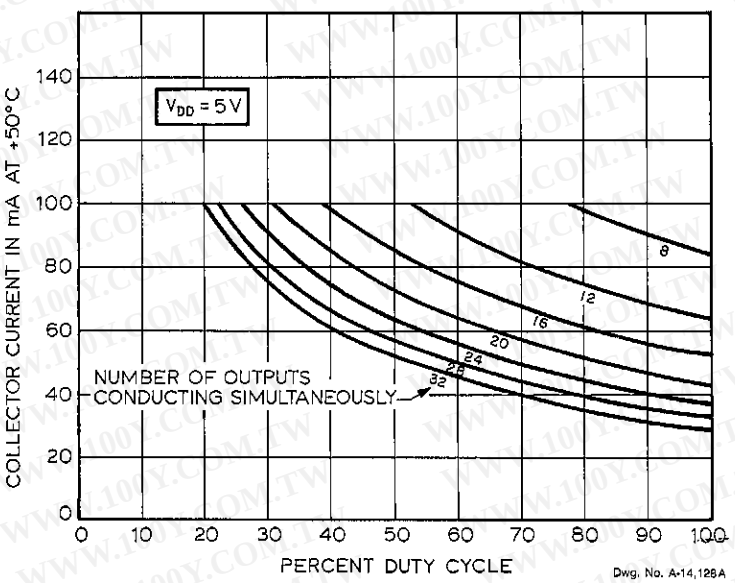


UCN-5833EP

ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +25°C



ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +50°C



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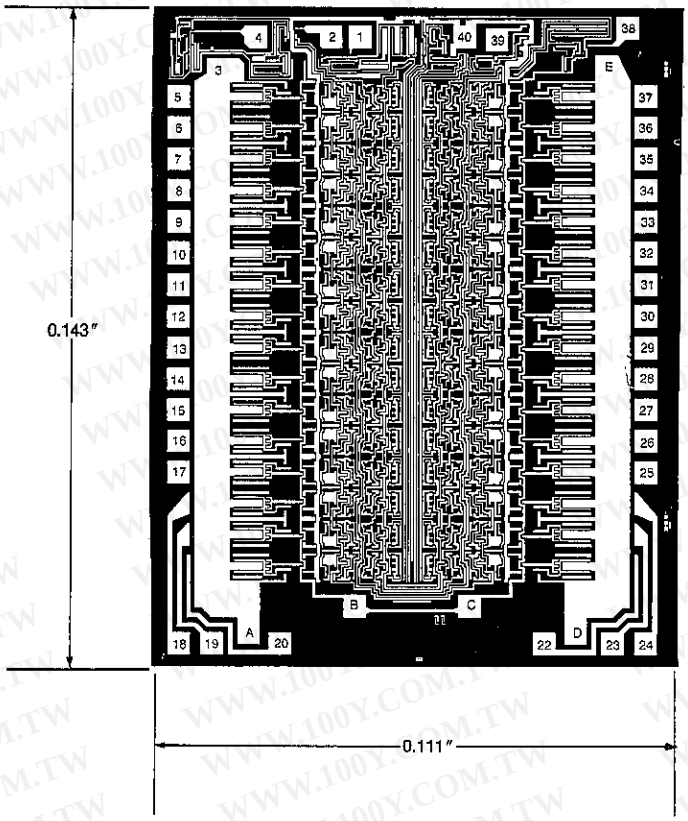
UCN-5833C



Dwg. No. A-13,052

UCN-5833C chips are of silicon planar epitaxial construction using a merged technology (bipolar power and low-power CMOS logic). They are identical to those used for packaged devices. The preferred method of sale for unpackaged die is in four-inch (100 mm) wafer form (UCN-5833CW). Users requiring separate, inspected die should contact the nearest Sprague sales office or representative. A select list of chip-processing operations, which offer value-added testing, inspection, and assembly, is available for referral.

All wafers from which chips are sold are processed through standard production techniques with 100% inspection after each critical process step. Die (in wafer form) are electrically tested as completely as practical. Defective devices are identified by an ink dot on the die. Complete conformance to all electrical specifications can be guaranteed (at additional cost) by performing measurements on packaged units assembled from a random sample of the device production lot.

Because Sprague Electric Company does not control the customer handling and packaging of die or wafers, Sprague Electric Company can assume no liability for final electrical or reliability failures that are determined to be the result of improper storage, assembly, or test by the customer.

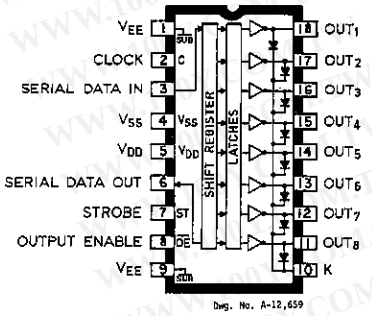
	PAD DESIGNATIONS	
PAD	UCN-5833A	UCN-5833C
1	V_{DD}	V_{DD}
2	SERIAL DATA IN	SERIAL DATA IN_1
3	POWER GROUND	POWER GROUND
4	STROBE	STROBE
5	OUT_1	OUT_1
6	OUT_2	OUT_2
7	OUT_3	OUT_3
8	OUT_4	OUT_4
9	OUT_5	OUT_5
10	OUT_6	OUT_6
11	OUT_7	OUT_7
12	OUT_8	OUT_8
13	OUT_9	OUT_9
14	OUT_{10}	OUT_{10}
15	OUT_{11}	OUT_{11}
16	OUT_{12}	OUT_{12}
17	OUT_{13}	OUT_{13}
18	OUT_{14}	OUT_{14}
19	OUT_{15}	OUT_{15}
A	—	POWER GROUND
20	OUT_{16}	OUT_{16}
B	—	LOGIC GROUND/SUB*
21	LOGIC GROUND/SUB*	—
C	—	LOGIC GROUND/SUB*
22	OUT_{17}	OUT_{17}
D	—	POWER GROUND
23	OUT_{18}	OUT_{18}
24	OUT_{19}	OUT_{19}
25	OUT_{20}	OUT_{20}
26	OUT_{21}	OUT_{21}
27	OUT_{22}	OUT_{22}
28	OUT_{23}	OUT_{23}
29	OUT_{24}	OUT_{24}
30	OUT_{25}	OUT_{25}
31	OUT_{26}	OUT_{26}
32	OUT_{27}	OUT_{27}
33	OUT_{28}	OUT_{28}
34	OUT_{29}	OUT_{29}
35	OUT_{30}	OUT_{30}
36	OUT_{31}	OUT_{31}
37	OUT_{32}	OUT_{32}
38	OUTPUT ENABLE	OUTPUT ENABLE
E	—	POWER GROUND
39	SERIAL DATA OUT	SERIAL DATA OUT_{32}
40	CLOCK	CLOCK

*The substrate must be connected to the most negative point in the external circuit to maintain isolation between drivers and to provide for normal transistor operation. For maximum output current capability, pads *A, D, E,* and *3* must all be bonded to power ground.

SERIES UCN-5840A
BIMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVERS

FEATURES

- 3.3 MHz Minimum Data-Input Rate
- CMOS, PMOS, NMOS, TTL Compatible
- Internal Pull-Up/Pull-Down Resistors
- Low-Power CMOS Logic and Latches
- High-Voltage Current-Sink Outputs
- Output Transient-Protection Diodes
- Single or Split Supply Operation
- 18-Pin Dual In-Line Plastic Package



Dwg. No. A-12,659

INTEGRATING low-power CMOS logic and bipolar output power drivers permit Series UCN-5840A integrated circuits to be used in a wide variety of peripheral power driver applications. The three devices in this series each have an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sink Darlington output drivers.

Except for maximum driver output voltage ratings, the UCN-5841A, UCN-5842A, and UCN-5843A are identical. The UCN-5843A offers premium performance with a minimum output-breakdown voltage rating of 100 V (50 V sustaining). The drivers can be operated with a split supply where the negative supply is up to −20 V.

The 500 mA outputs, with integral transient-suppression diodes, are suitable for use with relays, solenoids and other inductive loads.

BiMOS II latches have higher data-input rates than the original BiMOS circuits. With a 5 V logic supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL or DTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.

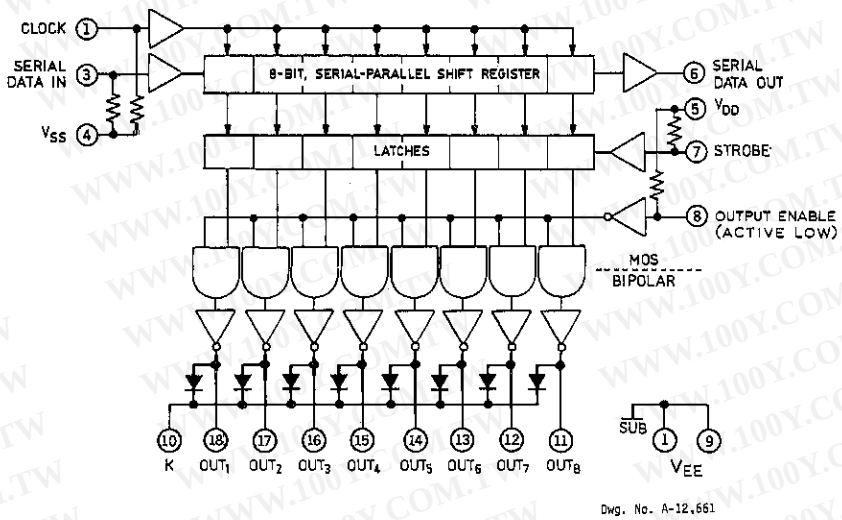
These devices are supplied in 18-pin dual in-line plastic packages for operation over the temperature range of −20°C to +85°C. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current might require a reduction in duty cycle. A copper-alloy lead frame provides for maximum package power dissipation.

ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature and V_{SS} = 0 V

Output Voltage, V_{CE} (UCN-5841A)	50 V
(UCN-5842A)	80 V
(UCN-5843A)	100 V
Output Voltage, $V_{CE(sus)}$ (UCN-5841A)	35 V†
(UCN-5842A)	50 V†
(UCN-5843A)	50 V†
Logic Supply Voltage Range, V_{DD}	4.5 V to 15 V
V_{DD} with Reference to V_{EE}	25 V
Emitter Supply Voltage, V_{EE}	−20 V
Input Voltage Range, V_{IN}	−0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT}	500 mA
Package Power Dissipation, P_D	1.82 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +125°C

†For inductive load applications.
*Derate at the rate of 18.2 mW/°C above T_A = +25°C

FUNCTIONAL BLOCK DIAGRAM



Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

MAXIMUM ALLOWABLE DUTY CYCLE

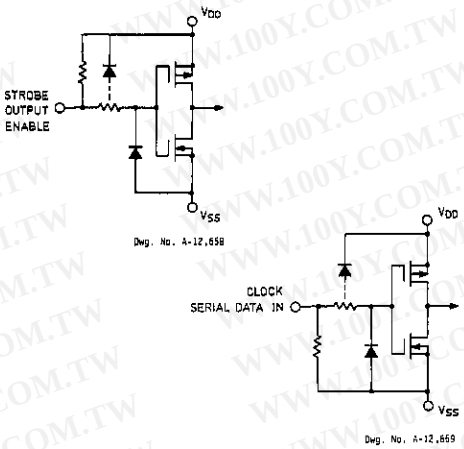
V_{DD} = 5.0 V

Number of Outputs ON (I_{OUT} = 200 mA V_{DD} = 5.0 V)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	85%	72%	64%	55%	46%
7	97%	82%	73%	63%	53%
6	100%	96%	85%	73%	62%
5	100%	100%	100%	88%	75%
4	100%	100%	100%	100%	93%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

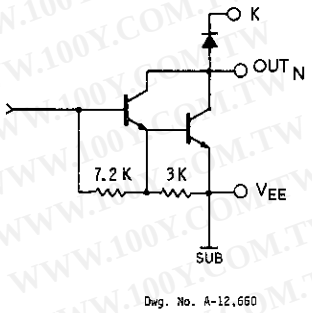
V_{DD} = 12 V

Number of Outputs ON (I_{OUT} = 200 mA V_{DD} = 12 V)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	80%	68%	60%	52%	44%
7	91%	77%	68%	59%	50%
6	100%	90%	79%	69%	58%
5	100%	100%	95%	82%	69%
4	100%	100%	100%	100%	86%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

TYPICAL INPUT CIRCUITS

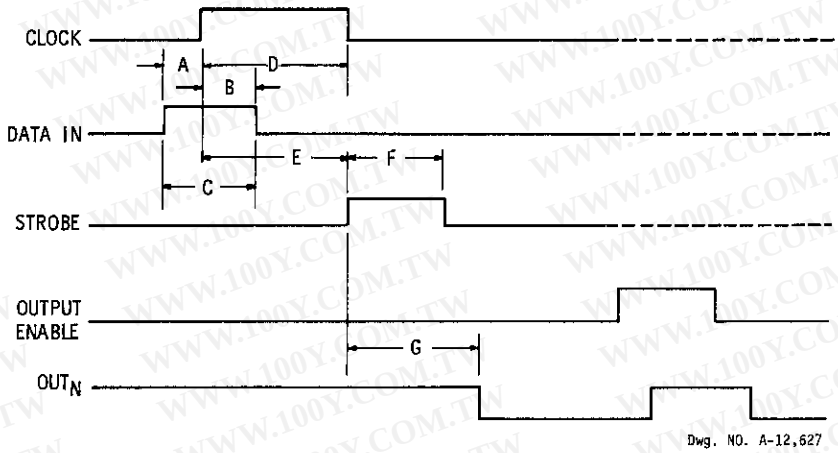


TYPICAL OUTPUT DRIVER



ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5\ V$, $V_{SS} = V_{EE} = 0\ V$ (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Unit
Output Leakage Current	I_{CEX}	UCN-5841A	$V_{OUT} = 50\ V$	—	50	µA
			$V_{OUT} = 50\ V$, $T_A = +70°C$	—	100	µA
		UCN-5842A	$V_{OUT} = 80\ V$	—	50	µA
			$V_{OUT} = 80\ V$, $T_A = +70°C$	—	100	µA
		UCN-5843A	$V_{OUT} = 100\ V$	—	50	µA
			$V_{OUT} = 100\ V$, $T_A = +70°C$	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	$I_{OUT} = 100\ mA$	—	1.1	V
			$I_{OUT} = 200\ mA$	—	1.3	V
			$I_{OUT} = 350\ mA$, $V_{DD} = 7.0\ V$	—	1.6	V
Collector-Emitter Sustaining Voltage	$V_{CE(sus)}$	UCN-5841A	$I_{OUT} = 350\ mA$, $L = 2\ mH$	35	—	V
		UCN-5842A	$I_{OUT} = 350\ mA$, $L = 2\ mH$	50	—	V
		UCN-5843A	$I_{OUT} = 350\ mA$, $L = 2\ mH$	50	—	V
Input Voltage	$V_{IN(0)}$	ALL		—	0.8	V
	$V_{IN(1)}$	ALL	$V_{DD} = 12\ V$	10.5	—	V
			$V_{DD} = 10\ V$	8.5	—	V
			$V_{DD} = 5.0\ V$	3.5	—	V
Input Resistance	R_{IN}	ALL	$V_{DD} = 12\ V$	50	—	kΩ
			$V_{DD} = 10\ V$	50	—	kΩ
			$V_{DD} = 5.0\ V$	50	—	kΩ
Supply Current	$I_{DD(ON)}$	ALL	All Drivers ON, $V_{DD} = 12\ V$	—	16	mA
			All Drivers ON, $V_{DD} = 10\ V$	—	14	mA
			All Drivers ON, $V_{DD} = 5.0\ V$	—	8.0	mA
	$I_{DD(OFF)}$	ALL	All Drivers OFF, $V_{DD} = 12\ V$	—	2.9	mA
			All Drivers OFF, $V_{DD} = 10\ V$	—	2.5	mA
			All Drivers OFF, $V_{DD} = 5.0\ V$	—	1.6	mA
Clamp Diode Leakage Current	I_R	UCN-5841A	$V_R = 50$	—	50	µA
		UCN-5842A	$V_R = 80\ V$	—	50	µA
		UCN-5843A	$V_R = 100\ V$	—	50	µA
Clamp Diode Forward Voltage	V_F	ALL	$I_F = 350\ mA$	—	2.0	V



TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS})

		V_{DD} = 5.0 V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C.	Minimum Data Pulse Width	150 ns
D.	Minimum Clock Pulse Width	150 ns
E.	Minimum Time Between Clock Activation and Strobe	300 ns
F.	Minimum Strobe Pulse Width	100 ns
G.	Typical Time Between Strobe Activation and Output Transition	500 ns

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial data entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

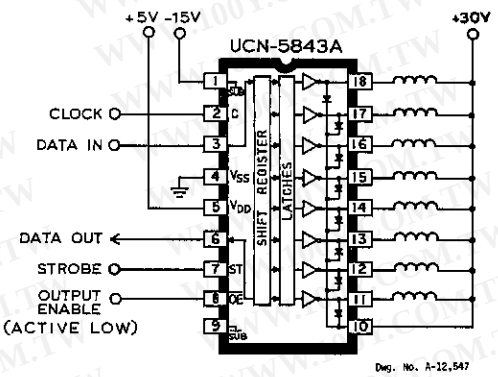
SERIES UCN-5840A TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 ..... I_8	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 ..... I_8	Output Enable	Output Contents I_1 I_2 I_3 ..... I_8
H	⎍	H R_1 R_2 ..... R_7	R_7				
L	⎍	L R_1 R_2 ..... R_7	R_7				
X	⎍	R_1 R_2 R_3 ..... R_8	R_8				
		X X X X	X	L	R_1 R_2 R_3 ..... R_8		
		P_1 P_2 P_3 ..... P_8	P_8	H	P_1 P_2 P_3 ..... P_8	L	P_1 P_2 P_3 ..... P_8
					X X X X	H	H H H ..... H

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

TYPICAL APPLICATION

RELAY/SOLENOID DRIVER



UCN-5851A/EP AND UCN-5852A/EP
BiMOS II 32-CHANNEL, SERIAL-INPUT DRIVERS
—Thin-Film Electroluminescent Display Row Drivers

FEATURES

- DMOS Outputs
- Output Breakdown >225 V
- Sink up to 120 mA
- Low-Power CMOS Inputs and Logic
- 6 MHz Data Input Rate
- Refresh and Output Enable Functions
- Replaces SN75551, SN75552

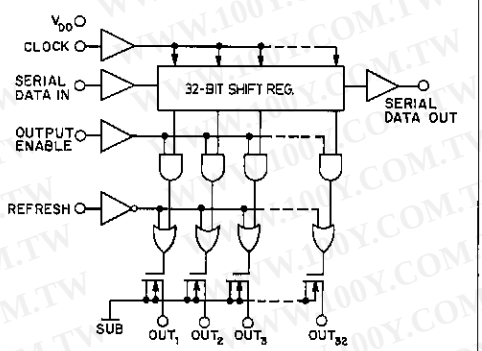
Thin-film electroluminescent display row driver applications are satisfied with the UCN-5851A/EP and UCN-5852A/EP 32-channel drivers. CMOS low-level logic, is combined with high-voltage (225 V), open-drain DMOS outputs. To facilitate pc board layout, serial data outputs run counterclockwise in the UCN-5851A/EP and clockwise in the UCN-5852A/EP.

The logic sections consist of a 32-bit shift register, refresh and output-enable gates. When both REFRESH and OUTPUT ENABLE are high, the contents of the register appears at the outputs. A serial shift register output is available to cascade shift registers. This output is not affected by the REFRESH or OUTPUT ENABLE.

The UCN-5851A and UCN-5852A are supplied in 40-pin dual in-line plastic packages with 0.600" (15.24 mm) row spacing. The UCN-5851EP and UCN-5852EP are packaged in 44-lead plastic chip carriers with 50-mil lead spacings ("J" lead bend) for surface-mount applications.

Companion TFEL column drivers are the Sprague UCN-5853A/EP and UCN-5854A/EP.

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-13,048

5

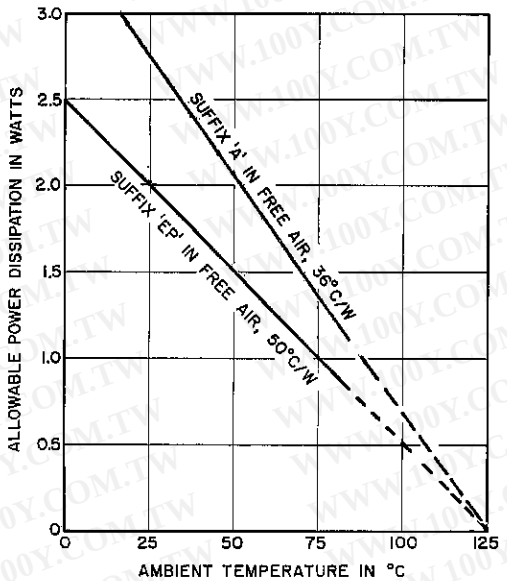
ABSOLUTE MAXIMUM RATINGS

Voltage Measurements
Referenced to Substrate

Supply Voltage, V_{DD} . . . . . 15 V
Output Voltage, V_{OUT} . . . . . 225 V
Input Voltage, V_{IN} . . . . . -0.3 V to V_{DD} $+0.3$ V
Output Current, I_{OUT} . . . . . 120 mA
Total Substrate Current, I_{SUB} . . . . . 1.5 A
Package Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . $-20°C$ to $+85°C$
Storage Temperature Range, T_S . . . $-55°C$ to $+125°C$

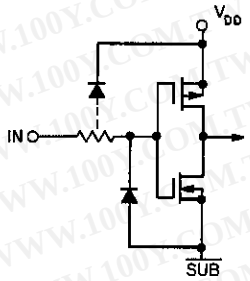
NOTE: Output current rating may be limited by duty cycle and ambient temperature (see graphs). Under any set of conditions, do not exceed the specified maximum current ratings or a junction temperature of +125°C.

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



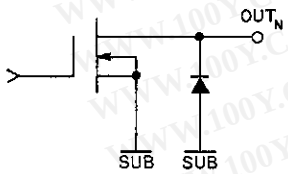
Dwg. No. A-13,033A

TYPICAL INPUT CIRCUIT



Dwg. No. A-13,039

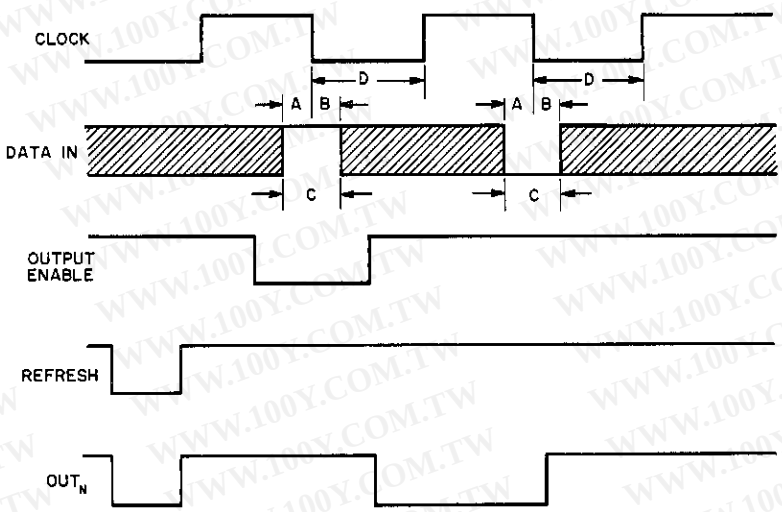
TYPICAL OUTPUT DRIVER



Dwg. No. A-13,040

ELECTRICAL CHARACTERISTICS at T_A = 0°C to +70°C, V_{DD} = 12 V, V_{SUB} = 0 (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Functional Supply Voltage Range	V_{DD}		4.5	12	15	V
Output Leakage Current	I_{OUT}	V_{OUT} = 225 V	—	—	10	μA
Output Voltage	$V_{OUT(0)}$	I_{OUT} = 20 mA, V_{DD} = 5 V	—	8.0	10	V
		I_{OUT} = 100 mA, V_{DD} = 12 V	—	15	30	V
Output Clamp Diode Voltage	V_F	I_F = 100 mA	—	1.8	2.5	V
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = −100 μA	10.5	—	—	V
	$V_{OUT(0)}$	I_{OUT} = 100 μA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	—	5.3	V
		V_{DD} = 12 V	10.5	—	12.3	V
	$V_{IN(0)}$		−0.3	—	0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = 12 V	—	—	1.0	μA
	$I_{IN(0)}$	V_{IN} = 0	—	—	−1.0	μA
Maximum Clock Frequency	f_{clk}	V_{DD} = 5.0 V	3.3	—	—	MHz
		V_{DD} = 12 V	—	7.5	—	MHz
Supply Current	I_{DD}	f_{clk} = 0	—	—	500	μA
Output Enable to Output Delay	t_{PHL}	C_L = 10 pF	—	200	500	ns
	t_{PLH}	C_L = 10 pF	—	250	500	ns
Output Fall Time	t_f	C_L = 10 pF	—	80	200	ns
Output Rise Time	t_r	C_L = 10 pF	—	300	500	ns



Dwg. No. A-13,041

TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and V_{SUB})

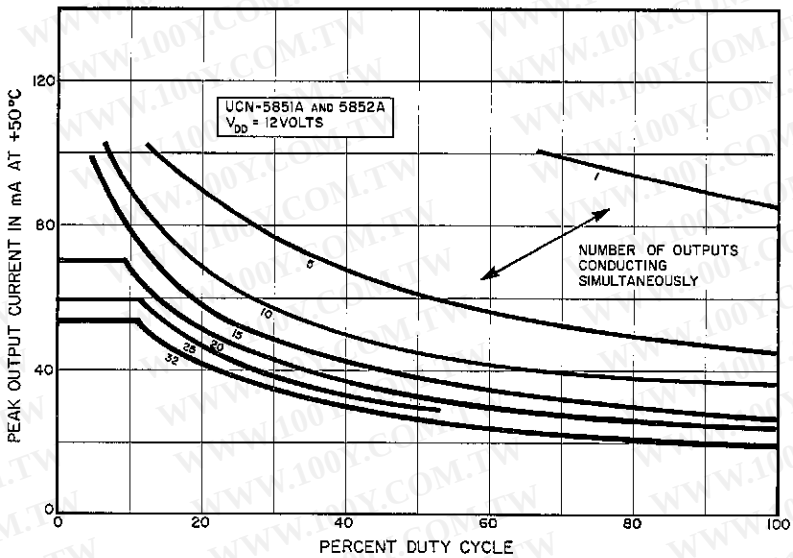
	V_{DD} = 5.0 V		V_{DD} = 12 V	
	Tested	Typ.	Typ.	Units
A. Min. Data Active Time Before Clock Pulse (Data Set-Up Time)	75	35	15	ns
B. Min. Data Active Time After Clock Pulse (Data Hold Time)	75	35	15	ns
C. Min. Clock Pulse Width	150	70	30	ns
D. Min. Clock Pulse Width	150	100	65	ns
Max. Clock Frequency	3.3	5.0	7.5	MHz

The logic section consists of a 32-bit shift register, 32 output-enable gates and 32 refresh gates. Typically, a composite row drive signal is externally generated by a high-voltage switching circuit and applied to the substrate common terminal. Serial data is entered into the shift register on the high-to-low transition of the clock input. When REFRESH is high, a high ENABLE input will allow those outputs with a high in their associated register to be turned ON, causing the corresponding row to be connected to the composite row drive signal. When the REFRESH input is low, all outputs are turned ON.

The serial data output from the shift register may be used to cascade additional devices. This output is not affected by the OUTPUT ENABLE or REFRESH inputs.

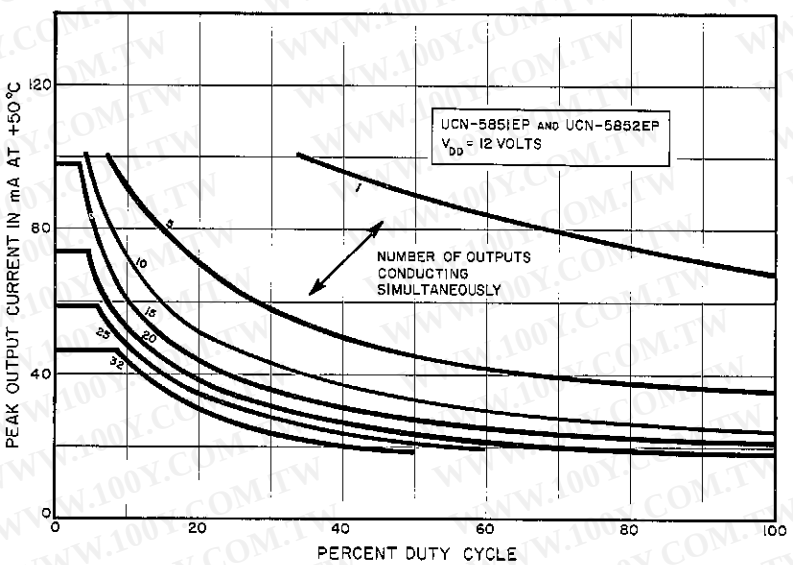
OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE

UCN-5851A AND UCN-5852A



Dwg. No. A-13,042

UCN-5851EP AND UCN-5852EP



Dwg. No. A-13,043

APPLICATIONS

Electroluminescent (EL) display panels are generally built as an X-Y matrix of rows and columns. Because of the construction of the panel, each cell, or pixel, that must be driven presents primarily a capacitive load (Fig. 1). The variable resistor models the electroluminescent effect, while the back-to-back Zener diodes account for the threshold voltage which must be reached prior to the emission of light. The EL display panel's capacitive nature requires that it be a-c driven.

REFRESH SCANNING

To be compatible with existing CRT systems, EL panels usually use a raster-scanning refresh approach. Refresh rates range from 60 Hz to 500 Hz. The higher the rate, the more power the panel consumes. At frequencies less than 500 Hz, the panel brightness varies linearly with excitation frequency (or the refresh rate).

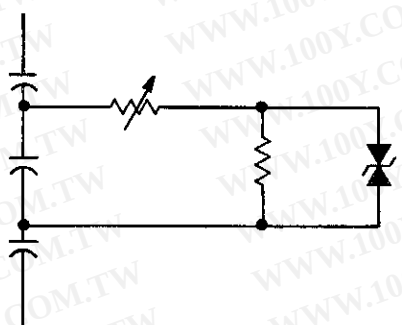
At the beginning of each scan, with the columns grounded, all rows receive a positive refresh pulse (Fig. 2) from the UCN-5851/52 row-drivers through the clamp diodes in the IC outputs (Fig. 3). Depending on the panel, the refresh-pulse voltage can be as high as +225 V.

Next, the row-driver IC is turned ON by the refresh signal so that the row-driver outputs follow the composite signal back to ground and allow the cell capacitances to discharge. Thereafter, the rows are left in a floating condition until each is selected in turn by the UCN-5851/52 to be driven to a negative potential.

The threshold voltage for light emission is reached by driving the rows negative (−160 V) and the columns positive (+50 V) relative to ground, resulting in a pixel voltage which equals the difference of the driving potentials (210 V, in this case). Individual pixel control is effected by selecting the rows one at a time and pulling high only those columns which correspond to the desired ON pixels. Higher voltage levels (to +80 V and to −225 V) will generate increased light levels.

5

EL CELL EQUIVALENT



Dwg. No. A-13,031

FIGURE 1

ENTERING THE DATA

Before a row is selected, all the data for that line must be registered and latched into the column driver's output latch. Data for subsequent lines can be clocked into the column registers as soon as the current data enters the output latches. The column drivers must be enabled during the time that the row-driver output goes negative.

A logic "1" represents an illuminated cell. Therefore, to turn a cell ON, a positive voltage is applied to the selected column. As shown in Figure 3, the −160 V on the selected row and +50 V on the selected column define the cell to be lit. The combined voltage difference of 210 V across the cell is above the electroluminescence threshold and therefore causes light generation.

APPLICATIONS

The worst-case row-driver current requirement is when all columns in a row are turned ON. If there are 256 rows and 512 columns in the panel and each cell presents a capacitance of 4 pF, then the minimum ramp time allowed is determined as follows:

$$dt = C\ dv/i$$
$$dt = (512 \times 4\ pF) \times 210\ V / 100\ mA$$
$$dt = 4.3\ \mu s$$

where 210 V is the total voltage difference between the row and the column electrodes, and 100 mA is the recommended maximum sink current. The 4.3 μs is then the minimum allowable ramp time for the composite-row driver supply voltage.

Similarly, when the positive refresh pulse is applied to all rows at the beginning of each scan, the worse-case current through the row-driver's clamp diode occurs when all the rows are at 0 V and the pulse suddenly switches to the positive refresh voltage. For a diode rating of 100 mA, the minimum allowable ramp time would again be 4.3 μs.

These minimum ramp times (dt) are smaller than those encountered in typical applications. Normally, the peak current will be lower than the 100 mA used in the examples shown and may be limited by the column driver's current capability.

The block diagram of a typical electroluminescent display, (Fig. 4), shows that the UCN-5851 row-drivers drive the odd rows and the UCN-5852 row-drivers the even rows. The odd and even rows are actuated alternately. The two drivers are identical except for the output-pin arrangements, which eliminates the need for pc board vias when connecting them to opposite sides of the panel.

Because the row-driver substrates are connected to the composite-row drive voltage (+210 V, ground, or −160 V), all clock, data, strobe, and enable signals to them must be level shifted. Optical isolators can be used very effectively. The column drivers are referenced to ground and therefore do not need such isolation.

ROW OUTPUT VOLTAGE SIGNALS

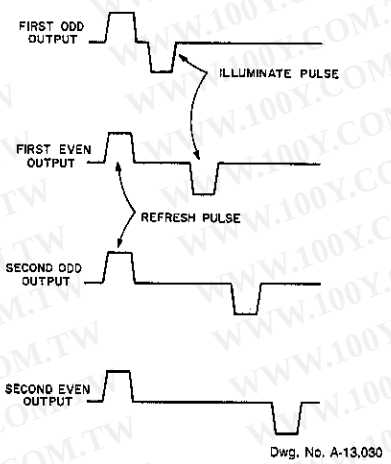


FIGURE 2

APPLICATIONS

SIMPLIFIED CELL DRIVER

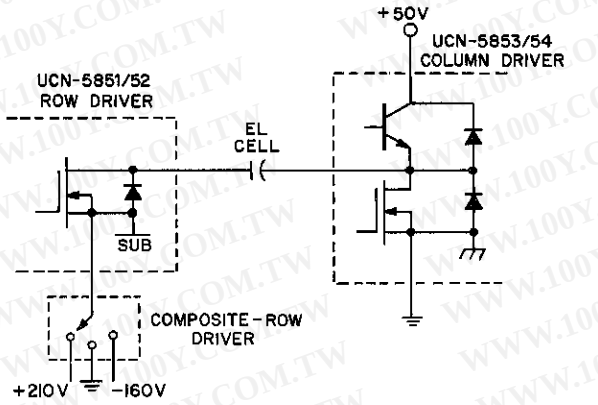


FIGURE 3

ELECTROLUMINESCENT DISPLAY

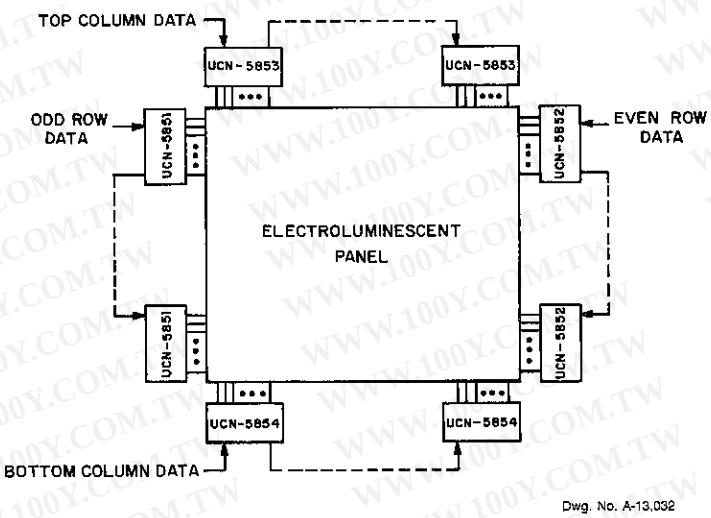


FIGURE 4

PIN DESIGNATIONS

PIN	UCN-5851A	UCN-5851EP	UCN-5852A	UCN-5852EP
1	OUT_{16}	OUT_{16}	OUT_{17}	OUT_{17}
2	OUT_{17}	OUT_{17}	OUT_{16}	OUT_{16}
3	OUT_{18}	OUT_{18}	OUT_{15}	OUT_{15}
4	OUT_{19}	OUT_{19}	OUT_{14}	OUT_{14}
5	OUT_{20}	OUT_{20}	OUT_{13}	OUT_{13}
6	OUT_{21}	OUT_{21}	OUT_{12}	OUT_{12}
7	OUT_{22}	OUT_{22}	OUT_{11}	OUT_{11}
8	OUT_{23}	OUT_{23}	OUT_{10}	OUT_{10}
9	OUT_{24}	OUT_{24}	OUT_{9}	OUT_{9}
10	OUT_{25}	OUT_{25}	OUT_{8}	OUT_{8}
11	OUT_{26}	OUT_{26}	OUT_{7}	OUT_{7}
12	OUT_{27}	OUT_{27}	OUT_{6}	OUT_{6}
13	OUT_{28}	OUT_{28}	OUT_{5}	OUT_{5}
14	OUT_{29}	OUT_{29}	OUT_{4}	OUT_{4}
15	OUT_{30}	OUT_{30}	OUT_{3}	OUT_{3}
16	OUT_{31}	OUT_{31}	OUT_{2}	OUT_{2}
17	OUT_{32}	OUT_{32}	OUT_{1}	OUT_{1}
18	SERIAL DATA OUT	SERIAL DATA OUT	SERIAL DATA OUT	SERIAL DATA OUT
19	ENABLE	NC	ENABLE	NC
20	CLOCK	NC	CLOCK	NC
21	SUBSTRATE	NC	SUBSTRATE	NC
22	V_{DD}	NC	V_{DD}	NC
23	REFRESH	ENABLE	REFRESH	ENABLE
24	SERIAL DATA IN	CLOCK	SERIAL DATA IN	CLOCK
25	NC	SUBSTRATE	NC	SUBSTRATE
26	OUT_{1}	V_{DD}	OUT_{32}	V_{DD}
27	OUT_{2}	REFRESH	OUT_{31}	REFRESH
28	OUT_{3}	SERIAL DATA IN	OUT_{30}	SERIAL DATA IN
29	OUT_{4}	NC	OUT_{29}	NC
30	OUT_{5}	OUT_{1}	OUT_{28}	OUT_{32}
31	OUT_{6}	OUT_{2}	OUT_{27}	OUT_{31}
32	OUT_{7}	OUT_{3}	OUT_{26}	OUT_{30}
33	OUT_{8}	OUT_{4}	OUT_{25}	OUT_{29}
34	OUT_{9}	OUT_{5}	OUT_{24}	OUT_{28}
35	OUT_{10}	OUT_{6}	OUT_{23}	OUT_{27}
36	OUT_{11}	OUT_{7}	OUT_{22}	OUT_{26}
37	OUT_{12}	OUT_{8}	OUT_{21}	OUT_{25}
38	OUT_{13}	OUT_{9}	OUT_{20}	OUT_{24}
39	OUT_{14}	OUT_{10}	OUT_{19}	OUT_{23}
40	OUT_{15}	OUT_{11}	OUT_{18}	OUT_{22}
41	—	OUT_{12}	—	OUT_{21}
42	—	OUT_{13}	—	OUT_{20}
43	—	OUT_{14}	—	OUT_{19}
44	—	OUT_{15}	—	OUT_{18}

UCN-5853A/EP AND UCN-5854A/EP
BiMOS II 32-CHANNEL, SERIAL-INPUT, LATCHED DRIVERS
—Thin-Film Electroluminescent Display Column Drivers

FEATURES

- Totem Pole Outputs
- High Output Breakdown
- Sink or Source up to 25 mA
- Low-Power CMOS Inputs and Logic
- 7.5 MHz Data Input Rate
- Strobe and Output Enable Functions
- Replaces SN75553 and SN75554

Thin-film electroluminescent display column driver applications are satisfied with the UCN-5853A/EP and UCN-5854A/EP BiMOS II 32-channel drivers. CMOS low-level logic, 60 V bipolar source drivers, and DMOS sink drivers are combined in a monolithic integrated circuit. To facilitate pc board layout, serial data outputs run clockwise in the UCN-5853A/EP and counterclockwise in the UCN-5854A/EP. The UCN-5853A/EP and UCN-5854A/EP are rated for operation with load voltages to 60 V. Selected devices (suffix "-1") are available for operation to 80 V.

The logic sections consist of a 32-bit shift register, 32 latches, and output enable gates. When OUTPUT ENABLE is high, the contents of the latches appear at the outputs. A serial shift register output is available to cascade shift registers. This output is not affected by the STROBE or OUTPUT ENABLE.

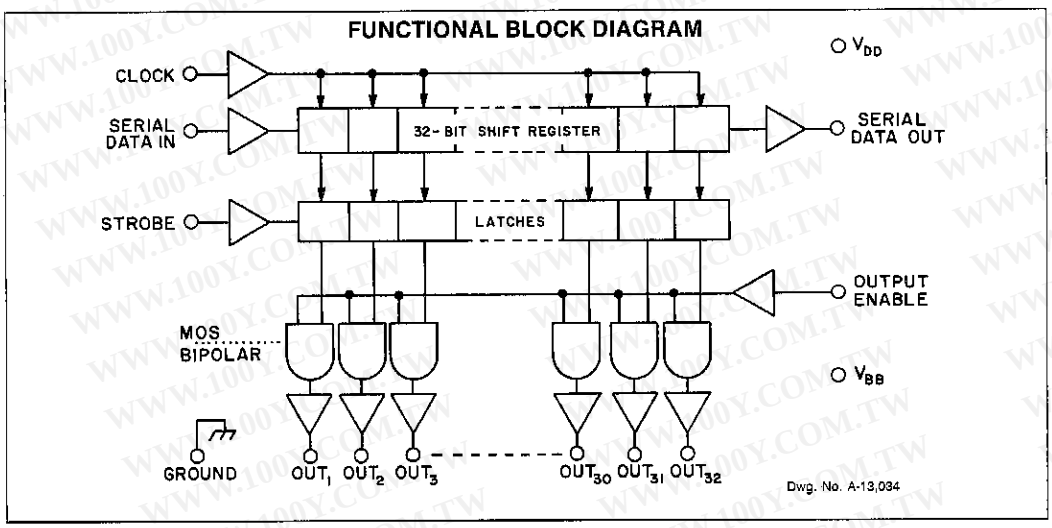
The output sections are high-voltage Darlington source drivers with DMOS sink drivers. The output configuration ensures that the output is not pulled down until the source drive has been turned OFF, eliminating the possibility of high crossover current.

The UCN-5853A and UCN-5854A are supplied in 40-pin dual in-line plastic packages with 0.600" (15.24 mm) row spacing. The UCN-5853EP and UCN-5854EP are packaged in 44-lead plastic chip carriers with 50-mil lead spacings ('J' lead bend) for surface-mount applications.

Companion TFEL row drivers are the UCN-5851A/EP and UCN-5852A/EP.

5

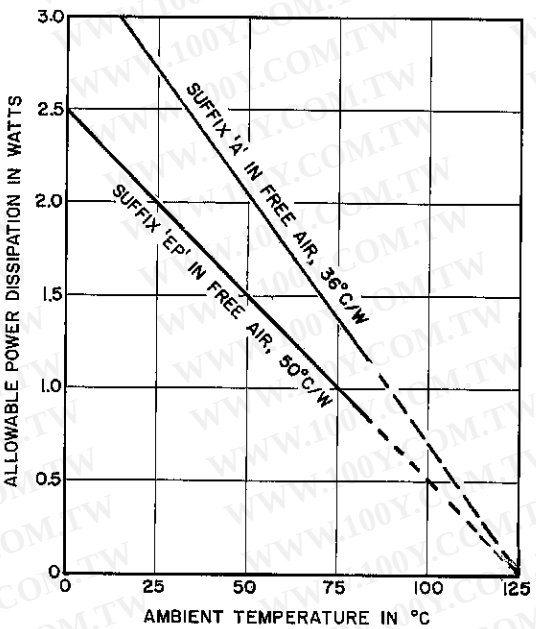
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

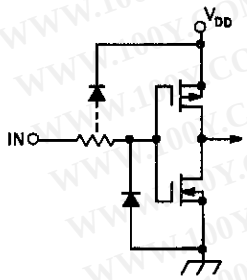
Supply Voltage, V_{DD} . . . . . 15 V
Supply Voltage, V_{BB}
(UCN-5853/54A, UCN-5853/54EP) . . . . . 60 V
(UCN-5853/54A-1, UCN-5853/54EP-1) . . . . . 80 V
Input Voltage Range, V_{IN} . . . . . -0.3 V to $V_{DD} + 0.3$ V
Output Current, I_{OUT} . . . . . ± 25 mA
Total Ground Current, I_{GND} . . . . . 700 mA
Package Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . . . . $-20°C$ to $+85°C$
Storage Temperature Range, T_S . . . . . $-55°C$ to $+125°C$

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



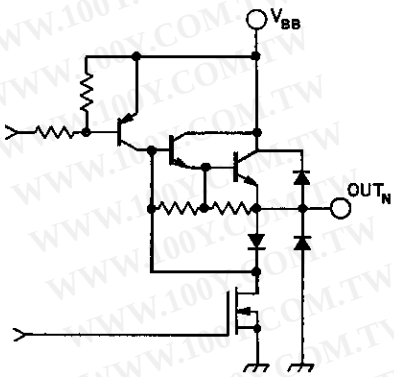
Dwg. No. A-13,033A

TYPICAL INPUT CIRCUIT



Dwg. No. A-13,035

TYPICAL OUTPUT DRIVER



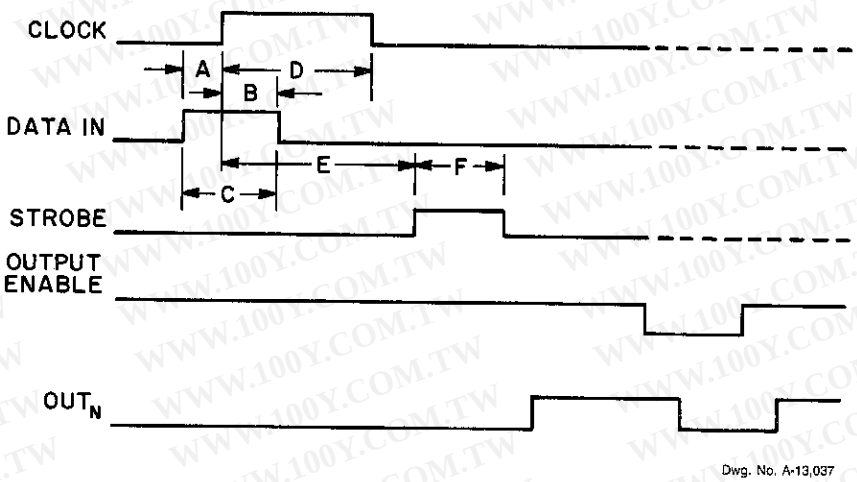
Dwg. No. A-13,036

ELECTRICAL CHARACTERISTICS at T_A = 0°C to +70°C, V_{DD} = 12 V, V_{BB} = 60 V (UCN-5853A/EP, UCN-5854A/EP) or V_{BB} = 80 V (Suffix '-1') unless otherwise specified

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Logic Supply Voltage Range	V_{DD}		4.5	12	15	V
Output Voltage	$V_{OUT(1)}$	I_{OUT} = −20 mA, V_{BB} = 60 V	57.5	—	—	V
		I_{OUT} = −20 mA, V_{BB} = 80 V*	77.5	—	—	V
	$V_{OUT(0)}$	I_{OUT} = 20 mA	—	6.0	10	V
Output Clamp Diode Voltage	V_F	I_F = 20 mA	—	2.0	2.5	V
Serial Output Voltage	$V_{OUT(1)}$	I_{OUT} = −100 µA	10.5	—	—	V
	$V_{OUT(0)}$	I_{OUT} = 100 µA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	V_{DD} = 10.8 V	10.0	—	11.1	V
		V_{DD} = 15 V	14.2	—	15.3	V
	$V_{ON(0)}$	V_{DD} = 10.8 V	−0.3	—	0.8	V
		V_{DD} = 15 V	−0.3	—	0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = 12 V	—	—	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0	—	—	−1.0	µA
Maximum Clock Frequency	f_{clk}	V_{DD} = 5.0 V	3.3	—	—	MHz
		V_{DD} = 12 V	—	7.5	—	MHz
Supply Current	I_{DD}	f_{clk} = 0, Outputs Low	—	—	0.5	mA
		f_{clk} = 0, Outputs High	—	3.0	5.0	mA
	I_{BB}	Outputs High, No Load	—	2.5	3.5	mA
		Outputs Low	—	—	0.5	mA
Output Enable to Ouput Delay	t_{PHL}	C_L = 10 pF	—	200	500	ns
	t_{PHL}	C_L = 10 pF	—	250	500	ns
Output Fall Time	t_f	C_L = 10 pF	—	80	200	ns
Output Rise Time	t_r	C_L = 10 pF	—	300	500	ns

*UCN-5853A/EP-1 and UCN-5854A/EP-1 only.

5



Dwg. No. A-13,037

TIMING CONDITIONS

(T_A = +25°C, V_{DD} = 12 V, Logic Levels are V_{DD} and Ground)

	Tested	Typ.	Units
A. Min. Data Active Time Before Clock Pulse (Data Set-Up Time)	75	15	ns
B. Min. Data Active Time After Clock Pulse (Data Hold Time)	75	15	ns
C. Min. Data Pulse Width	150	30	ns
D. Min. Clock Pulse Width	150	65	ns
E. Min. Time Between Clock Activation and Strobe	300	75	ns
F. Min. Strobe Pulse Width	100	50	ns
Max. Clock Frequency	3.3	7.5	MHz

The logic section consists of a 32-bit shift register, 32 latches, and 32 output-enable gates. Serial data is entered into the shift register on the low-to-high transition of the CLOCK input. A high STROBE input transfers the contents of the shift register to the outputs of the latches. When OUTPUT ENABLE is high, the contents of the latches appear at the outputs. The SERIAL DATA output is used to cascade shift registers. This output is not affected by STROBE or OUTPUT ENABLE.

APPLICATIONS

Electroluminescent (EL) display panels are generally built as an X-Y matrix of rows and columns. Because of the construction of the panel, each cell, or pixel, that must be driven presents primarily a capacitive load (Fig. 1). The variable resistor models the electroluminescent effect, while the back-to-back Zener diodes account for the threshold voltage which must be reached prior to the emission of light. The EL display panel's capacitive nature requires that it be a-c driven.

REFRESH SCANNING

To be compatible with existing CRT systems, EL panels usually use a raster-scanning refresh approach. Refresh rates range from 60 Hz to 500 Hz. The higher the rate, the more power the panel consumes. At frequencies less than 500 Hz, the panel brightness varies linearly with excitation frequency (or the refresh rate).

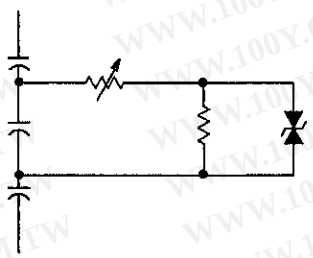
At the beginning of each scan, with the columns grounded, all rows receive a positive refresh pulse (Fig. 2) from the row-drivers through the clamp diodes in the IC outputs (Fig. 3). Depending on the panel, the refresh-pulse voltage can be as high as +225 V.

Next, the row-driver IC is turned ON by the refresh signal so that the row-driver outputs follow the composite signal back to ground and allow the cell capacitances to discharge. Thereafter, the rows are left in a floating condition until each is selected in turn by the row drivers to be driven to a negative potential.

The threshold voltage for light emission is reached by driving the rows negative (−160 V) and the columns positive (+50 V) relative to ground, resulting in a pixel voltage which equals the difference of the driving potentials (210 V, in this case). Individual pixel control is effected by selecting the rows one at a time and pulling high only those columns which correspond to the desired ON pixels. Higher voltage levels (to +80 V and to −225 V) will generate increased light levels.

5

EL CELL EQUIVALENT



Dwg. No. A-13,031

FIGURE 1

ENTERING THE DATA

Before a row is selected, all the data for that line must be registered and latched into the UCN-5853/54 column driver's output latch. Data for subsequent lines can be clocked into the column registers as soon as the current data enters the output latches. The column drivers must be enabled during the time that the row-driver output goes negative.

A logic "1" represents an illuminated cell. Therefore, to turn a cell ON, a positive voltage is applied to the selected column. As shown in Figure 3, the −160 V on the selected row and +50 V on the selected column define the cell to be lit. The combined voltage difference of 210 V across the cell is above the electroluminescence threshold and therefore causes light generation.

APPLICATIONS

The worst-case UCN-5853/54 DMOS sink driver current requirement is when all but one source driver are turned ON. That one low column driver must sink current which is a result of all the positive-going column drivers pulling all the floating rows positive. If there are 256 rows and 512 columns in the panel and each cell presents a capacitance of 4 pF, then:

$$dt = C\ dv/i$$
$$dt = (256 \times 4\ pF) \times 50\ V / 20\ mA$$
$$dt = 2.6\ \mu s$$

where 50 V is the column driver supply voltage and 20 mA is the recommended maximum current. The 2.6 μs is then the minimum allowable ramp-up time for the column-driver supply voltage.

Similarly, the worst-case source driver current requirement is when all sink drivers but one are turned ON. For a −20 mA recommended maximum source current, the minimum allowable ramp time would again be 2.6 μs.

These minimum ramp times (dt) are smaller than those encountered in typical applications.

The block diagram of a typical electroluminescent display is shown in Fig. 4. The UCN-5853 drive the top columns and UCN-5854 drive the bottom columns. They are actuated alternately. The two drivers are identical except for the output-pin arrangements, which eliminates the need for pc board vias when connecting them to opposite sides of the panel.

ROW OUTPUT-VOLTAGE SIGNALS

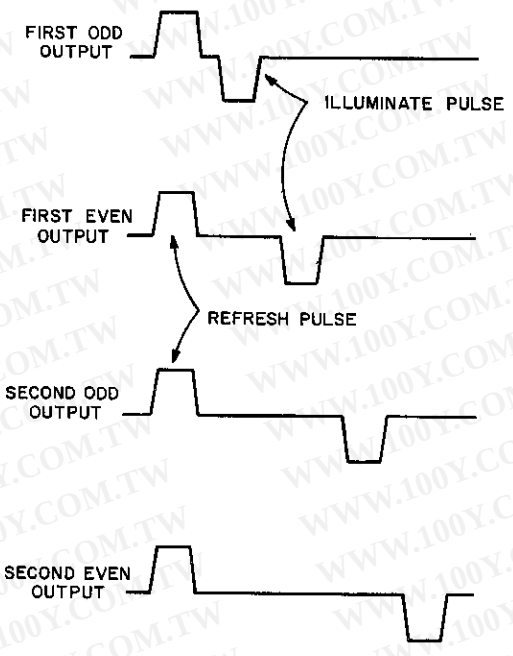


FIGURE 2

Dwg. No. A-13,030

APPLICATIONS

SIMPLIFIED CELL DRIVER

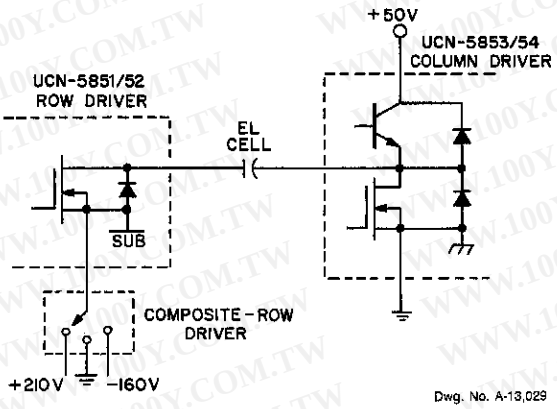


FIGURE 3

ELECTROLUMINESCENT DISPLAY

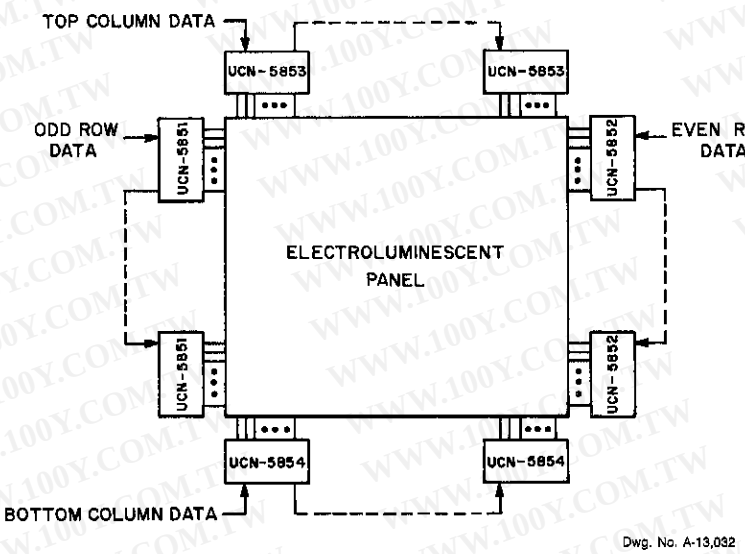


FIGURE 4

PIN DESIGNATIONS

PIN	UCN-5853A	UCN-5853EP	UCN-5854A	UCN-5854EP
1	OUT_{17}	OUT_{17}	OUT_{16}	OUT_{16}
2	OUT_{16}	OUT_{16}	OUT_{17}	OUT_{17}
3	OUT_{15}	OUT_{15}	OUT_{18}	OUT_{18}
4	OUT_{14}	OUT_{14}	OUT_{19}	OUT_{19}
5	OUT_{13}	OUT_{13}	OUT_{20}	OUT_{20}
6	OUT_{12}	OUT_{12}	OUT_{21}	OUT_{21}
7	OUT_{11}	OUT_{11}	OUT_{22}	OUT_{22}
8	OUT_{10}	OUT_{10}	OUT_{23}	OUT_{23}
9	OUT_{9}	OUT_{9}	OUT_{24}	OUT_{24}
10	OUT_{8}	OUT_{8}	OUT_{25}	OUT_{25}
11	OUT_{7}	OUT_{7}	OUT_{26}	OUT_{26}
12	OUT_{6}	OUT_{6}	OUT_{27}	OUT_{27}
13	OUT_{5}	OUT_{5}	OUT_{28}	OUT_{28}
14	OUT_{4}	OUT_{4}	OUT_{29}	OUT_{29}
15	OUT_{3}	OUT_{3}	OUT_{30}	OUT_{30}
16	OUT_{2}	OUT_{2}	OUT_{31}	OUT_{31}
17	OUT_{1}	OUT_{1}	OUT_{32}	OUT_{32}
18	SERIAL DATA OUT	SERIAL DATA OUT	SERIAL DATA OUT	SERIAL DATA OUT
19	CLOCK	IC*	CLOCK	IC*
20	GROUND	NC	GROUND	NC
21	V_{BB}	NC	V_{BB}	NC
22	V_{DD}	CLOCK	V_{DD}	CLOCK
23	STROBE	GROUND	STROBE	GROUND
24	SERIAL DATA IN	V_{BB}	SERIAL DATA IN	V_{BB}
25	OUTPUT ENABLE	V_{DD}	OUTPUT ENABLE	V_{DD}
26	OUT_{32}	STROBE	OUT_{1}	STROBE
27	OUT_{31}	SERIAL DATA IN	OUT_{2}	SERIAL DATA IN
28	OUT_{30}	OUTPUT ENABLE	OUT_{3}	OUTPUT ENABLE
29	OUT_{29}	NC	OUT_{4}	NC
30	OUT_{28}	OUT_{32}	OUT_{5}	OUT_{1}
31	OUT_{27}	OUT_{31}	OUT_{6}	OUT_{2}
32	OUT_{26}	OUT_{30}	OUT_{7}	OUT_{3}
33	OUT_{25}	OUT_{29}	OUT_{8}	OUT_{4}
34	OUT_{24}	OUT_{28}	OUT_{9}	OUT_{5}
35	OUT_{23}	OUT_{27}	OUT_{10}	OUT_{6}
36	OUT_{22}	OUT_{26}	OUT_{11}	OUT_{7}
37	OUT_{21}	OUT_{25}	OUT_{12}	OUT_{8}
38	OUT_{20}	OUT_{24}	OUT_{13}	OUT_{9}
39	OUT_{19}	OUT_{23}	OUT_{14}	OUT_{10}
40	OUT_{18}	OUT_{22}	OUT_{15}	OUT_{11}
41	—	OUT_{21}	—	OUT_{12}
42	—	OUT_{20}	—	OUT_{13}
43	—	OUT_{19}	—	OUT_{14}
44	—	OUT_{18}	—	OUT_{15}

*Internal Connection. Must be connected to V_{DD}

UCN-5857A/EP AND UCN-5859A/EP
32-OUTPUT 8-BIT ADDRESSABLE DRIVERS

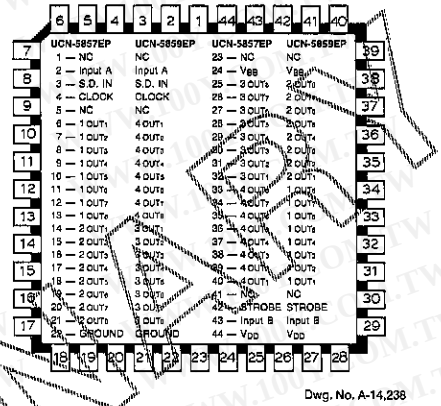
FEATURES

- 32 Totem Pole Outputs
- Output Breakdown of 100 V
- Output Current of ±20 mA
- Low-Power CMOS Logic
- Output Clamping Diodes

UCN-5857A/EP and UCN-5859A/EP are 8-bit addressable shift register drivers with 32-output capability. They employ totem pole outputs capable of maintaining an OFF voltage of 100 V and an ON current of ±20 mA. The devices include a two-line to four-line decoder that determines which set of outputs is controlled by the on-board eight-bit shift register.

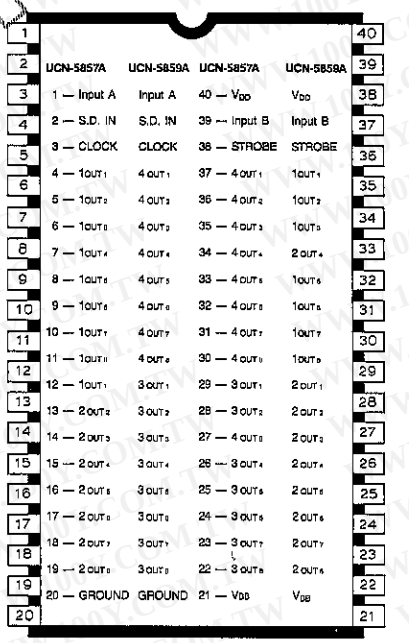
A low on the input will result in a high on the output. A high on the input will result in a low on the output. Outputs of this device are normally low. When the STROBE input is held low, outputs are controlled by the state of the shift register. When the STROBE is held high, all outputs remain low and are unaffected by the register contents. Output clamping for sink and source have been incorporated to guard against high and low transients.

These devices are furnished in a 40-pin dual in-line plastic package with 600-mil row centers or in a 44-pin plastic leaded chip carrier with 50-mil spacings (J lead bend) for surface-mount applications.



Dwg. No. A-14,238

PACKAGE 'EP'



Dwg. No. A-14,239

PACKAGE 'A'

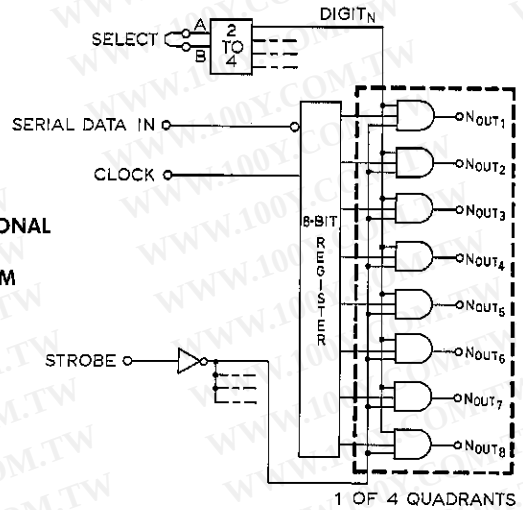
NOTE: S.D. IN = SERIAL DATA IN

ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

Output Voltage, V_{CE} ..... 100 V
Output Supply Voltage, V_{BB} ..... 100 V
Logic Supply Voltage, V_{DD} ..... 15 V
Output Current, I_{OUT} ..... ±20 mA
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD}+0.3 V
Package Power Dissipation, P_D ('A' Package) ..... 2.8 W*
('EP' Package) ..... 2.0 W*
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +125°C

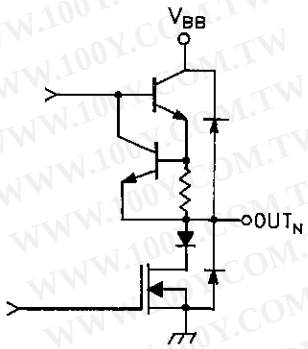
*Derate linearly to 0 W at T_A = +125°C

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-14,240

TYPICAL OUTPUT DRIVER



Dwg. No. A-14,241

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{BB} = 100 V, V_{DD} = 5 V (unless otherwise noted)

Characteristic	Symbol	Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{BB} = 100 V, V_{OUT} = 0 V	—	—	−100	µA
		V_{BB} = V_{OUT} = 100 V	—	—	100	µA
Output Saturation Voltage	$V_{OUT(1)}$	I_{OUT} = −1.0 mA	98	—	—	V
		I_{OUT} = −10 mA	97	—	—	V
		I_{OUT} = −15 mA	96	—	—	V
	$V_{OUT(0)}$	I_{OUT} = 1.0 mA, V_{DD} = 12 V	—	—	20	V
		I_{OUT} = 10 mA, V_{DD} = 12 V	—	—	4.0	V
		I_{OUT} = 15 mA, V_{DD} = 12 V	—	—	5.0	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	—	V
		V_{DD} = 10 V	8.5	—	—	V
		V_{DD} = 5.0 V	3.5	—	—	V
Input Resistance	R_{IN}	V_{DD} = 5.0 V to 12 V	1.0	—	—	MΩ
Supply Current	$I_{DD(LOW)}$	V_{DD} = 12 V, All outputs low	—	—	1.0	mA
	$I_{DD(HIGH)}$	V_{DD} = 12 V, 8 outputs high	—	—	1.0	mA
Output Clamp Voltage	$V_{OUT(CLAMP)}$	I_{OUT} = 20 mA	—	—	102.5	V
		I_{OUT} = −20 mA	—	—	−2.5	V
Output Short-Circuit Current	I_{SC}		—	—	−20	mA
High-Voltage Supply Current	$I_{BB(LOW)}$	V_{DD} = 12 V, All outputs low	—	—	1.0	mA
	$I_{BB(HIGH)}$	V_{DD} = 12 V, 8 outputs high	—	—	3.0	mA

UCN-5858A/EP AND UCN-5860A/EP
32-BIT SHIFT REGISTER/DRIVERS

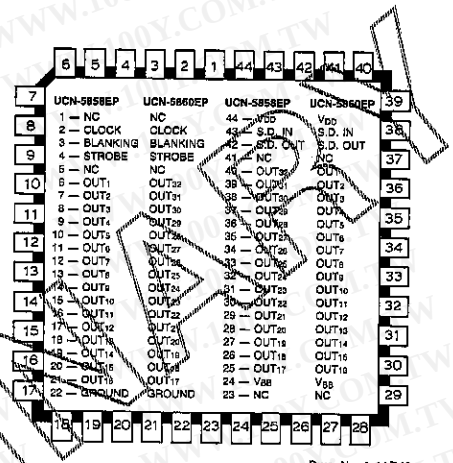
FEATURES

- 32 Totem Pole Outputs
- Output Breakdown of 100 V
- Output Current of ±20 mA
- Low-Power CMOS Logic
- Output Clamping Diodes
- UCN-5858 Replaces SN75501D

The UCN-5858A/EP and UCN-5860A/EP 32-channel shift register/drivers are used as row drivers for AC plasma displays. These devices are capable of maintaining an output OFF voltage of 100 V and an output ON current of ±20 mA. Outputs are totem pole design.

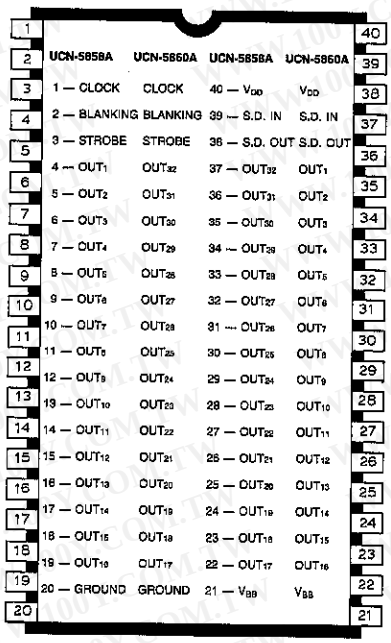
Output clamping for source and sink have been incorporated to guard against high and low transients. A low input will result in a low output. A high input will result in a high output. Outputs are controlled by their inputs when STROBE is low and BLANKING is high. When BLANKING is low, all outputs are low and unaffected by the register contents or STROBE. When STROBE is high, all outputs are unaffected by the register and are forced high (BLANKING held high).

These devices are furnished in a 40-pin dual in-line plastic package with 600-mil row centers ("A" package) or in a 44-pin plastic leaded chip carrier with 50-mil spacings for surface-mount applications.



Dwg. No. A-14,242

PACKAGE 'EP'



Dwg. No. A-14,243

PACKAGE 'A'

NOTE: S.D. IN = SERIAL DATA IN

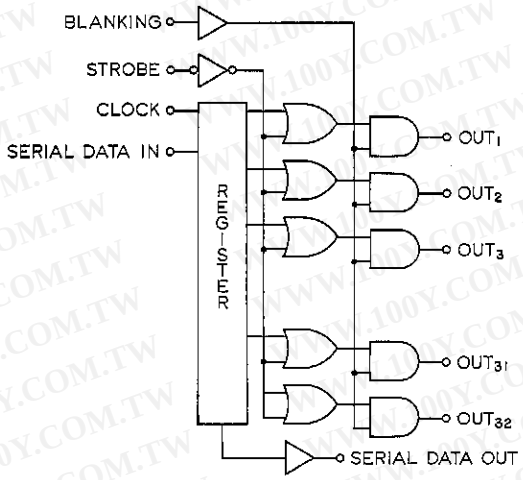
ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

Output Voltage, V_{CE} ..... 100 V
Output Supply Voltage, V_{BB} ..... 100 V
Logic Supply Voltage, V_{DD} ..... 15 V
Output Current, I_{OUT} ..... ±20 mA
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} +0.3 V
Package Power Dissipation, P_D ('A' Package) ..... 2.8 W*
('EP' Package) ..... 2.0 W*
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +125°C

*Derate linearly to 0 W at T_A = +125°C

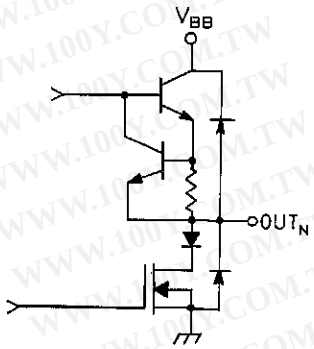
5

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-14,244

TYPICAL OUTPUT DRIVER



Dwg. No. A-14,241

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V_{BB} = 100$ V, $V_{DD} = 5$ V (unless otherwise noted)

Characteristic	Symbol	Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{BB} = 100$ V, $V_{OUT} = 0$ V	—	—	−100	μA
		$V_{BB} = V_{OUT} = 100$ V	—	—	100	μA
Output Saturation Voltage	$V_{OUT(1)}$	$I_{OUT} = -1.0$ mA	98	—	—	V
		$I_{OUT} = -10$ mA	97	—	—	V
		$I_{OUT} = -15$ mA	96	—	—	V
	$V_{OUT(0)}$	$I_{OUT} = 1.0$ mA, $V_{DD} = 12$ V	—	—	2.0	V
		$I_{OUT} = 10$ mA, $V_{DD} = 12$ V	—	—	4.0	V
		$I_{OUT} = 15$ mA, $V_{DD} = 12$ V	—	—	5.0	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	$V_{DD} = 12$ V	10.5	—	—	V
		$V_{DD} = 10$ V	8.5	—	—	V
		$V_{DD} = 5.0$ V	3.5	—	—	V
Input Resistance	R_{IN}	$V_{DD} = 5.0$ V to 12 V	1.0	—	—	MΩ
Supply Current	$I_{DD(LOW)}$	$V_{DD} = 12$ V, All outputs low	—	—	1.0	mA
	$I_{DD(HIGH)}$	$V_{DD} = 12$ V, 8 outputs high	—	—	1.0	mA
Output Clamp Voltage	$V_{OUT(CLAMP)}$	$I_{OUT} = 20$ mA	—	—	102.5	V
		$I_{OUT} = -20$ mA	—	—	−2.5	V
Output Short-Circuit Current	I_{SC}		—	—	−20	mA
High-Voltage Supply Current	$I_{BB(LOW)}$	$V_{DD} = 12$ V, All outputs low	—	—	1.0	mA
	$I_{BB(HIGH)}$	$V_{DD} = 12$ V, 8 outputs high	—	—	15	mA

UCN-5881EP
BiMOS II DUAL 8-BIT LATCHED DRIVER
With Read Back

FEATURES

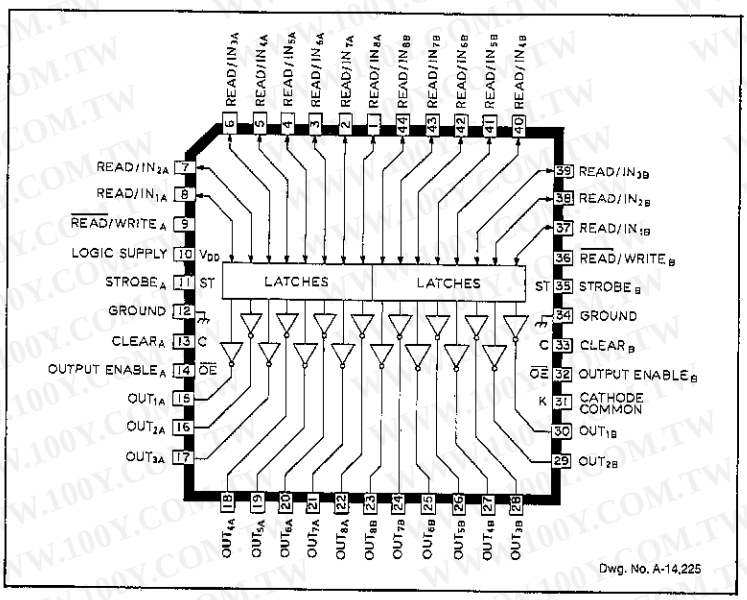
- 4.4 MHz Minimum Data Input Rate
- Low-Power CMOS Logic
- 20 V, 50 mA (Max.) Outputs
- Transient-Protected Outputs
- Thermal Shutdown Protection
- Low-Profile Leaded Chip Carrier

With 16 CMOS data latches (two sets of eight), CMOS control circuitry for each set of latches, and a bipolar saturated driver for each latch, the UCN-5881EP provides low-power interface with maximum flexibility. The driver includes thermal shutdown circuitry to protect against damage from high junction temperatures and clamp diodes for inductive load transient suppression.

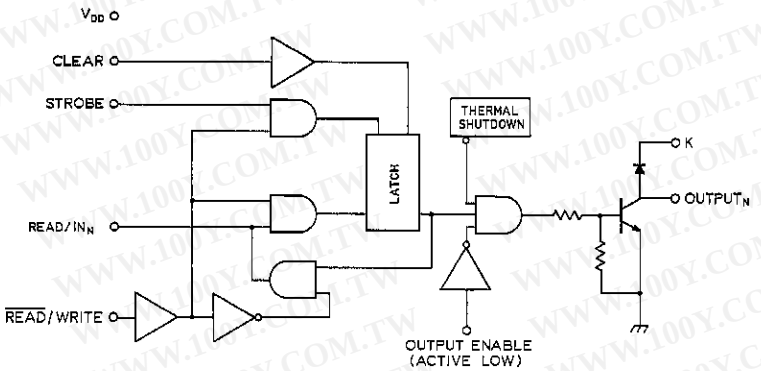
The CMOS inputs cause minimal circuit loading and are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull up resistors. When reading back, the data inputs will sink 8 mA (if its corresponding latch is low) or source 400 μA (if its corresponding latch is high). The read back feature is for error checking. It allows the system to verify that data has been received and latched.

The bipolar outputs are suitable for use with low-power relays, solenoids, and stepping motors. The very-low output saturation voltage makes this device well-suited for driving LED arrays. The output transistors are capable of sinking 50 mA and will maintain at least 20 V in the OFF state. Outputs may be paralleled for higher current capability.

The UCN-5881EP dual 8-bit latched sink driver is complemented by the UCN-5882EP dual 8-bit latched source driver. It is rated for operation over the temperature range of −20°C to +85°C and is supplied in a plastic 44-lead chip carrier conforming to the JEDEC MS-007AB outline.



FUNCTIONAL BLOCK DIAGRAM
(1 of 16 Channels)

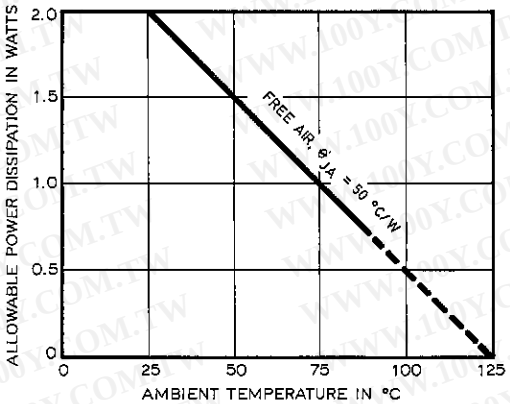


Dwg. No. A-14,227

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{OUT} . . . . . 20 V
Output Sustaining Voltage, $V_{CE(sus)}$ . . . . . 15 V
Output Current, I_{OUT} . . . . . 50 mA
Input Voltage Range, V_{IN} . . . . . -0.3 V to $V_{DD} + 0.3$ V
Logic Supply Voltage, V_{DD} . . . . . 15 V
Package Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . . . . $-20°C$ to $+85°C$
Storage Temperature Range, T_S . . . . . $-55°C$ to $+125°C$

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



Dwg. No. A-14,226

TRUTH TABLE

Read/In	Strobe	Clear	Output Enable	Read/Write	Latch Contents	Output
X	X	X	1	X	X	OFF
0	1	0	0	1	0	OFF
1	1	0	0	1	1	ON
X	0	0	0	1	n-1	n-1
X	X	1	X	X	0	OFF
n	X	0	X	0	n	n

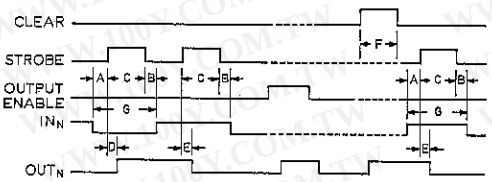
n = Present Latch Contents
n-1 = Previous Latch Contents

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V_{DD} = 5\ V$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 20\ V$	—	50	μA
Output Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 10\ mA$	—	0.1	V
		$I_{OUT} = 25\ mA$	—	0.5	V
Output Sustaining Voltage	$V_{CE(sus)}$	$I_{OUT} = 25\ mA$, $L = 2\ mH$	15	—	V
Input Voltage	$V_{IN(0)}$		−0.3	0.8	V
	$V_{IN(1)}$		3.5	5.3	V
Input Current	$I_{IN(0)}$	$V_{IN} = 0.8\ V$	—	−10	μA
	$I_{IN(1)}$	$V_{IN} = 5\ V$	—	10	μA
Readback Output Voltage	$V_{OUT(1)}$	$I_{OUT} = -400\ \mu A$	3.5	—	V
	$V_{OUT(0)}$	$I_{OUT} = 5.0\ mA$	—	0.8	V
Logic Supply Current	I_{DD}	All Drivers ON	—	12	mA
		All Drivers OFF	—	3.0	mA
Clamp Diode Leakage Current	I_R	$V_R = 20\ V$	—	50	μA
Clamp Diode Forward Voltage	V_F	$I_F = 50\ mA$	—	1.5	V

TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)



Dwg. No. A-14,226

A high on the $\overline{\text{READ}}$/WRITE input allows the circuit to accept data in. Information then present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

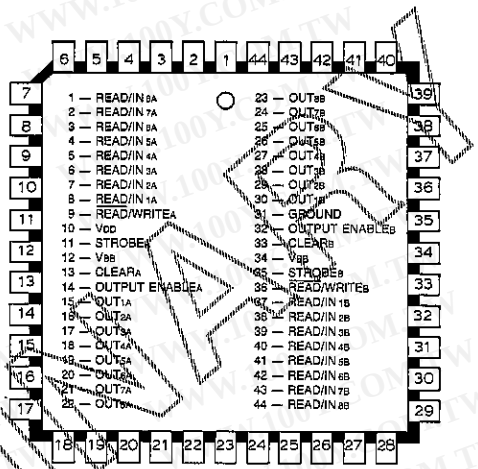
A low on the $\overline{\text{READ}}$/WRITE input will allow the latched data to be read back on the data input lines. The read back feature is for error checking applications and allows the system to verify that data has been received and latched.

	$V_{DD} = 5.0\ V$
A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time)	50 ns
B. Minimum Data Active Time After Strobe Disabled (Data Hold Time)	50 ns
C. Minimum Strobe Pulse Width	150 ns
D. Typical Time Between Strobe Activation and Output ON to OFF transition	500 ns
E. Typical Time Between Strobe Activation and Output OFF to ON transition	500 ns
F. Minimum Clear Pulse Width	225 ns
G. Minimum Data Pulse Width	125 ns

UCN-5882EP
BiMOS II DUAL 8-BIT LATCHED SOURCE DRIVER
With Read Back

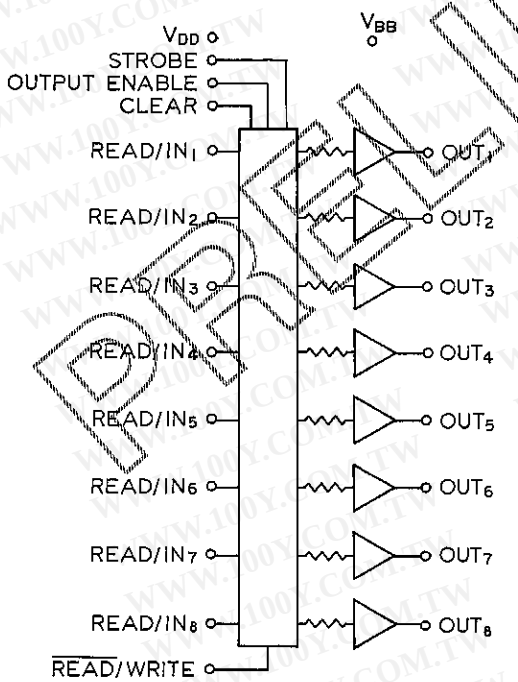
FEATURES

- READ/WRITE Inputs
- STROBE, CLEAR, OUTPUT ENABLE Functions
- Low-Power CMOS Logic
- 20 V, 50 mA Outputs
- Transient-Protected Outputs
- Thermal Shutdown Protection
- Low-Profile Leaded Chip Carrier



Dwg. No. A-14,248

FUNCTIONAL BLOCK DIAGRAM
½ UCN-5882EP



Dwg. No. A-14,247

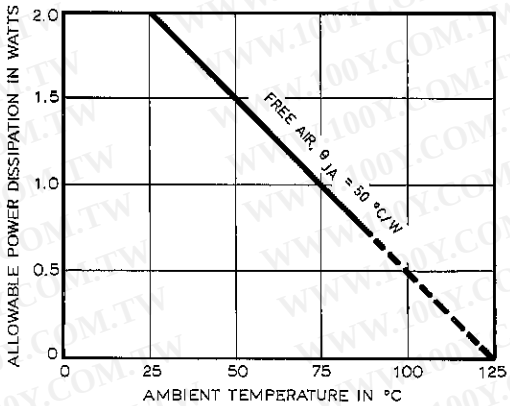
The UCN-5882EP has 16 CMOS data latches (two sets of eight), a bipolar non-Darlington driver for each latch, and CMOS control circuitry for two sets of common CLEAR, STROBE, and OUTPUT ENABLE functions. The bipolar/MOS combination provides low-power interface with maximum flexibility. The UCN-5882EP includes thermal shutdown to protect against thermal damage and has read back capabilities.

The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with low-power relays, solenoids, stepping motors, and LEDs.

ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

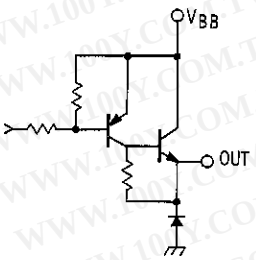
Output Voltage, V_{OUT}	20 V
Output Current, I_{OUT}	−50 mA
Input Voltage, V_{IN}	−0.3 V to V_{DD} + 0.3 V
Logic Supply Voltage, V_{DD}	15 V
Package Power Dissipation, P_D	See Graph
Junction Temperature, T_J	+125°C
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +125°C

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



Dwg. No. A-14,226

SOURCE DRIVER



Dwg. No. A-12,655

TRUTH TABLE

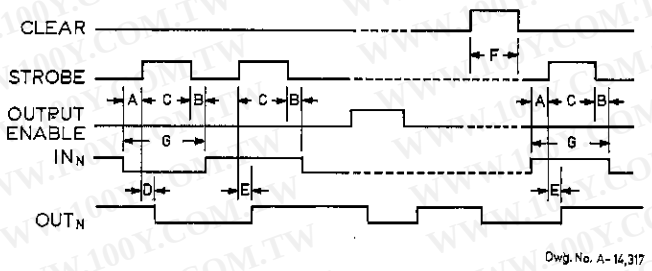
Read/In	Strobe	Clear	Output Enable	$\overline{\text{Read}}$/ Write	Latch Contents	Output
X	X	X	1	X	X	OFF
0	1	0	0	1	0	OFF
1	1	0	0	1	1	ON
X	0	0	0	1	n-1	n-1
X	X	1	X	X	0	OFF
n	X	0	X	0	n	n

n = Present Latch Contents.
n-1 = Previous Latch Contents.

5

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = 5 V, V_{BB} = 20 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V	—	50	µA
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = −25 mA	—	1.0	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = −25 mA, L = 2 mH	15	—	V
Input Voltage	$V_{IN(0)}$		−0.3	0.8	V
	$V_{IN(1)}$		3.5	5.3	V
Input Current	$I_{IN(0)}$	V_{IN} = 0.8 V	—	−10	µA
	$I_{IN(1)}$	V_{IN} = 5 V	—	10	µA
Read Back Output Voltage	$V_{OUT(1)}$	I_{OUT} = −400 µA	3.5	—	V
	$V_{OUT(0)}$	I_{OUT} = 5.0 mA	—	0.8	V
Logic Supply Current	I_{DD}		—	2.0	mA
Load Supply Current	I_{BB}	All Drivers ON, No Load	—	15	mA
		All Drivers OFF	—	50	µA
Clamp Diode Leakage Current	I_R	V_R = 20 V	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 50 mA	—	1.5	V



TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

	V_{DD} = 5.0 V
A. Minimum Data Active Time before Strobe Enabled (Data Set-Up Time)	50 ns
B. Minimum Data Active Time after Strobe Disabled (Data Hold Time)	50 ns
C. Minimum Strobe Pulse Width	150 ns
D. Typical Time Between Strobe Activation and Output ON to OFF Transition	6.0 μs
E. Typical Time Between Strobe Activation and Output OFF to ON Transition	500 ns
F. Minimum Clear Pulse Width	225 ns
G. Minimum Data Pulse Width	125 ns

A high on the $\overline{\text{READ}}$/WRITE input allows the circuit to accept data in. Information then present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their latches.

A low on the $\overline{\text{READ}}$/WRITE input will allow the latched data to be read back on the data input lines. The read back feature is for error checking applications and allows the system to verify that date has been received and latched.

UCN-5890A/B AND UCN-5891A/B BiMOS II 8-BIT, SERIAL-INPUT, LATCHED SOURCE DRIVERS

FEATURES

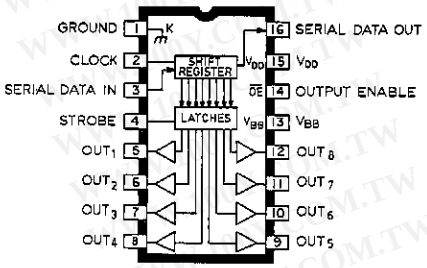
- 50 V or 80 V Source Outputs
- Output Current to −500 mA
- Output Transient-Suppression Diodes
- 3.3 MHz Minimum Data-Input Rate
- Low-Power CMOS Logic and Latches

PRIMARILY DESIGNED for use with thermal or electromagnetic printers, the UCN-5890A/B and UCN-5891A/B BiMOS II serial-input, latched drivers combine an 8-bit CMOS register, associated latches, and control circuitry (strobe and output enable) with Darlington sourcing outputs. They may also be used with relays or multiplexed LED displays within their output limitation of −500 mA per driver.

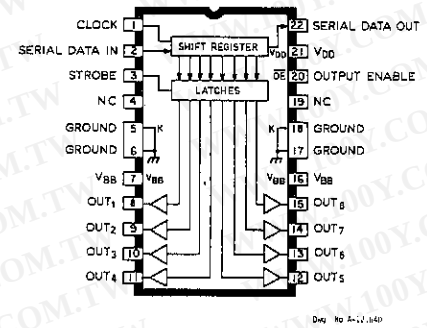
Suffix "A" devices are supplied in a standard 16-pin dual in-line plastic package. Complementary, 8-bit serial-input latched sink drivers are in Series UCN-5820A, described in Engineering Bulletin 26185.12. Suffix "B" devices are furnished in a 22-pin dual in-line package with heat-sink contact tabs that allows increased package power dissipation.

Electrical ratings for the four devices are identical except for allowable load voltage ratings. UCN-5890A and UCN-5890B are rated for operation with supply voltages of 20 V to 80 V and a minimum output sustaining voltage of 50 V. For applications using supply voltages of 20 V to 50 V (35 V sustaining), lower-cost UCN-5890A-2 and UCN-5890B-2 are recommended. The UCN-5891A and UCN-5891B are optimized for operation with supply voltages of 5 V to 50 V (35 V sustaining). A similar driver (featuring reduced output-saturation voltage), the UCN-5895A, is described in Engineering Bulletin 26182.14.

BiMOS II devices have much higher data-input rates than the original BiMOS circuits. With a 5 V supply, they will typically operate above 5 MHz. At 12 V, significantly higher speeds are obtained.



UCN-5890A
UCN-5891A



UCN-5890B
UCN-5891B

The CMOS inputs provide for minimum loading and are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors to ensure a proper input-logic high. A CMOS serial data output allows cascading these devices in multiple drive-line applications required by many dot matrix, alphanumeric, and bar graph displays.

All devices are rated for continuous operation over the temperature range of −20°C to +85°C. Because of limitations on package power dissipation, the simultaneous operation of all output drivers may require a reduction in duty cycle.

5

ABSOLUTE MAXIMUM RATINGS at $T_A = +25°C$

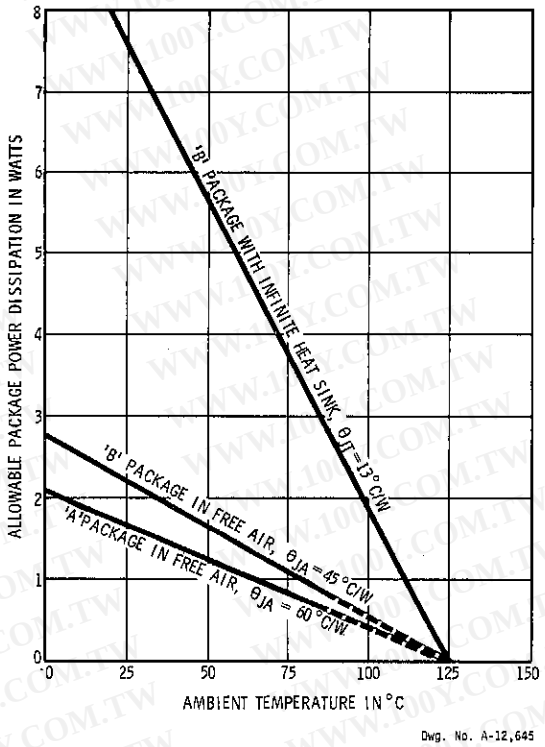
Output Voltage, V_{OUT} (UCN-5890A/B) . . . . . 80 V
(UCN-5890A/B-2) . . . . . 50 V
(UCN-5891A/B) . . . . . 50 V
Logic Supply Voltage Range, V_{DD} . . . . . 4.5 V to 15 V
Driver Supply Voltage Range, V_{BB}
(UCN-5890A/B) . . . . . 20 V to 80 V
(UCN-5890A/B-2) . . . . . 20 V to 50 V
(UCN-5891A/B) . . . . . 5.0 to 50 V
Input Voltage Range, V_{IN} . . . . . -0.3 V to $V_{DD} + 0.3$ V
Continuous Output Current, I_{OUT} . . . . . -500 mA
Allowable Package Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . . . . $-20°C$ to $+85°C$
Storage Temperature Range, T_S . . . . . $-55°C$ to $+125°C$

Caution: Sprague Electric CMOS devices have input static protection, but are susceptible to damage when exposed to extremely high static electrical charges.

Number of Outputs ON at $I_{OUT} = -200$ mA	Max. Allowable Duty Cycle at T_A of					
	50°C	60°C	70°C	50°C	60°C	70°C
	Package "A"			Package "B"		
8	40%	34%	28%	53%	46%	39%
7	45%	39%	33%	60%	52%	44%
6	53%	46%	39%	70%	61%	51%
5	63%	55%	46%	84%	73%	62%
4	79%	68%	58%	100%	91%	77%
3	100%	91%	77%	100%	100%	100%
2	100%	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%	100%

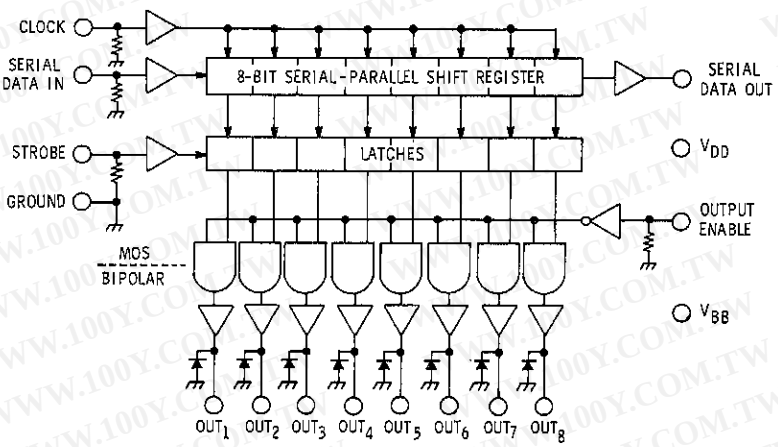
Also see Allowable Output Current graphs

ALLOWABLE AVERAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



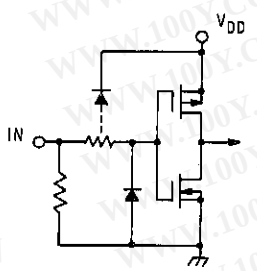
Dwg. No. A-12,645

FUNCTIONAL BLOCK DIAGRAM



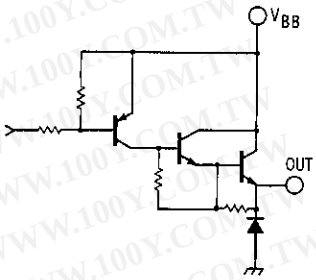
Dwg. No. A-12,654

TYPICAL INPUT CIRCUIT



Dwg. No. A-12,520

TYPICAL OUTPUT DRIVER

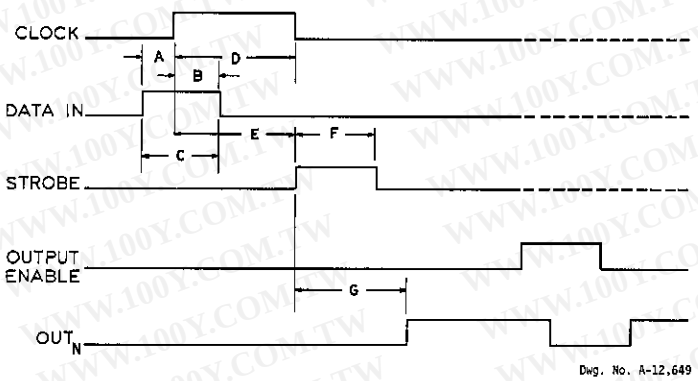


Dwg. No. A-12,648

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{BB} = 80$ V (UCN-5890A/B) or 50 V (UCN-5890A/B-2 & UCN-5891A/B), $V_{DD} = 5$ V to 12 V (unless otherwise noted)

Characteristic	Symbol	V_{BB}	Test Conditions	Limits		
				Min.	Max.	Units
Output Leakage Current	I_{CEX}	Max.	$T_A = +25°C$	—	−50	µA
			$T_A = +70°C$	—	−100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	50 V	$I_{OUT} = -100$ mA	—	1.8	V
			$I_{OUT} = -225$ mA	—	1.9	V
			$I_{OUT} = -350$ mA	—	2.0	V
Output Sustaining Voltage	$V_{CE(sus)}$	Max.	$I_{OUT} = -350$ mA, L = 2 mH, UCN-5890A/B-2 & UCN-5891A/B	35	—	V
			$I_{OUT} = -350$ mA, L = 2 mH, UCN-5890A & UCN-5890B only	50	—	V
Input Voltage	$V_{IN(1)}$	50 V	$V_{DD} = 5.0$ V	3.5	5.3	V
			$V_{DD} = 12$ V	10.5	12.3	V
	$V_{IN(0)}$	50 V	$V_{DD} = 5$ V to 12 V	−0.3	+0.8	V
Input Current	$I_{IN(1)}$	50 V	$V_{DD} = V_{IN} = 5.0$ V	—	50	µA
			$V_{DD} = V_{IN} = 12$ V	—	240	µA
Input Impedance	Z_{IN}	50 V	$V_{DD} = 5.0$ V	100	—	kΩ
			$V_{DD} = 12$ V	50	—	kΩ
Clock Frequency	f_c	50 V		3.3	—	MHz
Serial Data Output Resistance	R_{OUT}	50 V	$V_{DD} = 5.0$ V	—	20	kΩ
			$V_{DD} = 12$ V	—	6.0	kΩ
Turn-ON Delay	t_{PLH}	50 V	Output Enable to Output, $I_{OUT} = -350$ mA	—	2.0	µs
Turn-OFF Delay	t_{PHL}	50 V	Output Enable to Output, $I_{OUT} = -350$ mA	—	10	µs
Supply Current	I_{BB}	50 V	All outputs ON, All outputs open	—	10	mA
			All outputs OFF	—	200	µA
	I_{DD}	50 V	$V_{DD} = 5$ V, All outputs OFF, Inputs = 0 V	—	100	µA
			$V_{DD} = 12$ V, All outputs OFF, Inputs = 0 V	—	200	µA
			$V_{DD} = 5$ V, One output ON, All inputs = 0 V	—	1.0	mA
			$V_{DD} = 12$ V, One output ON, All inputs = 0 V	—	3.0	mA
Diode Leakage Current	I_R	Max.	$T_A = +25°C$	—	50	µA
			$T_A = +70°C$	—	100	µA
Diode Forward Voltage	V_F	Open	$I_F = 350$ mA	—	2.0	V

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.



TIMING CONDITIONS

(V_{DD} = 5.0 V, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) . . . . . 75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) . . . . . 75 ns
C. Minimum Data Pulse Width . . . . . 150 ns
D. Minimum Clock Pulse Width . . . . . 150 ns
E. Minimum Time Between Clock Activation and Strobe . . . . . 300 ns
F. Minimum Strobe Pulse Width . . . . . 100 ns
G. Typical Time Between Strobe Activation and Output Transition . . . . . 1.0 µs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

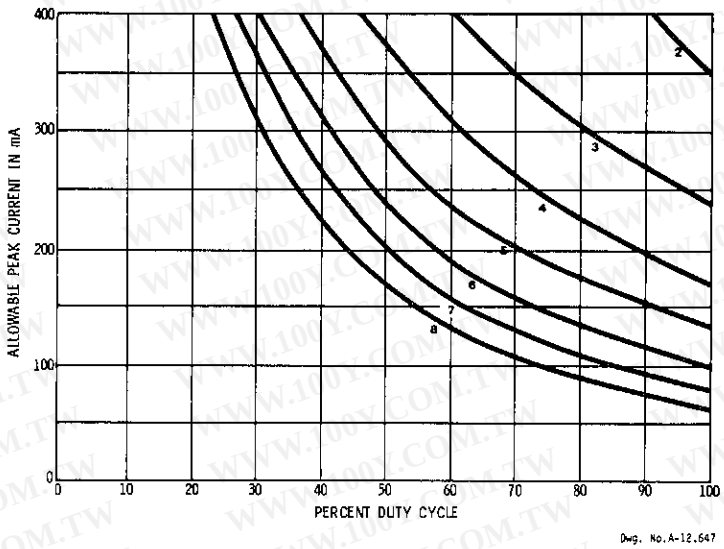
TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Output Enable	Output Contents
		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$			$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$
H	⎍	$H\ R_1\ R_2\ \ldots R_{N-2}\ R_{N-1}$	R_{N-1}				
L	⎍	$L\ R_1\ R_2\ \ldots R_{N-2}\ R_{N-1}$	R_{N-1}				
X	⎍	$R_1\ R_2\ R_3\ \ldots R_{N-1}\ R_N$	R_N				
		$X\ X\ X\ \ldots X\ X$	X	L	$R_1\ R_2\ R_3\ \ldots R_{N-1}\ R_N$		
		$P_1\ P_2\ P_3\ \ldots P_{N-1}\ P_N$	P_N	H	$P_1\ P_2\ P_3\ \ldots P_{N-1}\ P_N$	L	$P_1\ P_2\ P_3\ \ldots P_{N-1}\ P_N$
					$X\ X\ X\ \ldots X\ X$	H	$L\ L\ L\ \ldots L\ L$

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

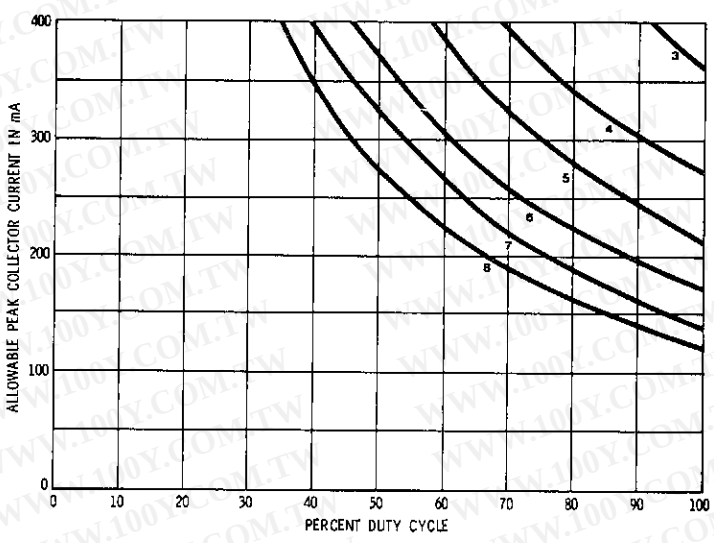
ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE
at +25°C Free-Air Temperature

UCN-5890A AND UCN-5891A



Dwg. No. A-12,647

UCN-5890B AND UCN-5891B



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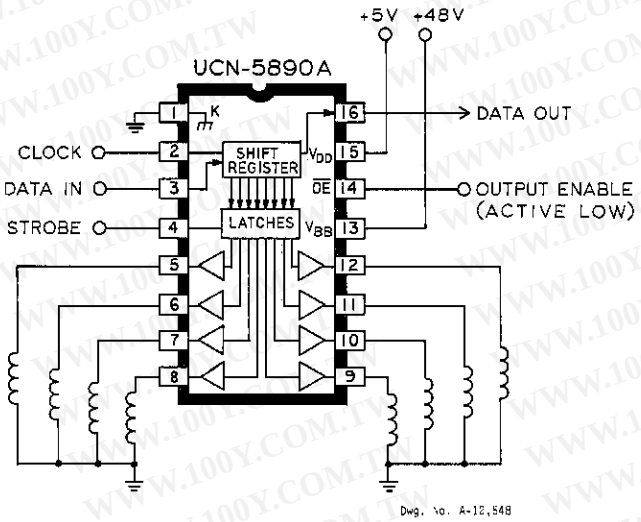
5

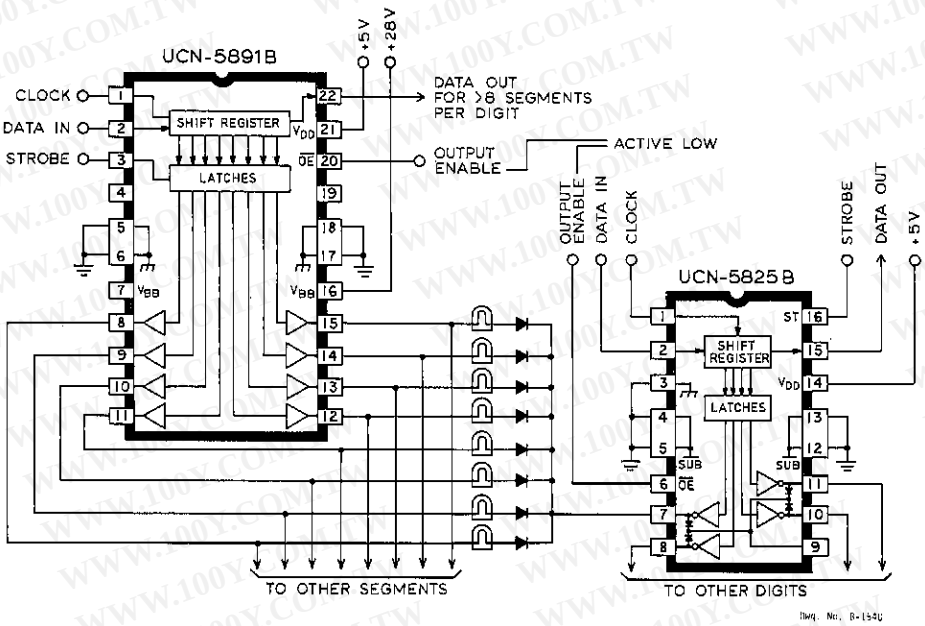
TYPICAL APPLICATIONS

SOLENOID OR RELAY DRIVER



Dwg. No. A-12,548

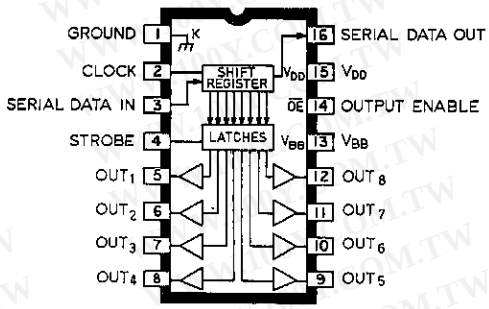
MULTIPLEXED INCANDESCENT LAMP DRIVER



UCN-5895A AND UCN-5895A-2 BiMOS II 8-BIT, SERIAL-INPUT, LATCHED SOURCE DRIVERS

FEATURES

- Low Output-Saturation Voltage
- Source Outputs to 50 V
- Output Current to −250 mA
- 3.3 MHz Minimum Data-Input Rate
- Low-Power CMOS Logic & Latches



Dwg. No. A-12,639

UCN-5895A AND UCN-5895A-2 BiMOS II serial-input, latched source drivers are designed for use in applications requiring low output-saturation voltages and currents to −250 mA per driver. Each driver combines an 8-bit CMOS register, associated latches and control circuitry (strobe and output enable), with saturated bipolar emitter-follower outputs. Typical loads are low-voltage LEDs and incandescent displays. They can also be used with multiplexed LED displays, thermal printers, or electromagnetic printers within their output limitations.

The UCN-5895A is rated for operation with supply voltages to 50 V and features a minimum output sustaining voltage of 35 V. The more economical UCN-5895A-2 is for use with supply voltages to 25 V (15 V sustaining). Under normal operation conditions, at +25°C, all outputs will source −120 mA continuously without derating. Similar drivers, featuring Darlington outputs for increased output ratings, are the UCN-5890A/B and UCN-5891A/B.

BiMOS II devices can operate at greatly improved data-input rates. With a 5 V supply, they will typically operate at better than 5 MHz. At 12 V, significantly higher speeds are obtained.

The CMOS inputs provide for minimum loading and are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors to ensure a proper input-logic high. A CMOS serial data output allows cascading these devices in multiple drive-line applications required by many dot matrix, alphanumeric, and bar graph displays.

These devices are rated for continuous operation over the temperature range of −20°C to +85°C. Because of limitations on package power dissipation, the simultaneous operation of all output drivers may require a reduction in duty cycle. The UCN-5895A and UCN-5895A-2 are supplied in standard 16-pin dual in-line plastic packages with copper lead frames for increased allowable package power dissipation.

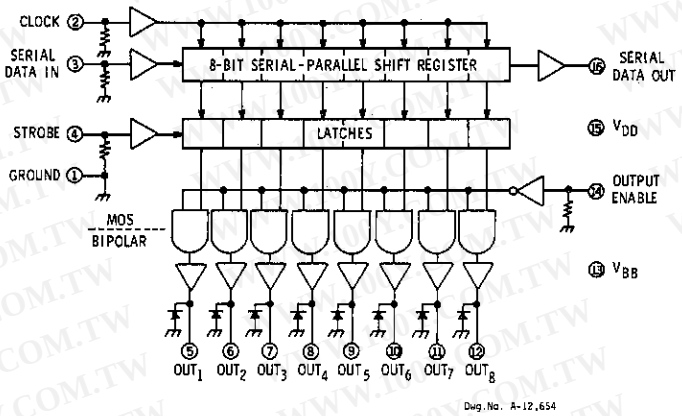
ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Output Voltage, V_{OUT} (UCN-5895A) . . . . . 50 V
(UCN-5895A-2) . . . . . 25 V
Logic Supply Voltage Range, V_{DD} . . . . . 4.5 V to 12 V
Driver Supply Voltage Range, V_{BB}
(UCN-5895A) . . . . . 5.0 V to 50 V
(UCN-5895A-2) . . . . . 5.0 V to 25 V
Input Voltage Range, V_{IN} . . . . . −0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT} . . . . . −250 mA
Allowable Package Power Dissipation, P_D . . . . . 1.67 W*
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +125°C

*Derate at the rate of 16.67 mW/°C above T_A = +25°C.

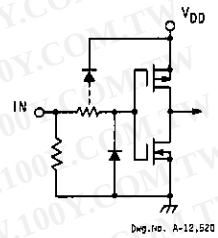
Caution: Sprague Electric CMOS devices have input static protection, but are susceptible to damage when exposed to extremely high static electrical charges.

FUNCTIONAL BLOCK DIAGRAM



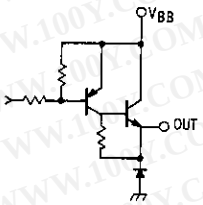
Dwg.No. A-12,654

TYPICAL INPUT CIRCUIT



Dwg.No. A-12,520

TYPICAL OUTPUT DRIVER

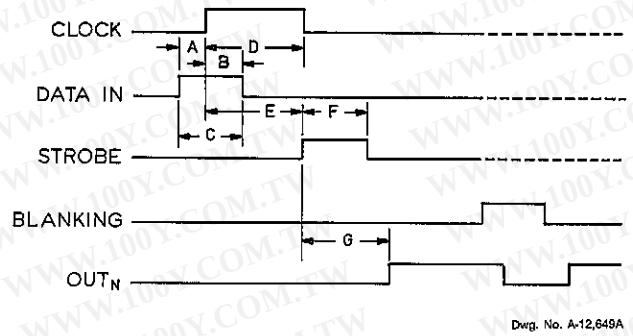


Dwg.No. A-12,655

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{BB} = 25$ V, $V_{DD} = 5$ V to 12 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{OUT}	$T_A = +25°C$	—	−50	µA
		$T_A = +70°C$	—	−100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = -60$ mA	—	1.1	V
		$I_{OUT} = -120$ mA	—	1.2	V
Output Sustaining Voltage	$V_{CE(sus)}$	$I_{OUT} = -120$ mA, L = 2 mH, UCN-5895A only	35	—	V
		$I_{OUT} = -120$ mA, L = 2 mH, UCN-5895A-2 only	15	—	V
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.5	5.3	V
		$V_{DD} = 12$ V	10.5	12.3	V
	$V_{IN(0)}$	$V_{DD} = 5$ V to 12 V	−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0$ V	—	50	µA
		$V_{DD} = V_{IN} = 12$ V	—	240	µA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	100	—	kΩ
		$V_{DD} = 12$ V	50	—	kΩ
Clock Frequency	f_c		3.3	—	MHz
Serial Data-Output Resistance	R_{OUT}	$V_{DD} = 5.0$ V	—	20	kΩ
		$V_{DD} = 12$ V	—	6.0	kΩ
Turn-ON Delay	t_{PLH}	Output Enable to Output, $I_{OUT} = -120$ mA	—	2.0	µs
Turn-OFF Delay	t_{PHL}	Output Enable to Output, $I_{OUT} = -120$ mA	—	10	µs
Supply Current	I_{BB}	All outputs ON, All outputs open	—	10	mA
		All outputs OFF	—	200	µA
	I_{DD}	$V_{DD} = 5$ V, All outputs OFF, Inputs = 0 V	—	100	µA
		$V_{DD} = 12$ V, All outputs OFF, Inputs = 0 V	—	200	µA
		$V_{DD} = 5$ V, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 12$ V, One output ON, All inputs = 0 V	—	3.0	mA
Diode Leakage Current	I_R	$V_R = 25$ V, $T_A = +25°C$	—	50	µA
		$V_R = 25$ V, $T_A = +70°C$	—	100	µA
Diode Forward Voltage	V_F	$I_F = 120$ mA	—	2.0	V

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.



Dwg. No. A-12,649A

TIMING CONDITIONS

(V_{DD} = 5.0 V, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) . . . . . 75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) . . . . . 75 ns
C. Minimum Data Pulse Width . . . . . 150 ns
D. Minimum Clock Pulse Width . . . . . 150 ns
E. Minimum Time Between Clock Activation and Strobe . . . . . 300 ns
F. Minimum Strobe Pulse Width . . . . . 100 ns
G. Typical Time Between Strobe Activation and Output Transition . . . . . 1.0 µs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

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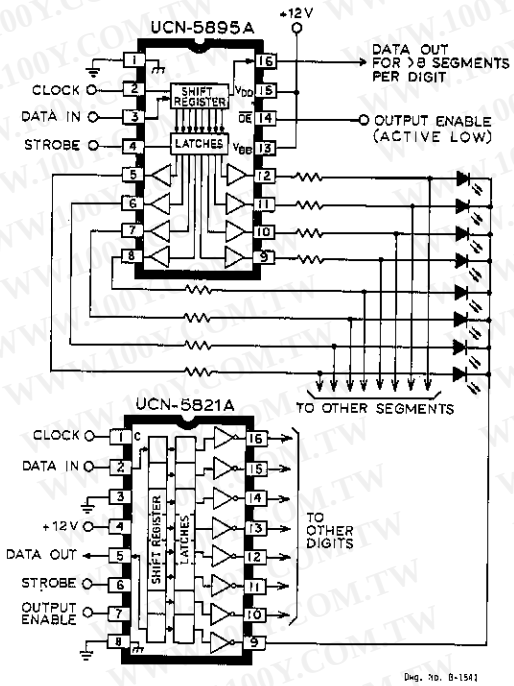
TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Blanking Input	Output Contents
		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$			$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$
H	⎍	$H\ R_1\ R_2\ \ldots R_{N-2} R_{N-1}$	R_{N-1}				
L	⎍	$L\ R_1\ R_2\ \ldots R_{N-2} R_{N-1}$	R_{N-1}				
X	⎍	$R_1\ R_2\ R_3\ \ldots R_{N-1} R_N$	R_N				
		$X\ X\ X\ \ldots X\ X$	X	L	$R_1\ R_2\ R_3\ \ldots R_{N-1} R_N$		
		$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$	P_N	H	$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$	L	$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$
					$X\ X\ X\ \ldots X\ X$	H	$L\ L\ L\ \ldots L\ L$

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

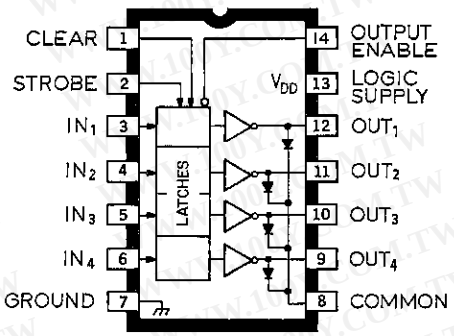
TYPICAL APPLICATION



UCN-5900A AND UCN-5901A
BiMOS III LATCHED DRIVERS

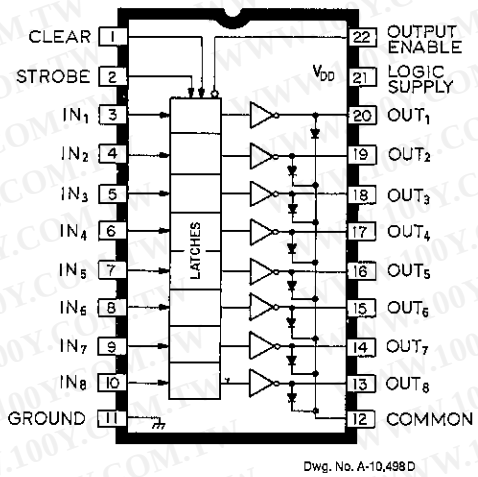
FEATURES

- High-Voltage, High-Current Outputs
- Output Sustaining Voltage of 90 V, Minimum
- Output Transient Protection
- 2 MHz Minimum Data Input Rate
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches



Dwg. No. A-10,498D

UCN-5900A



Dwg. No. A-10,498D

UCN-5901A

UCN-5900A and UCN-5901A latched drivers are high-voltage, high-current integrated circuits with four or eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, and other inductive loads requiring sustaining voltage ratings up to 90 V. UCN-5900A contains four latched drivers; UCN-5901A contains eight latched drivers.

The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or LSTTL circuits may require the use of appropriate pull-up resistors. BiMOS latches will typically operate at better than 3 MHz with a 5 V supply. With a 12 V supply, higher speeds are obtained.

Both units have open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 400 mA and will withstand at least 150 V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.

The UCN-5900A 4-latch device, is furnished in a standard 14-pin dual in-line plastic package. The UCN-5901A 8-latch device, is supplied in a 22-pin dual in-line plastic package with lead spacing on 0.400″ (10.16 mm) rows. To simplify circuit board layout, all outputs are opposite their respective inputs.

5

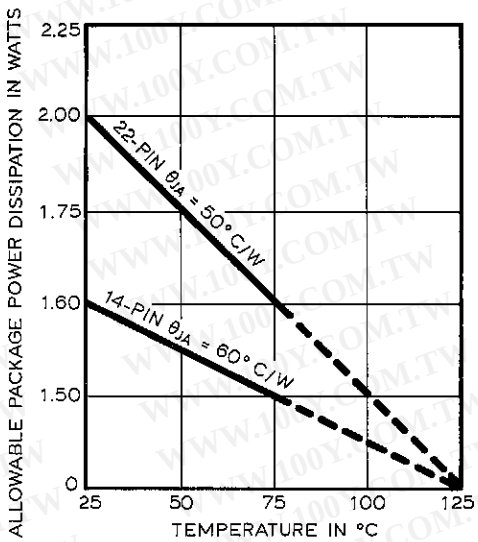
ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Output Voltage, V_{CE} . . . . . 150 V
Supply Voltage, V_{DD} . . . . . 15 V
Input Voltage Range, V_{IN} . . . . . −0.3 V to V_{DD} + 0.3 V
Continuous Collector Current, I_C . . . . . 400 mA
Package Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +125°C

Allowable combinations of output current, number of outputs conducting, and duty cycle are shown on following pages.

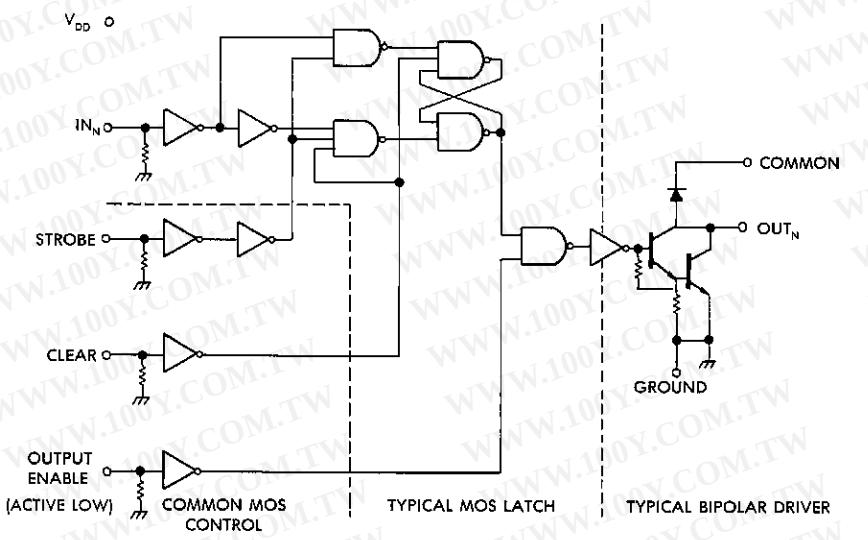
Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

ALLOWABLE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



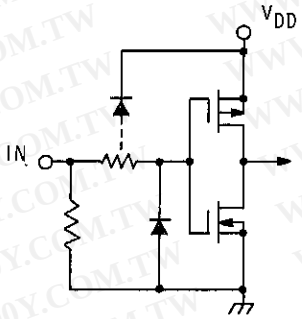
Dwg. No. A-14,220

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-10,495B

TYPICAL INPUT CIRCUIT



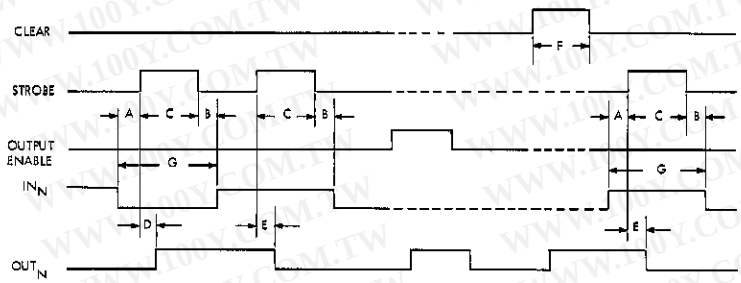
Dwg. No. A-12,520

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5$ V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	$V_{CE} = 150$ V, $T_A = +25°C$	—	—	50	µA
		$V_{CE} = 150$ V, $T_A = +70°C$	—	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100$ mA	—	1.2	1.4	V
		$I_C = 200$ mA	—	1.4	1.6	V
		$I_C = 350$ mA, $V_{DD} = 7.0$ V	—	1.6	1.9	V
Collector-Emitter Sustaining Voltage	$V_{CE(sus)}$	$I_C = 300$ mA, L = 2 mH	90	—	—	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	$V_{DD} = 12$ V	10.5	—	—	V
		$V_{DD} = 10$ V	8.5	—	—	V
		$V_{DD} = 5.0$ V (See Note)	3.5	—	—	V
Input Resistance	R_{IN}	$V_{DD} = 12$ V	50	200	—	kΩ
		$V_{DD} = 10$ V	50	300	—	kΩ
		$V_{DD} = 5.0$ V	50	600	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	$V_{DD} = 12$ V, Outputs Open	—	1.0	2.0	mA
		$V_{DD} = 10$ V, Outputs Open	—	0.9	1.7	mA
		$V_{DD} = 5.0$ V, Outputs Open	—	0.7	1.0	mA
	$I_{DD(OFF)}$ (Total)	$V_{DD} = 12$ V, Outputs Open, Inputs = 0 V	—	—	200	µA
		$V_{DD} = 5.0$ V, Outputs Open, Inputs = 0 V	—	50	100	µA
Clamp Diode Leakage Current	I_R	$V_R = 150$ V, $T_A = +25°C$	—	—	50	µA
		$V_R = 150$ V, $T_A = +70°C$	—	—	100	µA
Clamp Diode Forward Voltage	V_F	$I_F = 350$ mA	—	1.7	2.0	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".

5



Dwg. No. A-10,895A

TIMING CONDITIONS

T_A = +25°C, Logic Levels are V_{DD} and Ground

	V_{DD} = 5.0 V
A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time)	100 ns
B. Minimum Data Active Time After Strobe Disabled (Data Hold Time)	100 ns
C. Minimum Strobe Pulse Width	300 ns
D. Typical Time Between Strobe Activation and Output ON to OFF transition	500 ns
E. Typical Time Between Strobe Activation and Output OFF to ON transition	500 ns
F. Minimum Clear Pulse Width	300 ns
G. Minimum Data Pulse Width	500 ns

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

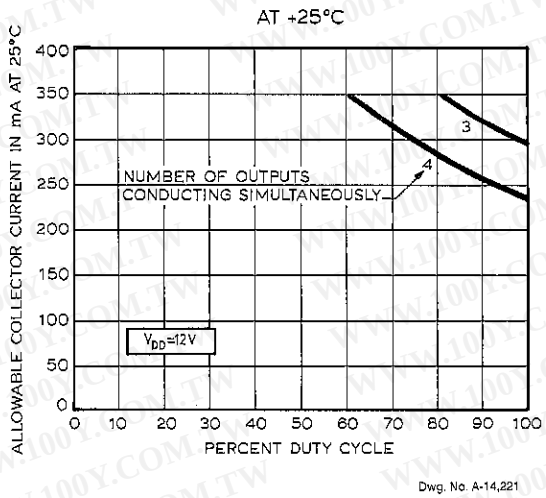
TRUTH TABLE

IN_N	STROBE	CLEAR	OUTPUT ENABLE	OUT_N t-1	OUT_N t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

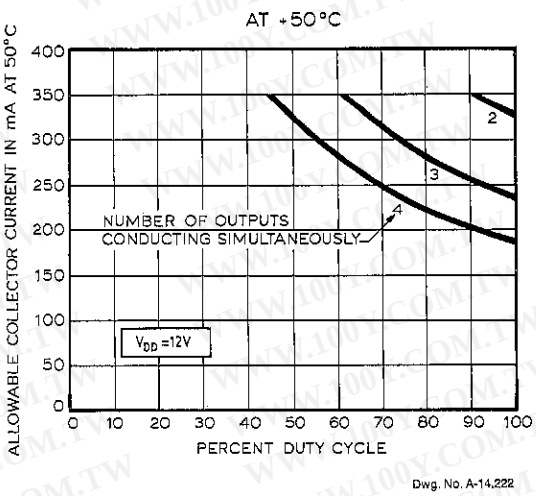
X = irrelevant
t-1 = previous output state
t = present output state

COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE

UCN-5900A



Dwg. No. A-14,221



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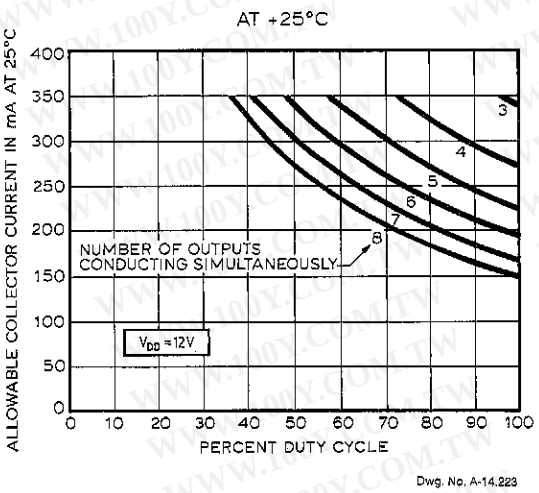
UCN-5901A



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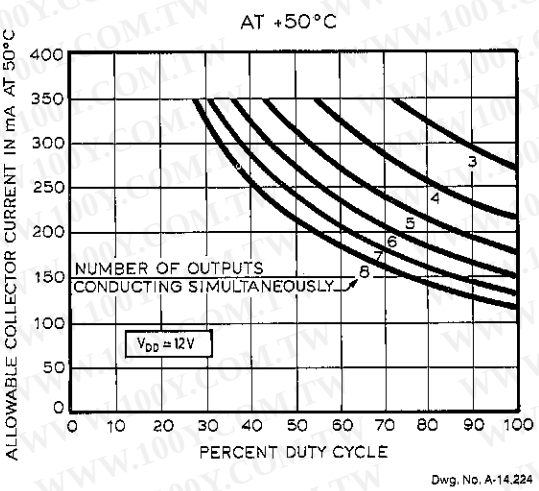
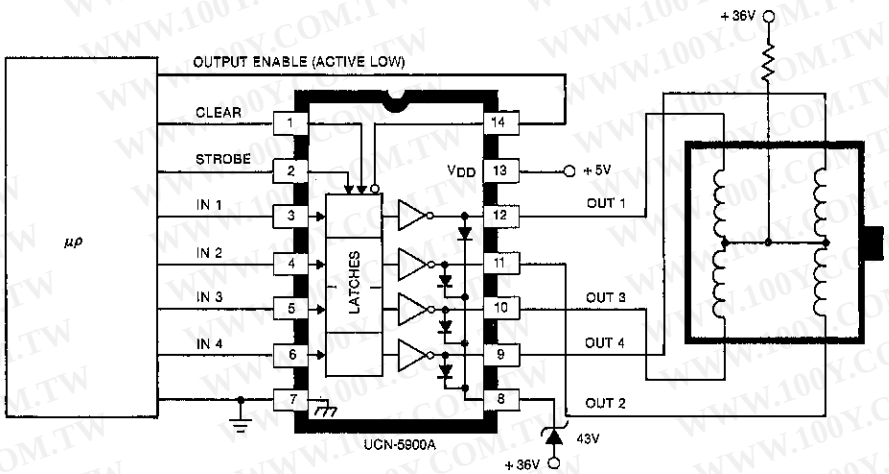


Dwg. No. A-14,224

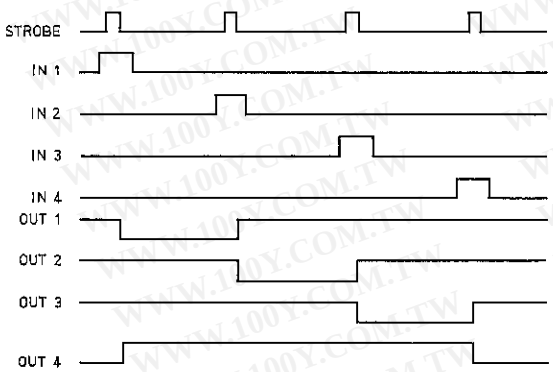
TYPICAL APPLICATION

UNIPOLAR STEPPER-MOTOR DRIVER



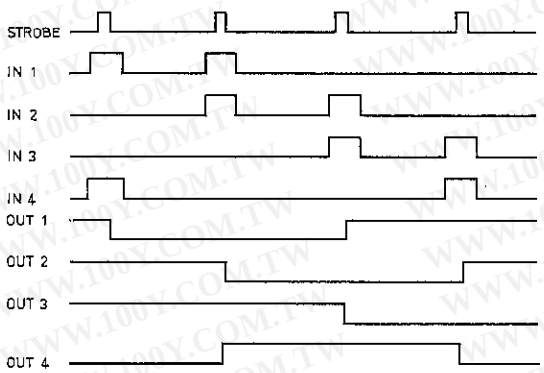
Dwg. No. A-13,677

UNIPOLAR WAVE DRIVE



Dwg. No. A-11,446

UNIPOLAR 2-PHASE DRIVE



Dwg. No. A-11,447

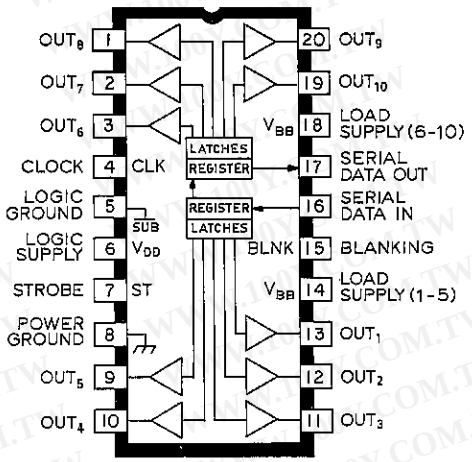
UCN-5910A HIGH-VOLTAGE BiMOS III 10-BIT, SERIAL-INPUT, LATCHED DRIVER

FEATURES

- To 150 V Output Breakdown
- 50 mA Push-Pull Outputs
- 3 MHz Minimum Data Input Rate
- Low-Power CMOS Latches
- Blanking and Strobe Functions

UCN-5910A is a smart power integrated circuit combining high-speed CMOS logic and high-voltage, power driver outputs. This serial-input, latched driver is especially useful with ink-jet and piezoelectric printers, large flat-panel vacuum-fluorescent or AC plasma displays. The UCN-5910A has an output rating of 150 V and ±50 mA. For applications requiring output ratings to only 135 V, the economical type UCN-5910A-2 is recommended. The lower-cost device is identical to the basic part, except for the minimum output breakdown voltage.

The 10-bit CMOS shift register and latches are designed for operation over a logic supply range of 5 V to 12 V. The high-impedance inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or LSTTL may require the use of appropriate pull-up resistors to ensure an input logic high. Using BiMOS III logic for improved data entry rates, the CMOS circuitry will operate at better than 3.3 MHz with a 5 V supply. With a 12 V supply, significantly higher speeds are obtained. A CMOS serial-data output allows cascading devices for multiple drive-line applications required by many dot matrix, alphanumeric, and bar graph displays.



Dwg. No. A-13,678A

The output drivers are high-voltage Darlington source drivers with DMOS sink drivers. Especially important when driving loads of 100 V or more, the active pull-down function provides better output switching than passive pulldowns.

The UCN-5910A and UCN-5910A-2 are supplied in 20-pin dual in-line plastic packages. They can be operated over the temperature range of −20°C to +85°C. Copper lead frames allow all outputs (50% duty cycle) to be operated at ±20 mA at ambient temperatures up to +30°C, or at ±15 mA to +55°C.

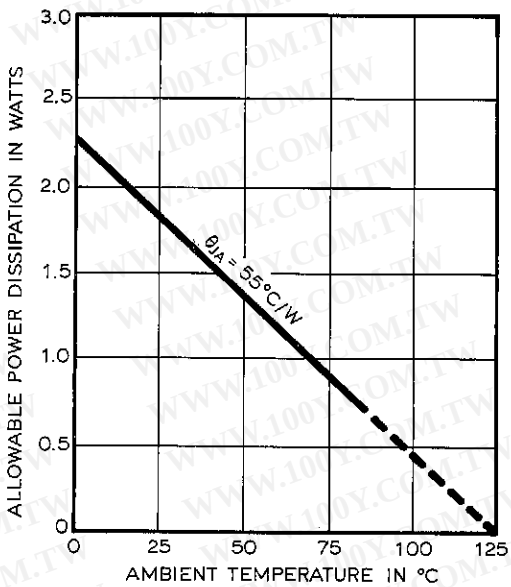
5

ABSOLUTE MAXIMUM RATINGS
at $T_A = +25°C$

Driver Supply Voltage, V_{BB} (UCN-5910A) . . . . . 150 V
(UCN-5910A-2) . . . . . 135 V
Output Current, I_{OUT} . . . . . ±50 mA
Logic Supply Voltage, V_{DD} . . . . . 15 V
Input Voltage, V_{IN} . . . . . −0.3 V to V_{DD} + 0.3 V
Package Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +125°C

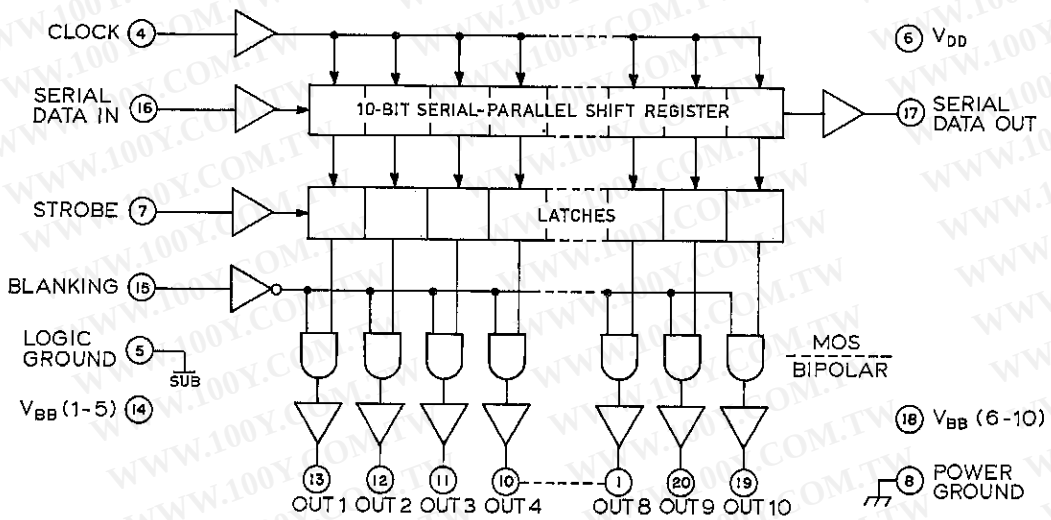
Caution: Sprague Electric CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

ALLOWABLE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



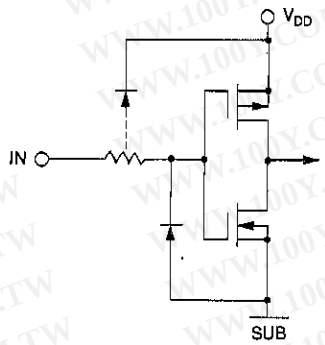
Dwg. No. A-14,213

FUNCTIONAL BLOCK DIAGRAM



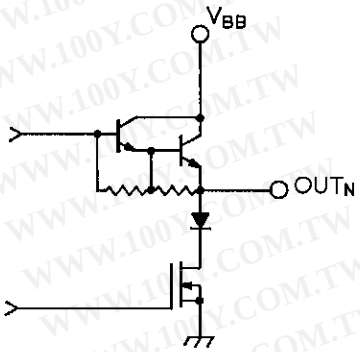
Dwg. No. A-14,214

TYPICAL INPUT CIRCUIT



Dwg. No. A-13,050

TYPICAL OUTPUT DRIVER



Dwg. No. A-14,219

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 135 V (UCN-5910A-2) or 150 V (UCN-5910A), unless otherwise noted.

Characteristic	Symbol	Test Conditions	Limits @ V_{DD} = 5 V			Limits @ V_{DD} = 12 V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V, T_A = +70°C	—	−5.0	−15	—	−5.0	−15	µA
Output Voltage	$V_{OUT(1)}$	I_{OUT} = −40 mA, V_{BB} = 135 V	130	—	—	130	—	—	V
		I_{OUT} = −40 mA, V_{BB} = 150 V*	145	—	—	145	—	—	V
	$V_{OUT(0)}$	I_{OUT} = 5 mA	—	2.0	3.5	—	2.0	3.5	V
		I_{OUT} = 40 mA	—	—	—	—	15	25	V
Output Pull-Down Current	$I_{OUT(0)}$	V_{OUT} = 5 V to V_{BB}	10	—	—	—	—	—	mA
		V_{OUT} = 20 V to V_{BB}	—	—	—	25	—	—	mA
Input Voltage	$V_{IN(1)}$		3.5	—	5.3	10.5	—	12.3	V
	$V_{IN(0)}$		−0.3	—	+0.8	−0.3	—	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	—	0.05	0.5	—	0.1	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	−0.05	−0.5	—	−1.0	−1.0	µA
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = −200 µA	4.5	4.7	—	11.7	11.8	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	—	200	250	—	100	200	mV
Maximum Clock Frequency	f_{clk}		3.3	5.0	—	—	7.5	—	MHz
Supply Current	$I_{DD(1)}$	All Outputs High	—	350	500	—	700	850	µA
	$I_{DD(0)}$	All Outputs Low	—	350	500	—	700	850	µA
	$I_{BB(1)}$	Outputs High, No Load	—	1.0	2.0	—	1.0	2.0	mA
	$I_{BB(0)}$	Outputs Low	—	10	100	—	10	100	µA
Blanking to Output Delay	t_{PHL}	C_L = 30 pF	—	300	550	—	250	500	ns
	t_{PLH}	C_L = 30 pF	—	750	1000	—	750	1000	ns
Output Fall Time	t_f	C_L = 30 pF	—	500	750	—	300	550	ns
Output Rise Time	t_r	C_L = 30 pF	—	1100	1350	—	1100	1350	ns

Negative current is defined as coming out of (sourcing) the specified device pin.
*UCN-5910A only.

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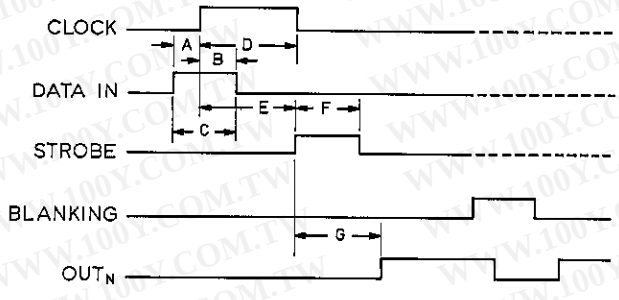


Dwg. No. A-12,649A

TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and Ground)

	V_{DD} = 5.0 V
A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B. Minimun Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C. Minimum Data Pulse Width	150 ns
D. Minimum Clock Pulse Width	150 ns
E. Minimum Time Between Clock Activation and Strobe	300 ns
F. Minimum Strobe Pulse Width	100 ns
G. Typical Time Between Strobe Activation and Output Transition	750 ns

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents $I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$	Serial Data Output	Strobe Input	Latch Contents $I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$	Blanking	Output Contents $I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$
H	⎍	H $R_1\ R_2\ \ldots R_{N-2}\ R_{N-1}$	R_{N-1}				
L	⎍	L $R_1\ R_2\ \ldots R_{N-2}\ R_{N-1}$	R_{N-1}				
X	⎍	$R_1\ R_2\ R_3\ \ldots R_{N-1}\ R_N$	R_N				
		X X X ... X X	X	L	$R_1\ R_2\ R_3\ \ldots R_{N-1}\ R_N$		
		$P_1\ P_2\ P_3\ \ldots P_{N-1}\ P_N$	P_N	H	$P_1\ P_2\ P_3\ \ldots P_{N-1}\ P_N$	L	$P_1\ P_2\ P_3\ \ldots P_{N-1}\ P_N$
					X X X ... X X	H	L L L ... L L

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

RELIABILITY OF SERIES UCN-4800A AND UCN-5800A BiMOS DRIVERS

THIS REPORT SUMMARIZES accelerated-life tests that have been performed on Series UCN-4800A and UCN-5800A BiMOS integrated circuits and provides information that can be used to calculate the failure rate at any junction operating temperature.

INTRODUCTION

Product-reliability improvement is a continuous and evolving process at Sprague Electric Company. Ongoing life tests, environmental tests, and stress tests are performed to establish failure rates and monitor established process-control procedures. Failures are analyzed to determine design changes or process improvements that can be implemented to improve device reliability.

The reliability of integrated circuits can be measured by qualification tests, burn-in, and accelerated-life tests:

1) Qualification testing is performed at an ambient temperature of +125°C, reduced so as to limit junction temperature to +150°C, for 1000 hours with an LTPD = 5 in accordance with MIL-STD-883B. This testing is normally conducted in response to a specific customer request or requirement. Qualification testing highlights design problems or gross processing problems, but does not provide sufficient data to generate accurate failure-rate data in a reasonable period of time.
2) Burn-in is intended to remove infant-mortality rejects and is conducted at +150°C for 96 hours or at +125°C for 168 hours. An analysis of test results from Sprague Electric's Double-Deuce™ burn-in program found that most failures are due to slight parametric shifts. Catastrophic failures, which would cause user-equipment failure, are typically less than 0.1%.
3) Accelerated-life testing is performed at temperatures above +125°C and is used to generate failure-rate data.

ACCELERATED-LIFE TESTS

Sprague Electric performs accelerated-life tests on integrated circuits at junction temperatures of +150°C or +175°C at the recommended operating voltages. The internal power dissipation on some high-power circuits requires the ambient temperature to be lower than +150°C to keep the junction temperature between +150°C and +175°C.

In these tests, failures are produced so that the statistical life distribution can be established. The distribution cannot be established without failures. High-temperature accelerated-life testing is necessary to accumulate data in reasonable time periods. It has been established that the failure mechanisms at all temperatures in these tests are identical. Temperatures above +175°C are not generally used for the following reasons:

a) Industry-standard molding compounds degrade and release contaminants (halides) at approximately +200°C.
b) Life-test boards constructed with materials capable of withstanding exposure to temperatures greater than +175°C have been deemed to be cost prohibitive.
c) Increases in junction leakage currents may increase the power dissipation and device temperature to an indeterminate level.

Table I contains data produced by life tests that were conducted at +150°C. The data include the number of units in each sample, and the time periods during which failures occurred. The total time-on-test varies, with priority changes influencing allocation of oven and board space, as new products are introduced. The time intervals between test readings were chosen for ease of plotting on log-normal paper.

The acceleration factor calculated using the Arrhenius equation, and a 1 eV activation energy, is approximately 5× for each 25°C temperature rise in junction temperature and is multiplicative.[1] This allows the data to be compared to qualification life-test data by equating 200 hours at +150°C to 1000 hours at +125°C.

The data at the bottom of Table I are compiled by calculating the probability of success (P_s), the cumulative probability of success, the probability of failure (P_f) and the percentage of failed units in each time period.

The cumulative percent of failures is plotted on log-normal plotting paper in Figure 1. This paper has a logarithmic time-scale axis and a probability-scale axis. A log-normal distribution plots as a straight line. A line of best fit is drawn through the plotted points and extended to determine the median life-time at the 50% fail-point. The median life at a junction temperature of +150°C is, in this case, 31,000 hours.

The log-normal distribution is commonly used because most semiconductor device data fit such a distribution.[2] When the median life has been found at the elevated temperature, it can be converted to the lower temperature of the actual application. The Arrhenius equation, which relates the reaction rate to temperature, is used to make this conversion.[1]

TABLE I
TEST RESULTS AT T_J = +150°C

		HOURS ON TEST											
TEST NUMBER	QTY.	48	90	150	300	600	1200	1800	2400	3000	5000	6000	7000
		NUMBER OF FAILURES											
1	35	0	0	0	0	0	0	0	0	0	0	5	7
2	25	0	0	3	0	1	6	—	—	—	—	—	—
3	21	0	1	—	—	—	—	—	—	—	—	—	—
4	30	0	0	4	9	—	—	—	—	—	—	—	—
5	17	0	0	0	0	2	0	0	0	0	1	0	2
6	20	0	0	3	10	0	—	—	—	—	—	—	—
7	20	0	0	0	0	0	2	0	1	0	0	—	—
8	25	0	0	1	0	2	0	2	0	0	0	1	—
9	25	0	0	0	1	0	0	0	0	0	2	—	—
10	25	0	0	0	0	0	0	—	—	—	—	—	—
11	30	0	0	0	0	0	0	0	—	—	—	—	—
12	30	0	0	0	0	0	0	0	—	—	—	—	—
13	30	0	0	0	5	0	0	0	0	0	—	—	—
14	30	0	0	0	0	0	1	0	2	—	—	—	—
15	26	0	0	0	—	—	—	—	—	—	—	—	—
16	30	0	0	0	0	—	—	—	—	—	—	—	—
17	20	1	0	0	1	0	0	—	—	—	—	—	—
18	25	0	0	0	0	0	0	—	—	—	—	—	—
19	28	0	0	0	0	0	0	—	—	—	—	—	—
20	45	0	0	0	0	0	0	—	—	—	—	—	—
21	25	0	0	0	0	0	—	—	—	—	—	—	—
TOTAL ON TEST		562	561	540	503	430	387	228	166	136	111	69	44
TOTAL FAILURES		1	1	11	26	5	9	2	3	0	3	6	9
TOTAL GOOD		561	560	529	477	425	378	226	163	136	108	63	35
P_s		.998	.998	.980	.948	.988	.977	.991	.982	1.00	.973	.913	.795
Cumulative P_s		.998	.996	.976	.926	.915	.894	.886	.870	.870	.846	.773	.615
$P_f = 1 - P_s$		.002	.004	.024	.074	.085	.106	.114	.130	.130	.154	.227	.385
% Failures		0.18	.036	2.39	7.43	8.51	10.6	11.4	13.0	13.0	15.4	22.7	38.5

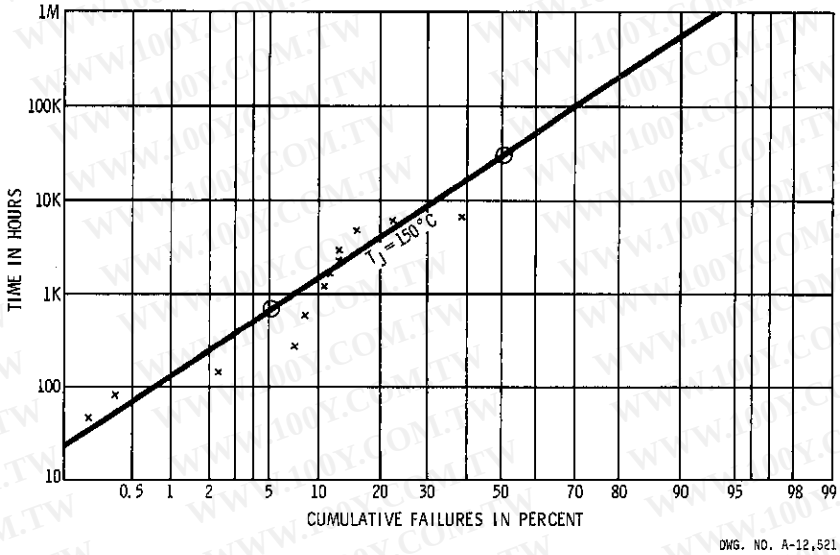


Figure 1
CUMULATIVE PERCENT FAILURES

The Arrhenius equation is:

$$V_r = V_r^o e^{-\epsilon/kT}$$

where V_r^o = a constant
ϵ = activation energy
k = Boltzmann's constant
T = absolute temperature in degrees Kelvin

An activation energy of 1.0 electron-volt was established by testing Series ULN-2000A, Series UDN-5710M, and Series UDN-2980A devices at multiple temperatures. Failure analysis of devices rejected during that testing also supports this activation energy, as failures were mainly due to increased leakages, reduced beta, and surface inversion.[3]

The median life-point is drawn on Arrhenius graph paper in Figure 2. The Arrhenius plot gives a graphical solution, rather than a mathematical solution, to the problem of equivalent median lifetime at any junction temperature. A line is drawn through this point (or points when multiple temperatures are used) with a slope of $\epsilon = 1.0$ eV.

Although not as statistically accurate as the median lifetime, the *5%* fail-point can be read from Figure 1 and plotted parallel to the median-life line in Figure 2.

The median life at reduced junction temperatures can now be determined using Figure 2. It must be emphasized that this is junction temperature and *not* ambient temperature. The temperature rise at the junction due to internal power dissipation must be taken into account using the formula:

$$T_J = P_D\theta_{JA} + T_A \quad \text{or} \quad T_J = P_D\theta_{JC} + T_C$$

The median lifetime, or 50% fail-point, as graphically determined in Figure 2, is approximately 22 years at +125°C or 190 years at +100°C junction temperature.

The approximate failure rate (FR) may be determined from FR = 1/Median Life, where Median Life is taken from Figure 2 at the intersection of the junction-temperature line and median-life line. The actual instantaneous failure rate can be calculated using a Goldwaite plot.[4] However, this approximation is very close. At +100°C the failure rate would be:

$$FR = 1/(1.7 \times 10^6 \text{ hours})$$
$$= 0.06\%/1000 \text{ hours} = 600 \text{ FIT}$$

where *FIT* = failures per 10^9 unit-hours

Other failure-rate values have been calculated and appear in Table II.

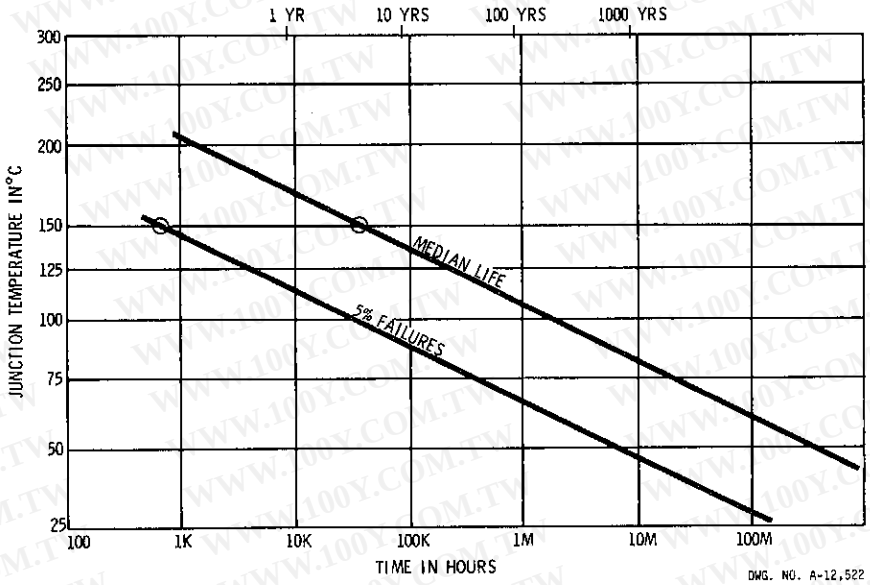


Figure 2
MEDIAN LIFE

TABLE II
SERIES UCN-4800A AND UCN-5800A FAILURE RATE

T_j (°C)	Median Life (h)	Failure Rate (%/1000h)	Failures In Time (No./10^9 unit-hours)
125	2×10^5	0.5	5000
100	1.7×10^6	0.06	600
75	1.7×10^7	0.006	60
50	3×10^8	0.0003	3

CONCLUSION

The relationship between temperature and failure rate is well documented and is an important factor in all designs. Load currents, duty cycle, and ambient temperature must be considered by the design engineer to establish a junction-temperature limit that provides a failure rate within design objectives.

Figure 2 shows that a design with a continuous operating junction temperature of +100°C (internal power dissipation plus external ambient temperature) would reach the 5% failure point in 3.8 years. Lowering the junction temperature to +75°C increases the time to the 5% failure point to 42 years.

A complete sequence of environmental tests, including temperature cycle, pressure cooker, and biased humidity tests, are continuously monitored to ensure that assembly and package technology remain within established units.

The environmental tests and accelerated-life tests establish a base line for comparisons of new processes and materials.

REFERENCES

1) Manchester, K.E., and Bird, D.W., "Thermal Resistance: A Reliability Consideration," *IEEE Transactions*, Vol. CHMT-3, No. 4, 1980, pp. 580-587 (Sprague Technical Paper TP 80-2).

2) Peck, D. S., and Trapp, O. D., *Accelerated Testing Handbook*, Technology Associates, 1978, pp. 2-1 through 2-6.

3) *ibid.*, p. 6-7.

4) Goldwaite, L. R., "Failure Rate Study for the Log-Normal Lifetime Model," *Proceedings of the 7th Symposium on Reliability and Quality Control*, 1961, pp. 208-213.

BiMOS II POWER DRIVERS

THE second generation of merged CMOS/bipolar integrated circuits extends the lead in innovative interface forged by Sprague Electric's original BiMOS power drivers.

Higher-density CMOS logic gives BiMOS II integrated circuits improved switching speeds at reduced costs. With a 5 V supply, second generation BiMOS typically operates at data input rates above 5 MHz; at 12 V, significantly higher speeds are obtainable. The BiMOS II series also offers new and improved functions.

Reliable, single-chip BiMOS II solutions are available for a wide variety of peripheral and power interface problems. Two or more devices are no longer required to interface low-level (TTL, CMOS, NMOS, PMOS) LSI or microprocessor functions with power loads such as LEDs, gas-discharge or vacuum-fluorescent displays, relays, solenoids, thermal printers, motors, impact printer hammers, and incandescent lamps. Since all BiMOS devices include logic and control in addition to power functions, they also free the microprocessor from many housekeeping tasks.

SERIES UCN-5900 BiMOS III
***HIGH-VOLTAGE* INTERFACE DRIVERS**

THE original UCN-4800 BiMOS interface integrated circuit designs evolved into high-speed UCN-5800 BiMOS II designs. Improvements continue with the new 150 V Sprague Series UCN-5900 *BiMOS III* designs.

Original BiMOS Type Number	BiMOS II Type Number	BiMOS III Type Number
UCN-4401A (50 V)	UCN-5800A (50 V)	UCN-5900A (150 V)
UCN-4801A (50 V)	UCN-5801A (50 V)	UCN-5901A (150 V)
UCN-4810A-1 (80 V)	UCN-5810A-1 (80 V)	UCN-5910A (150 V)

5

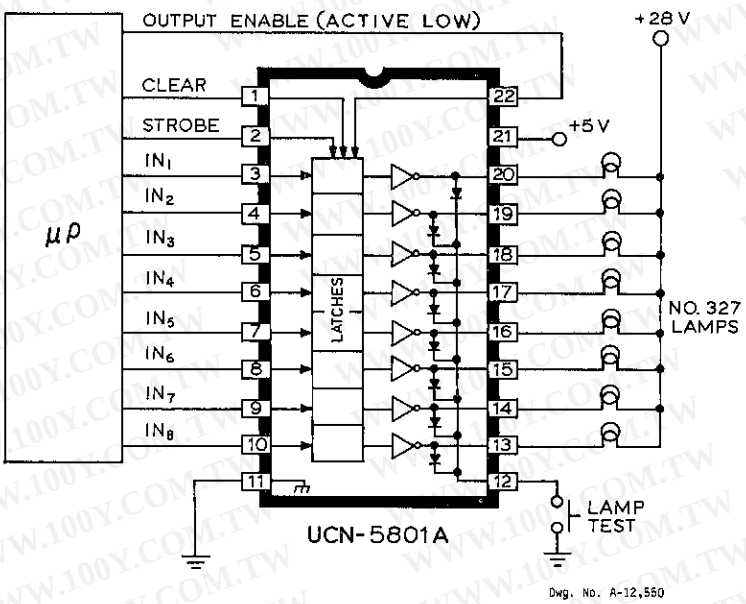
INCANDESCENT LAMP DRIVERS

EACH of the UCN-5800A or UCN-5801A open-collector Darlington outputs will sink up to 500 mA and will sustain at least 50 V in the OFF state. The high peak current rating of these devices allows their use with the high inrush (10×) currents normally associated with incandescent lamps. Internal diodes can be used to perform the lamp test function. Package power limitations normally disallow simultaneous and continuous operation of all outputs at the rated maximum current: Either a reduction in output current or a suitable combination of duty cycle and number of active outputs is usually required.

The UCN-5800A is supplied in a standard 14-lead DIP. The UCN-5801A is furnished in a 22-lead DIP with 0.400" row spacing.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage . . . . . 45 V
Logic Supply Voltage Range . . . . . 5.0 V to 12 V
Continuous Output Current . . . . . 350 mA



PLANAR GAS-DISCHARGE DISPLAY DRIVERS

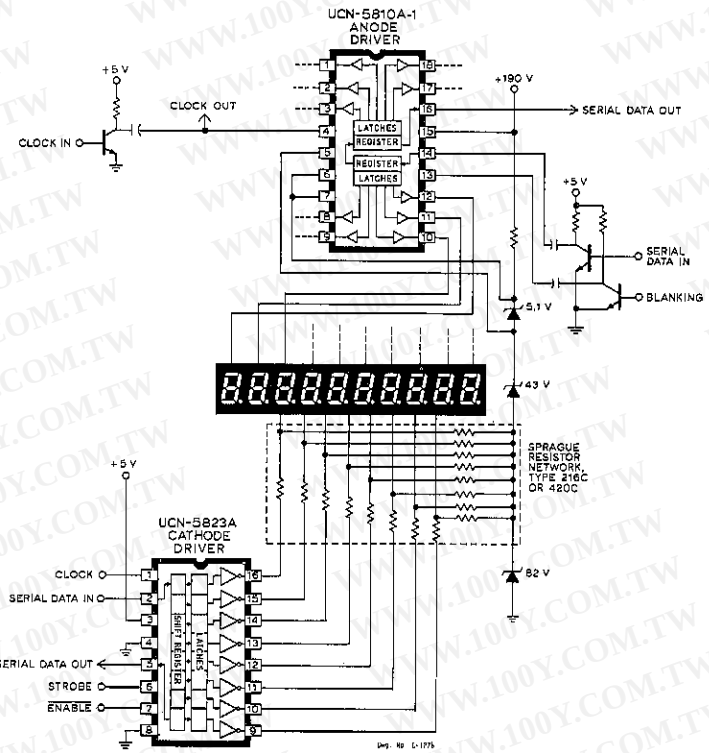
COMBINING the high-voltage UCN-5810A-1, UCN-5812A-1, or UCN-5818A-1 serial-input, latched source driver with the UCN-5823A serial-input, latched sink driver provides a simple way to drive multiplexed high-voltage planar gas-discharge displays.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage
- UCN-5810A-1, UCN-5812A-1, UCN-5818A-1 . . . . . 75 V
- UCN-5823A . . . . . 95 V

Logic Supply Voltage Range . . . . . 5.0 V to 12 V

Continuous Output Current
- UCN-5810A-1, UCN-5812A-1, UCN-5818A-1 . . . . . −25 mA
- UCN-5823A . . . . . 350 mA



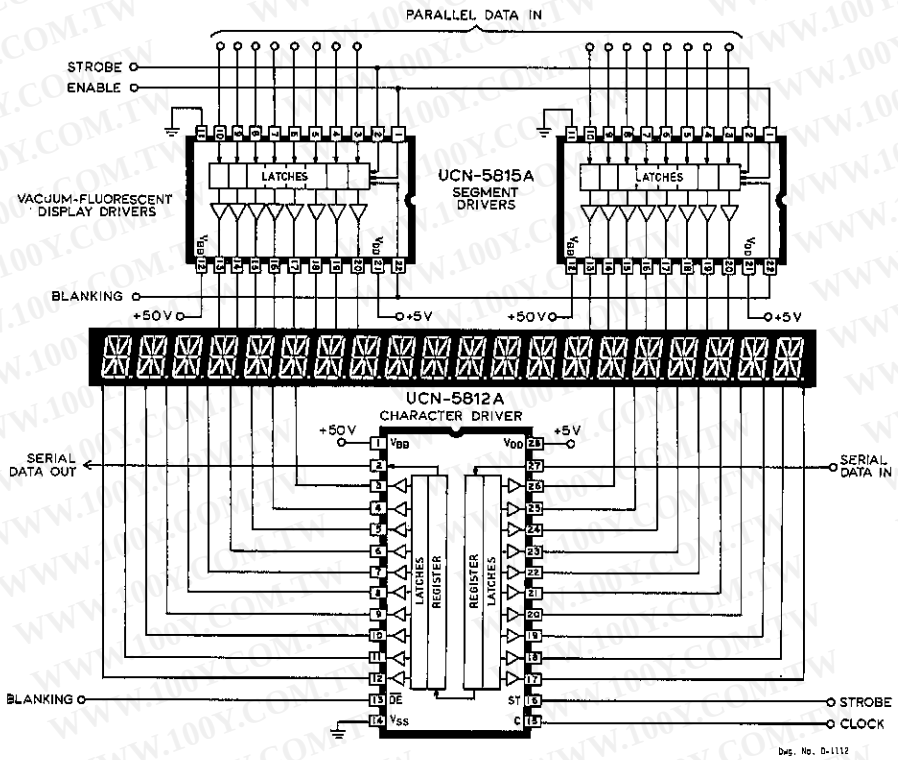
VACUUM-FLUORESCENT DISPLAY DRIVERS

THE UCN-5815A 8-bit, latched, source driver provides a practical means of driving the segments, dots (matrix panel), or bars of multiplexed high-voltage vacuum-fluorescent displays. The UCN-5810A (10-bit), UCN-5812A (20-bit), or UCN-5818A (32-bit) serial-input, latched source drivers are well-suited for use as character or digit drivers. The high-voltage versions (suffix -1) can also be used to drive the anodes of planar gas-discharge displays.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage
- UCN-5810A, UCN-5812A, UCN-5818A ..... 55 V
- UCN-5810A-1, UCN-5812A-1, UCN-5818A-1 ..... 75 V

Logic Supply Voltage Range ..... 5.0 V to 12 V
Continuous Output Current ..... −25 mA



MULTIPLEXED INCANDESCENT LAMP DRIVERS

IN ORDER to obtain brightness equivalent to normal d-c operation, multiplexed incandescent displays must be operated at a voltage:

$$E_{MPX} = E_{DC}\sqrt{N}$$

where E_{MPX} = the recommended operating supply voltage,
E_{DC} = the rated d-c lamp voltage, and
N = the number of digits being multiplexed.

Multiplexed lamps also require isolation diodes to prevent sneak series/parallel paths to unaddressed elements.

Serial-input, latched source drivers provide simple, compact, and economical segment drivers for mutiplexed incandescent lamp applications. The UCN-5890A/B and UCN-5891A/B feature high-voltage, high-current (500 mA, peak) Darlington outputs. The UCN-5895A has saturated outputs for minimum voltage drop and will source up to 250 mA per driver. The drivers are supplied in an economical 16-pin "A" package or, for improved package power dissipation, a 22-pin "B" package. In either package style, UCN-5890, UCN-5891 and UCN-5895 are pin-compatible except for output ratings.

High-current UCN-5825B or UCN-5826B serial-input, latched sink drivers are used to drive the digits. Their high peak current rating is required to withstand the substantial inrush currents created by cold filaments. These BiMOS II power drivers also include internal thermal shutdown circuitry.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage
- UCN-5825B ..... 55 V
- UCN-5826B ..... 75 V
- UCN-5890A/B ..... 75 V
- UCN-5891A/B ..... 45 V
- UCN-5895A ..... 45 V

Logic Supply Voltage Range ..... 5.0 V to 12 V

Continuous Output Current
- UCN-5825B ..... 1.75 A
- UCN-5826B ..... 1.75 A
- UCN-5890A/B ..... −350 mA
- UCN-5891A/B ..... −350 mA
- UCN-5895A ..... −120 mA

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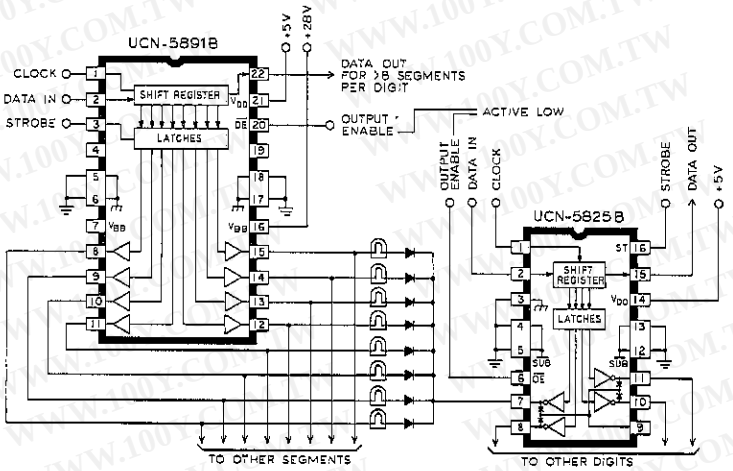


MULTIPLEXED LED DRIVERS

LATCHED source drivers are simple, compact, and economical segment drivers for multiplexed LED and incandescent lamp applications. The UCN-5895A features saturated outputs for minimum voltage drop. It sources a minimum of 120 mA per driver. The source driver is supplied in an economical 16-pin 'A' package.

A typical common-cathode LED display driver application is shown below. The high-current UCN-5821A, a latched sink driver, is used to drive the digits. Common-anode LED displays would require the use of the UCN-5891A source driver and UCN-5821A sink driver.

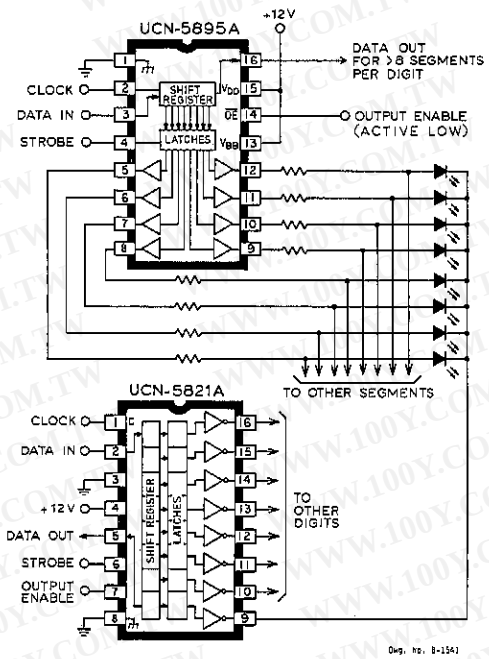
In order to obtain sufficient brightness, multiplexed LED displays must typically be operated at greatly increased current. Appropriate current limiting is required.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage
- UCN-5821A ..... 45 V
- UCN-5890A/B ..... 75 V
- UCN-5891A/B ..... 45 V
- UCN-5895A ..... 45 V

Logic Supply Voltage Range ..... 5.0 V to 12 V

Continuous Output Current
- UCN-5821A ..... 350 mA
- UCN-5890A/B ..... −350 mA
- UCN-5891A/B ..... −350 mA
- UCN-5895A ..... −120 mA



UNIPOLAR MOTOR DRIVERS

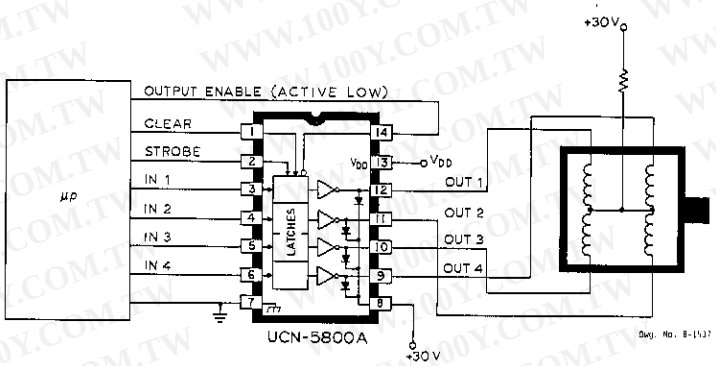
DRIVING unipolar motors is but one of the many successful applications for the UCN-5800A, UCN-5801A, UCN-5813B, and UCN-5814B BiMOS II latched sink drivers. The UCN-5801A is an eight-channel driver. The rest are four-channel drivers. The UCN-5814B includes CHIP ENABLE and CLEAR functions. Its larger 22-lead dual in-line package also allows increased package power dissipation without the use of an external heat sink. All devices contain CMOS data latches, CMOS control circuitry, and high-voltage, high-current bipolar Darlington outputs. Internal transient-protection diodes for use with inductive loads are included with all devices.

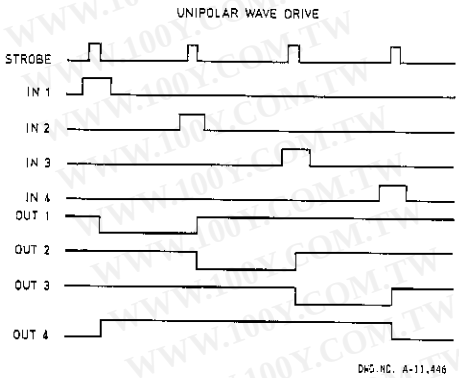
RECOMMENDED MAX. OPERATING CONDITIONS

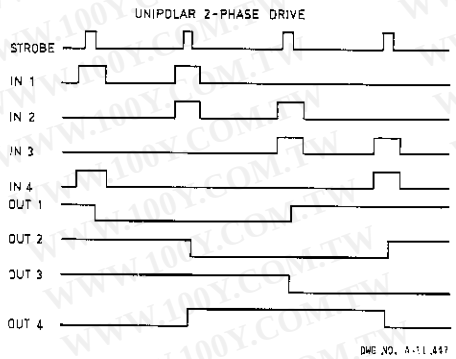
Output Voltage (Inductive Load)
- UCN-5800A, UCN-5801A, UCN-5813B, UCN-5814B ..... 35 V
- UCN-5813B-1, UCN-5814B-1 ..... 50 V

Logic Supply Voltage Range ..... 5.0 V to 12 V

Continuous Output Current
- UCN-5800A ..... 350 mA
- UCN-5801A ..... 350 mA
- UCN-5813B/B-1 ..... 1.5 A
- UCN-5814B/B-1 ..... 1.5 A







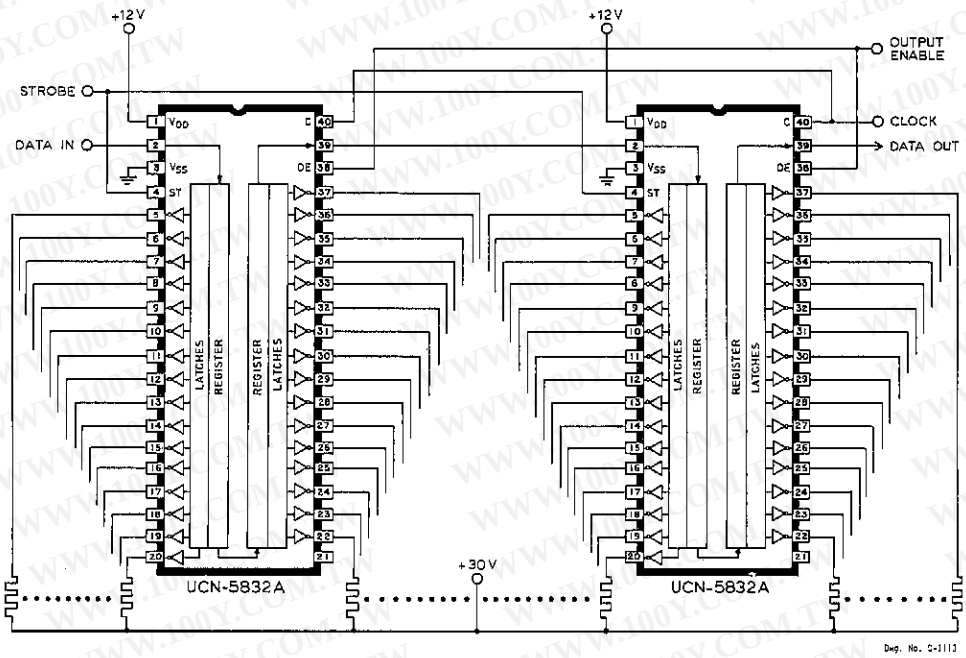
THERMAL PRINTHEAD DRIVER

DESIGNED primarily for use with thermal printheads, the UCN-5832A is optimized for low output-saturation voltage and high-speed operation. Each device has 32 bipolar, open-collector saturated outputs, a CMOS data latch for each driver, a 32-bit CMOS shift register, and CMOS control circuitry. A CMOS serial data output allows these devices to be cascaded in applications requiring more than 32 bits.

The UCN-5832A is supplied in a 40-pin DIP with 0.600" row spacing. Under normal conditions, all outputs will sustain 100 mA continuously without derating. They can also be supplied in unpackaged chip form or in a leaded chip carrier.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage . . . . . 40 V
Logic Supply Voltage Range . . . . . 5.0 V to 12 V
Continuous Output Current . . . . . 100 mA



IMPACT PRINT-HAMMER DRIVERS

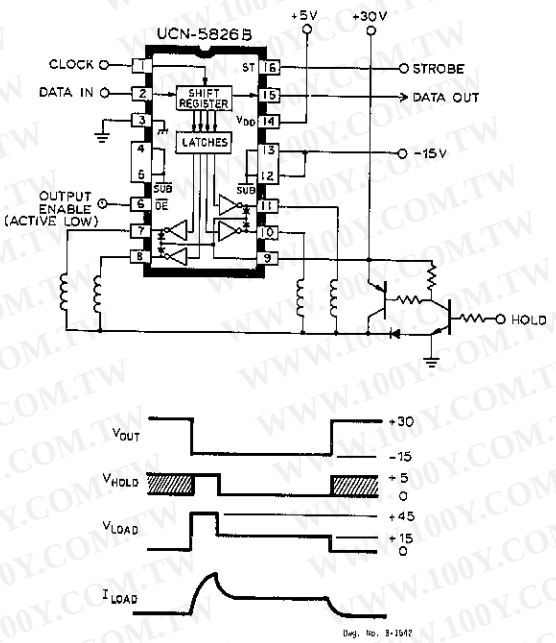
THE UCN-5825B and UCN-5826B 4-bit shift register/latched drivers are specifically designed for use with high-current inductive loads such as impact printers, solenoid, relays, and stepper motors. A CMOS serial data output allows cascading drivers where more than 4 bits is required. Except for output-voltage ratings, the two drivers are identical.

A bilevel current driver is shown. This application takes advantage of the split supply capability of the device. A relatively high turn-on current provides for high-speed operation and overcomes the inertia of a heavy solenoid or relay armature. The reduced holding current generates minimum heat and allows for improved power supply efficiency.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage (Inductive Load)
- UCN-5825B ..... 35 V
- UCN-5826B ..... 60 V

Logic Supply Voltage Range ..... 5.0 V to 12 V
Continuous Output Current ..... 1.75 A



RELAY AND SOLENOID DRIVERS

BiMOS II DRIVERS provide an interface flexibility beyond the reach of standard logic buffers and power-driver arrays. Drivers with internal transient-suppression diodes are ideal for use with relay and solenoid loads.

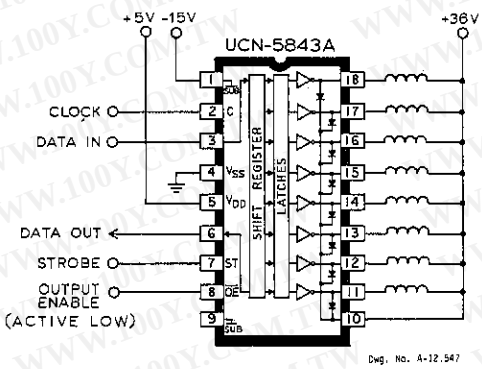
Series UCN-5840A sink drivers feature isolated logic and power grounds that allow split-supply operation or isolated grounds for reduction of transients and noise currents on common logic/load ground lines. The UCN-5890A and UCN-5890B source drivers require load supply voltages of at least 20 V. For lower-voltage operation, the UCN-5891A or UCN-5891B is recommended.

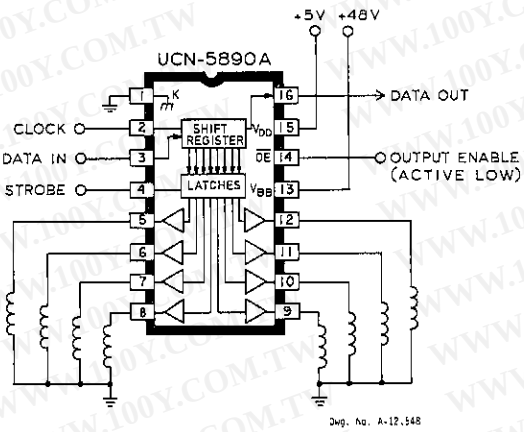
The serial DATA OUTPUT allows cascading for interface applications requiring additional drive lines. The OUTPUT ENABLE can also provide a CHIP ENABLE function that uses a minimum number of drive lines to control output from several packages in a simple multiplex scheme.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage (Inductive Load)
- UCN-5841A . . . . . 35 V
- UCN-5842A . . . . . 50 V
- UCN-5843A . . . . . 60 V
- UCN-5890A/B . . . . . 50 V
- UCN-5891A/B . . . . . 35 V

Logic Supply Voltage Range . . . . . 5.0 V to 12 V
Continuous Output Current . . . . . 350 mA



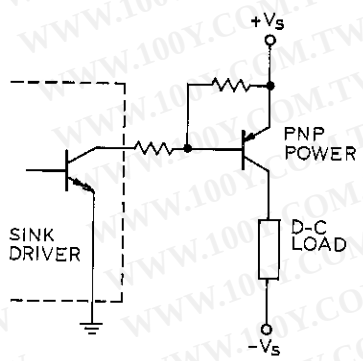


MULTI-CHANNEL INTERFACE TO HIGH-POWER LOADS

SPRAGUE BiMOS II power drivers can also be used as multi-channel pre-drivers for discrete high-current semiconductors, reducing the need for many discrete components. BiMOS II sink drivers provide enough switching current to the bases of discrete PNP power transistors for load currents of up to 20 A. Higher load currents can be obtained by using power Darlington devices. BiMOS II source drivers may require discrete Darlington power drivers for significant load currents, but have the advantage of allowing rather wide load-voltage swings.

Higher voltage requirements can be satisfied with discrete semiconductors or with the BiMOS III devices described below.

For a-c loads, source drivers can be used to provide gate current (with appropriate current limiting) to a power SCR or triac. This scheme can provide an economical approach to many applications such as driving incandescent lamps or a-c motors with current levels of up to 20 A.



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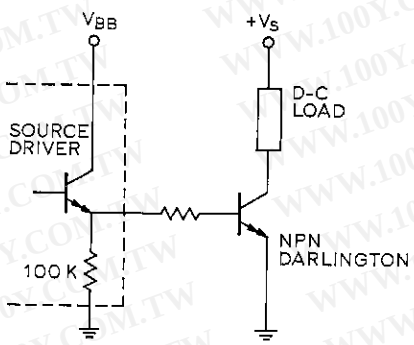

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BiMOS ICs FOR ELECTROLUMINESCENT DISPLAYS

INTRODUCTION

Sprague Electric Company has introduced a new set of 32-channel EL driver chips that utilize the patented BiMOS process. BiMOS incorporates CMOS and high-voltage bipolar devices on the same junction-isolated substrate. Among the advantages of BiMOS technology are microprocessor compatability, low-power logic with superior noise immunity and supply voltage range, high-current bipolar output capability, and space-saving integration with its corresponding component-count reduction. A brief description of the BiMOS process and the ac TFEL drive scheme is followed by an analysis of the design and performance of the row and column driver chips, UCN-5851/52 and UCN-5853/54, respectively. The row driver chip incorporates a 32-bit shift register with OUTPUT ENABLE and STROBE together with 32 high-voltage open-drain DMOS transistors, each capable of withstanding 280 V and sinking 120 mA. The column driver chip is composed of a 32-bit shift register, 32-bit latch, OUTPUT ENABLE circuitry and 32 source-sink outputs rated at 80 V and ± 20 mA. Each chip is pin-compatible with existing 32-channel EL drivers, and is available with clockwise or counter-clockwise output sequencing to facilitate layout of printed circuit boards.

THE EL SYSTEM

The electroluminescent display is a matrix of pixels, usually square, formed by the intersections of row and column electrodes that are bonded to the back and front, respectively, of the insulated active layer. The active region consists of an electroluminescent layer (ZnS doped with Mg) electrically isolated on both sides by an oxide dielectric. The intersection points of the row and column electrodes form capacitors that, when charged beyond a certain threshold voltage, provide sufficient electric field for photonic emission in the luminescent layer. Although the brightness vs. applied waveform characteristics of these pixel-capacitors are not fully understood, present refresh drive techniques produce a display with high readability, that is, good contrast under a variety of light conditions and an extremely wide viewing angle.

The threshold voltage for light emission is reached by driving the rows negative (-140 V) and the columns positive ($+40$ V to $+80$ V) relative to ground, resulting in a pixel voltage which equals the sum of both driving potentials. Individual pixel control is accomplished by selecting the rows one at a time and pulling high only those columns which correspond to ON pixels. (Figure 1).

After each complete scan, the entire display is refreshed by pulling all rows up to a high positive voltage through the row driver clamp diodes. This action reverses the applied pixel field, causing an additional light pulse and supplying the necessary bipolar drive waveform. The entire display is strobed about 60 times a second, resulting in a flicker-free image. The typical display size of 256 rows by 512 columns provides reasonable graphics capability and can display 25 lines of 80 characters each.

PROCESS TECHNOLOGY

The UCN-5851/4 EL driver chip set is fabricated using Sprague's highly adaptive BiMOS II process. Through this fusion of CMOS, bipolar and high-voltage DMOS technologies, Sprague enables the user to link microprocessors with high-voltage, high-current, and high-speed peripheral devices. The use of epitaxy permits the incorporation of high-performance, high-voltage bipolar devices while also maintaining controllable MOS thresholds. The up-down isolation that forms the device tubs permits the use of resurf field control, yielding N-channel DMOS devices that break down above 250 V. The up-down technique also reduces chip area by minimizing isolation-wall side diffusion.

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EL BLOCK DIAGRAM

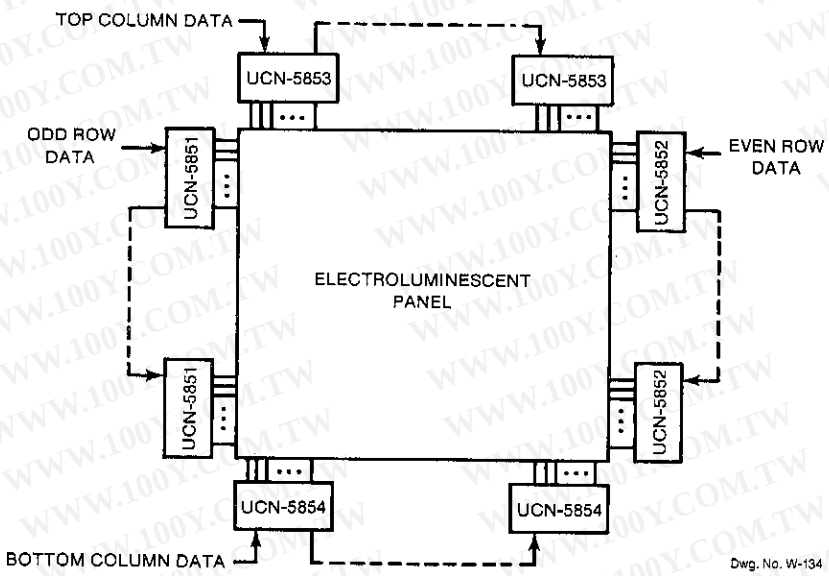

FIGURE 1

BIPOLAR PROCESS CROSS-SECTION

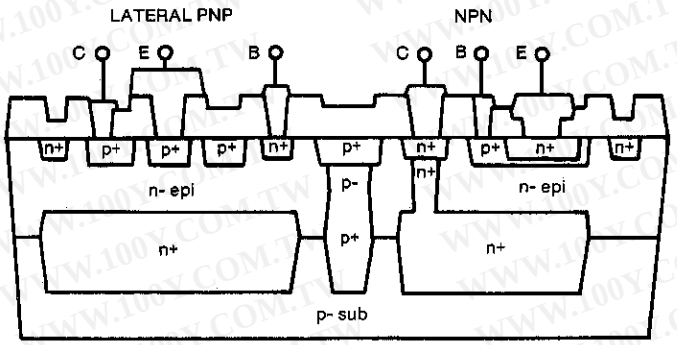

FIGURE 2

MOS PROCESS CROSS-SECTION

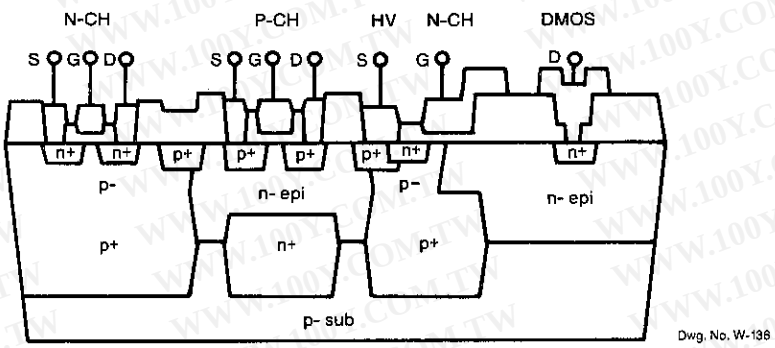

FIGURE 3

Figures 2 and 3 show process cross-sections for BiMOS II. The devices available are low-voltage PMOS, low-voltage NMOS, lateral PNP, vertical NPN and N-channel DMOS transistors. The low-voltage NMOS devices are built in the p-well, which also serves as the DMOS gate region and upper isolation. The P+ buried layer beneath the low-voltage NMOS prevents parasitic CMOS latch-up, and also serves as the lower isolation. The low-voltage PMOS and lateral PNP transistors are built with the same P+ diffusion, which is suitably controlled to provide the NPN base regions and low-resistivity diffused resistors. The shallow N+ regions serve as low-voltage NMOS sources and drains, and also as the NPN emitter diffusions. Also available to the designer are polysilicon resistors at 2kΩ per square.

The voltage capabilities of the NPN and PNP transistors range from 5 V to 100 V, depending on layout spacings. Higher voltage devices require N+ guard rings as shown in the bipolar cross-section. The high-voltage PNP requires field plating for reliability considerations. The high-voltage N-channel DMOS, field plated over drain and body regions, may be constructed to yield breakdowns from 100 V to over 300 V. Test devices are still being characterized to determine the effects of the P+ buried layer resurf shelf on breakdown voltage.

ROW DRIVER BLOCK DIAGRAM

The UCN-5851/52 row driver function is shown in the block diagram of Figure 4. The row driver consists of a 32-bit shift register with OUTPUT ENABLE and STROBE lines which can be used to turn all 32 outputs ON or OFF. Data enters the shift register on the high-to-low clock transition, a logic "1" input causing the corresponding DMOS output to pull low. Typically, a single "1" is clocked through the shift register and the rows are pulled low one at a time using OUTPUT ENABLE. After a complete scan the substrate common (GND) pin is pulled high, forward-biasing the body-

ROW DRIVER BLOCK DIAGRAM

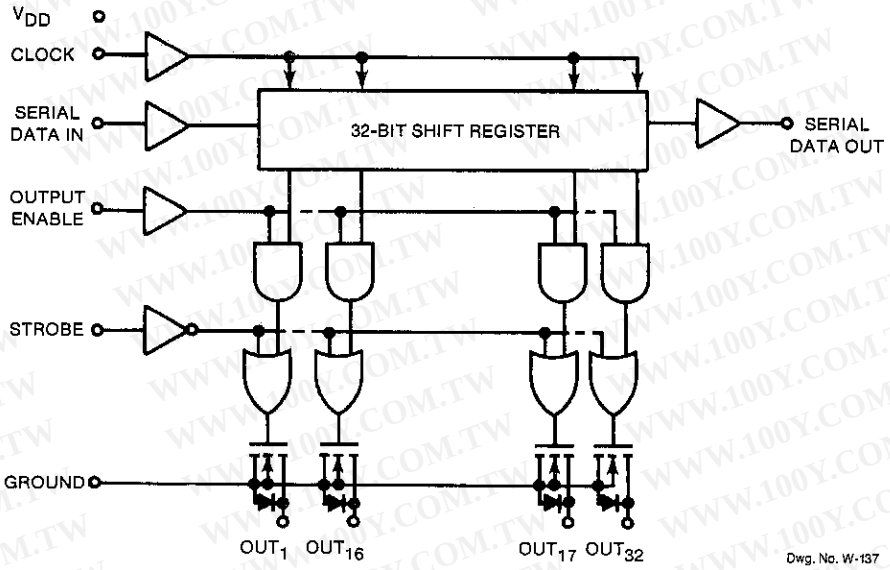

FIGURE 4

drain diodes present in each DMOS structure, and pulling all outputs high.

Since the DMOS gates switch between ground and V_{DD}, output current capability is strongly affected by the logic supply voltage. At V_{DD}, = 5 V, the output ON resistance is about 300Ω, decreasing to approximately 100Ω at V_{DD} = 12 V. A serial DATA OUT pin is provided for cascading the shift register.

COLUMN DRIVER BLOCK DIAGRAM

The block diagram of Figure 5 shows the UCN-5853/54 column driver. Like the row driver, the device contains a 32-bit shift register with a serial output for cascading additional drivers. However, data enters the shift register on the low-to-high clock transition, with a data "1" causing the corresponding output to turn ON. In this state the output sources

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COLUMN DRIVER BLOCK DIAGRAM

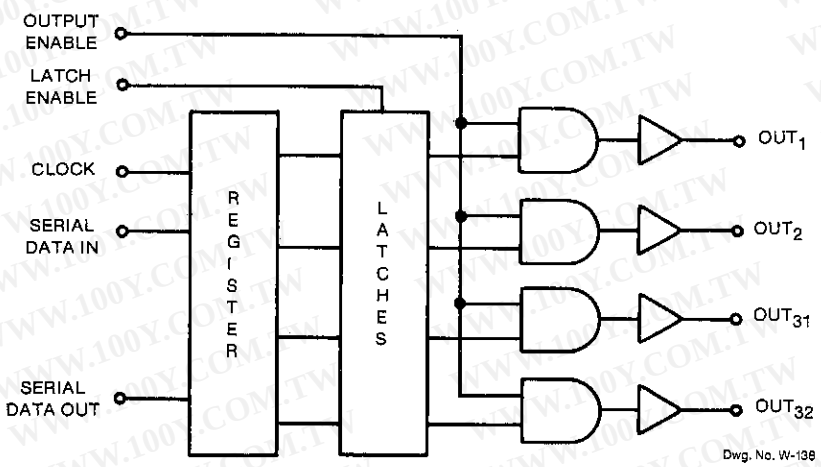

FIGURE 5

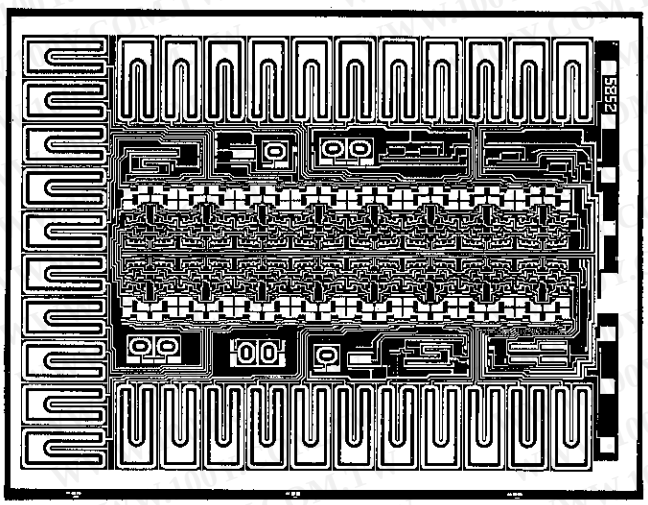

FIGURE 6

current from the high-voltage Darlington drive, causing an ON pixel. The column driver also contains a 32-bit latch that serves to hold currently displayed information while a new set of data is being clocked through the shift register. The transfer of data from shift register to latch is controlled by the LATCH ENABLE input. The shift register data present at the negative-going edge of the LATCH ENABLE signal is retained in the latch. An OUTPUT ENABLE "0" causes all outputs to pull low regardless of the data present in the latch. The ground-clamp diode shown is the inherent N-DMOS body/drain diode, while the supply rail diode is an added diffusion in the high-voltage pocket.

ROW DRIVER PHOTO

Figure 6 shows the row driver layout in silicon form. The 32-bit shift register and gating logic are contained in the center, and the large NMOS and PMOS transistors, which drive the output gates, can be seen on either side of the CMOS array. The 32 high-voltage N-channel outputs are lateral open-drain DMOS devices. These occupy three sides of the chip, while the remaining end is used for logic and ground pads. All front-end buffers and input protection are contained in the spaces between the CMOS logic and DMOS outputs. In addition, eight small high-voltage test devices can be seen in areas adjoining the logic buffers.

COLUMN DRIVER PHOTO

The silicon implementation of the column driver chip can be seen in Figure 7. As in the row driver, the center area contains the CMOS logic array, which is comprised of a 32-bit shift register, 32-bit latch, gating logic, and inverters to drive the source and sink sections of the output cells. All logic and supply pads are on one end of the chip flanked by their resective buffers and input protection. The other three sides of the chip contain the 32 sink-source outputs, 10 of which were relocated to the chip end to facilitate bonding. The Darlington source drivers can be seen just inside the high-voltage supply metal bus, while the output pads and lateral high-voltage N-channel DMOS sink transistors lie outside on the periphery of the chip.

COLUMN DRIVER OUTPUT SECTION

The column driver output section is shown in Figure 8. It consists of a bipolar level shift, bipolar source drive and lateral N-channel DMOS sink transistor. The level shift is driven by the CMOS logic through a resistor divider, which minimizes the static logic current (I_{DD}) when the source input is high. The level shift current, drawn from the high-voltage supply rail, is limited to about 60 μA per channel. This yields about 2.0 mA per chip, a 70 percent improvement over first generation EL column drivers. The level

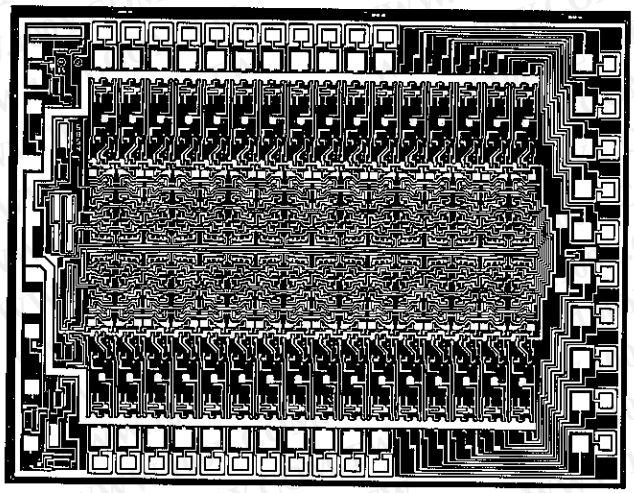

FIGURE 7

shift drives a high-voltage lateral PNP which in turn drives the Darlington output. The gate of the DMOS sink transistor is driven by the CMOS logic, out-of-phase with the source input.

The circuit configuration ensures minimum crossover current, because the DMOS transistor must turn OFF the source drive before any current may be pulled from the output. This feature also bypasses any turn-off delay associated with the slow lateral PNP transistor, enabling the output structure to switch at speeds greater than 400 kHz. The series diode does not add appreciably to the DMOS saturation voltage.

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COLUMN DRIVER LEVEL SHIFT AND OUTPUT

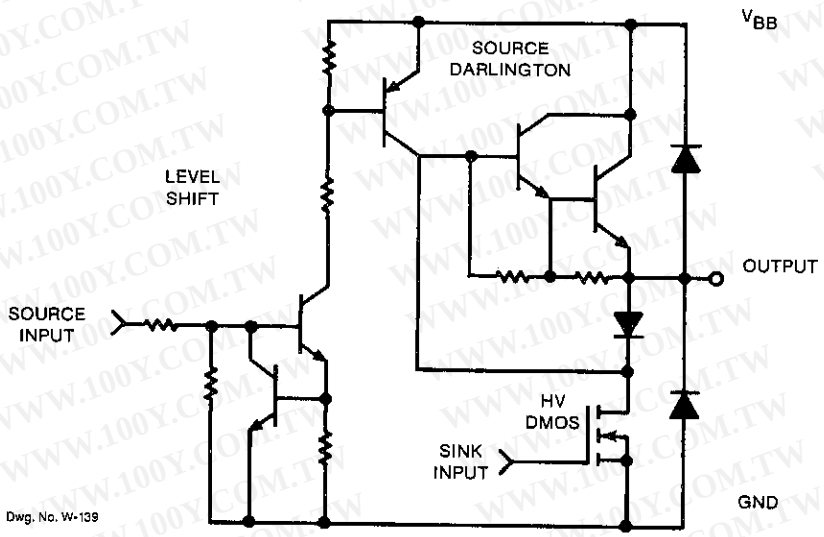

FIGURE 8

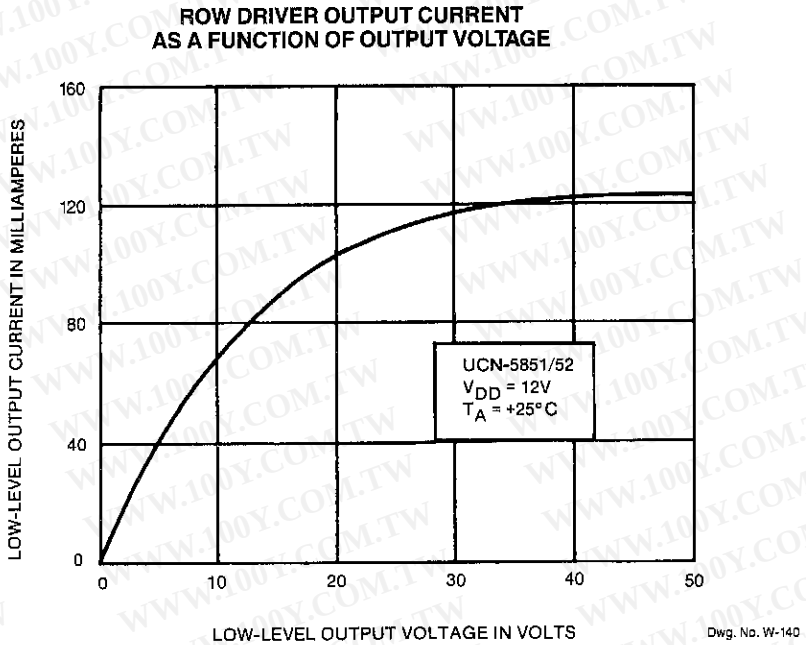

FIGURE 9

ROW DRIVER RESULTS

The current and voltage characteristics of the high-voltage open-drain DMOS device are shown in the graph of Figure 9. At +25°C, the typical ON resistance is 100Ω and the saturation current (taken at V_{DS} = 30 V) is about 120 mA, a 50 percent improvement over first generation devices. The saturation current varies with temperature from 87 mA at +125°C to 132mA at 0°C. At a sink current of 50mA, the voltage drop is 6.5 V at +25°C, increasing to 13.2 V at +125°C, yielding a temperature coefficient of 67mV/°C.

In the OFF state, leakage is typically below 0.1 μA and is constant until avalanche breakdown is encountered at about 280 V. The device can switch 250 V and 120 mA. No latching will occur, even if the load is decreased to 0Ω raising the instantaneous power dissipation to over 30 W. This square safe operating area enhances the reliability of the device while increasing the scope of possible applications. The switching speed, though probably limited by the CMOS output inverter current capability, exceeds 1MHz. The body-drain diode exhibits a voltage drop of 1.15 V at 100mA. Logic power dissipation is 0.1mW at f_{CLK} = 10kHz, increasing to 10mW at a 1MHz clock rate.

COLUMN DRIVER RESULTS

The capability of the column driver is determined by the sink and source current capability, and by the speed and efficiency of the push-pull output stage. The graph in Figure 10 illustrates the current capability of the bipolar Darlington source driver. The saturation voltage in the linear region, measuring 2.5 V at 20mA, is better than can be economically achieved using a MOS source device. This voltage is important because it represents power wasted in the column driver outputs each time a pixel is turned ON. A 1 V difference in source saturation voltage may lead to as much as 250mW of unnecessary power dissipation. At 20mA, the source saturation voltage varies from 2.05 V at 0°C to 1.9 V at +125°C, giving a temperature coefficient of −1.2m V/°C.

COLUMN DRIVER SOURCE CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

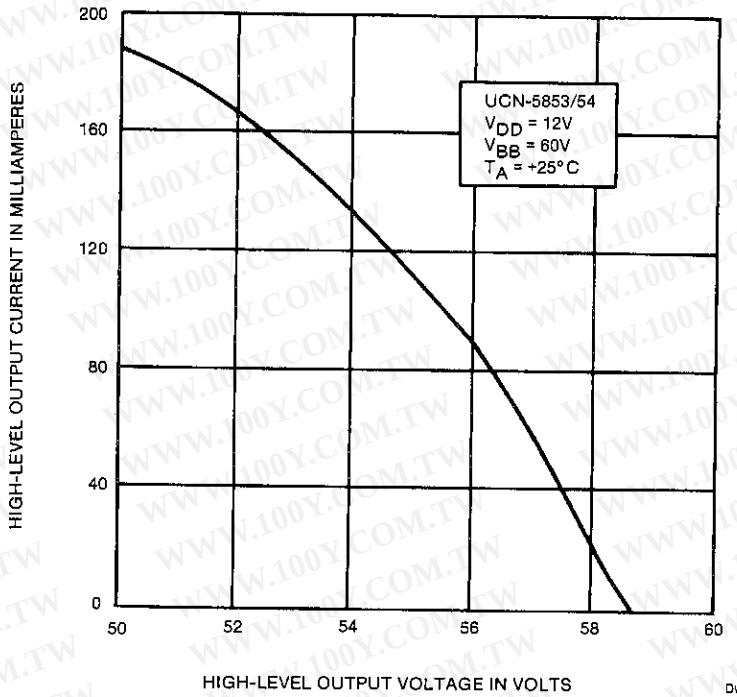

FIGURE 10

The voltage/current characteristic of the N-channel DMOS sink device is shown in Figure 11. At +25°C, the ON resistance is 305Ω. The saturation current is 41mA, measured at 25 V. At 20mA, V_{DS} varies from 6.6 V at 0°C to 8.2 V at +125°C, yielding a 12.8mV/°C temperature coefficient. The body/drain diode in the DMOS device shows a forward voltage drop of 1.18 V at 20mA (+25°C). The V_{BB} rail clamp diode drops 0.91 V at 20mA and +25°C. The actual breakdown voltage from the V_{BB} rail to ground exceeds 90 V.

The output switching speed exceeds 400kHz at 80 V with a 30pF load to ground. Investigation is currently underway to determine the output power dissipation due to switching losses and capacitive charging, which varies with output switching speed and duty cycle. Static leakage is very low during both high and low output states. The logic dissipation is about 0.1mW at f_{CLK} = 10kHz under typical conditions, increasing to 8.5mW at a 1 MHz clock rate.

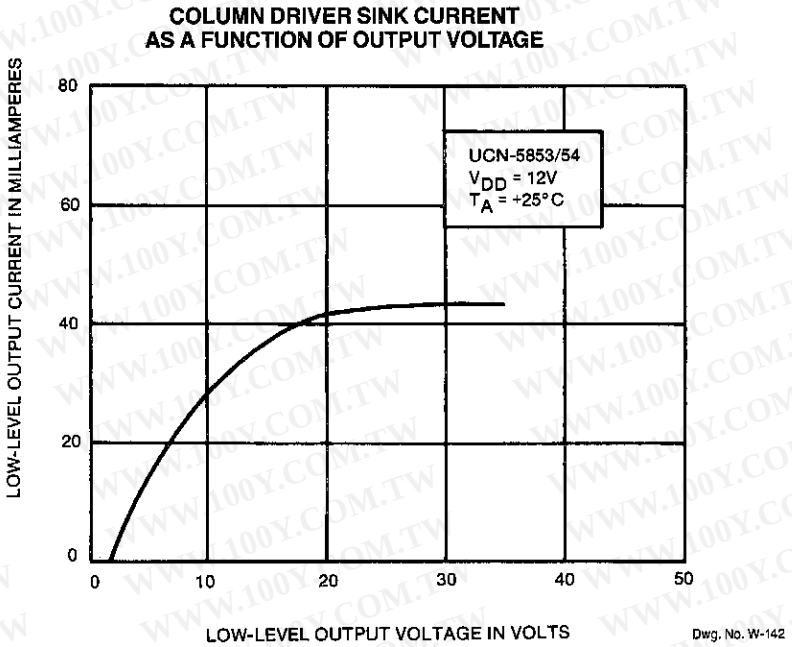

FIGURE 11

CONCLUSION

The Sprague UCN-5851/52 and UCN-5853/54 EL driver chip set offers increased performance and reliability, meeting the increasing demands of the display industry. Higher voltage column drivers mean increased display brightness and contrast, while giving the assurance of a larger safety margin in operation. Greater current capability minimizes pixel brightness variations, which can be caused by varying line resistances and changing electrode capacitances. The higher current and high speed also permit the use of larger panels as user needs increase. The ruggedness of these drivers is enhanced by the wide current and voltage margins, as well as by the square safe operating area of the sink devices, and the high-current clamp diodes. Both parts are available in 40-pin DIPs (plastic and cer-DIP), 44-pin plastic leadless chip carriers, 44-pin hermetic cerquad packages, and in chip form for TAB installation.

References

Texas Instruments Display Driver Handbook, 1983.

Driving Large Matrix AC Thin-Film Electroluminescent Displays, by Greg Draper.

Thin-Film Electroluminescent Displays, by Christopher N. King, SID Seminar Digest, April-May 1985.

BiMOS: A MERGED TECHNOLOGY FOR CUSTOM AND SEMI-STANDARD POWER INTERFACE ICs

BiMOS power interface continues to advance its technological capability, expand to new applications and users, afford a growing product selection, provide cost-reduction solutions, and offer improved reliability and increased alternate sourcing. However, with the recent focus on other merged technologies, many have overlooked BiMOS. This paper highlights limits, relative merits, and newer developments in BiMOS power integrated circuits.

INTRODUCTION

Smart power interface ICs originated within Sprague Electric in 1977, and became a quiet revolution with an intuitive, innovative shaping of technology to satisfy a need. These power integrated circuits began with a creative evolution of power interface circuitry dating to 1970. The merging of bipolar (Bi) with CMOS (MOS) logic was driven by an exploding need for power interface compatible with microprocessors. Initially, it combined a quad "D" latch with four high-current/high-voltage Darlington outputs. Although not normally attempted, both a *new product* and a *new process* were *concurrently* and *successfully attempted*. The breakthrough spawned semi-standard BiMOS power interface.

Semi-standard power interface ICs were the response to applications-driven or market-driven developments that propelled BiMOS as a very important technology. This market (applications) driven strategy produced a variety of products targeted, increasingly, toward specific applications and multiple customer use. Expectations are for this to continue. However, other forces (particularly the focus on semi-custom ICs and the ability to simplify customizing) are stimulating an increased *diversity*. With a mature process, a CAD library and tools, *diversity* means keen interest in and heightened demand for custom BiMOS power integrated circuits.

Table 1 — BiMOS Evolution

BiMOS	CMOS Logic			Bipolar Power			Relative Traits	
	Dimension	Logic	Speed	Outputs and Ratings			Advances	Merit/$
I	8 μN/10 μP	5-18 V	1 MHz	NPN/PNP	<100 V	>500 mA	Oldest	Good
II	8 μN/10 μP	5-15 V	5 MHz	NPN/PNP	<100 V	>2 A	Speed/Size	Lower
III	8 μN/12 μP	5-15 V	5 MHz	+ DMOS	>200 V	>100 mA	High Voltage	Modest
IV	5.5 μN/7 μP	5-7 V	5 MHz	All	<100 V	>2 A	Density/$	Lowest

DIVERSITY: DRIVING FORCE

Forces of diversity include systems manufacturers striving for new products rapidly tailored for specific applications, an acute awareness of semi-custom and custom ICs, increased semiconductor supplier use of CAD design and chip layout, automated processing, manufacturing, and testing of ICs, and (everywhere) swift, fierce international competition. All of these factors (and more) are stimulating new demands for a competitive advantage. They are accelerating the need for semi-standard (applications-driven) and custom smart power BiMOS ICs.

Aiding movement toward greater diversity are expanded product offerings, a large number of new users, ever-broadening applications, and recent technological developments. From inception in 1977, BiMOS has become a mature, high-volume technology that has advanced and diversified with later generations. Second generation BiMOS provides size and chip-cost reductions and greatly improved switching speeds. Another later generation (BiMOS IV) cut chip size even further to reduce cost per output. BiMOS III provides high-voltage outputs (150-200 V).

More recent circuits often include functions not originally used. Added to the bipolar power/CMOS logic basics are analog functions (control and amplifiers) and protective circuitry (thermal, over-current). This potential for diversity is also enhanced by possible combinations of bipolar (power or analog), CMOS logic, power (vertical) DMOS outputs, high-voltage (lateral) DMOS outputs, and improved protection diodes.

The potential for further diversity involves a better awareness of the technology and a determination of whether a circuit should be custom or semi-standard. Many new IC programs have begun as discussions of custom devices, only to evolve into non-proprietary semi-standard ICs as volume criteria, design funding and decision delays preclude exclusive use.

TECHNOLOGY CHARACTERISTICS

Over the past several years BiMOS has followed an Olympian path (faster, higher, farther) as developments in process technology, increases in voltage, current, and power, and many new circuit functions and applications have formed an explosive, accelerating force dubbed "smart power." From the original quad latch/driver IC rated at 50 V/500 mA per output, BiMOS has expanded to 32-bit drivers (64-bit in the offing), 200 V levels, 2 A/output, and a variety of shift registers, latches, random logic, protection diodes, and protective circuitry such as thermal shutdown. Logic (shift register) speeds have climbed to over 5 MHz (from 1 MHz, 5 V logic) as CMOS was shrunk to improve performance and reduce cost. The conservative approach to BiMOS has resulted in 3.5-4 A peak ratings for 2 A driver outputs, and, often, the option of voltage selections that exceed nominal ratings at very little additional cost.

The evolutionary changes in circuit capabilities and specifications are listed in Table 1. Early concerns included faster shift register speeds, smaller and lower cost chips, and high-reliability military packaging and screening. Subsequently, concerns for higher current and power, considerably higher voltages (>100V), smaller packages (now SMD versions), and more outputs per chip (serial-input ICs) spurred further variations of BiMOS. The characteristics of BiMOS I through IV offer a technology choice based upon system design requirements, although the first generation (BiMOS I) is no longer used for new designs. The second generation (BiMOS II) will be superseded, primarily, by the smaller BiMOS IV versions.

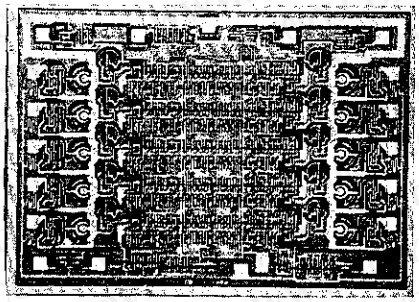

FIGURE 1
UCN-4810 10-Bit Driver — 60V, 50 mA
16050 sq. mils

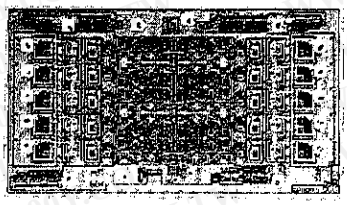

FIGURE 2
UCN-5810 10-Bit Driver — 60V, 50 mA
8885 sq. mils

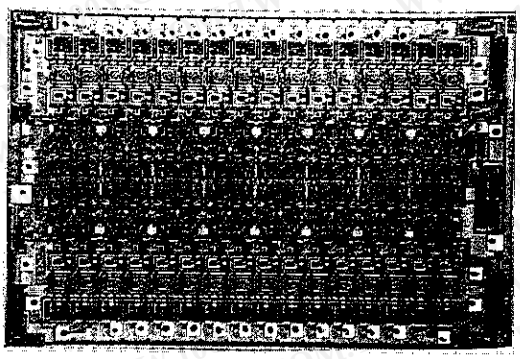

FIGURE 3
UCN-5818 32-Bit Driver — 60V, 50 mA
23495 sq. mils

All BiMOS versions now have metal-gate CMOS inputs; however, the use of silicon gate technology may further enhance BiMOS power interface. Current density requirements dictate use of heavy (thick) aluminum interconnect for the high-current circuitry, and the 25 kÅ metallization has complicated any early change to silicon gate CMOS. It should be noted that polysilicon is now used for high-value circuit resistors in a number of the present power integrated circuits, so a future conversion to silicon gate technology is anticipated. Also of concern is the increasing use of two-level metallization (now used for high-current bipolar power integrated circuits). As chip outputs increase in number and current, the two-level interconnect offers advantages of current density (per unit area) and positively affects both performance and cost.

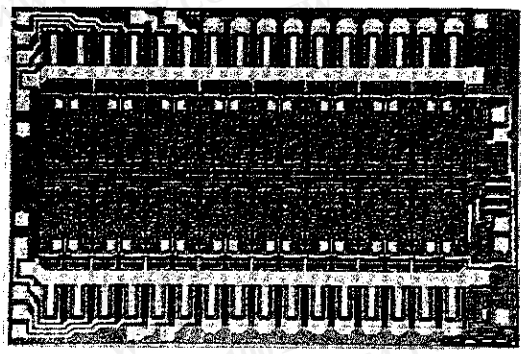

FIGURE 4
UCN-5832 32-Bit Driver — 40V, 150 mA
23250 sq. mils

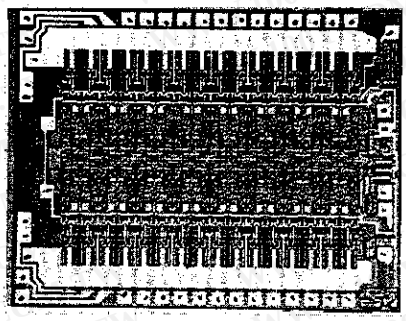

FIGURE 5
UCN-5833 32-Bit Driver — 40V, 100 mA
15873 sq. mils

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EVOLUTION

An important comparison is shown in Figures 1 through 5. In Figure 1 is an early BiMOS interface IC, a 10-bit serial-to-parallel driver rated at 60V and 50 mA. In the second generation UCN-5810 (Figure 2), the chip area is reduced by *45 percent*, while logic speed

increased by about *500 percent*. The 32-bit UCN-5818 in Figure 3 (also BiMOS II), is only 46 percent larger than the chip in Figure 1, although it contains 32 rather than 10 outputs.

Another 32-bit BiMOS II power integrated circuit (UCN-5832, Figure 4) is approximately the same size, but contains 32 outputs each rated at 100 mA and 50 V. Compare this to a BiMOS IV version with similar ratings, the UCN-5833 shown in Figure 5. A BiMOS IV version of Figure 3 would be a chip with about the same dimensions as those of Figure 5.

The BiMOS evolution has produced much more complex power integrated circuits without increasing chip size. This increase in circuit density dramatically affects performance and cost while adding new prospects for single-chip interface ICs.

One BiMOS development is embodied in the larger, high-voltage UCN-5910 (not shown). This BiMOS III (150-200 V) 10-bit IC is a functional equivalent to Figures 1 and 2. The present high-voltage technology yields chips comparable in size to the original BiMOS ICs, although switching performance is far inferior to the BiMOS II and IV processes. The hybrid nature of the newer BiMOS, with its ability to provide high-voltage lateral DMOS, may allow shrinking of many future high-voltage smart power ICs, especially those with low to modest current outputs.

Another aspect of the evolution is illustrated by higher power ICs. The *original* BiMOS power integrated circuit was the UCN-4401, a quad latch/driver rated at 50 V (inductive, 35 V) and 500 mA per output. The much newer, high-power UCN-5826 is a four-bit serial-to-parallel IC with a 60 V (inductive) sustaining voltage rating and a conservative, continuous current rating of 2 A (peak, 3.5-4 A). Despite addition of a shift register, improvement of inductive voltage capability, and dramatically increased output current, the change in chip size was minimal (from 7200 to 19300 sq. mils). Future designs with bipolar outputs and two-level interconnect will further reduce the size of high-current chips and allow lower output ON impedance to minimize power dissipation. Merged chip designs, needing increased switching speed and improved safe operating area, will adopt increased use of high-current DMOS (vertical) outputs. BiMOS offers a mix-and-match technology that can combine vertical and lateral DMOS outputs with the older, proven bipolar types.

TECHNOLOGY COMPARISON

Distinguishing between competing power IC technologies is increasingly difficult, and especially so among the merged processes. BiMOS is based upon a bipolar process. Adding CMOS logic means additional process and masking steps beyond either linear bipolar or

Table 2 — Technology Comparison

	Output Characteristics			Logic Traits			Technological Merit		
Process	Limits	Drive	Form	Density	Power	Speed	Complexity	Cost	Maturity
Bipolar	8 A/60 V	High	PNP/NPN	Low	High	Slow	Low	Low	Oldest
I^2L	8 A/35 V	High	PNP/NPN	Medium	Modest	Modest	Low/Mild	Mid	Proven
BiMos	4 A/200 V	High	PNP/NPN	High	Very Low	Fast	High	High	Proven
C/VDMOS	2 A/60 V	Low	NMOS[1]	High	Very Low	Fast	High	High	Recent
C/LDMOS	0.5 A/300 V	Low	NMOS[2]	High	Very Low	Fast	High	High	Proven

NOTES:
1) Bootstrapping NMOS normally used for source outputs, although PNP can be implemented.
2) Bootstrapping required (charge-pump circuitry and emitter-follower scheme) for source outputs.
3) I^2L: Includes both single and double epitaxial process limits.
4) C/VDMOS = CMOS/Vertical DMOS
5) C/LDMOS = CMOS/Lateral (high-voltage) DMOS

I²L. Presently, BiMOS provides power and analog bipolar, CMOS logic (metal-gate, medium-density), high-voltage, medium-current lateral DMOS, high-current, medium-voltage vertical DMOS, improved (very low parasitic beta) flyback diodes, polysilicon or diffused resistors and protective functions:

Bipolar
- Power Outputs — NPN and PNP
- Analog Amplification and Control
- Diodes — Output Transient Protection

Merged Outputs
- P-Channel/NPN (Source)
- N-Channel/NPN (Sink)

MOS
- CMOS Logic (Analog Possible)
- Power Outputs — Vertical DMOS (N-Channel)
- High-Voltage Outputs — Lateral DMOS (NMOS)

Control/Protective
- Thermal Shutdown
- Over-Current
- Over-Voltage
- Power-On Reset

Passive Components
- Diffused Resistors 150 Ω /square
- Polysilicon Resistors — 2 kΩ/square

Compared to competing technologies, BiMOS offers a greater variety of output ratings and functions, speed and power advantages of CMOS logic, and competitive cost. It provides single-chip, complex, multiple output Smart Power ICs, proven military reliability, and a maturity unequaled by other alternatives.

The evolution of BiMOS semi-standard power interface started with a user need to combine a power array (bipolar) with an octal latch (CMOS) and continues to provide performance, size/space, reliability, and cost advantages. (One 32-bit IC approaches five cents an output.) Although these semi-standard, applications oriented power integrated circuits will endure, another potential and largely overlooked market exists in *custom* BiMOS power. With the tools listed previously, user/vendor partnerships can create new and superior products for nearly any system.

Highlighting the possibilities are recent activities with innovative leaders in:

Appliances
ATE/Instrumentation
Automotive
Brushless DC Motors
Flat Panel Displays
Military Avionics
Printers (Impact and Impactless)
Telecommunications

Many of these discussions have focused on design and development of generic or semi-standard BiMOS ICs. However, recent dialogue has, increasingly, been oriented toward custom programs. A particular system design might be optimized with a different combination or number of the ingredients listed earlier. Examples include a 24-bit driver, a 115 V line-operated brushless dc motor circuit, special ICs for telecom, MUX driver ICs for automotive, and CMOS logic readback for ATE and instrumentation.

CUSTOM BiMOS

Originally developed for specific applications and functions, BiMOS power integrated circuit technology is now a ready, mature, and cost-effective approach for *custom* programs. It must be noted that Sprague does *not* envision a workable semi-custom potential for BiMOS power ICs. The variables of voltage, current, logic, output lines, protection, packaging and testing tend to overwhelm any prospect of creating semi-custom chips. The established direction toward semi-standard ICs will continue but many new activities will branch into custom ICs.

The creation of a custom BiMOS power integrated circuit, optimized for a specific system, is quite straightforward and uses a proven CAD cellular library of functions (latch, S/R, thermal shutdown) and components (bipolar power cells, PNPs) to assemble a new circuit. However, despite this cellular design technique, new BiMOS power integrated circuits are much like other custom designs and take much longer than any conventional semi-custom design. The disadvantages of design funding and longer program schedules may be

balanced by the cost and performance advantages of an optimized, volume design. With improvements in logistics, the elapsed time for a custom BiMOS design is expected to diminish, and allow an early strategic advantage to the swift and sure.

APPLICATIONS EXAMPLES

As mentioned previously, opportunities abound for both custom and semi-standard BiMOS. Certain types of systems have a greater leverage factor (many power integrated circuits per design) than others. Impact and thermal printers, flat panel displays, and ATE (automated test equipment) represent types of uses with a high content of Smart Power ICs. To illustrate, typical printer examples are shown in Figures 6 and 7.

An example of a high-efficiency impact printer, using a split supply (bilevel current drive) is shown in Figure 6. Previously these printers have used vast quantities of TO-220 discretes. With this BiMOS design, both component count and cost are greatly reduced.

Another example is thermal printer drive. High-speed, high-resolution systems require a great many drive lines, as do flat panel, matrix displays. Space, package size, cost per output, and switching speed are important. Figure 7 is an example of a smart 32-bit driver (used both in chip and PLCC form) to meet space/resolution constraints. Newer BiMOS power integrated circuits dissipate considerable power, and high pin-count power packages are needed as output lines and currents escalate.

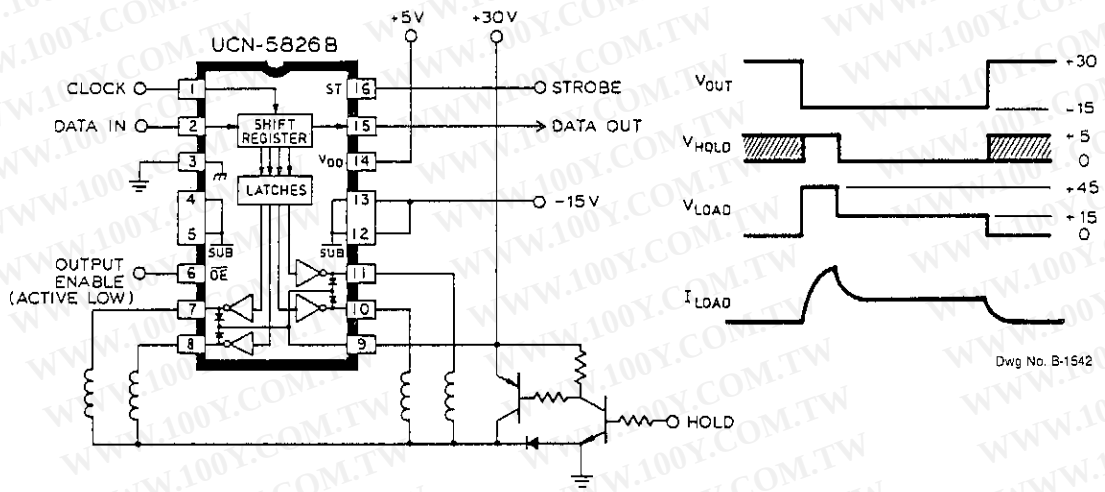

FIGURE 6
Serial-Input, High-Power (2 A) Impact Printer Driver

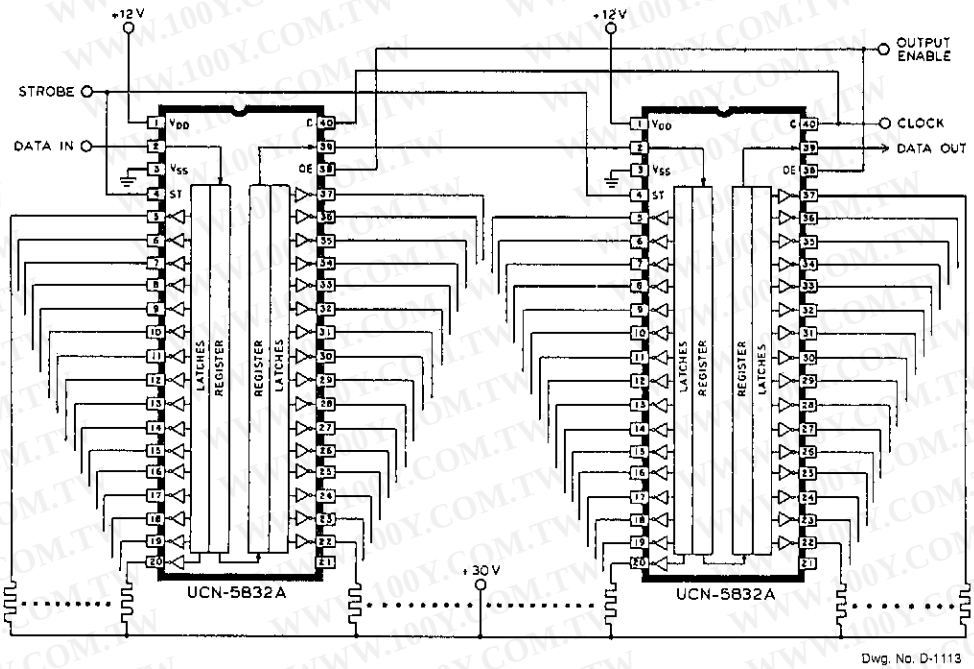

FIGURE 7
Serial-Input, 32-Bit Thermal Printhead Driver

CONCLUSION

Opportunities for custom BiMOS power interface are increasing. Users can take advantage of several years of evolution of design and process; a CAD library, automated testing, proven reliability, and cost and size reductions all gained through production experience. Technologically, BiMOS power affords an array of unsurpassed capabilities but lacks exploitation in custom ICs. Systems requiring many output lines are the most natural targets, although use is more limited by imagination than any other factor.

The increasing need for innovative products, rapidly executed and offering strategic advantages, focuses on greater diversity for system, function, and components. Key aspects of the increased use of custom BiMOS power ICs are maturity, technological advantages, innovation, swift execution, and diversity. Change and progress are relentless. BiMOS power is the ready-made technology for many of today's custom power ICs.

NOTES