



NC7WZ07 TinyLogic® UHS Dual Buffer (Open Drain Outputs)

Features

- Ultra-High Speed: t_{pZL} 2.3ns (Typical)
- High I_{OL} Output Drive: ± 24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range: 1.65V to 5.50V
- Power Down High Impedance Inputs/Outputs
- Over-Voltage Tolerance Inputs Facilitate 5V to 3V Translation
- Proprietary Noise/EMI Reduction Circuitry
- Ultra-Small MicroPak™ Packages

Description

The NC7WZ07 is a dual buffer with open drain outputs from Fairchild's Ultra-High Speed (UHS) series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra-high speed with high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over a very broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} range. The inputs and outputs are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 7V independent of V_{CC} operating voltage.

Ordering Information

Part Number	Top Mark	Package	Packing Method
NC7WZ07P6X	Z07	6-Lead SC70, EIAJ SC88 1.25mm Wide	3000 Units on Tape & Reel
NC7WZ07L6X	D3	6-Lead MicroPak™, 1.00mm Wide	5000 Units on Tape & Reel
NC7WZ07FHX	D3	6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch	5000 Units on Tape & Reel

Connection Diagrams



Figure 1. Logic Symbol

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Pin Configurations

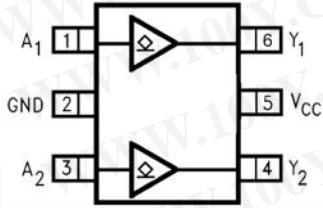


Figure 2. SC70 (Top View)

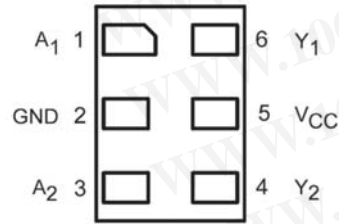


Figure 3. MicroPak™ (Top Through View)

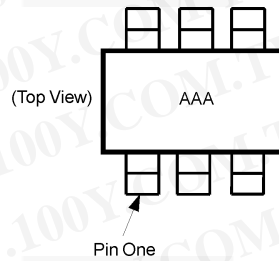


Figure 4. Pin 1 Orientation

Notes:

1. AAA represents product code top mark (see *Ordering Information*).
2. Orientation of top mark determines pin one location.
3. Reading the top mark left to right, pin one is the lower left pin.

Pin Definitions

Pin # SC70	Pin # MicroPak™	Name	Description
1	1	A ₁	Input
2	2	GND	Ground
3	3	A ₂	Input
4	4	Y ₂	Output
5	5	V _{CC}	Supply Voltage
6	6	Y ₁	Output

Function Table

Y = A

Inputs	Output
A	Y
L	L
H	H*

H = HIGH Logic Level

L = LOW Logic Level

H* = High Impedance Output State, Open Drain

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V _{CC}	Supply Voltage		-0.5	7.0	V
V _{IN}	DC Input Voltage		-0.5	7.0	V
V _{OUT}	DC Output Voltage		-0.5	7.0	V
I _{IK}	DC Input Diode Current	V _{IN} < -0.5V		-50	mA
I _{OK}	DC Output Diode Current	V _{OUT} < -0.5V		-50	mA
I _{OUT}	DC Output Current			±50	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current			±100	mA
T _{STG}	Storage Temperature Range		-65	+150	°C
T _J	Junction Temperature Under Bias			+150	°C
T _L	Junction Lead Temperature (Soldering, 10 Seconds)			+260	°C
P _D	Power Dissipation at +85°C	SC70-6		180	mW
		MicroPak™-6		130	
		MicroPak2™-6		120	
ESD	Human Body Model, JEDEC:JESD22-A114			4000	V
	Charge Device Model, JEDEC:JESD22-C101			2000	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V _{CC}	Supply Voltage Operating		1.65	5.50	V
	Supply Voltage Data Retention		1.5	5.5	
V _{IN}	Input Voltage		0	5.5	V
V _{OUT}	Output Voltage		0	5.5	V
t _r , t _f	Input Rise and Fall Times	V _{CC} at 1.8V, ±0.15V, 2.5V ± 0.2V	0	20	ns/V
		V _{CC} at 3.3V ± 0.3V	0	10	
		V _{CC} at 5.0V ± 0.5V	0	5	
T _A	Operating Temperature		-40	+85	°C
θ _{JA}	Thermal Resistance	SC70-6		425	°C/W
		MicroPak™-6		500	
		MicroPak2™-6		560	

Note:

4. Unused inputs must be held HIGH or LOW. They may not float.

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DC Electrical Characteristics

Symbol	Parameter	V _{CC}	Conditions	T _A =+25°C			T _A =-40 to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V _{IH}	HIGH Level Input Voltage	1.65 to 1.95		0.75V _{CC}			0.75V _{CC}		V
		2.30 to 5.50		0.70V _{CC}			0.70V _{CC}		
V _{IL}	LOW Level Input Voltage	1.65 to 1.95				0.25V _{CC}	0.25V _{CC}		V
		2.30 to 5.50				0.30V _{CC}	0.30V _{CC}		
I _{LKG}	HIGH Level Output Leakage Current	1.65 to 5.50	V _{IN} =V _{IH} , V _{OUT} =V _{CC} or GND			±5		±10	μA
V _{OL}	LOW Level Output Voltage	1.65	V _{IN} =V _{IL} , I _{OL} =100μA		0.00	0.10		0.00	V
		1.80			0.00	0.10		0.10	
		2.30			0.00	0.10		0.10	
		3.00			0.00	0.10		0.10	
		4.50			0.00	0.10		0.10	
		1.65	I _{OL} =4mA		0.80	0.24		0.24	
		2.30	I _{OL} =8mA		0.10	0.30		0.30	
		3.00	I _{OL} =16mA		0.16	0.40		0.40	
		3.00	I _{OL} =24mA		0.24	0.55		0.55	
		4.50	I _{OL} =32mA		0.25	0.55		0.55	
I _{IN}	Input Leakage Current	0 to 5.5	0 ≤ V _{IN} ≤ 5.5V			±0.1		±1.0	μA
I _{OFF}	Power Off Leakage Current	0	V _{IN} or V _{OUT} =5.5V			1		10	μA
I _{CC}	Quiescent Supply Current	1.65 to 5.50	V _{IN} =5.5V, GND			1		10	μA

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AC Electrical Characteristics

Symbol	Parameter	V _{CC}	Conditions	T _A =+25°C			T _A =-40 to +85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t _{PZL} , t _{PLZ}	Propagation Delay	1.65	C _L =50pF, R _U =500Ω, R _D =500Ω, V _I =2 x V _{CC}	1.8	6.6	11.5	1.8	12.6	ns	Figure 5 Figure 6
		1.80		1.8	5.5	9.5	1.8	10.5		
		2.50 ± 0.20		1.2	3.7	5.8	1.2	6.4		
		3.30 ± 0.30		0.8	2.9	4.4	0.8	4.8		
		5.00 ± 0.50		0.5	2.3	3.5	0.5	3.9		
		1.65		1.8	5.5	11.5	1.8	12.6		
		1.80		1.8	4.3	9.5	1.8	10.5		
		2.50 ± 0.20		1.2	2.8	5.8	1.2	6.4		
		3.30 ± 0.30		0.8	2.1	4.4	0.8	4.8		
		5.00 ± 0.50		0.5	1.4	3.5	0.5	3.9		
C _{IN}	Input Capacitance	0			2.5				pF	
C _{OUT}	Output Capacitance	0			4.0					
C _{PD}	Power Dissipation Capacitance ⁽⁵⁾	3.30			3				pF	Figure 7
		5.00			4					

Note:

5. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression: I_{CCD}=(C_{PD})(V_{CC})(f_{IN})+(I_{CC}static).

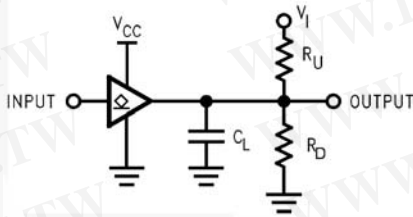


Figure 5. AC Test Circuit

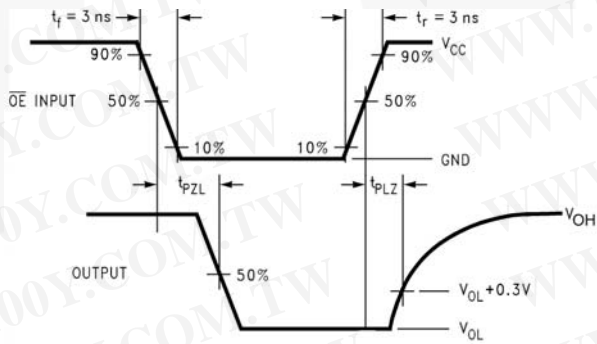


Figure 6. AC Waveforms

Notes:

6. C_L includes load and stray capacitance.
7. Input PRR = 1.0MHz, t_w = 500ns.

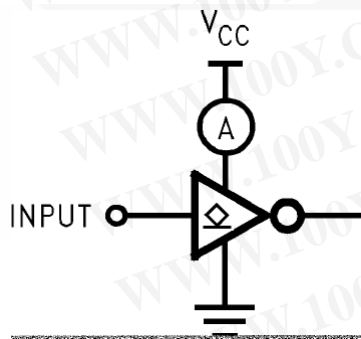


Figure 7. I_{CCD} Test Circuit

Note:

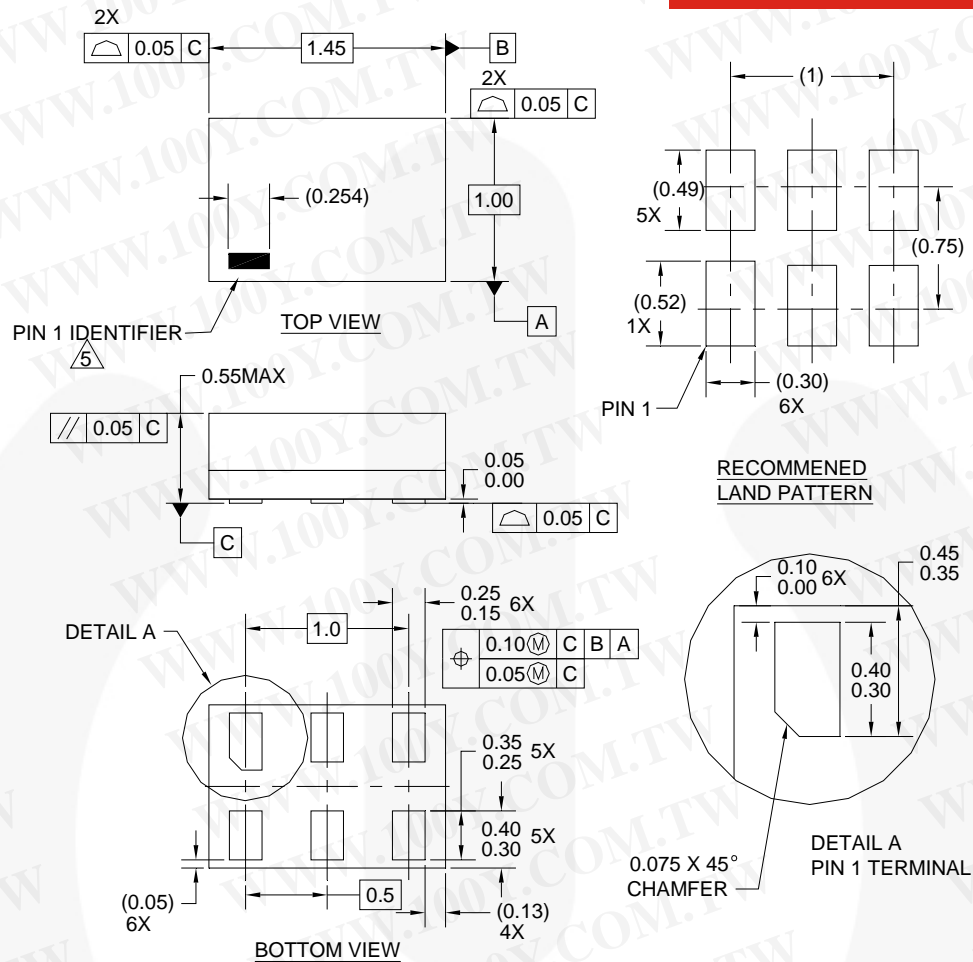
8. Input=AC Waveform; t_r=t_f=1.8ns.
9. PRR=Variable; Duty Cycle=50%.

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Physical Dimensions



- Notes:
1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
 2. DIMENSIONS ARE IN MILLIMETERS
 3. DRAWING CONFORMS TO ASME Y14.5M-1994
 4. FILENAME AND REVISION: MAC06AREV4
 5. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

Figure 9. 6-Lead, MicroPak™, 1.0mm Wide

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Tape and Reel Specification

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http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
L6X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

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Physical Dimensions

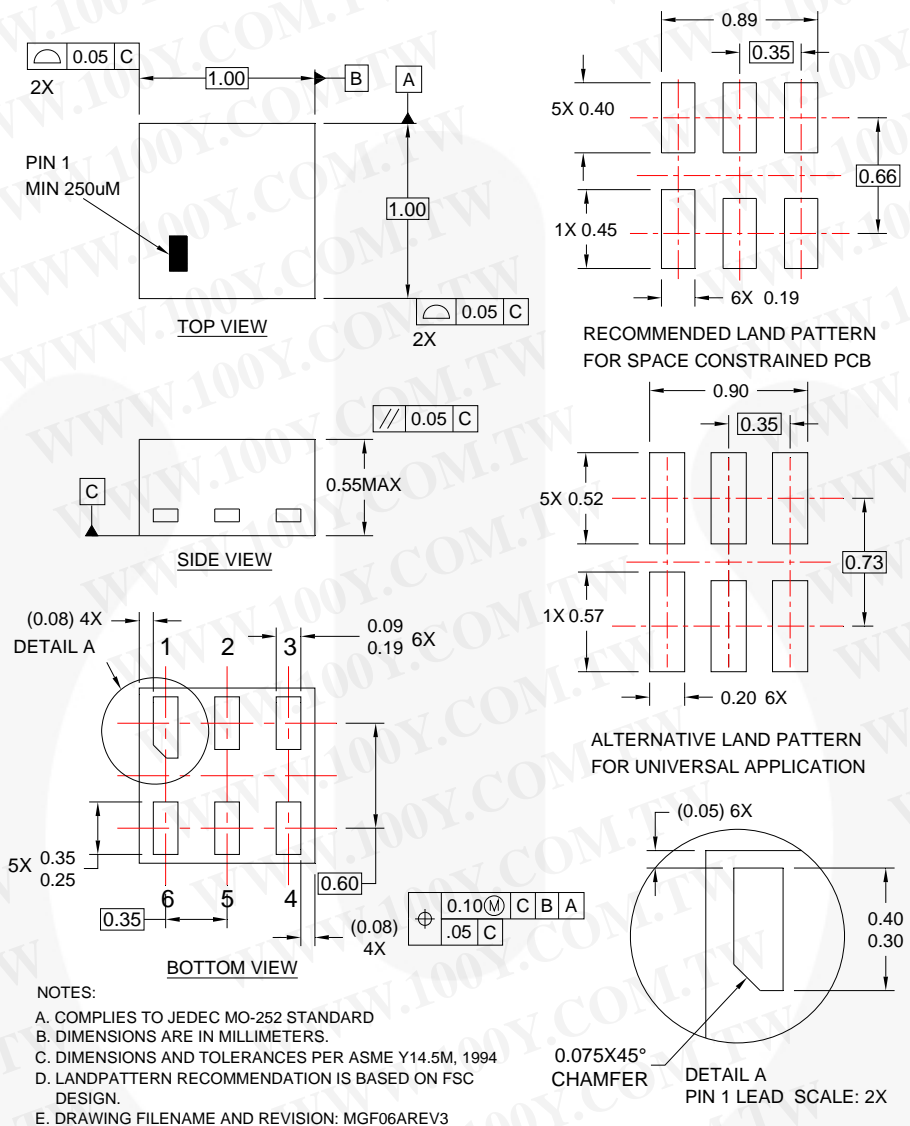


Figure 10. 6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch

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Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/packaging/MicroPAK2_6L_tr.pdf.





Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
FHX	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed



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