CLARE
An IXYS Company

IXD_609
9-Ampere Low-Side Ultrafast MOSFET Drivers

Features

- 9A Peak Source/Sink Drive Current
- Wide Operating Voltage Range: 4.5V to 35V
- -40°C to +125°C Extended Operating Temperature Range
- Logic Input Withstands Negative Swing of up to 5V
- Matched Rise and Fall Times
- Low Propagation Delay Time
- Low, 10μA Supply Current
- Low Output Impedance

Applications

- Efficient Power MOSFET and IGBT Switching
- Switch Mode Power Supplies
- Motor Controls
- DC to DC Converters
- Class-D Switching Amplifiers
- Pulse Transformer Driver

Description

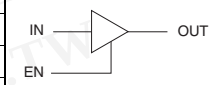
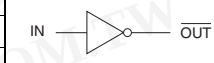
The IXDD609/IXDI609/IXDN609 high-speed gate drivers are especially well suited for driving the latest IXYS MOSFETs and IGBTs. The IXD_609 high-current output can source and sink 9A of peak current while producing voltage rise and fall times of less than 25ns. The input is CMOS compatible, and is virtually immune to latch up. Proprietary circuitry eliminates cross-conduction and current "shoot-through." Low propagation delay and fast, matched rise and fall times make the IXD_609 family ideal for high-frequency and high-power applications.

The IXDD609 is configured as a non-inverting driver with an enable, the IXDN609 is configured as a non-inverting driver, and the IXDI609 is configured as an inverting driver.

The IXD_609 family is available in a standard 8-lead DIP (PI); an 8-lead SOIC (SIA); an 8-lead Power SOIC with an exposed metal back (SI); an 8-lead DFN (D2); a 5-lead TO-263 (YI); and a 5-lead TO-220 (CI).

Pb RoHS 2002/95/EC e3

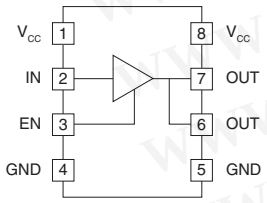
Ordering Information

Part Number	Logic Configuration	Package Type	Packing Method	Quantity
IXDD609D2TR		8-Lead DFN	Tape & Reel	2000
IXDD609SI		8-Lead Power SOIC with Exposed Metal Back	Tube	100
IXDD609SITR		8-Lead Power SOIC with Exposed Metal Back	Tape & Reel	2000
IXDD609SIA		8-Lead SOIC	Tube	100
IXDD609SIATR		8-Lead SOIC	Tape & Reel	2000
IXDD609PI		8-Lead DIP	Tube	50
IXDD609CI		5-Lead TO-220	Tube	50
IXDD609YI		5-Lead TO-263	Tube	50
IXDI609SI		8-Lead Power SOIC with Exposed Metal Back	Tube	100
IXDI609SITR		8-Lead Power SOIC with Exposed Metal Back	Tape & Reel	2000
IXDI609SIA		8-Lead SOIC	Tube	100
IXDI609SIATR		8-Lead SOIC	Tape & Reel	2000
IXDI609PI		8-Lead DIP	Tube	50
IXDI609CI		5-Lead TO-220	Tube	50
IXDI609YI		5-Lead TO-263	Tube	50
IXDN609SI		8-Lead Power SOIC with Exposed Metal Back	Tube	100
IXDN609SITR		8-Lead Power SOIC with Exposed Metal Back	Tape & Reel	2000
IXDN609SIA		8-Lead SOIC	Tube	100
IXDN609SIATR		8-Lead SOIC	Tape & Reel	2000
IXDN609PI		8-Lead DIP	Tube	50
IXDN609CI		5-Lead TO-220	Tube	50
IXDN609YI		5-Lead TO-263	Tube	50

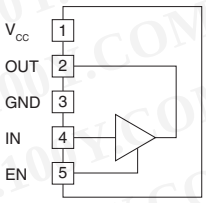
1 Specifications

1.1 Lead Configurations

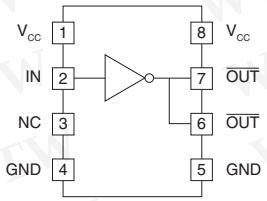
IXDD609 D2 / PI / SI / SIA



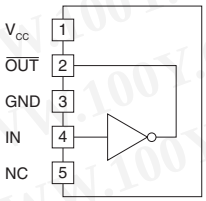
IXDD609 CI / YI



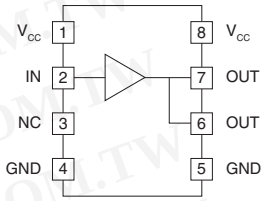
IXDI609 PI / SI / SIA



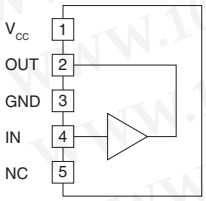
IXDI609 CI / YI



IXDN609 PI / SI / SIA



IXDN609 CI / YI



1.2 Lead Definitions

Lead Name	Description
IN	Logic Input
EN	Output Enable - Drive lead low to disable output, and force output to a high impedance state
OUT	Output - Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT
$\overline{OUT}$	Inverted Output - Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT
V_{CC}	Supply Voltage - Provides power to the device
GND	Ground - Common ground reference for the device
NC	Not connected

1.3 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage	V_{CC}	-	40	V
All Other Leads	-	-0.3	V_{CC}+0.3	V
Output Current	I_{OUT}	-	±9	A
Junction Temperature	T_J	-55	+150	°C
Storage Temperature	T_{STG}	-65	+150	°C

Unless stated otherwise, absolute maximum electrical ratings are at 25°C

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage	V_{CC}	4.5	35	V
Operating Temperature Range	T_A	-40	+125	°C

1.5 Electrical Characteristics: T_A = 25°C

Test Conditions: 4.5V ≤ V_{CC} ≤ 35V (unless otherwise noted).

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Input Voltage, High	4.5V ≤ V_{CC} ≤ 18V	V_{IH}	3.0	-	-	V
Input Voltage, Low	4.5V ≤ V_{CC} ≤ 18V	V_{IL}	-	-	0.8	
Input Voltage Range	-	V_{IN}	-5	-	V_{CC}+0.3	
Input Current	0V ≤ V_{IN} ≤ V_{CC}	I_{IN}	-10	-	10	µA
EN Input Voltage, High	IXDD609 only	V_{ENH}	2/3V_{CC}	-	-	V
EN Input Voltage, Low	IXDD609 only	V_{ENL}	-	-	1/3V_{CC}	
Output Voltage, High	-	V_{OH}	V_{CC}-0.025	-	-	V
Output Voltage, Low	-	V_{OL}	-	-	0.025	
Output Resistance, High State	V_{CC}=18V, I_{OUT}=-10mA	R_{OH}	-	0.6	1	Ω
Output Resistance, Low State	V_{CC}=18V, I_{OUT}=10mA	R_{OL}	-	0.4	0.8	
Output Current, Continuous	Limited by package power dissipation	I_{DC}	-	-	±2	A
Rise Time	C_{LOAD}=10nF, V_{CC}=18V	t_R	-	22	35	ns
Fall Time	C_{LOAD}=10nF, V_{CC}=18V	t_F	-	15	25	
On-Time Propagation Delay	C_{LOAD}=10nF, V_{CC}=18V	t_{ONDLY}	-	40	60	
Off-Time Propagation Delay	C_{LOAD}=10nF, V_{CC}=18V	t_{OFFDLY}	-	42	60	
Enable to Output-High Delay Time (IXDD609 Only)	V_{CC}=18V	t_{ENOH}	-	25	60	
Disable to High Impedance State Delay Time (IXDD609 Only)	V_{CC}=18V	t_{DOLD}	-	35	60	
Enable Pull-Up Resistor	-	R_{EN}	-	200	-	kΩ
Power Supply Current	V_{CC}=18V, V_{IN}=3.5V	I_{CC}	-	1	2	mA
	V_{CC}=18V, V_{IN}=0V		-	-	10	µA
	V_{CC}=18V, V_{IN}=V_{CC}		-	-	10	

1.6 Electrical Characteristics: T_A = - 40°C to +125°C

Test Conditions: 4.5V ≤ V_{CC} ≤ 35V, T_J < 150°C (unless otherwise noted).

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Input Voltage, High	4.5V ≤ V_{CC} ≤ 18V	V_{IH}	3.3	-	-	V
Input Voltage, Low	4.5V ≤ V_{CC} ≤ 18V	V_{IL}	-	-	0.65	
Input Voltage Range	-	V_{IN}	-5	-	V_{CC}+0.3	
Input Current	0V ≤ V_{IN} ≤ V_{CC}	I_{IN}	-10	-	10	µA
Output Voltage, High	-	V_{OH}	V_{CC}-0.025	-	-	V
Output Voltage, Low	-	V_{OL}	-	-	0.025	
Output Resistance, High State	V_{CC}=18V, I_{OUT}=-10mA	R_{OH}	-	-	2	Ω
Output Resistance, Low State	V_{CC}=18V, I_{OUT}=10mA	R_{OL}	-	-	1.5	
Output Current, Continuous	Limited by package power dissipation	I_{DC}	-	-	±1	A
Rise Time	C_{LOAD}=10nF, V_{CC}=18V	t_R	-	-	40	ns
Fall Time	C_{LOAD}=10nF, V_{CC}=18V	t_F	-	-	30	
On-Time Propagation Delay	C_{LOAD}=10nF, V_{CC}=18V	t_{ONDLY}	-	-	75	
Off-Time Propagation Delay	C_{LOAD}=10nF, V_{CC}=18V	t_{OFFDLY}	-	-	75	
Enable to Output-High Delay Time	IXDD609 only	t_{ENOH}	-	-	75	
Disable to High Impedance State Delay Time	IXDD609 only	t_{DOLD}	-	-	75	
Power Supply Current	V_{CC}=18V, V_{IN}=3.5V	I_{CC}	-	1	2.5	mA
	V_{CC}=18V, V_{IN}=0V		-	-	150	µA
	V_{CC}=18V, V_{IN}=V_{CC}		-	-	150	

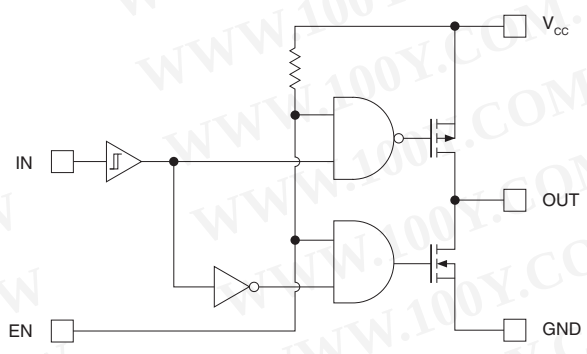
2 Thermal Characteristics

Package	Parameter	Symbol	Rating	Units
D2 (8-Lead DFN)	Thermal Resistance, Junction-to-Ambient	θ_{JA}	35	°C/W
CI (5-Lead TO-220)			36	
PI (8-Lead DIP)			125	
SI (8-Lead Power SOIC)			85	
SIA (8-Lead SOIC)			120	
YI (5-Lead TO-263)			46	
CI (5-Lead TO-220)	Thermal Resistance, Junction-to-Case	θ_{JC}	3	°C/W
SI (8-Lead Power SOIC)			10	
YI (5-Lead TO-263)			2	

3 Functional Description

3.1 IXDD609 Functional Block Diagram

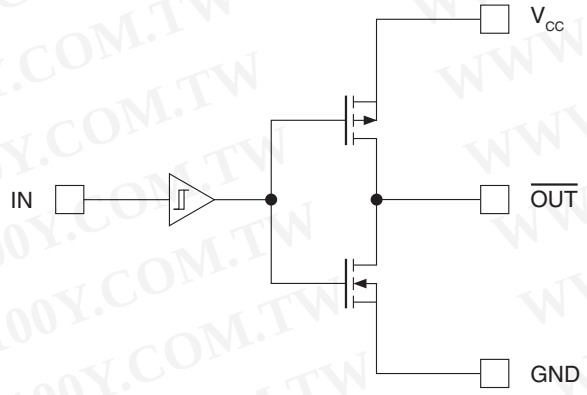
IXDD609



IN	EN	OUT
0	1 or open	0
1	1 or open	1
0	0	Z
1	0	Z

3.2 IXDI609 Functional Block Diagram

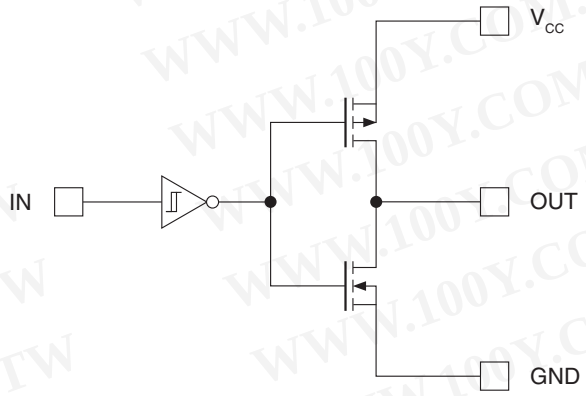
IXDI609



IN	$\overline{OUT}$
0	1
1	0

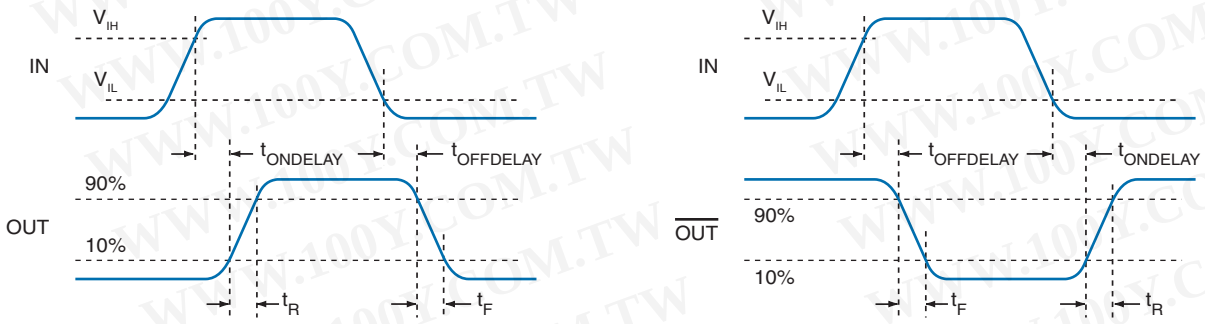
3.3 IXDN609 Functional Block Diagram

IXDN609

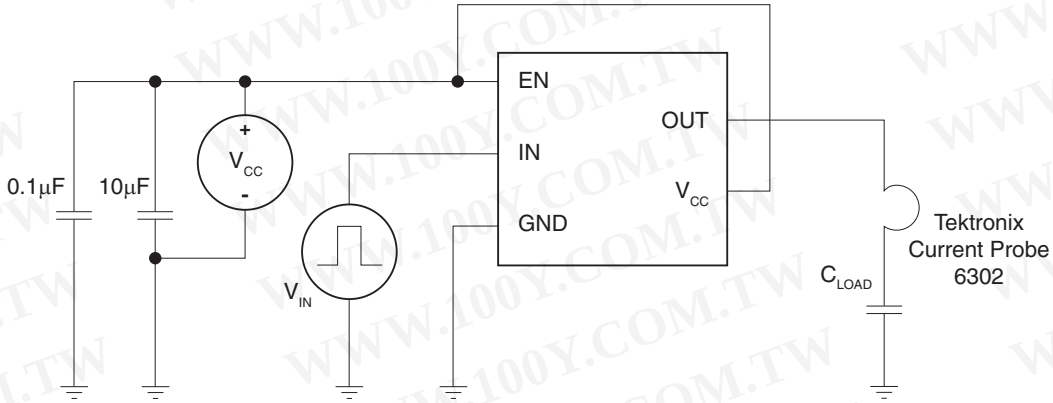


IN	OUT
0	0
1	1

3.4 Timing Diagrams

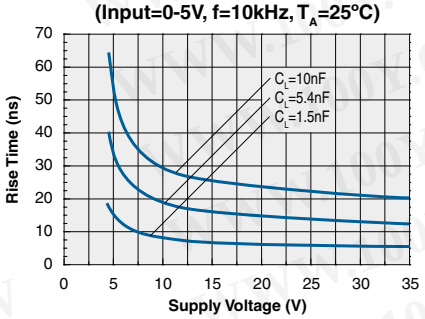


3.5 Characteristics Test Diagram

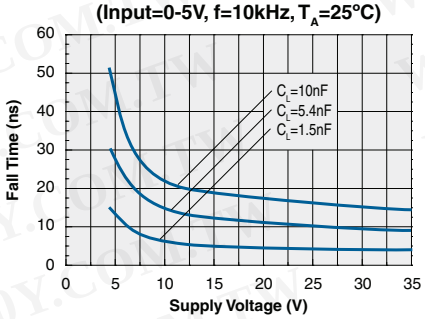


4 Performance Data

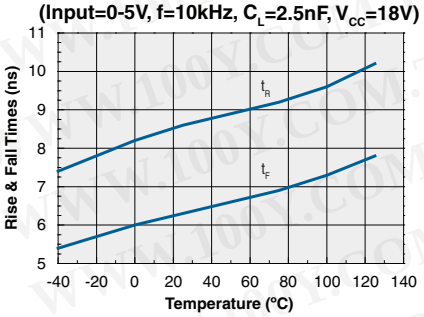
Rise Time vs. Supply Voltage
(Input=0-5V, f=10kHz, T_A=25°C)



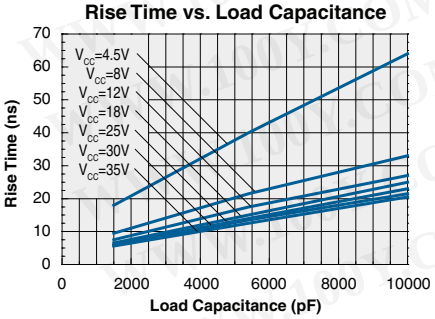
Fall Time vs. Supply Voltage
(Input=0-5V, f=10kHz, T_A=25°C)



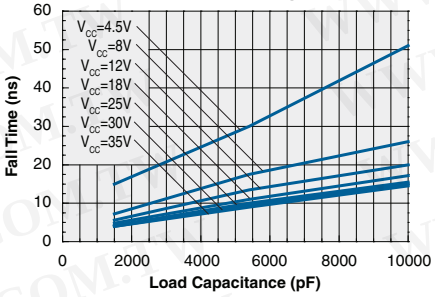
Rise and Fall Times vs. Temperature
(Input=0-5V, f=10kHz, C_L=2.5nF, V_{CC}=18V)



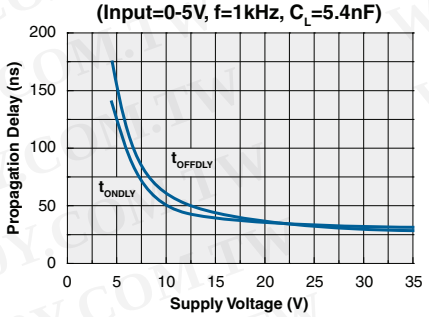
Rise Time vs. Load Capacitance



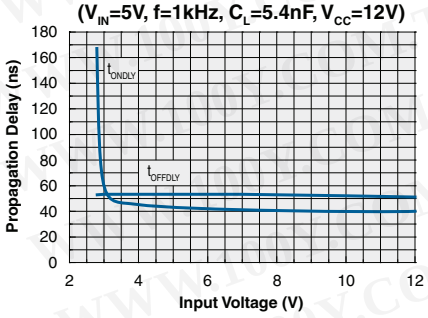
Fall Time vs. Load Capacitance



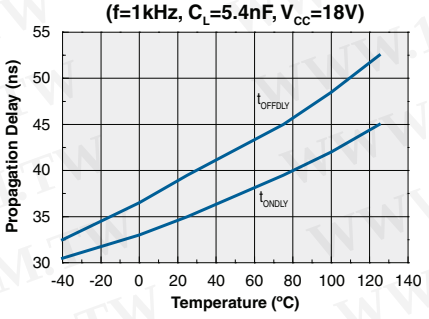
Propagation Delay vs. Supply Voltage
(Input=0-5V, f=1kHz, C_L=5.4nF)



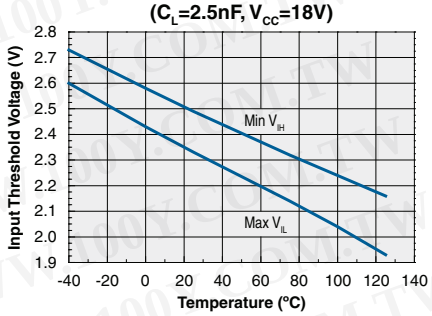
Propagation Delay vs. Input Voltage
(V_{IN}=5V, f=1kHz, C_L=5.4nF, V_{CC}=12V)



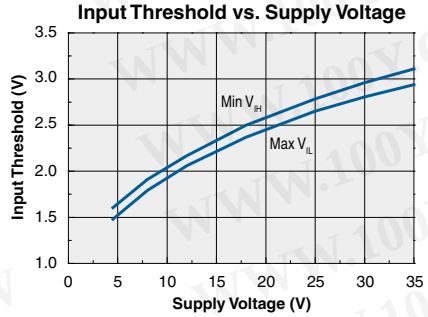
Propagation Delay
vs. Junction Temperature
(f=1kHz, C_L=5.4nF, V_{CC}=18V)



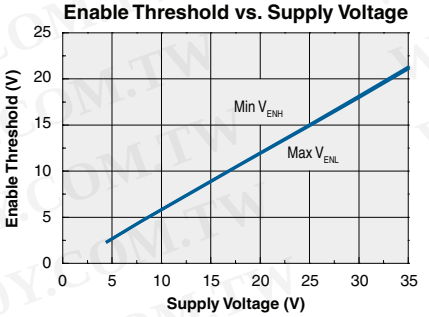
Input Threshold Voltage
vs. Temperature
(C_L=2.5nF, V_{CC}=18V)



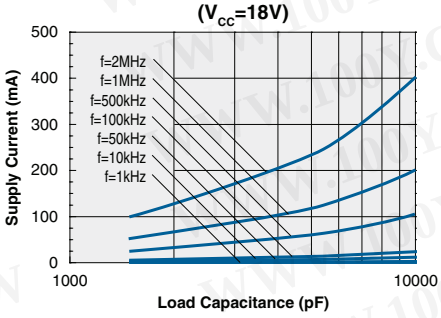
Input Threshold vs. Supply Voltage



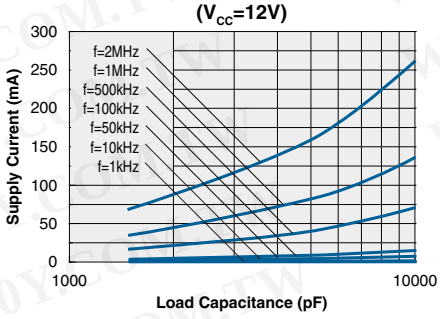
Enable Threshold vs. Supply Voltage



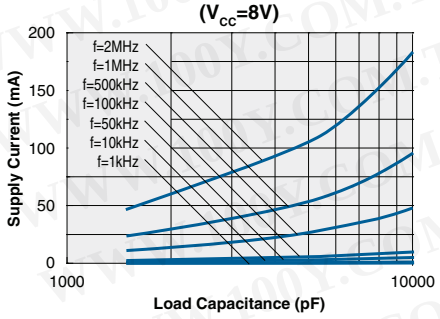
Supply Current vs. Load Capacitance (V_{CC}=18V)



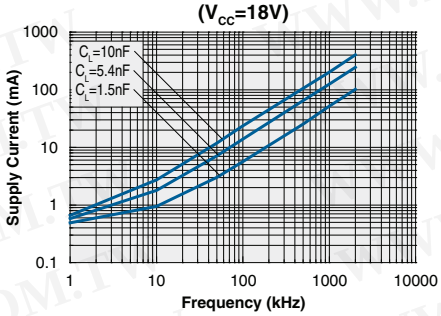
Supply Current vs. Load Capacitance (V_{CC}=12V)



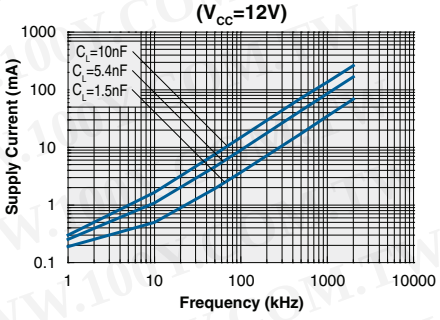
Supply Current vs. Load Capacitance (V_{CC}=8V)



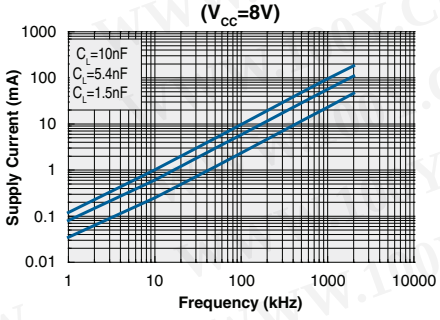
Supply Current vs. Frequency (V_{CC}=18V)



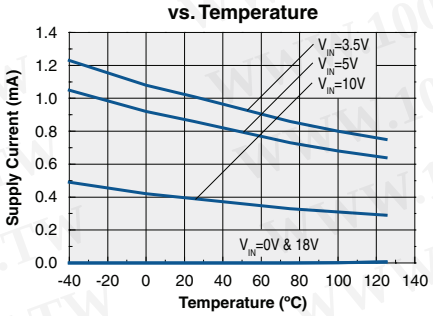
Supply Current vs. Frequency (V_{CC}=12V)



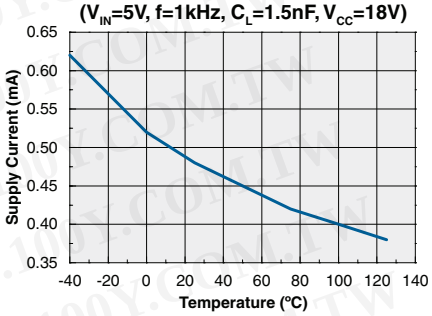
Supply Current vs. Frequency (V_{CC}=8V)



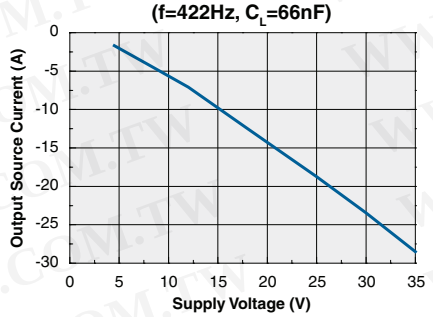
Quiescent Supply Current vs. Temperature



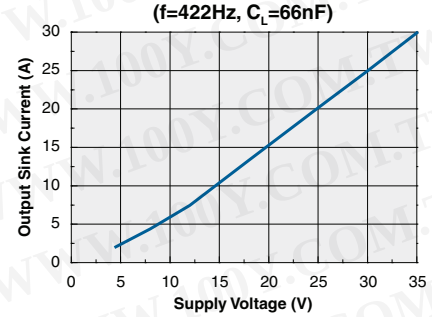
Dynamic Supply Current vs. Temperature (V_{IN}=5V, f=1kHz, C_L=1.5nF, V_{CC}=18V)



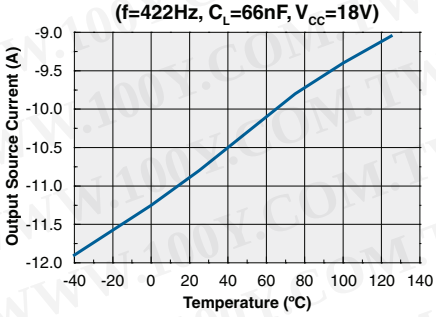
Output Source Current vs. Supply Voltage (f=422Hz, C_L=66nF)



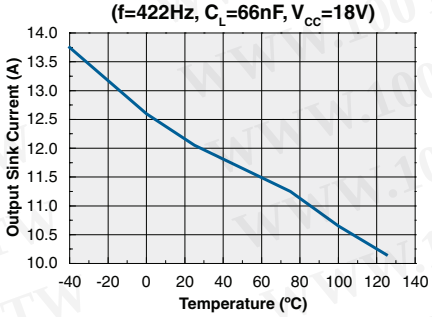
Output Sink Current vs. Supply Voltage (f=422Hz, C_L=66nF)



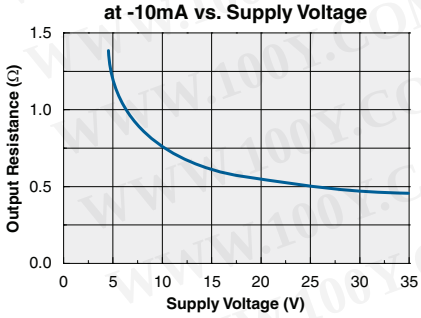
Output Source Current vs. Temperature (f=422Hz, C_L=66nF, V_{CC}=18V)



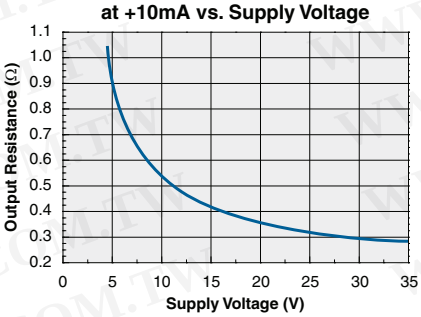
Output Sink Current vs. Temperature (f=422Hz, C_L=66nF, V_{CC}=18V)



High State Output Resistance at -10mA vs. Supply Voltage



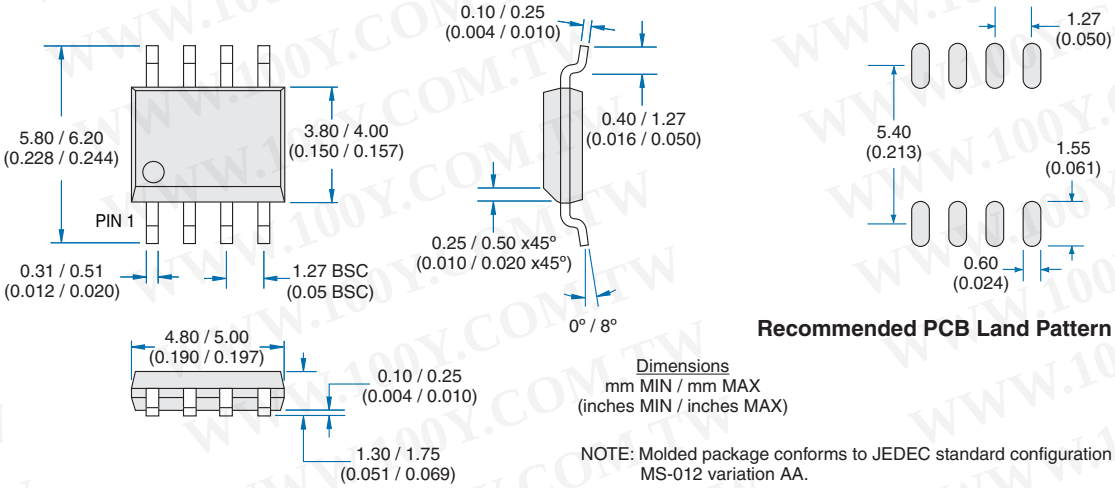
Low State Output Resistance at +10mA vs. Supply Voltage



5 Manufacturing Information

5.1 Mechanical Dimensions

5.1.1 IXD_609SIA (8-Lead SOIC)

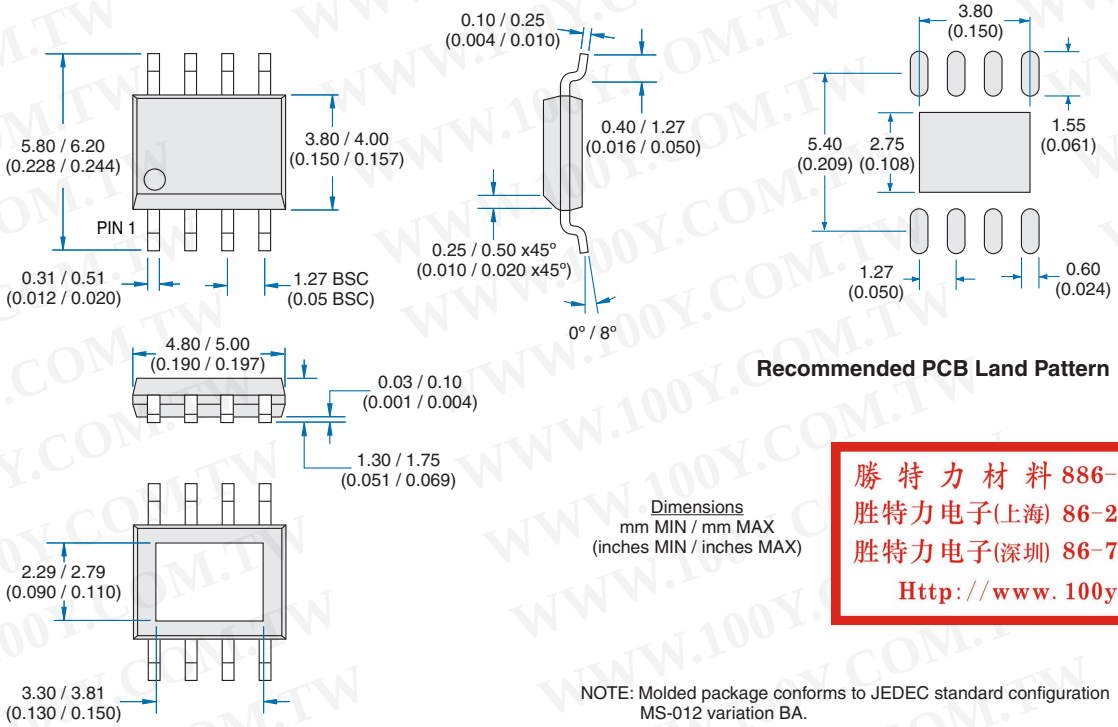


Recommended PCB Land Pattern

Dimensions
mm MIN / mm MAX
(inches MIN / inches MAX)

NOTE: Molded package conforms to JEDEC standard configuration MS-012 variation AA.

5.1.2 IXD_609SI (8-Lead Power SOIC with Exposed Metal Back)

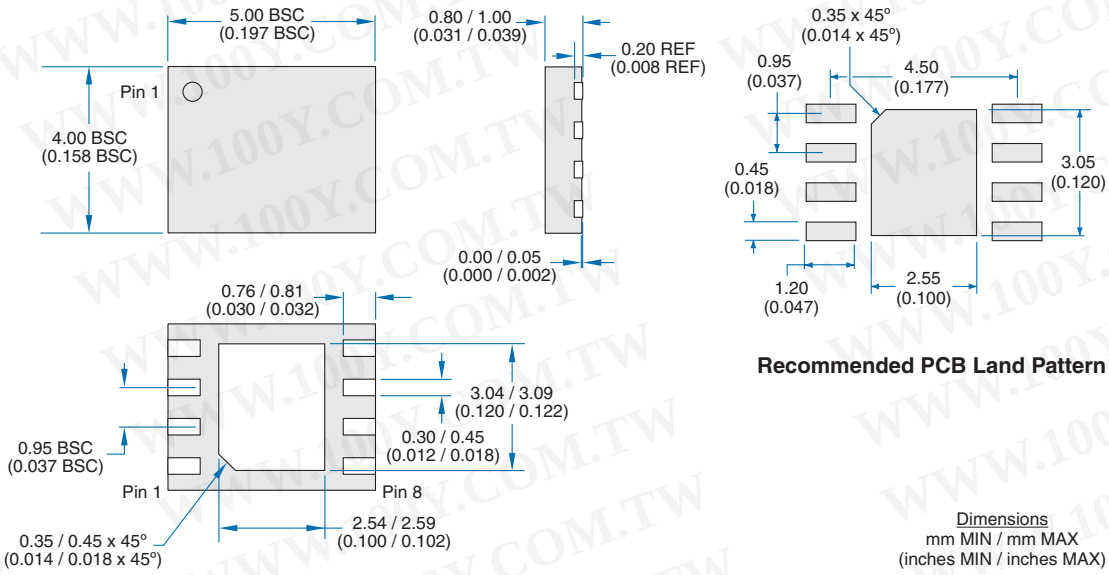


Recommended PCB Land Pattern

Dimensions
mm MIN / mm MAX
(inches MIN / inches MAX)

NOTE: Molded package conforms to JEDEC standard configuration MS-012 variation BA.

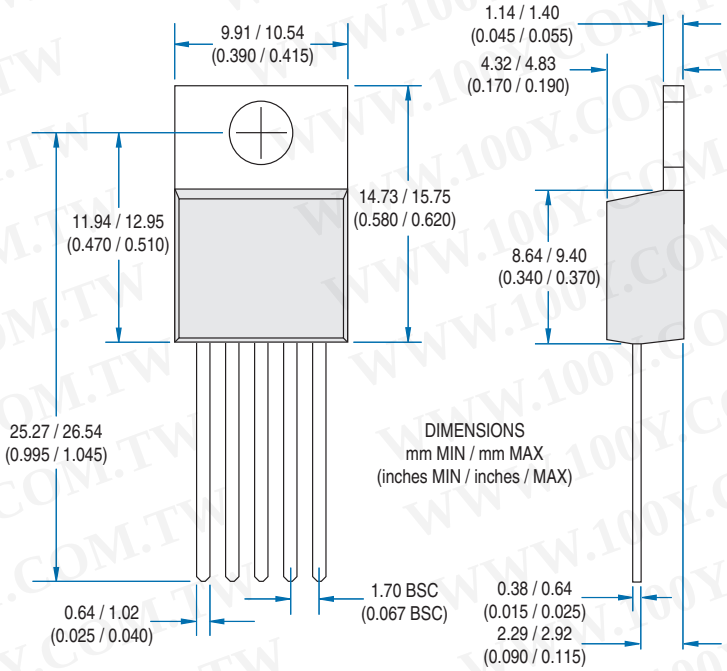
5.1.3 IXDD609D2 (8-Lead DFN)



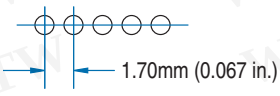
Recommended PCB Land Pattern

Dimensions
mm MIN / mm MAX
(inches MIN / inches MAX)

5.1.4 IXD_609CI (5-Lead TO-220)

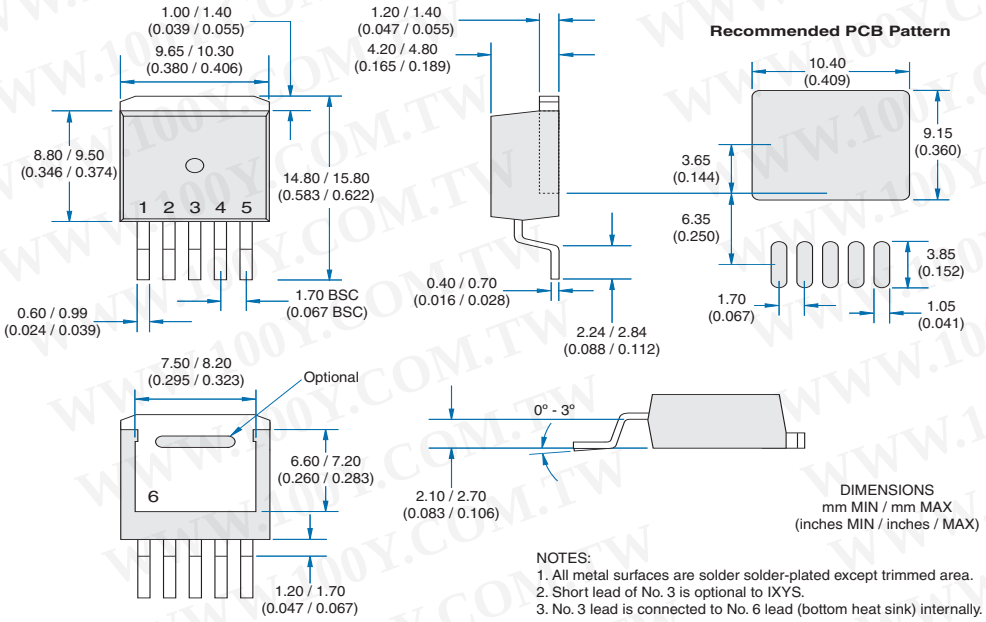


Recommended Hole Pattern
Finished Hole Diameter = 1.45mm (0.057 in.)



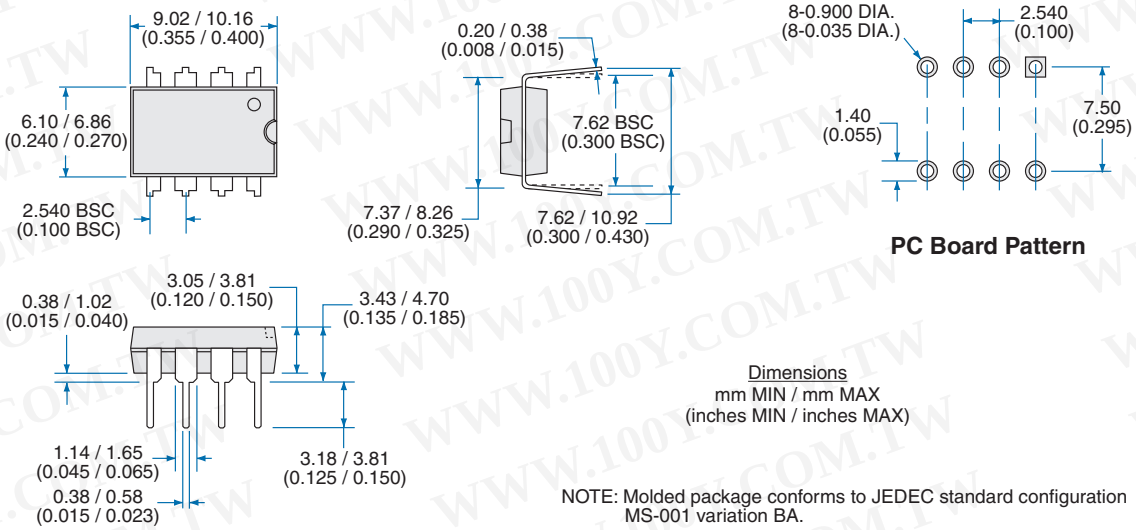
NOTES:
1. This drawing will meet all dimensions requirement of JEDEC outlines TS-001AA and 5-lead version TO-220AB.
2. Mounting hole diameter: 3.53 / 3.96 (0.139 / 0.156)

5.1.5 IXD_609YI (5-LeadTO-263)



NOTES:
1. All metal surfaces are solder solder-plated except trimmed area.
2. Short lead of No. 3 is optional to IXYS.
3. No. 3 lead is connected to No. 6 lead (bottom heat sink) internally.

5.1.6 IXD_609PI (8-Lead DIP)



Dimensions
mm MIN / mm MAX
(inches MIN / inches MAX)

NOTE: Molded package conforms to JEDEC standard configuration MS-001 variation BA.

For additional information please visit our website at: www.clare.com

Specification: DS-IXD_609-R00F

8/24/2010