



The Future of Analog IC Technology®

# MP4021

Universal AC Input, Isolated, Primary-Side Control LED Controller with Active PFC

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

MPS CONFIDENTIAL AND PROPRIETARY INFORMATION – 3CEMS USE ONLY

## DESCRIPTION

The MP4021 is a primary-side-control offline LED lighting controller which can achieve high power factor and accurate LED current for an isolate lighting application in a single stage converter. The proprietary real current control method can control the LED current accurately from the primary side information. It can significantly simplify the LED lighting system design by eliminating the secondary side feedback components and the optocoupler.

The MP4021 integrates power factor correction function and works in boundary conduction mode for reducing the MOSFET switching losses.

The extremely low start-up current and the quiescent current can reduce the power consumption thus lead to an excellent efficiency performance.

The multi-protection function of MP4021 can greatly enhance the system reliability and safety. The MP4021 features over-voltage protection, short-circuit protection, cycle-by-cycle current limit, VCC UVLO and auto-restart over-temperature protection.

The MP4021 is available in a small SOIC8 package.

## FEATURES

- Real Current Control Without Secondary-feedback Circuit
- High Current Accuracy Of Line Regulation
- High Power Factor: >0.95 Over the Universal Input
- Boundary Conduction Mode Operation
- Ultra-low (10µA) Start Up Current
- Low (1mA) Quiescent Current
- Input UVLO
- Cycle-by-cycle Current Limit
- Over-voltage Protection
- Short-circuit Protection
- Over-temperature Protection
- Available in a SOIC8 Package

## APPLICATIONS

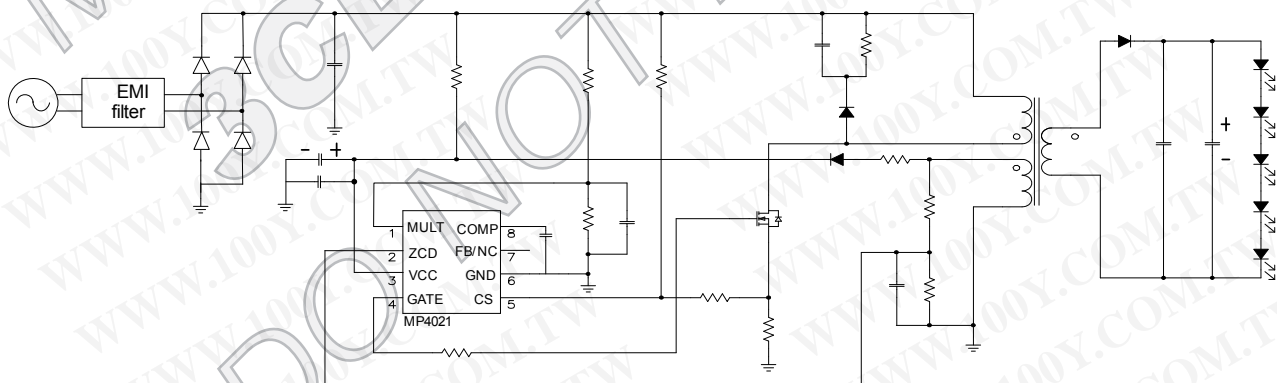
- Isolated, Solid State Lighting
- Industrial and Commercial Lighting
- Residential Lighting

"MPS" and "The Future of Analog IC Technology" are Registered Trademarks of Monolithic Power Systems, Inc.

The MP4021 is under patent pending.

**勝特力材料 886-3-5753170**  
**勝特力电子(上海) 86-21-34970699**  
**勝特力电子(深圳) 86-755-83298787**  
[Http://www.100y.com.tw](http://www.100y.com.tw)

## TYPICAL APPLICATION

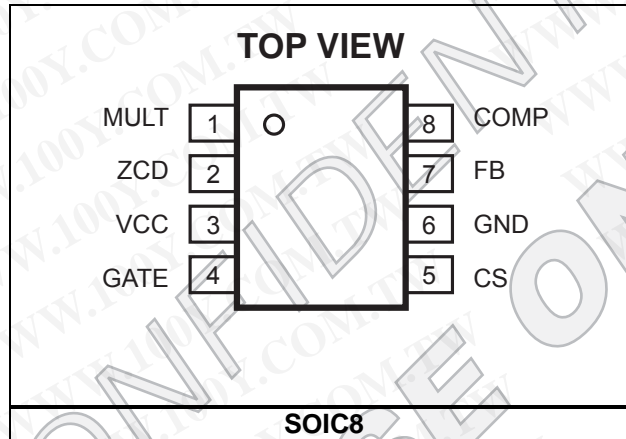


**ORDERING INFORMATION**

Part Number*	Package	Top Marking	Free Air Temperature (T <sub>A</sub> )
MP4021DS	SOIC8	MP4021	-40°C to +85°C

\* For Tape & Reel, add suffix -Z (e.g. MP4021DS-Z);  
 For RoHS Compliant Packaging, add suffix -LF (e.g. MP4021DS-LF-Z)

**PACKAGE REFERENCE**



**ABSOLUTE MAXIMUM RATINGS (1)**

Input Voltage V <sub>CC</sub> .....	-0.3V to +30V
Analog Inputs and Outputs .....	-0.3V to 8V
ZCD Pin Maximum Current .....	-50mA~10mA
Max. Gate Current .....	±1.2A
Continuous Power Dissipation (T <sub>A</sub> = +25°C) (2)	
SOIC8 .....	1.3W
Junction Temperature .....	150°C
Lead Temperature .....	260°C
Storage Temperature .....	-65°C to +150°C

**Recommended Operating Conditions (3)**

Supply Voltage V <sub>CC</sub> .....	10.3V to 23V
Operating Junct. Temp (T <sub>J</sub> ) .....	-40°C to +125°C

**Thermal Resistance (4) θ<sub>JA</sub> θ<sub>JC</sub>**

SOIC8 .....	96	45	°C/W
-------------	----	----	------

**Notes:**

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T<sub>J</sub>(MAX), the junction-to-ambient thermal resistance θ<sub>JA</sub>, and the ambient temperature T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>0</sub>(MAX)=(T<sub>J</sub>(MAX)-T<sub>A</sub>)/ θ<sub>JA</sub>. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operation conditions.
- Measured on JESD51-7 4-layer board.

**ELECTRICAL CHARACTERISTICS**

$V_{CC} = 14V, T_A = +25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Supply Voltage</b>						
Operating Range	$V_{CC}$	After turn on	10.3		23	V
Turn On Threshold	$V_{CC\_on}$		11	12	13	V
Turn Off Threshold	$V_{CC\_off}$		7	7.6	8.2	V
Hysteretic Voltage	$V_{CC\_hys}$		3.2		3.8	V
Clamp Voltage	$V_z$	$I_{CC}=20mA$		30		V
<b>Supply Current</b>						
Start up Current	$I_{startup}$	$V_{CC}=11V$		20	30	$\mu A$
Quiescent Current	$I_q$	No switch		1	2	mA
Operating Current	$I_{CC}$	$F_s = 70kHz$		2	5	mA
<b>Multiplier</b>						
Operation Range	$V_{MULT}$		0		3	V
Gain <sup>(5)</sup>	K		0.5	0.6	0.8	1/V
<b>Error Amplifier</b>						
Feedback Voltage	$V_{FB}$		0.386	0.4	0.414	V
Transconductance	$G_{EA}$			100		$\mu A/V$
Voltage Gain	$V_{EA}$			400		V/V
Upper clamp Voltage	$V_{COMP\_H}$		5.3	5.65	6	V
Lower clamp Voltage	$V_{COMP\_L}$		0.7	0.9	1.1	V
Max Source Current	$I_{COMP}$			75		$\mu A$
Max Sink Current	$I_{COMP}$			-200		$\mu A$
<b>Current Sense Comparator</b>						
Leading edge blanking time	$T_{LEB}$			280		ns
Current sense clamp voltage	$V_{CS\_clamp}$		2.4	2.9	3.4	V
<b>Zero Current Detector</b>						
Zero Current Detect threshold	$V_{ZCD\_T}$	Falling edge		0.35		V
Zero Current Detect Hystestic	$V_{ZCD\_Hy}$			550		mV
Over-voltage Threshold	$V_{ZCD\_OVP}$	1us delay after turn-off	5.2	5.5	5.8	V
Minimum off time	$T_{off\_min}$		2	3.5	5	$\mu s$
<b>Starter</b>						
Start timer period	$T_{start}$			130		$\mu s$
<b>Gate Driver</b>						
Output clamp voltage	$V_{gate-clamp}$		11	13	15	V
Max source current	$I_{gate-source}$			1		A
Max sink current	$I_{gate-sink}$			-1.2		A

Notes: 5) The multiplier output is given by:  $V_{cs}=K \cdot V_{mult} \cdot (V_{comp}-0.9)$



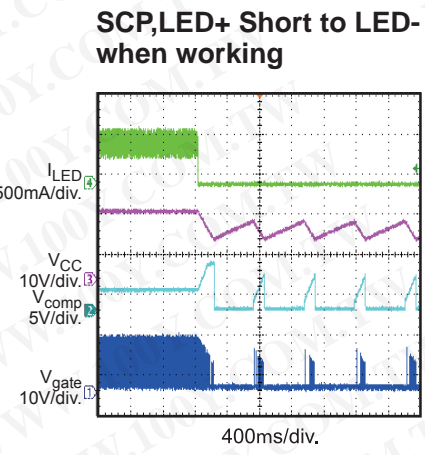
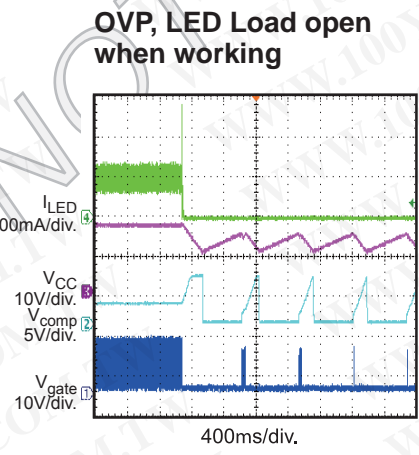
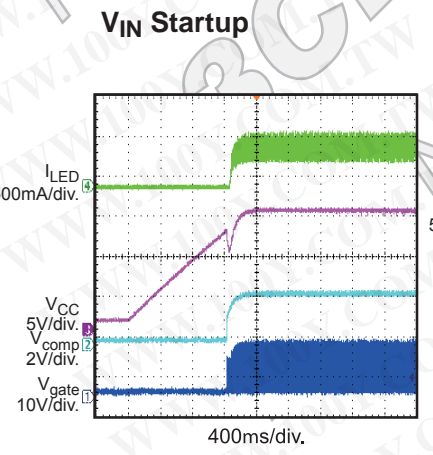
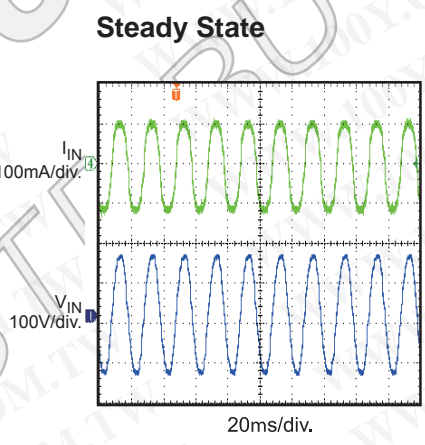
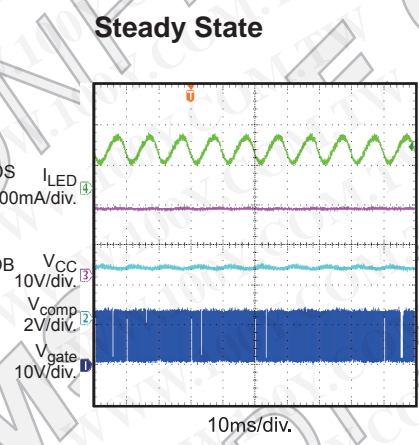
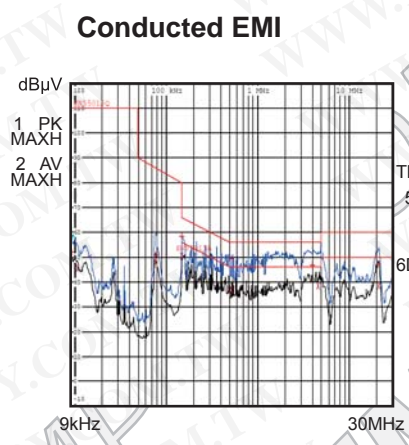
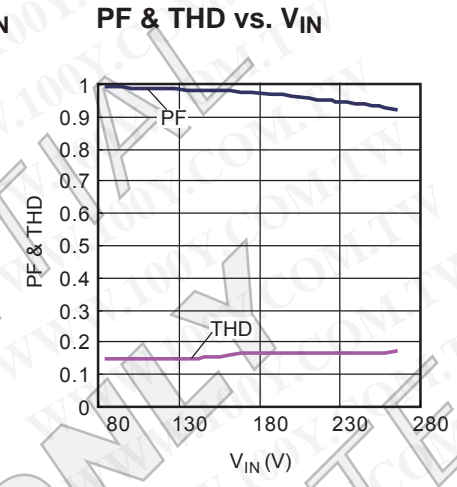
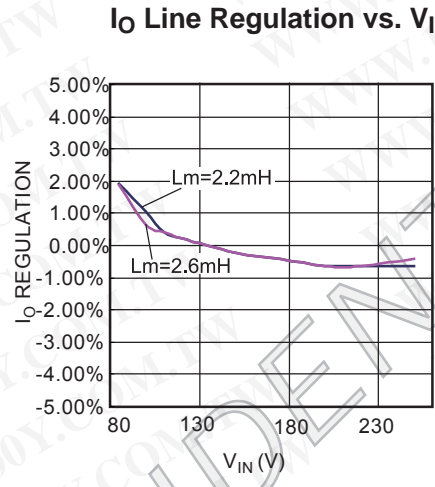
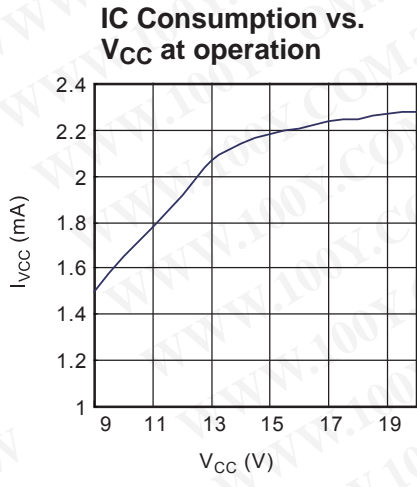
**PIN FUNCTIONS**

Pin #	Name	Pin Function
1	MULT	One of the input pin of the internal multiplier. Connects this pin to the tap of resistor divider from the rectified voltage of the AC line. The half-wave sinusoid signal in this pin is provided a reference signal for the internal current control loop.
2	ZCD	Zero current detection pin. A negative going edge triggers the turn on signal of the external MOSFET, connects this pin through a resistor divider from the auxiliary winding to GND. Over-voltage condition is detected through ZCD, if ZCD voltage is higher than the over-voltage-protection (OVP) threshold after a blanking time 1us, the over-voltage condition is detected.
3	VCC	Supply voltage pin. This pin supply power both for control signal and the gate drive signal. Connect this pin to an external bulk capacitor of typically 22uF with a 100pF ceramic cap to reduce the noise.
4	GATE	Gate drive output pin. The totem pole output stage is able to drive high power MOSFET with a peak current of 1A source capability and 1.2A sink capability. The high level voltage of this pin is clamped to 13V to avoid excessive gate drive voltage.
5	CS	Current sense pin. The MOSFET current is sensed via a resistor, the resulting voltage compared to the internal sinusoid shaped current reference signal to determine when the MOSFET turns off. A feed-forward from the rectified voltage of the AC line is recommended to add to get an excellent line regulation. If the voltage in this pin is higher than the current limit threshold 2.8V after some blanking time in the turning on interval, the gate signal will be turned off.
6	GND	Ground pin. Current return of the control signal and the gate drive signal.
7	FB/NC	Feedback signal Pin. If using primary side control, this pin can be NC.
8	COMP	Loop Compensation pin. Connects a compensation network to stabilize the LED driver and get an accurate LED current of the LED driver.

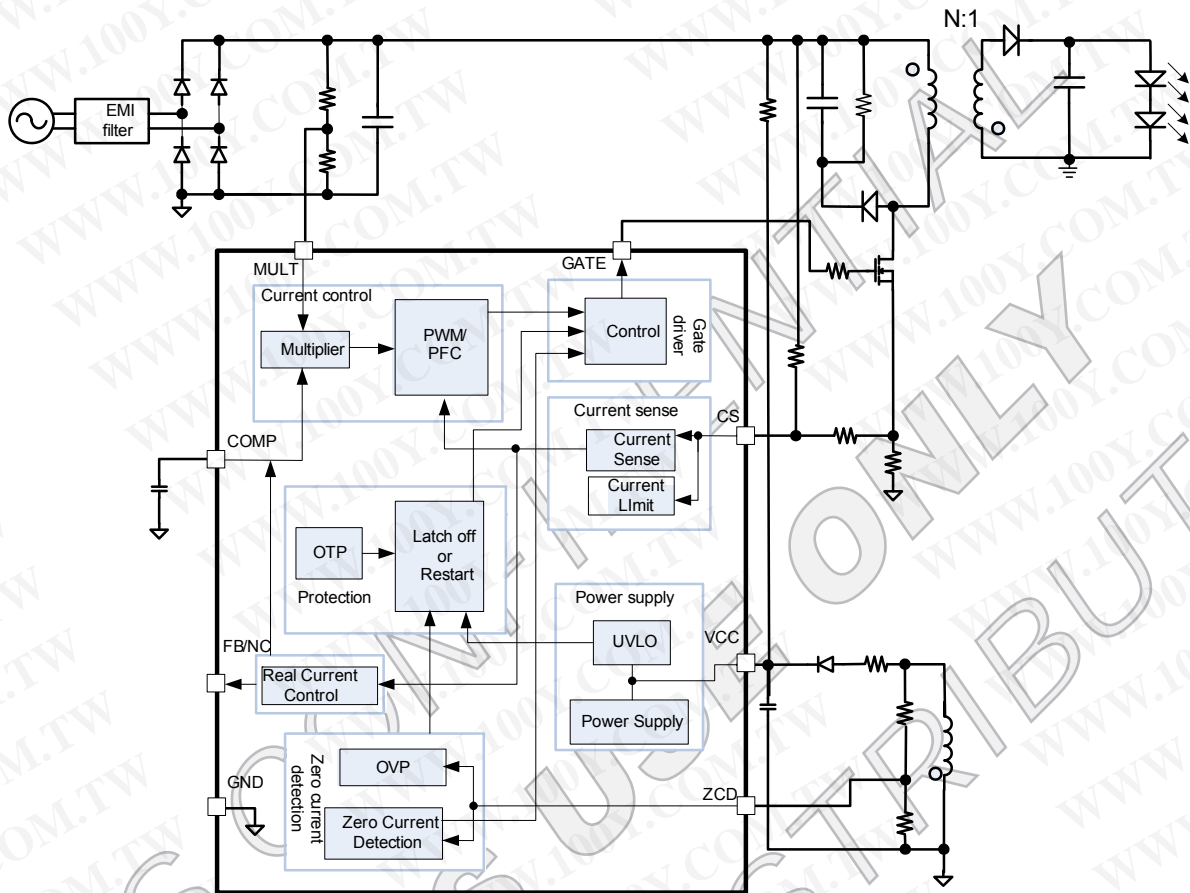
**MPS CONFIDENTIAL AND PROPRIETARY INFORMATION –3CEMS USE ONLY**

**TYPICAL PERFORMANCE CHARACTERISTICS**

$V_{IN} = 110VAC$ , 5 LEDs in series,  $I_o = 500mA$ ,  $V_o = 16V$ ,  $L_m = 2.2mH$ ,  $N_p:N_s:N_{aux} = 144:24:24$



**FUNCTION DIAGRAM**



**Figure 1—MP4021 Function Block Diagram**



## OPERATION

The MP4021 is a primary side control offline LED controller which incorporates all the features for high performance LED lighting. LED current can be accurately controlled with the real current control method from the primary side information. High power factor can also be achieved to eliminate the pollution to the AC line.

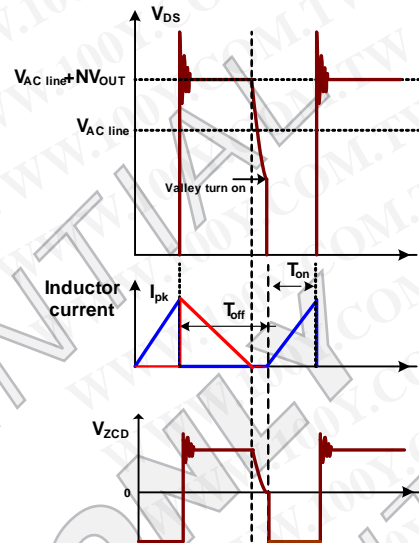
### Start Up

Initially, VCC of the MP4021 is charged through the start up resistor from the AC line, when VCC reaches 12V, the control logic works and the gate drive signal begins to switch. Then the power supply is taken over by the auxiliary winding.

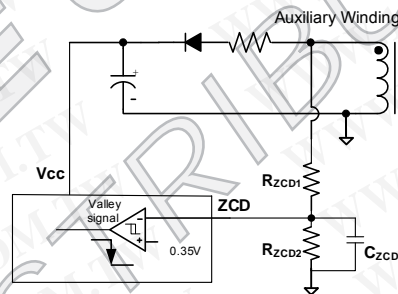
The MP4021 will shutdown as soon as VCC pin is lower than 7.6V.

### Boundary Conduction Mode Operation

During the external MOSFET on time ( $t_{ON}$ ), the rectified input voltage is applied across the primary side inductor ( $L_m$ ) and the primary current increases linearly from zero to the peak value ( $I_{pk}$ ). When the external MOSFET turns off, the energy stored in the inductor forces the secondary side diode to be turn-on, and the current of the inductor begins to decrease linearly from the peak value to zero. When the current decreases to zero, the parasitic resonant of inductor and all the parasitic capacitance makes the MOSFET drain-source voltage decrease, this decreasing is also reflected on the auxiliary winding (see Figure 2). The zero-current detector in ZCD pin generates the turn on signal of the external MOSFET when the ZCD voltage is lower than 0.35V and ensures the MOSFET turn on at a valley voltage (see Figure 3).



**Figure 2—Boundary Conduction Mode**



**Figure 3—Zero Current Detector**

As a result, there are virtually no primary switch turn-on losses and no secondary diode reverse-recover losses. It ensures high efficiency and low EMI noise.

### Real Current Control

The proprietary real current control method allows the MP4021 controlling the secondary side LED current from the primary side information. The output LED mean current can be calculated approximately as:

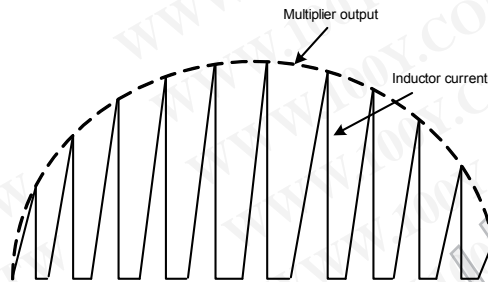
$$I_o \approx \frac{N \cdot V_{FB}}{2 \cdot R_s}$$

N—Turn ratio of primary side to secondary side  
 $V_{FB}$ —The feedback reference voltage (typical 0.4)  
 $R_s$ —The sensing resistor connected between the MOSFET source and GND.

**MPS CONFIDENTIAL AND PROPRIETARY INFORMATION –3CEMS USE ONLY**

**Power Factor Correction**

The MULT pin is connected to the tap of the resistor divider from the rectified instantaneous line voltage and fed as one input of the Multiplier. The output of the multiplier will be shaped as sinusoid too. This signal provides the reference for the current comparator and comparing with the primary side inductor current which sets the primary peak current shaped as sinusoid with the input line voltage. High power factor can be achieved.

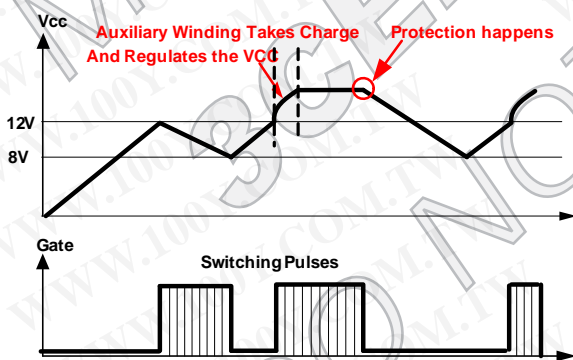


**Figure 4—Power Factor Correction Scheme**

The maximum voltage of the multiplier output to the current comparator is clamped to 2.9V to get a cycle-by-cycle current limitation.

**VCC Under-voltage Lockout**

When the VCC voltage drops below UVLO threshold 7.6V, the MP4021 stops switching and totally shuts down, the VCC will restart charging by the external start up resistor from AC line. Figure 5 shows the typical waveform of VCC under-voltage lockout



**Figure 5—VCC Under-Voltage Lockout**

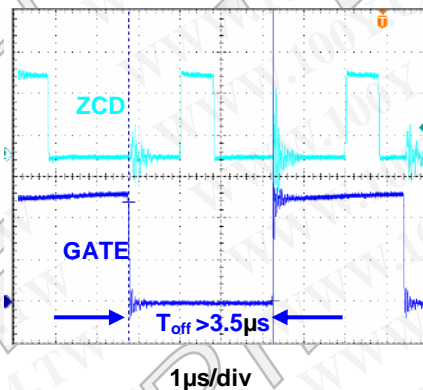
**Auto Starter**

The MP4021 integrates an auto starter, the starter starts timing when the MOSFET is turned

on, if ZCD fails to send out another turn on signal after 130µs, the starter will automatically send out the turn on signal which can avoid the IC unnecessary shut down by ZCD missing detection.

**Minimum Off Time**

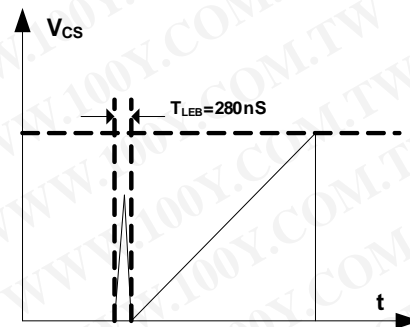
The MP4021 operates with variable switching frequency, the frequency is changing with the input instantaneous line voltage. To limit the maximum frequency and get a good EMI performance, MP4021 employs an internal minimum off time limiter—3.5µs, show as figure 6.



**Figure 6—Minimum Off Time**

**Leading Edge Blanking**

In order to avoid the premature termination of the switching pulse due to the parasitic capacitance discharging at MOSFET turning on, an internal leading edge blanking (LEB) unit is employed between the CS Pin and the current comparator input. During the blanking time, the path, CS Pin to the current comparator input, is blocked. Figure 7 shows the leading edge blanking.



**Figure 7—Leading Edge Blanking**



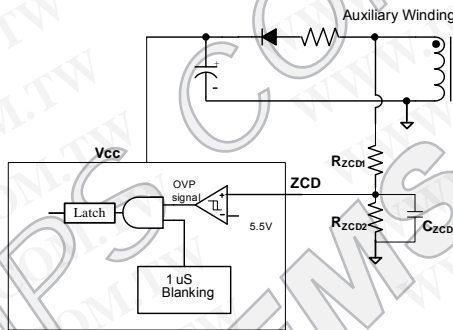
**MPS CONFIDENTIAL AND PROPRIETARY INFORMATION –3CEMS USE ONLY**

**Output Over-Voltage Protection (OVP)**

Output over voltage protection can prevent the components from damage in the over voltage condition. The positive plateau of auxiliary winding voltage is proportional to the output voltage, the OVP uses the auxiliary winding voltage instead of directly monitoring the output voltage, the OVP sample is shown in figure 8. Once the ZCD pin voltage is higher than 5.5V, the OVP signal will be triggered and latched, the gate driver will be turned off and the IC work at quiescent mode, the VCC voltage dropped below the UVLO which will make the IC shut down and the system restarts again. The output OVP setting point can be calculated as:

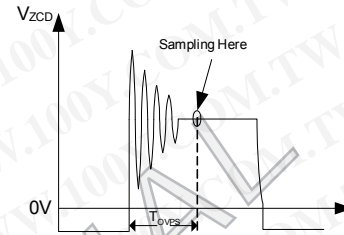
$$V_{out\_ovp} \cdot \frac{N_{aux}}{N_{sec}} \cdot \frac{R_{ZCD2}}{R_{ZCD1} + R_{ZCD2}} = 5.5$$

- $V_{out\_ovp}$ —Output over voltage protection point
- $N_{aux}$ —The auxiliary winding turns
- $N_{sec}$ —The secondary winding turns



**Figure 8—OVP Sample Unit**

To avoid the mis-trigger OVP by the oscillation spike after the switch turns off, the OVP sampling has a TOVPS blanking period, typical 1us, shown in figure 9.



**Figure 9—ZCD Voltage and OVP Sample**

**Output Short Circuit Protection**

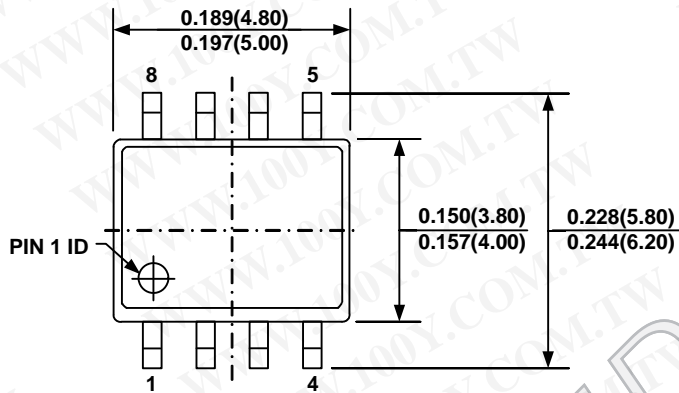
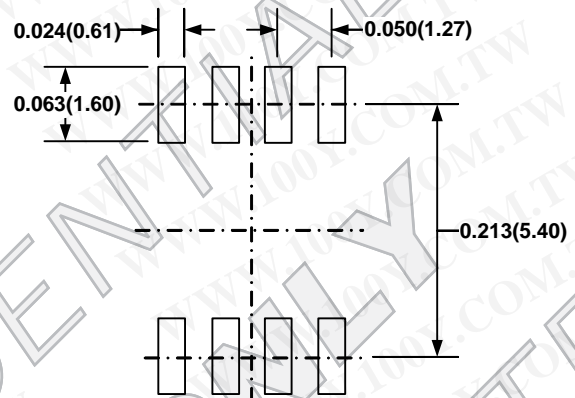
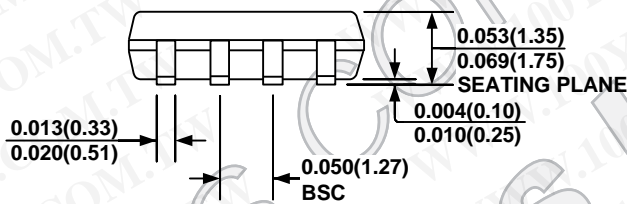
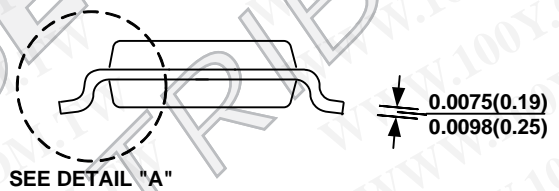
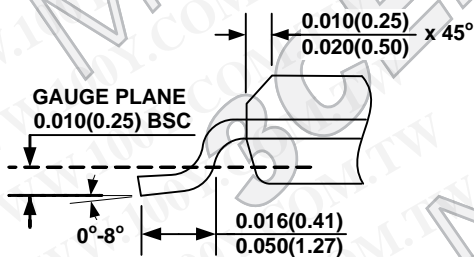
When the output short circuit happens, the positive plateau of auxiliary winding voltage is also near zero, the VCC can not be held on and it will drop below VCC UVLO. The IC will shut down and restart again.

**Thermal Shut Down**

To prevent from any lethal thermal damage, when the inner temperature exceeds 150DegC, the MP4021 shuts down switching cycle and latched until VCC drop below UVLO and restart again.

**Design Example**

For the design example, please refer to MPS application note AN038 for the detailed design procedure and information.

**PACKAGE INFORMATION**
**SOIC8**

**TOP VIEW**

**RECOMMENDED LAND PATTERN**

**FRONT VIEW**

**SIDE VIEW**

**DETAIL "A"**
**NOTE:**

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

**NOTICE:** The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.