

40-BIT AC-PDP DRIVER

DESCRIPTION

The μPD16305 is an AC plasma display panel (PDP) row driver which uses a high withstand voltage CMOS process. It is composed of a 40-bit bidirectional shift register, latch circuit, and a high withstand voltage CMOS driver block. The logic block operates on a 5V power supply (CMOS level input), enabling direct connection to a microcomputer. The driver block is implemented by means of 200V, 400mA high withstand voltage CMOS.

FEATURES

- High withstand voltage CMOS structure
- High withstand voltage, high current output (200V, 400mA)
- On-chip 40-bit bidirectional shift register
- Low power dissipation (1mA max. Ta = -40 to +85 °C)
- Wide operating temperature range (-40 to +85 °C)

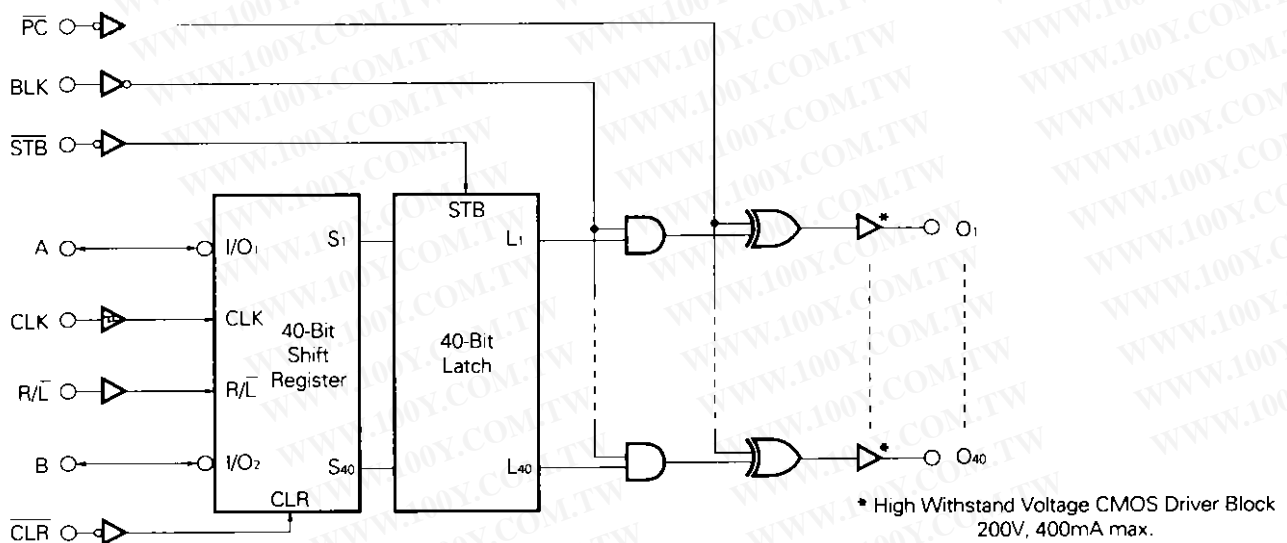
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ORDERING INFORMATION

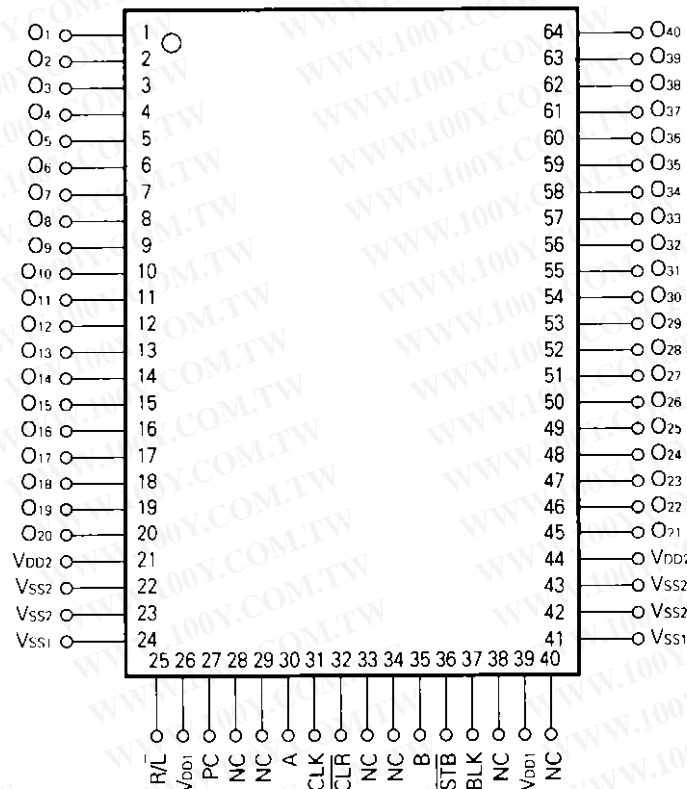
Part Number	Package	Quality Grade
μPD16305GF-3L9	80-pin plastic QFP (3-directional leads)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



- Ensure that the VDD1, VDD2, VSS1 and VSS2 pins are all used, and that VSS1 and VSS2 are used at the same potential (connect at same point near IC).
- Pin 33 is connected to the lead frame, and must therefore be left open.

DESCRIPTION OF PINS

Pin Symbol	Pin Name	Pin No.	Description
BLK	Output blank input	37	See truth table
A	RIGHT data input/output	30	Serial data input/output* When R/L = H A: Input B: Output When R/L = L A: Output B: Input
B	LEFT data input/output	35	
CLK	Clock input	31	Shift executed on rise
STB	Latch enable input	36	H:Latch, L: Data-through
R/L	Shift direction control input	25	H: Right shift mode A→O1→... O40→B L: Left shift mode B→O40→... O1→A
CLR	Clear input	32	L: Shift register ALL L
PC	Polarity reversal input	27	See truth table
O1 to O40	High withstand voltage outputs	1 to 20 45 to 64	200V, 400mA max.
VDD1	Logic block power supply	26, 39	5V ± 10%
VDD2	Driver block power supply	21, 44	30V to 180V
VSS1	Logic block ground	24, 41	Connect to system GND
VSS2	Driver block ground	22, 23, 42, 43	Connect to system GND at same point.
NC	Unused pins	28, 29, 33, 34, 38, 40	Non-connection Ensure that pin 33 is left open.

* Data resulting from inversion of the data input is input to the shift register, and data resulting from inversion of the shift register data is output to the output.

TRUTH TABLE 1 (Shift Register Block)

R/L	CLK	A	B	Shift Register
H	↑	Input	Output	Right shift execution
H	H or L			Hold
L	↑	Output	Input	Left shift execution
L	H or L			Hold

TRUTH TABLE 2 (Latch Block)

STB	Operation
H	Data immediately prior to STB becoming H is held
L	Shift register data is output

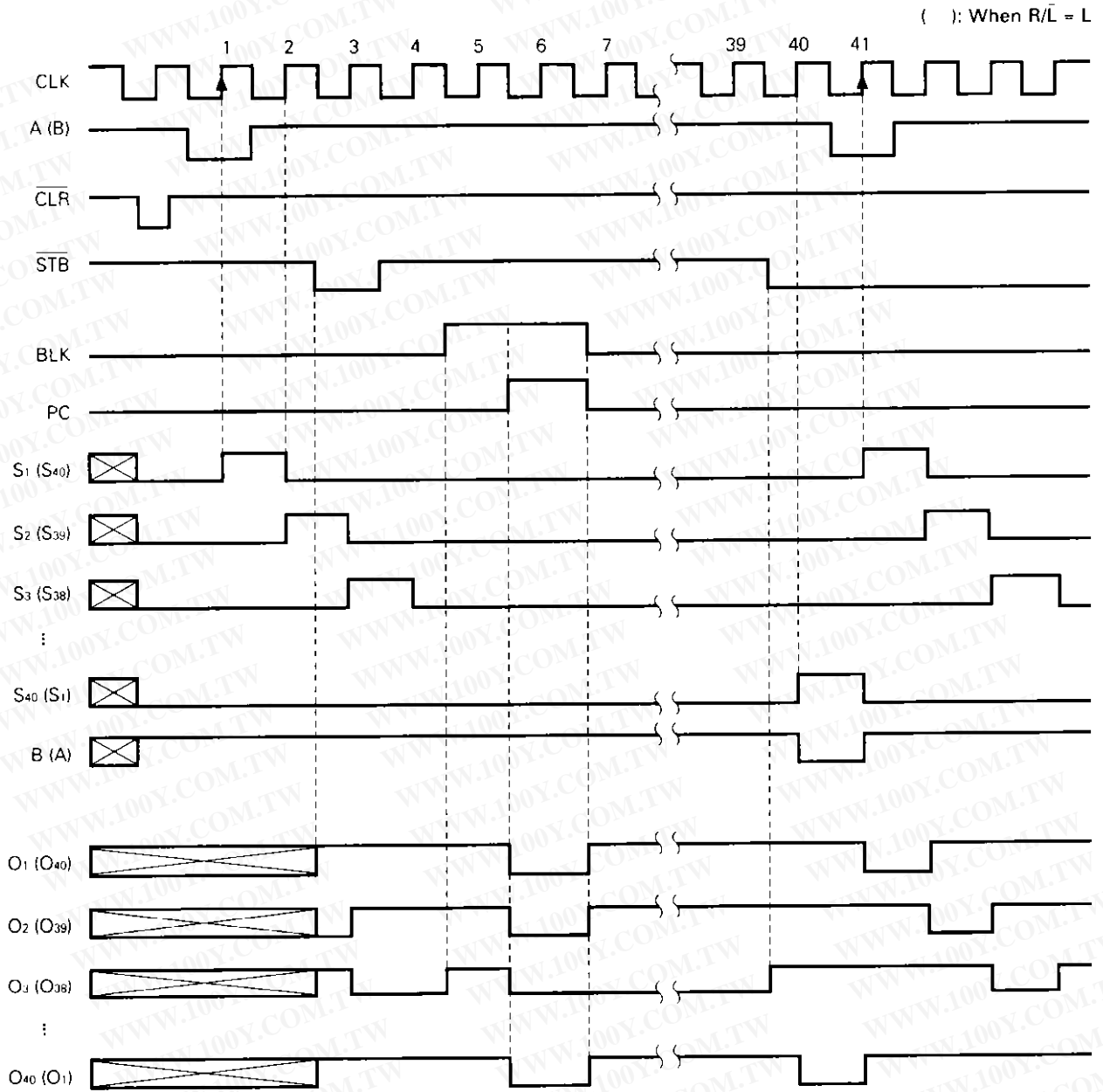
TRUTH TABLE 3 (Driver Block)

DATA	BLK	PC	On	Remarks
H	L	L	H	
L	L	L	L	
H	L	H	L	
L	L	H	H	
x	H	L	H	All outputs H
x	H	H	L	All outputs L

H : High level
 L : Low level
 x : H or L
 DATA : Data input to A (B)

Caution To prevent latch up breakdown, the power should be turned on in the order V_{DD1}, logic signal, V_{DD2}. It should be turned off in the opposite order.

TIMING CHART



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C, Vss1 = Vss2 = 0V)

PARAMETER	SYMBOL	RATING	UNIT
Logic block supply voltage	VDD1	- 0.5 to + 7.0	V
Driver block supply voltage	VDD2	- 0.5 to + 200	V
Logic block input voltage	Vi	- 0.5 to VDD1 + 0.5	V
Driver block output current	Io	400 *	mA
Input current	Ii	± 25	mA
Permissible package loss	Pd	1000	mW
Operating temperature	T _{opt.}	- 40 to + 85	°C
Storage temperature	T _{stg.}	- 65 to + 150	°C

* Duty ≤ 1/40

RECOMMENDED OPERATING CONDITIONS (Ta = - 40 to + 85 °C, Vss1 = Vss2 = 0V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Logic block supply voltage	VDD1	4.5	5.0	5.5	V
Driver block supply voltage	VDD2	30		180	V
Input voltage high	V _{IH}	0.7 · VDD1		VDD1	V
Input voltage low	V _{IL}	0		0.2 · VDD1	V
Driver output current	Io			± 300	mA

ELECTRICAL SPECIFICATIONS (Ta = 25 °C, VDD1 = 4.5 to 5.5V, VDD2 = 180V, VSS1 = VSS2 = 0V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output voltage high	V _{OH1}	0.9 · V _{DD1}			V	Logic I _{OH} = - 1mA
Output voltage low	V _{OL1}			0.1 · V _{DD1}	V	Logic I _{OL} = 1mA
Output voltage high	V _{OH21}	160	172		V	O ₁ to O ₄₀ , I _{OH} = - 150mA
	V _{OH22}	140	163		V	O ₁ to O ₄₀ , I _{OH} = - 300mA
Output voltage low	V _{OL21}		10	20	V	O ₁ to O ₄₀ , I _{OL} = 150mA
	V _{OL22}		35	40	V	O ₁ to O ₄₀ , I _{OL} = 300mA
Input current	I _I			± 1	μA	V _I = V _{DD1} or V _{SS1}
Input voltage high	V _{IH}	0.7 · V _{DD1}			V	
Input voltage low	V _{IL}			0.2 · V _{DD1}	V	
Static consumption current	I _{DD1}			100	μA	Logic Ta = - 40 to + 85 °C
	I _{DD1}		0.02	10	μA	Logic Ta = 25 °C
	I _{DD2}			1	mA	Driver Ta = - 40 to + 85 °C
	I _{DD2}		0.4	100	μA	Driver Ta = 25 °C

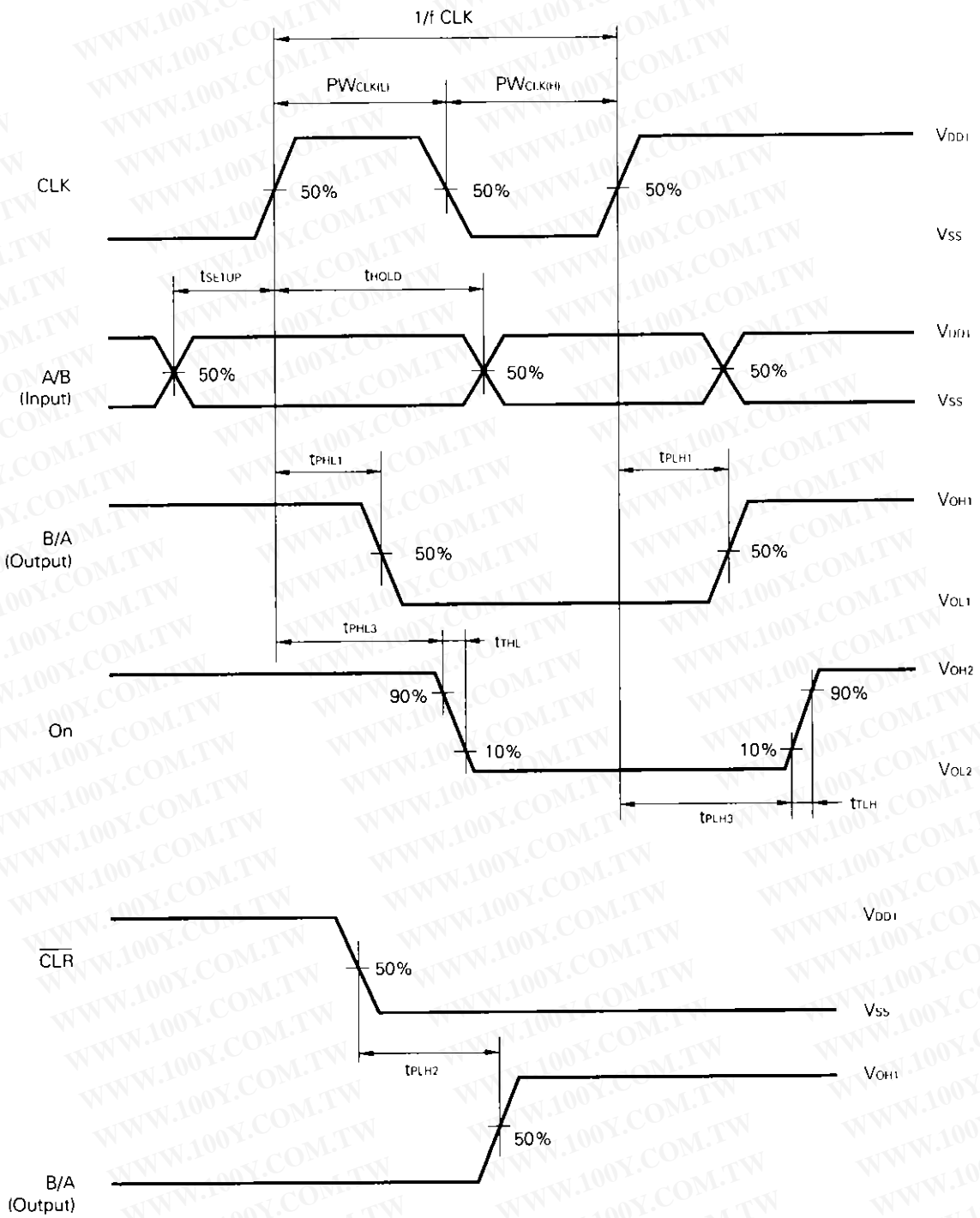
SWITCHING CHARACTERISTICS ($T_a = 25\text{ }^\circ\text{C}$, $V_{DD1} = 5\text{V}$, $V_{DD2} = 180\text{V}$, Logic $C_L = 15\text{pF}$, Driver $C_L = 50\text{pF}$)

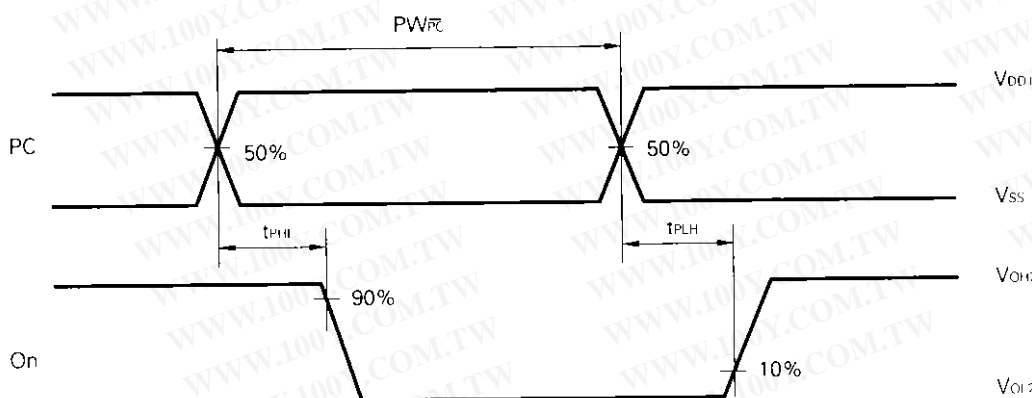
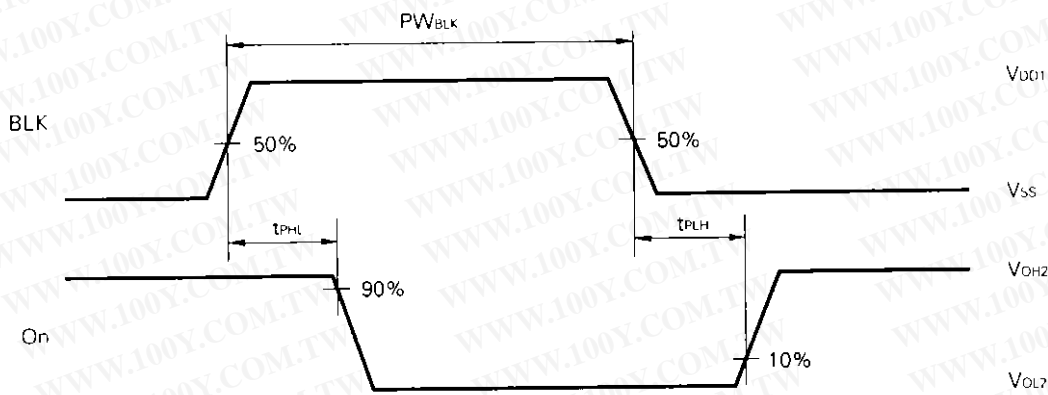
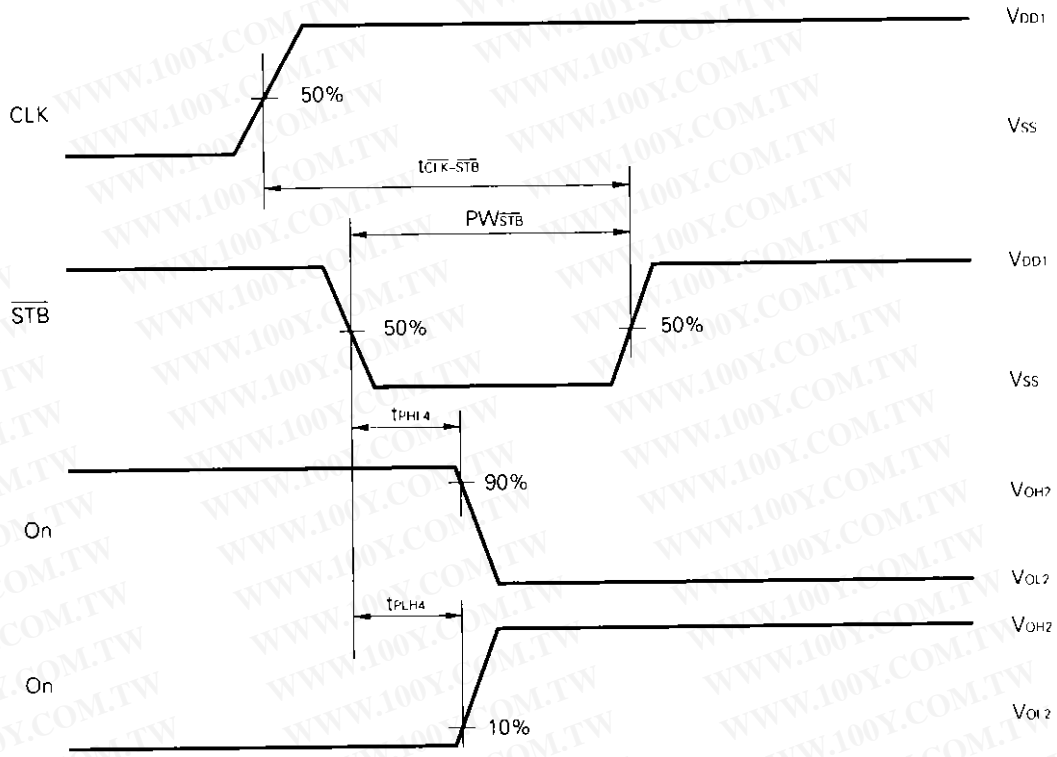
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Transmission delay time	t_{PHL1}		60	120	ns	CLK→A/B
	t_{PLH1}		60	120	ns	
	t_{PLH2}		70	120	ns	CL \bar{R} →A/B
	t_{PHL3}		110	200	ns	CLK→O ₁ to O ₄₀
	t_{PLH3}		110	200	ns	
	t_{PHL4}		90	200	ns	$\bar{S}T\bar{B}$ →O ₁ to O ₄₀
	t_{PLH4}		90	200	ns	
	t_{PHL5}		90	220	ns	BLK→O ₁ to O ₄₀
	t_{PLH5}		90	220	ns	
	t_{PHL6}		120	220	ns	PC→O ₁ to O ₄₀
t_{PLH6}		120	220	ns		
Rise time	t_{TLH}		30	100	ns	O ₁ to O ₄₀
Fall time	t_{THL}		50	100	ns	O ₁ to O ₄₀
Maximum clock frequency (DATA)	f_{max}	15	25		MHz	Duty = 50%
Input capacitance	C_i		10	15	pF	

REQUIRED TIMING CONDITIONS ($T_a = -40\text{ to }+85\text{ }^\circ\text{C}$, $V_{DD1} = 4.5\text{ to }5.5\text{V}$)

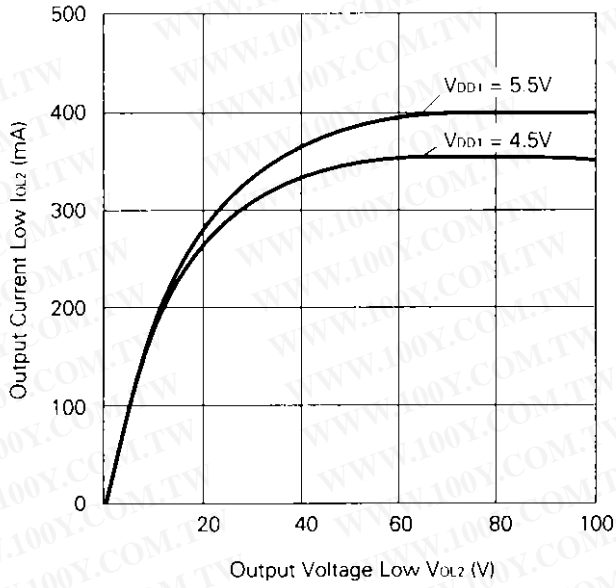
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Clock pulse width	PW_{CLK}	30			ns	
Strobe pulse width	PW_{STB}	60			ns	
Blank pulse width	PW_{BLK}	200			ns	
PC pulse width	PW_{PC}	300			ns	
Clear pulse width	PW_{CLR}	120			ns	
Data setup time	t_{SETUP}	20			ns	
Data hold time	t_{HOLD}	5			ns	
Clock-strobe time	$t_{CLK-STB}$	120			ns	CLK↑ →STB↑

SWITCHING CHARACTERISTIC WAVEFORMS

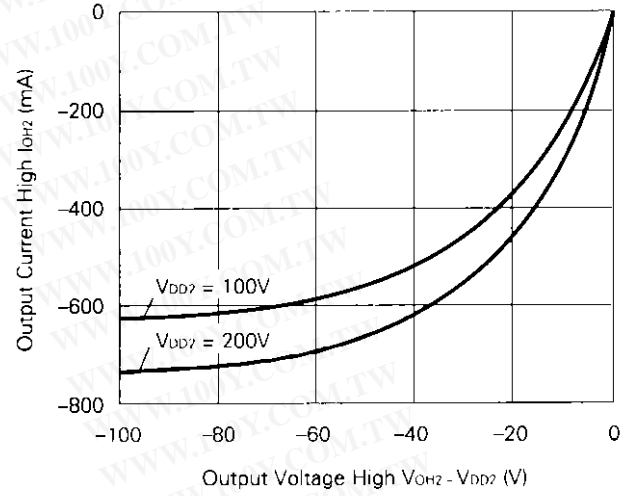




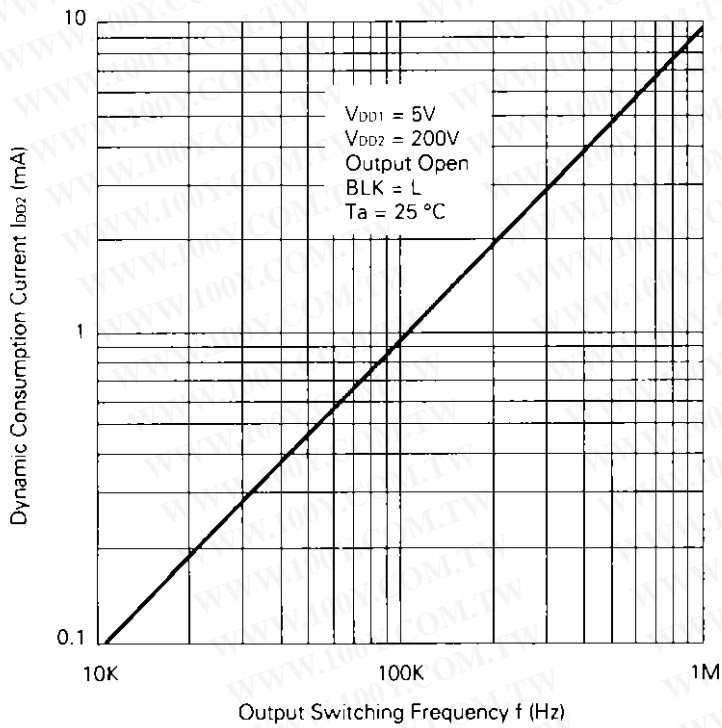
I_{OL2} – V_{OL2} Characteristic
 (Pulse Measurement 300 μs, T_a = 25 °C)



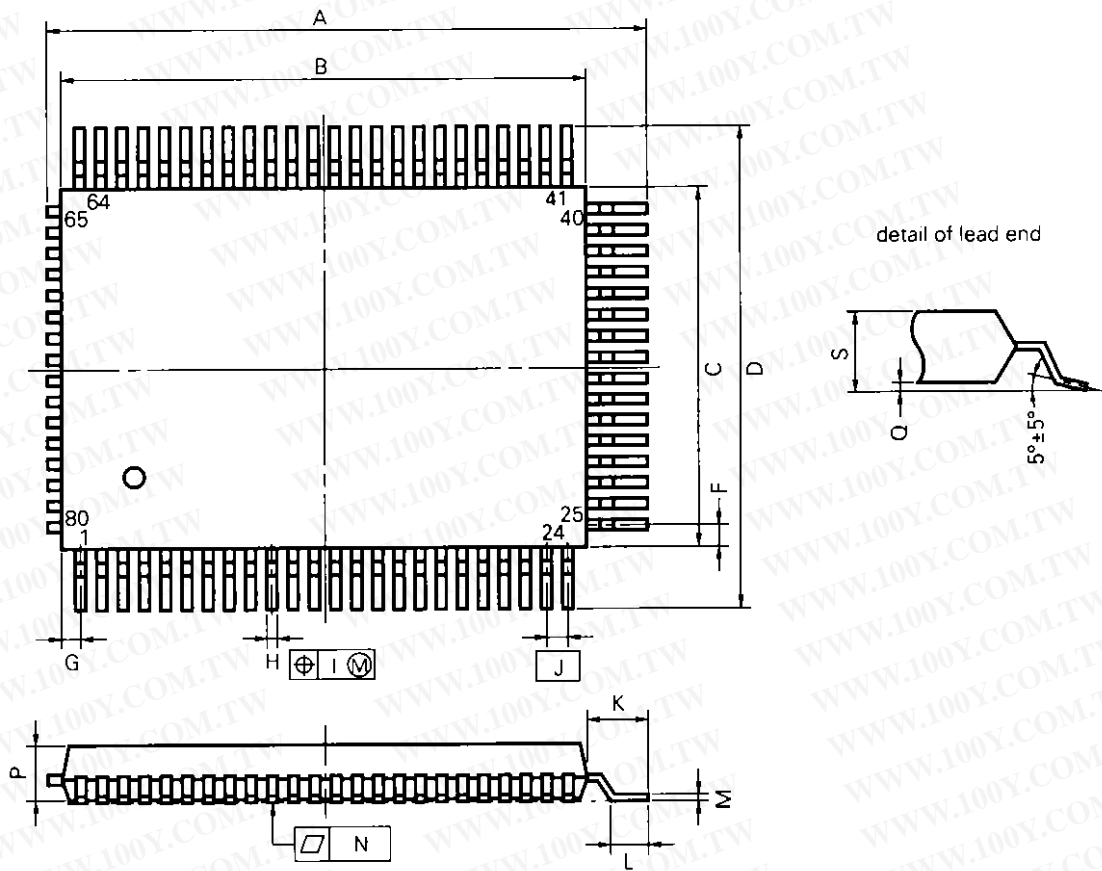
I_{OH2} – V_{OH2} Characteristic
 (Pulse Measurement 300 μs, T_a = 25 °C)



Dynamic Consumption Current Characteristic (Per Channel)



PACKAGE INFORMATION
80 PIN PLASTIC QFP (THREE DIRECTIONS) (14x20)



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (I.P.) at maximum material condition.

P80GF-80-3L9-1

ITEM	MILLIMETERS	INCHES
A	22.3±0.4	0.878±0.016
B	20.0±0.2	0.795 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	0.8	0.031
H	0.35±0.10	0.014 ^{+0.004} _{-0.005}
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071 ^{+0.008} _{-0.009}
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.003}
N	0.15	0.006
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended in the table below.
 For soldering methods and conditions other than those recommended, please contact our salesman.

Surface Mount Type

For details of recommended soldering conditions for the surface mounting type, refer to the information document "Surface Mount Technology Manual" (IEI-1207).

μPD16305GF-3L9

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230 °C, Duration: 30 sec. max. (at 210 °C or above) Number of times: once, Time limit: None*	IR30-00
VPS	Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above) Number of times: once, Time limit: None*	VP15-00
Pin part heating	Pin part temperature: 300°C or less, Duration: 10 sec. max., Time limit: None*	○

* For the storage period after dry-pack decapsulation, storage conditions are max. 25°C, 65% RH.

Note Use of more than one soldering method should be avoided (except in the case of pin part heating).

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