

DATA SHEET



PCF8566

Universal LCD driver for low
multiplex rates

Product specification
Supersedes data of 1997 Apr 02
File under Integrated Circuits, IC12

1998 May 04

勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-54151736
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)



Universal LCD driver for low multiplex rates

PCF8566**CONTENTS**

| | | | |
|------|---|--------|---|
| 1 | FEATURES | 8 | LIMITING VALUES |
| 2 | GENERAL DESCRIPTION | 9 | HANDLING |
| 3 | ORDERING INFORMATION | 10 | DC CHARACTERISTICS |
| 4 | BLOCK DIAGRAM | 11 | AC CHARACTERISTICS |
| 5 | PINNING | 12 | APPLICATION INFORMATION |
| 6 | FUNCTIONAL DESCRIPTION | 13 | CHIP DIMENSIONS AND BONDING PAD LOCATIONS |
| 6.1 | Power-on reset | 14 | PACKAGE OUTLINES |
| 6.2 | LCD bias generator | 15 | SOLDERING |
| 6.3 | LCD voltage selector | 15.1 | Introduction |
| 6.4 | LCD drive mode waveforms | 15.2 | DIP |
| 6.5 | Oscillator | 15.2.1 | Soldering by dipping or by wave |
| 6.6 | Internal clock | 15.2.2 | Repairing soldered joints |
| 6.7 | External clock | 15.3 | SO and VSO |
| 6.8 | Timing | 15.3.1 | Reflow soldering |
| 6.9 | Display latch | 15.3.2 | Wave soldering |
| 6.10 | Shift register | 15.3.3 | Repairing soldered joints |
| 6.11 | Segment outputs | 16 | DEFINITIONS |
| 6.12 | Backplane outputs | 17 | LIFE SUPPORT APPLICATIONS |
| 6.13 | Display RAM | 18 | PURCHASE OF PHILIPS I ² C COMPONENTS |
| 6.14 | Data pointer | | |
| 6.15 | Subaddress counter | | |
| 6.16 | Output bank selector | | |
| 6.17 | Input bank selector | | |
| 6.18 | Blinker | | |
| 7 | I ² C-BUS DESCRIPTION | | |
| 7.1 | Bit transfer | | |
| 7.2 | Start and stop conditions | | |
| 7.3 | System configuration | | |
| 7.4 | Acknowledge | | |
| 7.5 | PCF8566 I ² C-bus controller | | |
| 7.6 | Input filters | | |
| 7.7 | I ² C-bus protocol | | |
| 7.8 | Command decoder | | |
| 7.9 | Display controller | | |
| 7.10 | Cascaded operation | | |

Universal LCD driver for low multiplex rates

PCF8566



1 FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2, 3 or 4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$ or $\frac{1}{3}$
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24×4 -bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2.5 to 6 V power supply range
- Low power consumption
- Power saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576C
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40 lead plastic very small outline package (VSO40; SOT158-1)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

3 ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|-------------|---------|--|----------|
| | NAME | DESCRIPTION | VERSION |
| PCF8566P | DIP40 | plastic dual in-line package; 40 leads (600 mil) | SOT129-1 |
| PCF8566T | VSO40 | plastic very small outline package; 40 leads | SOT158-1 |

Universal LCD driver for low multiplex rates

PCF8566

4 BLOCK DIAGRAM

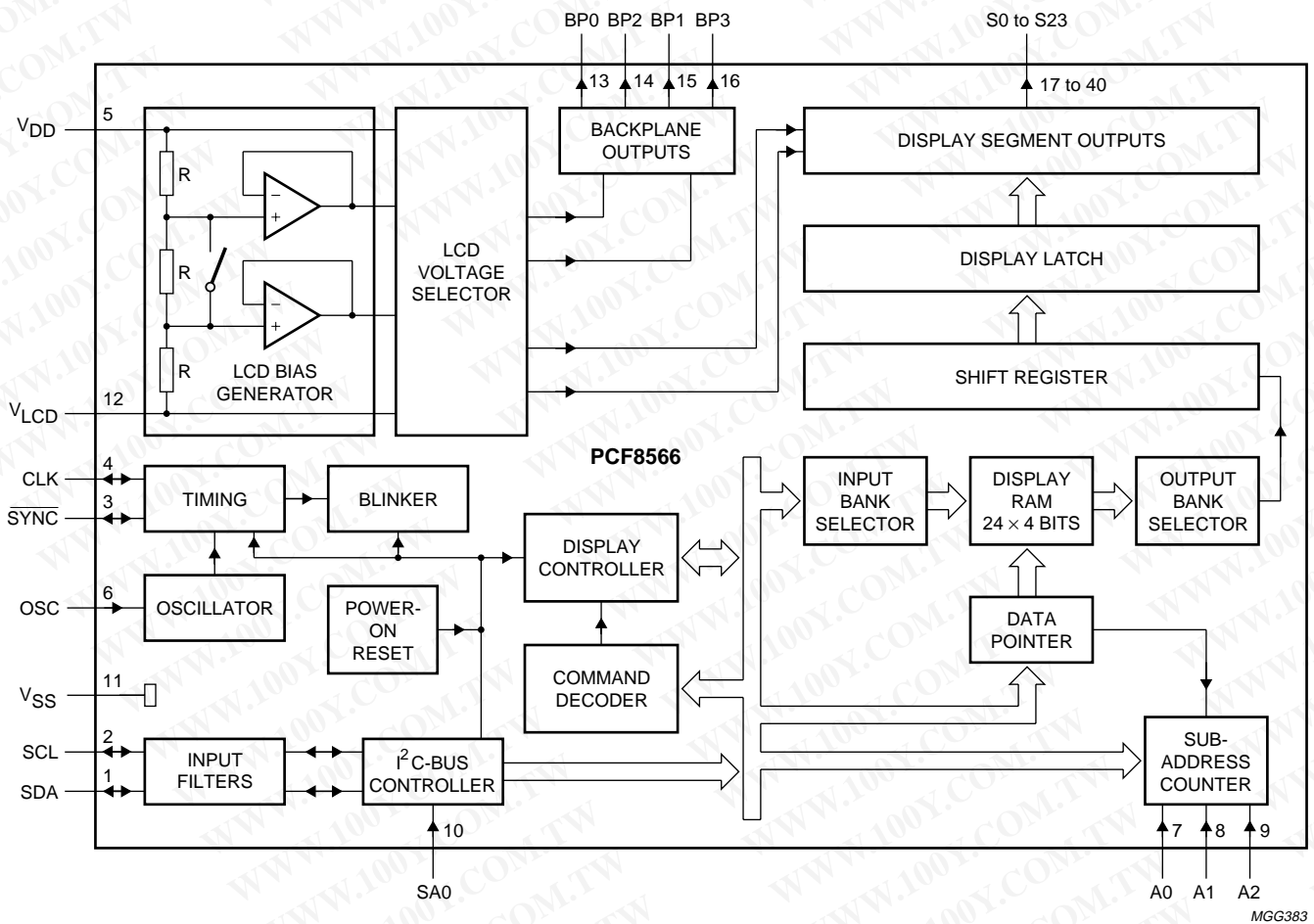


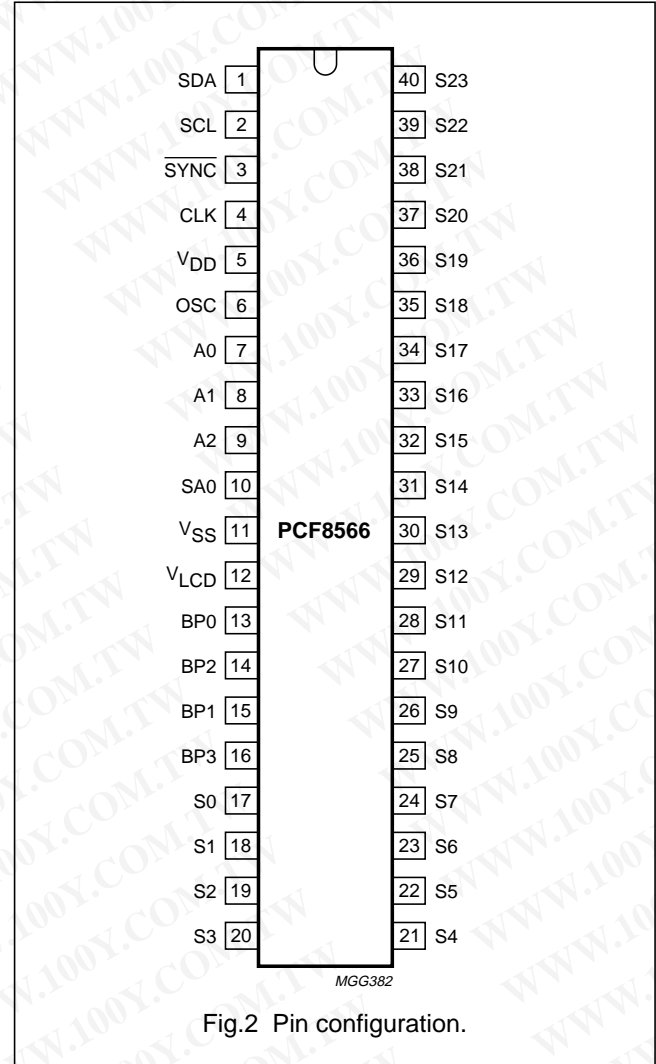
Fig.1 Block diagram.

Universal LCD driver for low multiplex rates

PCF8566

5 PINNING

| SYMBOL | PIN | DESCRIPTION |
|------------------|----------|--|
| SDA | 1 | I ² C-bus data input/output |
| SCL | 2 | I ² C-bus clock input/output |
| SYNC | 3 | cascade synchronization input/output |
| CLK | 4 | external clock input/output |
| V _{DD} | 5 | positive supply voltage |
| OSC | 6 | oscillator input |
| A0 | 7 | I ² C-bus subaddress inputs |
| A1 | 8 | |
| A2 | 9 | |
| SA0 | 10 | I ² C-bus slave address bit 0 input |
| V _{SS} | 11 | logic ground |
| V _{LCD} | 12 | LCD supply voltage |
| BP0 | 13 | LCD backplane outputs |
| BP2 | 14 | |
| BP1 | 15 | |
| BP3 | 16 | |
| S0 to S23 | 17 to 40 | LCD segment outputs |



勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

Universal LCD driver for low multiplex rates

PCF8566

6 FUNCTIONAL DESCRIPTION

The PCF8566 is a versatile peripheral device designed to interface any microprocessor to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to 4 backplanes and up to 24 segments. The display configurations possible with the PCF8566 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig.3. The host microprocessor/microcontroller maintains the two-line I²C-bus communication channel with the PCF8566. The internal oscillator is selected by tying OSC (pin 6) to V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

Table 1 Selection of display configurations

| ACTIVE BACKPLANE OUTPUTS | NUMBER OF SEGMENTS | 7-SEGMENT NUMERIC | 14-SEGMENT ALPHANUMERIC | DOT MATRIX |
|--------------------------|--------------------|----------------------------------|-------------------------------------|------------------|
| 4 | 96 | 12 digits + 12 indicator symbols | 6 characters + 12 indicator symbols | 96 dots (4 × 24) |
| 3 | 72 | 9 digits + 9 indicator symbols | 4 characters + 16 indicator symbols | 72 dots (3 × 24) |
| 2 | 48 | 6 digits + 6 indicator symbols | 3 characters + 6 indicator symbols | 48 dots (2 × 24) |
| 1 | 24 | 3 digits + 3 indicator symbols | 1 character + 10 indicator symbols | 24 dots |

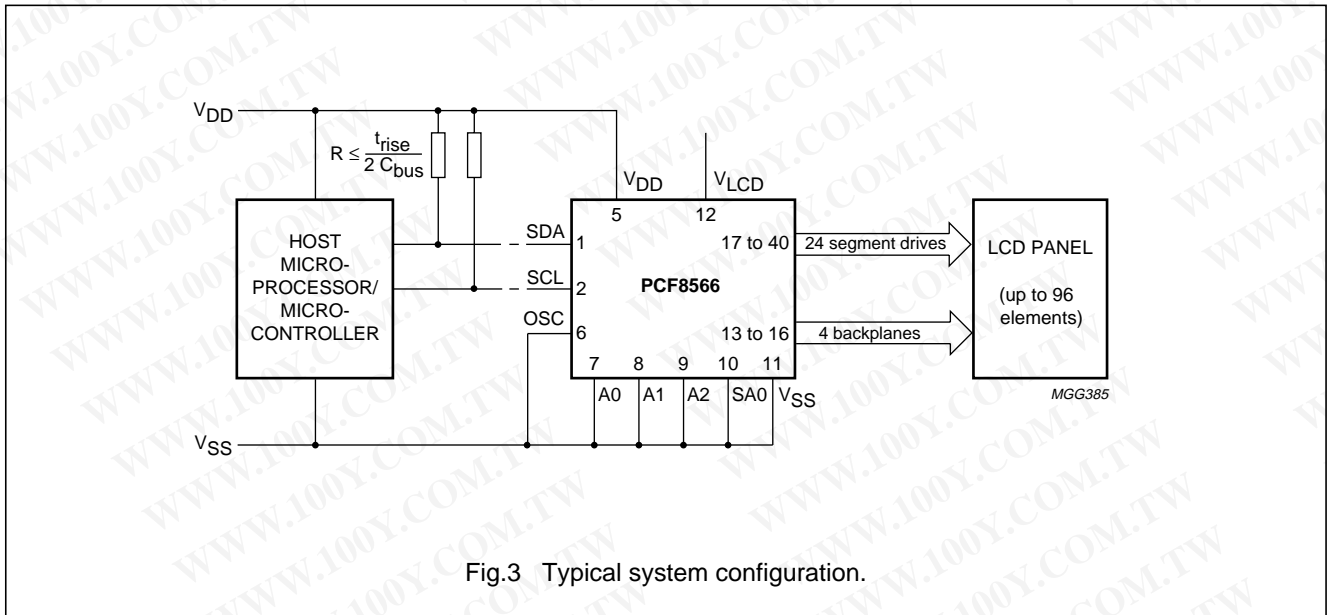


Fig.3 Typical system configuration.

Universal LCD driver for low multiplex rates

PCF8566

6.1 Power-on reset

At power-on the PCF8566 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}
2. All segment outputs are set to V_{DD}
3. The drive mode '1 : 4 multiplex with $\frac{1}{3}$ bias' is selected
4. Blinking is switched off
5. Input and output bank selectors are reset (as defined in Table 5)
6. The I²C-bus interface is initialized
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I²C-bus should be avoided for 1 ms following power-on to allow completion of the reset action.

6.2 LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD} . The centre resistor can be switched out of circuit to provide a $\frac{1}{2}$ bias voltage level for the 1 : 2 multiplex configuration.

6.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

A practical value of V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \geq 3 V_{th}$. Multiplex drive ratios of 1 : 3 and 1 : 4 with $\frac{1}{2}$ bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1.732$ for 1 : 3 multiplex or $\sqrt{21}/3 = 1.528$ for 1 : 4 multiplex). The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

1 : 3 multiplex ($\frac{1}{2}$ bias):

$$V_{op} = \sqrt{6} V_{op(mrs)} = 2.449 V_{off(rms)}$$

1 : 4 multiplex ($\frac{1}{2}$ bias):

$$V_{op} = \sqrt[4]{3}/3 V_{off(rms)} = 2.309 V_{off(rms)}$$

These compare with $V_{op} = 3 V_{off(rms)}$ when $\frac{1}{3}$ bias is used.

Table 2 Preferred LCD drive modes: summary of characteristics

| LCD DRIVE MODE | LCD BIAS CONFIGURATION | $\frac{V_{off(rms)}}{V_{op}}$ | $\frac{V_{on(rms)}}{V_{op}}$ | $D = \frac{V_{on(rms)}}{V_{off(rms)}}$ |
|------------------|--------------------------|-------------------------------|------------------------------|--|
| Static (1 BP) | static (2 levels) | 0 | 1 | ∞ |
| 1 : 2 MUX (2 BP) | $\frac{1}{2}$ (3 levels) | $\sqrt{2}/4 = 0.354$ | $\sqrt{10}/4 = 0.791$ | $\sqrt{5} = 2.236$ |
| 1 : 2 MUX (2 BP) | $\frac{1}{3}$ (4 levels) | $\frac{1}{3} = 0.333$ | $\sqrt{5}/3 = 0.745$ | $\sqrt{5} = 2.236$ |
| 1 : 3 MUX (3 BP) | $\frac{1}{3}$ (4 levels) | $\frac{1}{3} = 0.333$ | $\sqrt{33}/9 = 0.638$ | $\sqrt{33}/3 = 1.915$ |
| 1 : 4 MUX (4 BP) | $\frac{1}{3}$ (4 levels) | $\frac{1}{3} = 0.333$ | $\sqrt{3}/3 = 0.577$ | $\sqrt{3} = 1.732$ |

Universal LCD driver for low multiplex rates

PCF8566

6.4 LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig.4.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8566 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

The backplane and segment drive waveforms for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

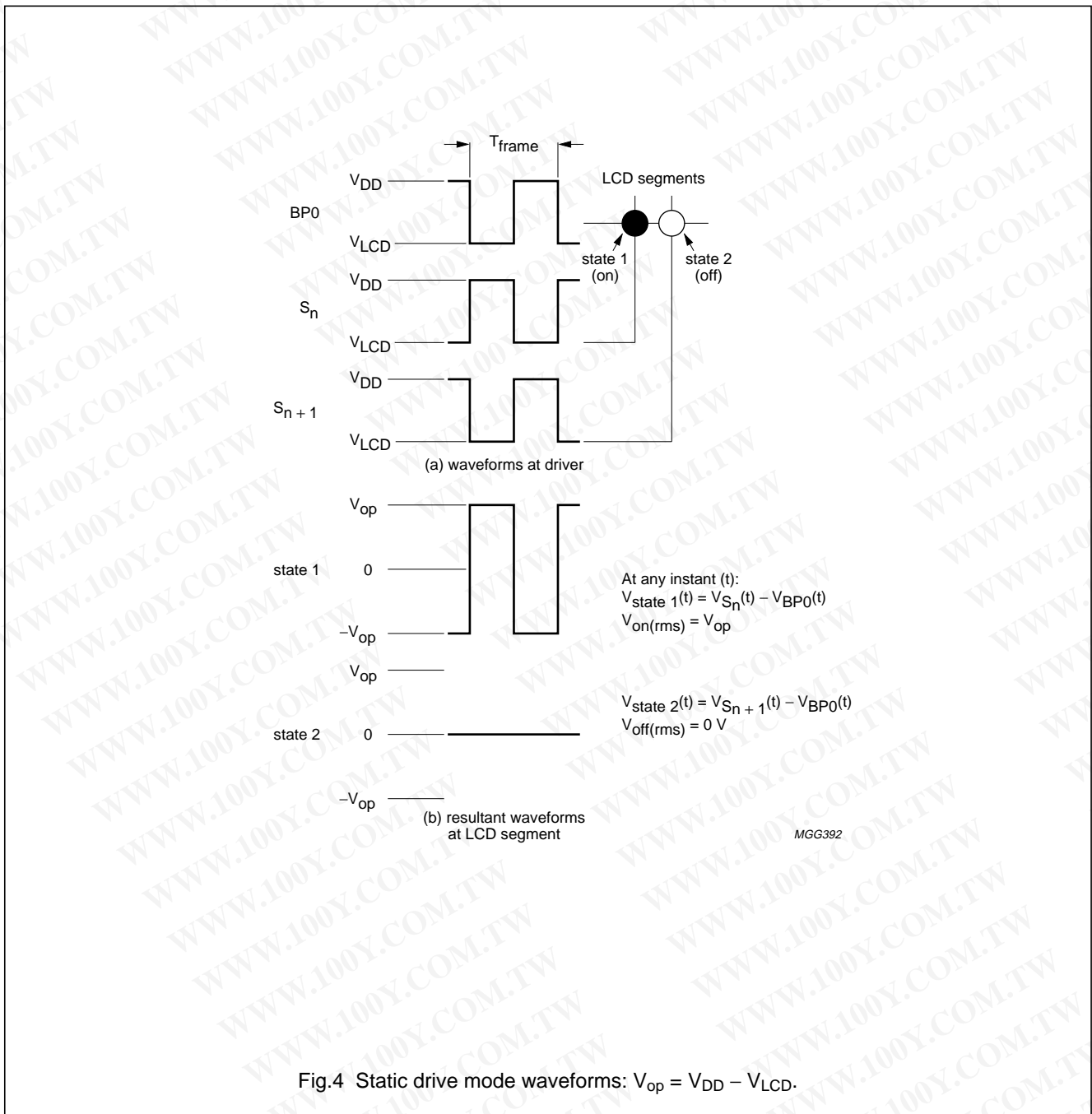


Fig.4 Static drive mode waveforms: V_{op} = V_{DD} - V_{LCD}.

Universal LCD driver for low multiplex rates

PCF8566

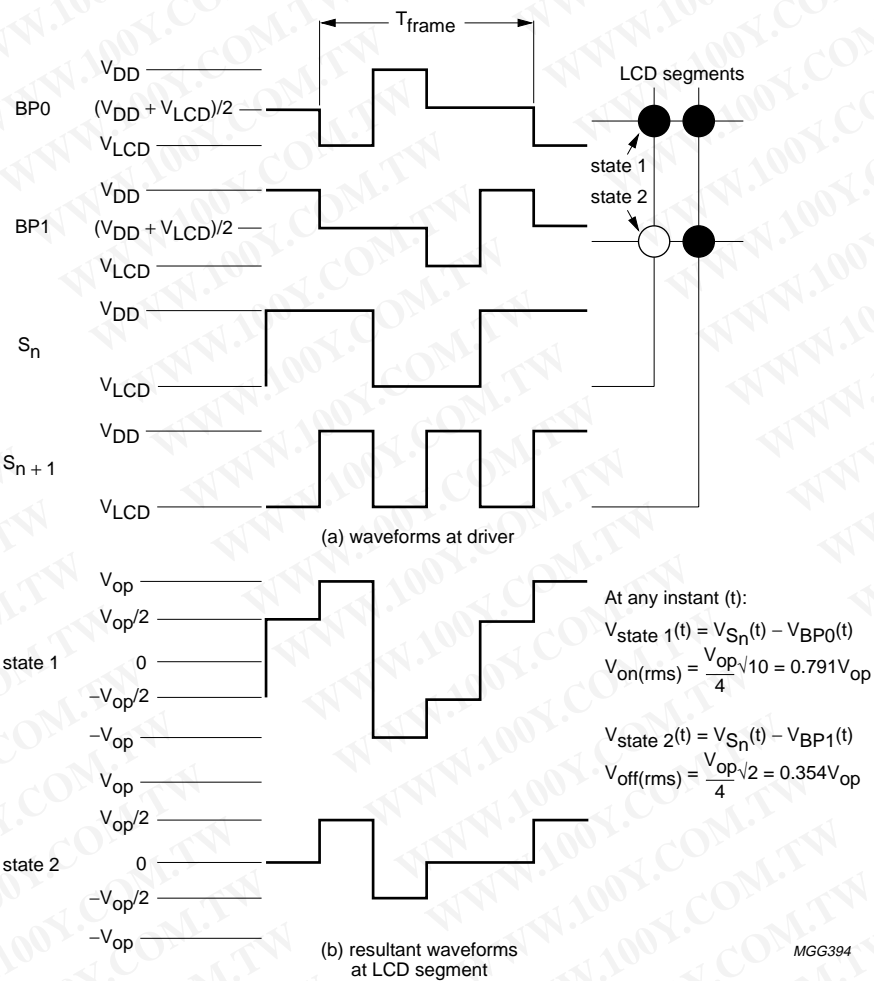
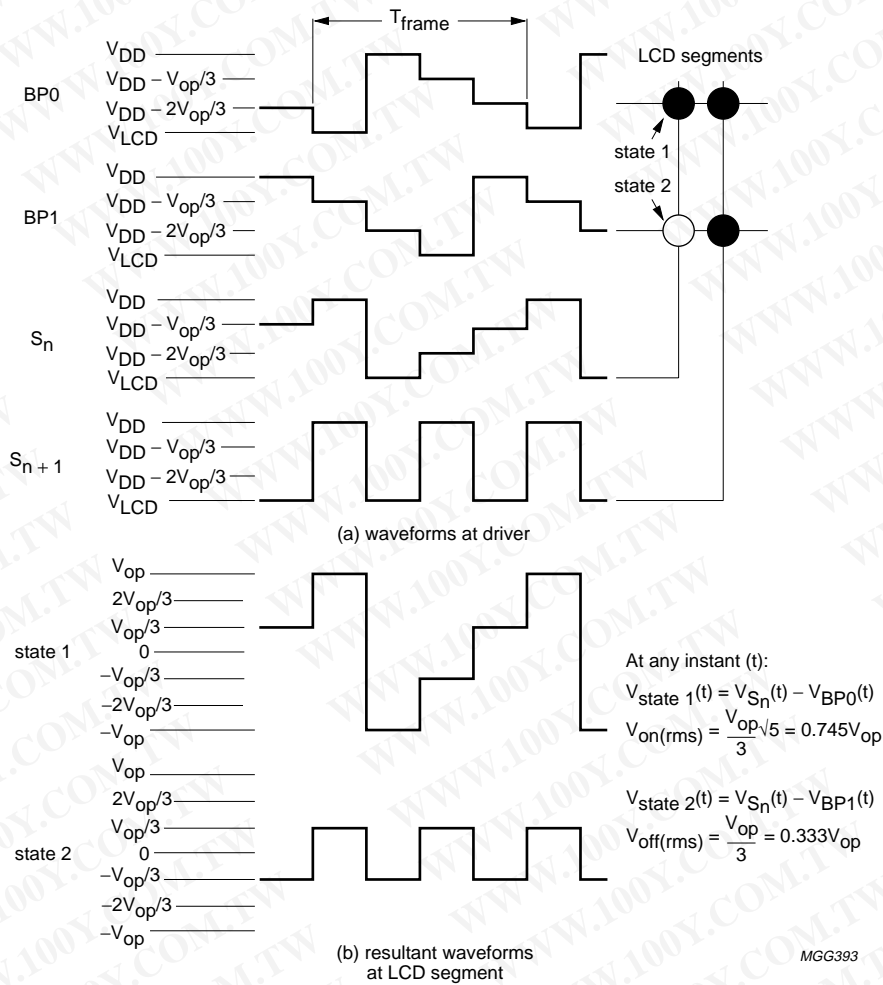


Fig.5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

Universal LCD driver for low multiplex rates

PCF8566



勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

Fig.6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

Universal LCD driver for low multiplex rates

PCF8566

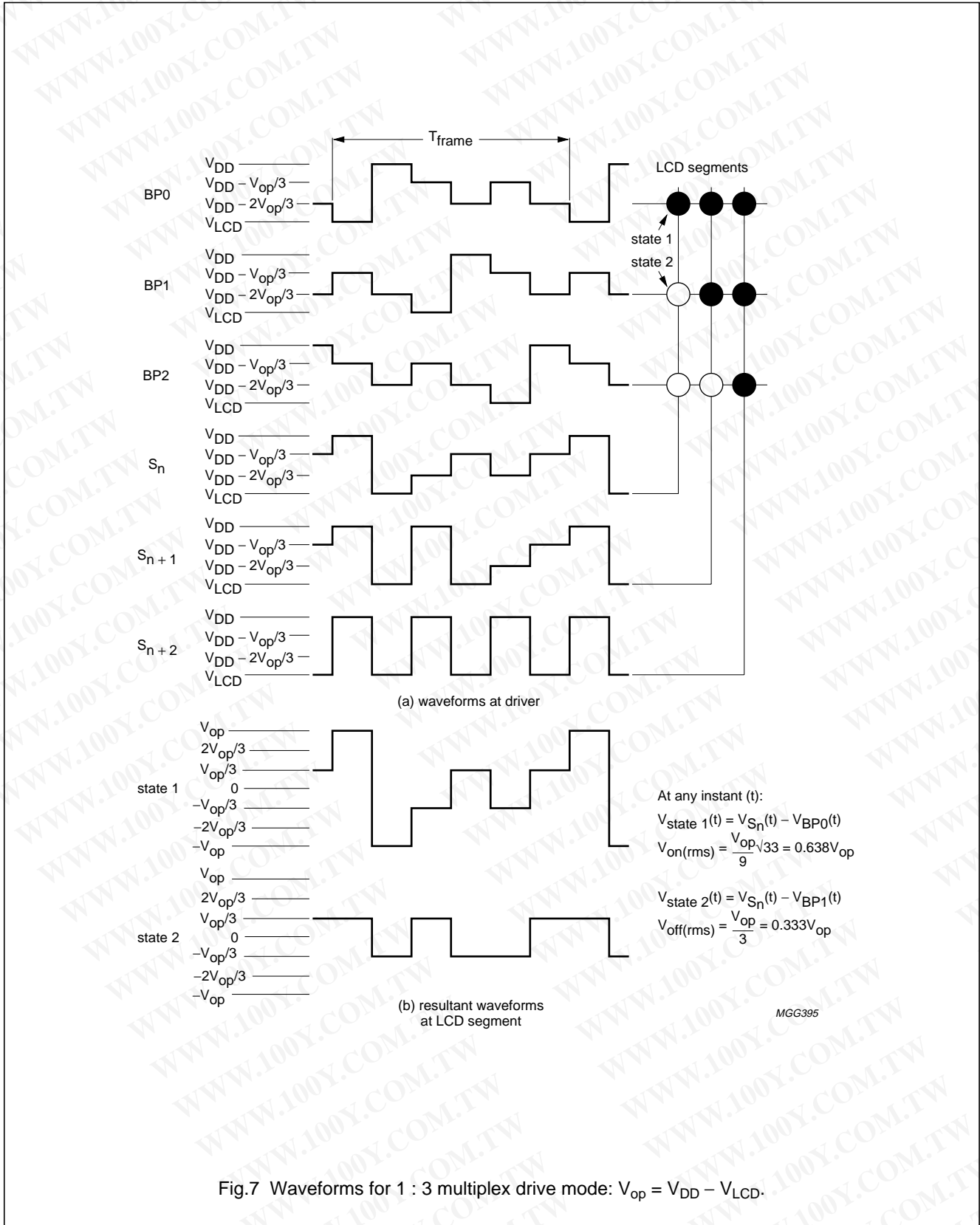


Fig.7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Universal LCD driver for low multiplex rates

PCF8566

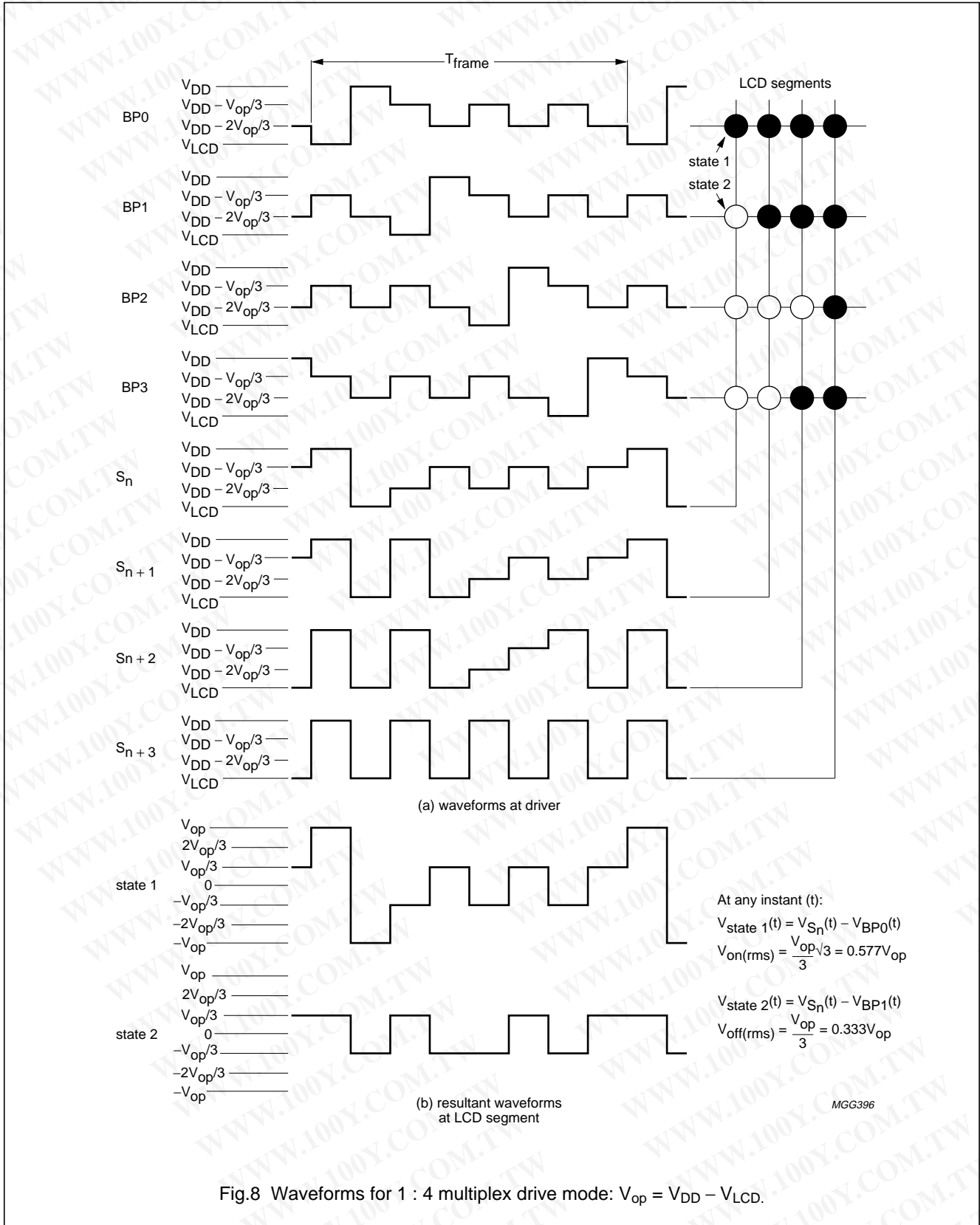


Fig.8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Universal LCD driver for low multiplex rates

PCF8566

6.5 Oscillator

The internal logic and the LCD drive signals of the PCF8566 or PCF8576 are timed either by the built-in oscillator or from an external clock.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I²C-bus. To allow I²C-bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

6.6 Internal clock

When the internal oscillator is used, OSC (pin 6) should be tied to V_{SS} . In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8566s and PCF8576s in the system.

6.7 External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD} ; CLK (pin 4) then becomes the external clock input.

6.8 Timing

The timing of the PCF8566 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal SYNC maintains the correct timing relationship between the PCF8566s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by MODE SET commands when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

| PCF8566 MODE | f_{frame} | NOMINAL f_{frame} (Hz) |
|-------------------|----------------|--------------------------|
| Normal mode | $f_{CLK}/2880$ | 64 |
| Power saving mode | $f_{CLK}/480$ | 64 |

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation.

The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I²C-bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I²C-bus but no data loss occurs.

6.9 Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

6.10 Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

6.11 Segment outputs

The LCD drive section includes 24 segment outputs S0 to S23 (pins 17 to 40) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 24 segment outputs are required the unused segment outputs should be left open-circuit.

6.12 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

6.13 Display RAM

The display RAM is a static 24 × 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state.

Universal LCD driver for low multiplex rates

PCF8566

| drive mode | LCD segments | LCD backplanes | display RAM filling order | transmitted display byte | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------------|--------------|----------------|---|--------------------------|-----|-----|---------|---------|---------|-----|-----|-----|---------|----|---|---|---|----|---|---|---|---|----|---|---|----|---|---|---|---|---|---|---|---|---|---|----|---|---|--|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|
| static | | | <table border="1"> <thead> <tr> <th></th> <th>n</th> <th>n+1</th> <th>n+2</th> <th>n+3</th> <th>n+4</th> <th>n+5</th> <th>n+6</th> <th>n+7</th> </tr> </thead> <tbody> <tr> <td>bit/ BP</td> <td>0</td> <td>c</td> <td>b</td> <td>a</td> <td>f</td> <td>g</td> <td>e</td> <td>d</td> </tr> <tr> <td></td> <td>1</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> </tr> <tr> <td></td> <td>2</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> </tr> <tr> <td></td> <td>3</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> </tr> </tbody> </table> | | n | n+1 | n+2 | n+3 | n+4 | n+5 | n+6 | n+7 | bit/ BP | 0 | c | b | a | f | g | e | d | | 1 | x | x | x | x | x | x | x | | 2 | x | x | x | x | x | x | x | | 3 | x | x | x | x | x | x | x | <p>MSB</p> <p>LSB</p> <table border="1"> <tr> <td>c</td> <td>b</td> <td>a</td> <td>f</td> <td>g</td> <td>e</td> <td>d</td> <td>DP</td> </tr> </table> | c | b | a | f | g | e | d | DP |
| | n | n+1 | n+2 | n+3 | n+4 | n+5 | n+6 | n+7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| bit/ BP | 0 | c | b | a | f | g | e | d | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 1 | x | x | x | x | x | x | x | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 2 | x | x | x | x | x | x | x | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 3 | x | x | x | x | x | x | x | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c | b | a | f | g | e | d | DP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 : 2 multiplex | | | <table border="1"> <thead> <tr> <th></th> <th>n</th> <th>n+1</th> <th>n+2</th> <th>n+3</th> </tr> </thead> <tbody> <tr> <td>bit/ BP</td> <td>0</td> <td>a</td> <td>f</td> <td>e</td> </tr> <tr> <td></td> <td>1</td> <td>b</td> <td>g</td> <td>c</td> </tr> <tr> <td></td> <td>2</td> <td>x</td> <td>x</td> <td>x</td> </tr> <tr> <td></td> <td>3</td> <td>x</td> <td>x</td> <td>x</td> </tr> </tbody> </table> | | n | n+1 | n+2 | n+3 | bit/ BP | 0 | a | f | e | | 1 | b | g | c | | 2 | x | x | x | | 3 | x | x | x | <p>MSB</p> <p>LSB</p> <table border="1"> <tr> <td>a</td> <td>b</td> <td>f</td> <td>g</td> <td>e</td> <td>c</td> <td>d</td> <td>DP</td> </tr> </table> | a | b | f | g | e | c | d | DP | | | | | | | | | | | | | | | | | | | | |
| | n | n+1 | n+2 | n+3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| bit/ BP | 0 | a | f | e | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 1 | b | g | c | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 2 | x | x | x | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 3 | x | x | x | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | b | f | g | e | c | d | DP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 : 3 multiplex | | | <table border="1"> <thead> <tr> <th></th> <th>n</th> <th>n+1</th> <th>n+2</th> </tr> </thead> <tbody> <tr> <td>bit/ BP</td> <td>0</td> <td>b</td> <td>a</td> </tr> <tr> <td></td> <td>1</td> <td>DP</td> <td>d</td> </tr> <tr> <td></td> <td>2</td> <td>c</td> <td>g</td> </tr> <tr> <td></td> <td>3</td> <td>x</td> <td>x</td> </tr> </tbody> </table> | | n | n+1 | n+2 | bit/ BP | 0 | b | a | | 1 | DP | d | | 2 | c | g | | 3 | x | x | <p>MSB</p> <p>LSB</p> <table border="1"> <tr> <td>b</td> <td>DP</td> <td>c</td> <td>a</td> <td>d</td> <td>g</td> <td>f</td> <td>e</td> </tr> </table> | b | DP | c | a | d | g | f | e | | | | | | | | | | | | | | | | | | | | | | | | | |
| | n | n+1 | n+2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| bit/ BP | 0 | b | a | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 1 | DP | d | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 2 | c | g | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 3 | x | x | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b | DP | c | a | d | g | f | e | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 : 4 multiplex | | | <table border="1"> <thead> <tr> <th></th> <th>n</th> <th>n+1</th> </tr> </thead> <tbody> <tr> <td>bit/ BP</td> <td>0</td> <td>a</td> </tr> <tr> <td></td> <td>1</td> <td>c</td> </tr> <tr> <td></td> <td>2</td> <td>b</td> </tr> <tr> <td></td> <td>3</td> <td>DP</td> </tr> </tbody> </table> | | n | n+1 | bit/ BP | 0 | a | | 1 | c | | 2 | b | | 3 | DP | <p>MSB</p> <p>LSB</p> <table border="1"> <tr> <td>a</td> <td>c</td> <td>b</td> <td>DP</td> <td>f</td> <td>e</td> <td>g</td> <td>d</td> </tr> </table> | a | c | b | DP | f | e | g | d | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | n | n+1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| bit/ BP | 0 | a | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 1 | c | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 2 | b | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 3 | DP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| a | c | b | DP | f | e | g | d | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

MBE534

Fig.10 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C-bus (X = data bit unchanged).

Universal LCD driver for low multiplex rates

PCF8566

6.16 Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8566 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

6.17 Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

6.18 Blinker

The display blinking capabilities of the PCF8566 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 4 Blinking frequencies

| BLINKING MODE | NORMAL OPERATING MODE RATIO | POWER-SAVING MODE RATIO | NOMINAL BLINKING FREQUENCY f_{blink} (Hz) |
|---------------|-----------------------------|-------------------------|---|
| Off | – | – | blinking off |
| 2 Hz | $f_{\text{CLK}}/92160$ | $f_{\text{CLK}}/15360$ | 2 |
| 1 Hz | $f_{\text{CLK}}/184320$ | $f_{\text{CLK}}/30720$ | 1 |
| 0.5 Hz | $f_{\text{CLK}}/368640$ | $f_{\text{CLK}}/61440$ | 0.5 |

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

Universal LCD driver for low multiplex rates

PCF8566

7 I²C-BUS DESCRIPTION

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

7.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

7.3 System configuration

A device generating a message is a 'transmitter', a device receiving a message is a 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

7.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

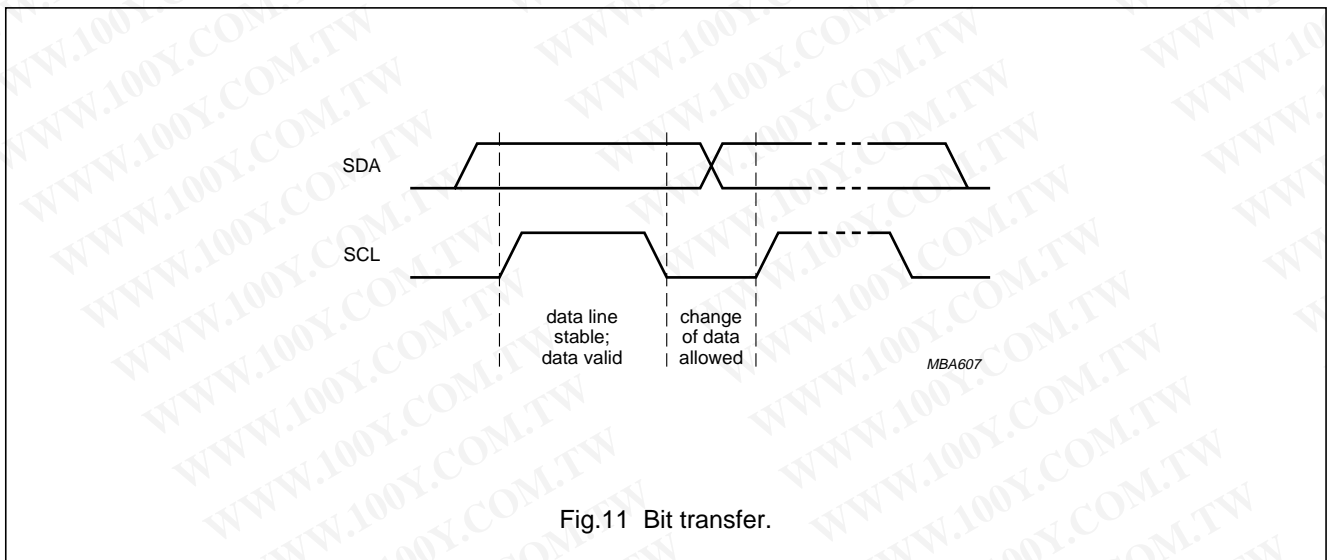


Fig.11 Bit transfer.

Universal LCD driver for low multiplex rates

PCF8566

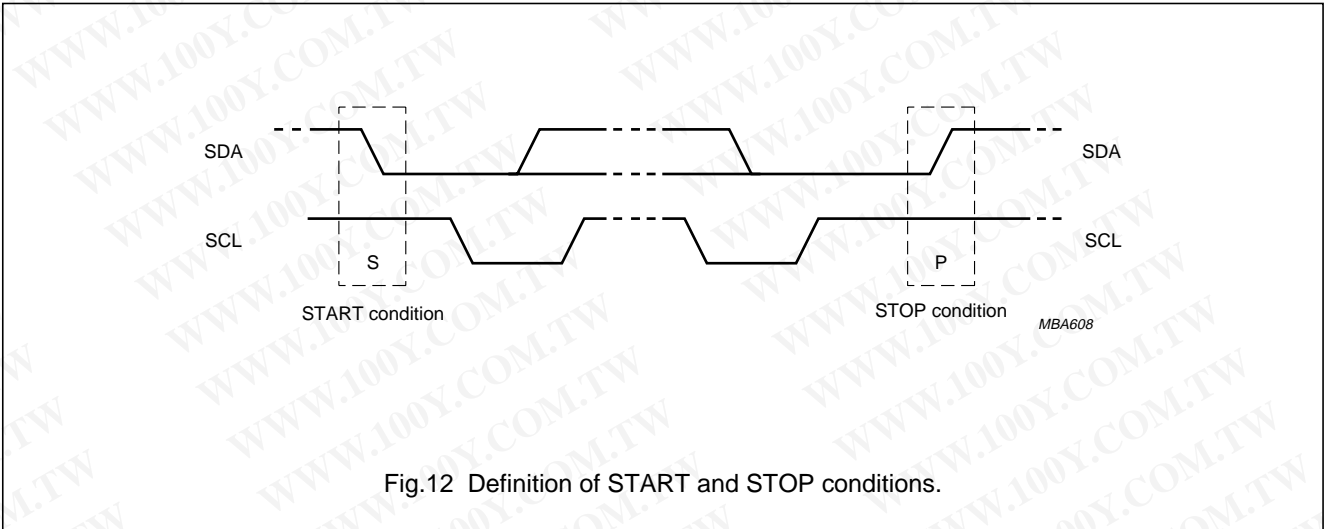


Fig.12 Definition of START and STOP conditions.

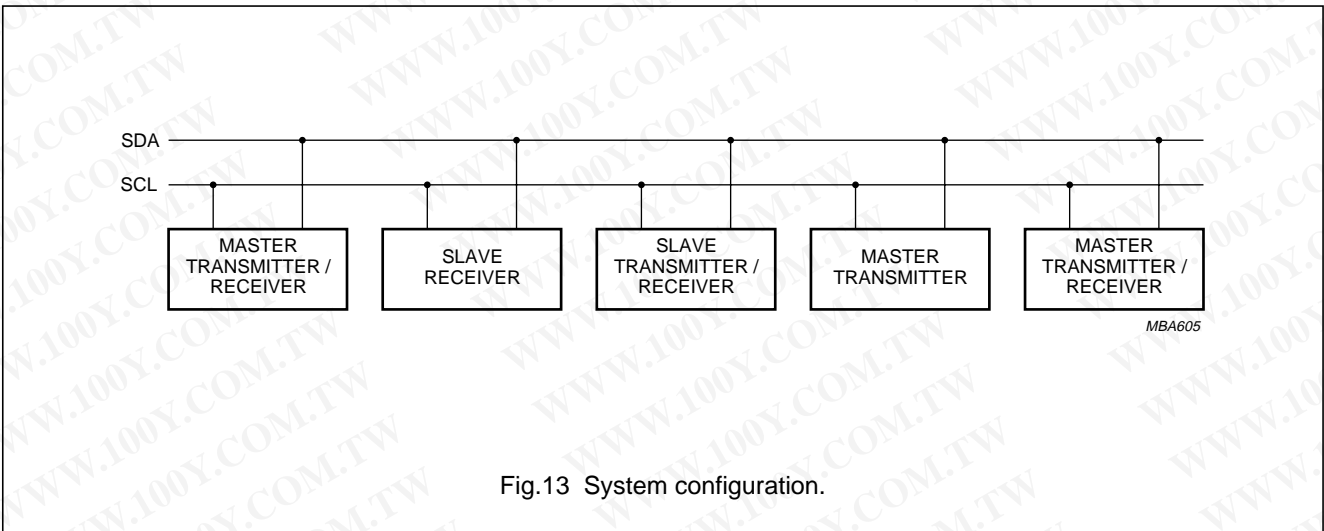


Fig.13 System configuration.

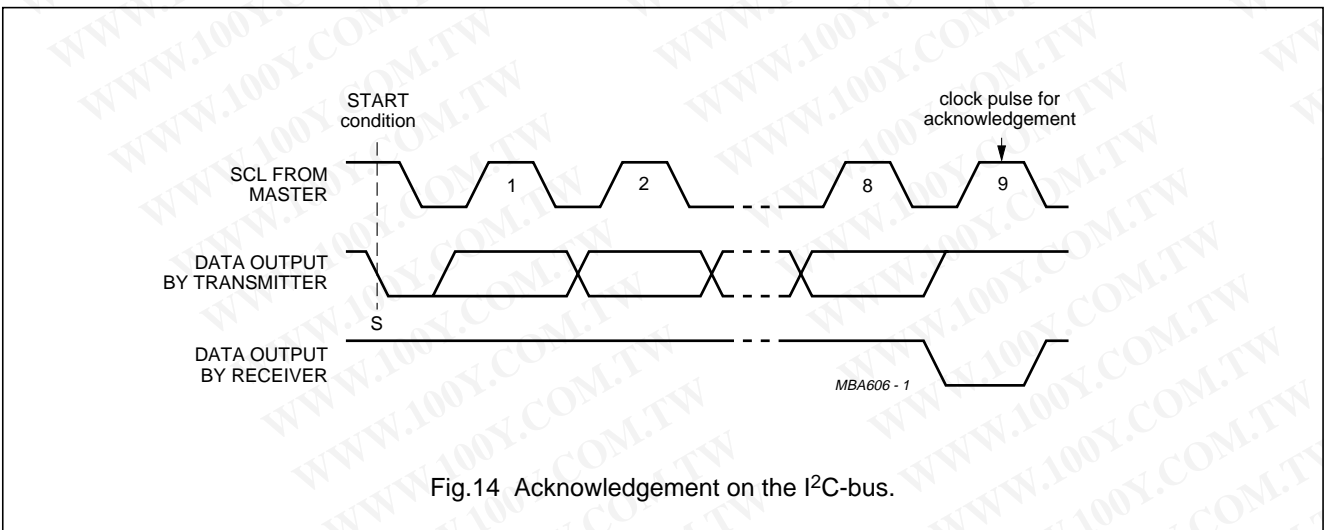


Fig.14 Acknowledgement on the I²C-bus.

Universal LCD driver for low multiplex rates

PCF8566

7.5 PCF8566 I²C-bus controller

The PCF8566 acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCF8566 are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally left open-circuit or tied to V_{SS} which defines the hardware subaddress 0.

In multiple device applications A0, A1 and A2 are left open-circuit or tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C-bus slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8566 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8566 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C-bus and serves to slow down fast transmitters. Data loss does not occur.

7.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.7 I²C-bus protocol

Two I²C-bus slave addresses (0111110 and 0111111) are reserved for PCF8566. The least-significant bit of the slave address that a PCF8566 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8566 can be distinguished on the same I²C-bus which allows:

1. Up to 16 PCF8566s on the same I²C-bus for very large LCD applications
2. The use of two types of LCD multiplex on the same I²C-bus.

The I²C-bus protocol is shown in Fig.15. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of the two PCF8566 slave addresses available. All PCF8566s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8566s with the alternative SA0 level ignore the whole I²C-bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8566s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8566s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8566 device.

The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8566. After the last display byte, the I²C-bus master issues a STOP condition (P).

7.8 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. All available commands carry a continuation bit C in their most-significant bit position (see Fig.16). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command.

If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

The five commands available to the PCF8566 are defined in Table 5.

Universal LCD driver for low multiplex rates

PCF8566

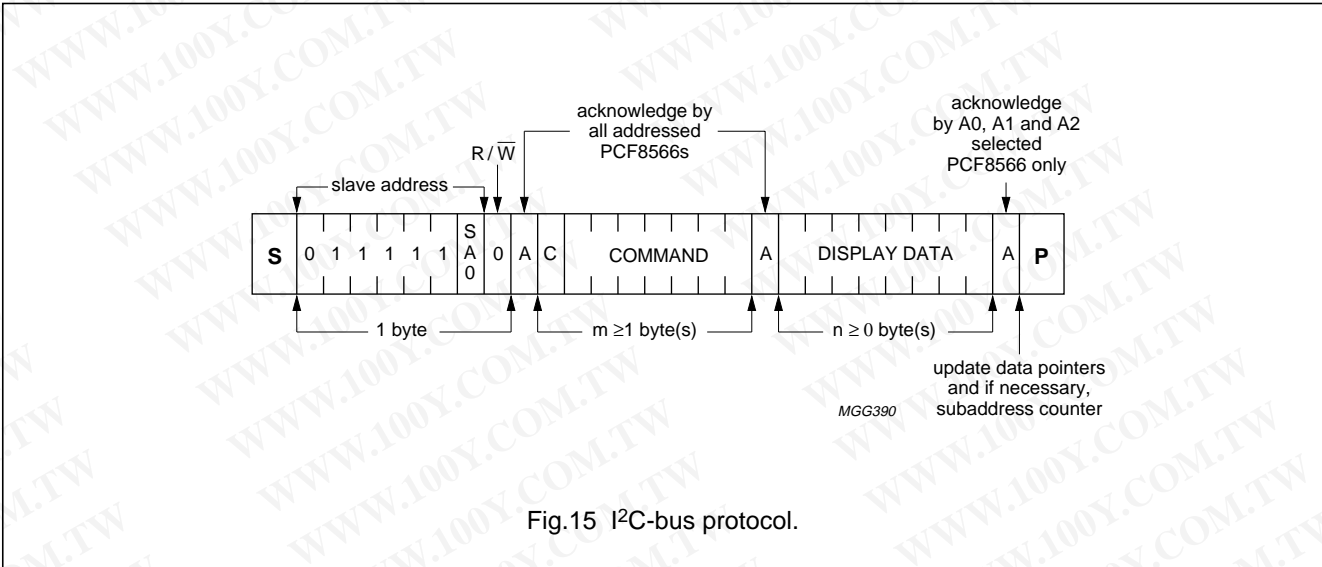


Fig.15 I²C-bus protocol.

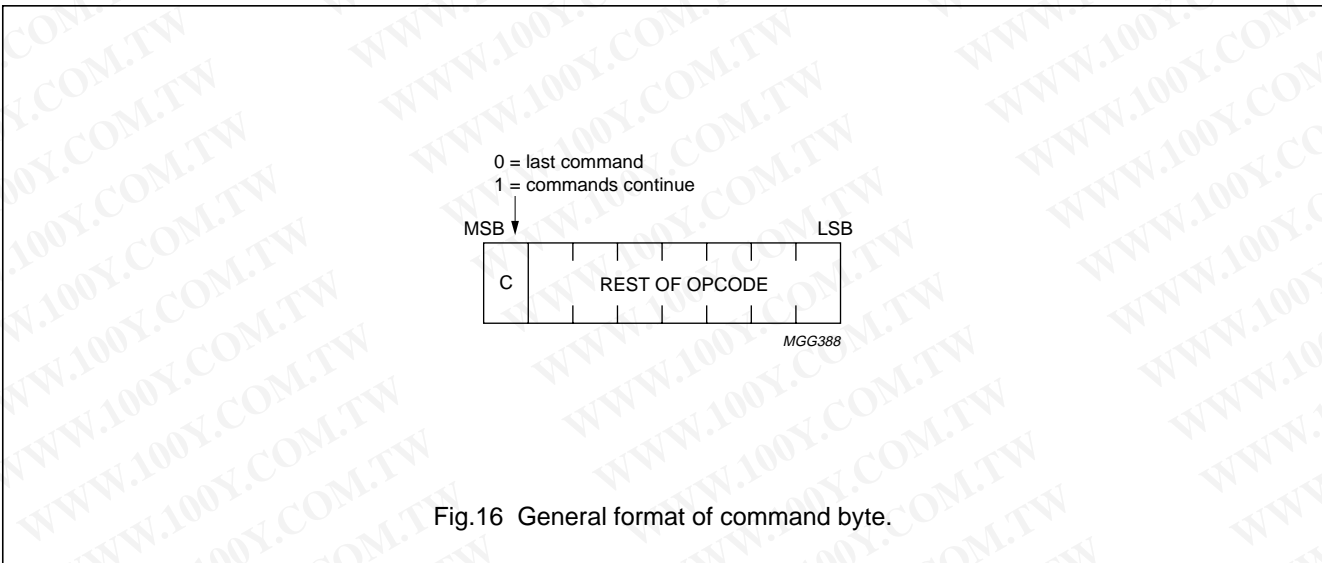


Fig.16 General format of command byte.

勝特力材料 86-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

Universal LCD driver for low multiplex rates

PCF8566

Table 5 Definition of PCF8566 commands

| COMMAND/OPCODE | | | | | | | | OPTIONS | DESCRIPTION |
|--------------------------|---|---|----|----|----|-----|-----|--------------|---|
| Mode set | | | | | | | | | |
| C | 1 | 0 | LP | E | B | M1 | M0 | see Table 6 | defines LCD drive mode |
| | | | | | | | | see Table 7 | defines LCD bias configuration |
| | | | | | | | | see Table 8 | defines display status; the possibility to disable the display allows implementation of blinking under external control |
| | | | | | | | | see Table 9 | defines power dissipation mode |
| Load data pointer | | | | | | | | | |
| C | 0 | 0 | P4 | P3 | P2 | P1 | P0 | see Table 10 | five bits of immediate data, bits P4 to P0, are transferred to the data pointer to define one of twenty-four display RAM addresses |
| Device select | | | | | | | | | |
| C | 1 | 1 | 0 | 0 | A2 | A1 | A0 | see Table 11 | three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses |
| Bank select | | | | | | | | | |
| C | 1 | 1 | 1 | 1 | 0 | I | O | see Table 12 | defines input bank selection (storage of arriving display data) |
| | | | | | | | | see Table 13 | defines output bank selection (retrieval of LCD display data) |
| | | | | | | | | | the BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes |
| Blink | | | | | | | | | |
| C | 1 | 1 | 1 | 0 | A | BF1 | BF0 | see Table 14 | defines the blinking frequency |
| | | | | | | | | see Table 15 | selects the blinking mode; normal operation with frequency set by bits BF1 and BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes |

Table 6 LCD drive mode

| LCD DRIVE MODE | BIT M1 | BIT M0 |
|------------------|--------|--------|
| Static (1 BP) | 0 | 1 |
| 1 : 2 MUX (2 BP) | 1 | 0 |
| 1 : 3 MUX (3 BP) | 1 | 1 |
| 1 : 4 MUX (4 BP) | 0 | 0 |

Universal LCD driver for low multiplex rates

PCF8566

Table 7 LCD bias configuration

| LCD BIAS | BIT B |
|--------------------|-------|
| $\frac{1}{3}$ bias | 0 |
| $\frac{1}{2}$ bias | 1 |

Table 8 Display status

| DISPLAY STATUS | BIT E |
|------------------|-------|
| Disabled (blank) | 0 |
| Enabled | 1 |

Table 9 Power dissipation mode

| MODE | BIT LP |
|-------------------|--------|
| Normal mode | 0 |
| Power-saving mode | 1 |

Table 10 Load data pointer

| BITS | P4 | P3 | P2 | P1 | P0 |
|-------------------------------|----|----|----|----|----|
| 5-bit binary value of 0 to 23 | | | | | |

Table 11 Device select

| BITS | A0 | A1 | A2 |
|------------------------------|----|----|----|
| 3-bit binary value of 0 to 7 | | | |

Table 12 Input bank selection

| STATIC | 1 : 2 MUX | BIT 1 |
|-----------|---------------|-------|
| RAM bit 0 | RAM bits 0, 1 | 0 |
| RAM bit 2 | RAM bits 2, 3 | 1 |

Table 13 Output bank selection

| STATIC | 1 : 2 MUX | BIT 0 |
|-----------|---------------|-------|
| RAM bit 0 | RAM bits 0, 1 | 0 |
| RAM bit 2 | RAM bits 2, 3 | 1 |

Table 14 Blinking frequency

| BLINK FREQUENCY | BIT BF1 | BIT BF0 |
|-----------------|---------|---------|
| Off | 0 | 0 |
| 2 Hz | 0 | 1 |
| 1 Hz | 1 | 0 |
| 0.5 Hz | 1 | 1 |

Table 15 Blink mode selection

| BLINK MODE | BIT A |
|----------------------|-------|
| Normal blinking | 0 |
| Alternation blinking | 1 |

7.9 Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8566 and coordinates their effects.

The controller is also responsible for loading display data into the display RAM as required by the filling order.

7.10 Cascaded operation

In large display configurations, up to 16 PCF8566s can be distinguished on the same I²C-bus by using the 3-bit hardware subaddress (A0, A1 and A2) and the programmable I²C-bus slave address (SA0). It is also possible to cascade up to 16 PCF8566s. When cascaded, several PCF8566s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8566s of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (Fig. 17).

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCF8566s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8566s with differing SA0 levels are cascaded). $\overline{\text{SYNC}}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8566 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times.

Should synchronization in the cascade be lost, it will be restored by the first PCF8566 to assert $\overline{\text{SYNC}}$. The timing relationships between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8576 are shown in Fig. 18. The waveforms are identical with the parent device PCF8576. Cascade ability between PCF8566s and PCF8576s is possible, giving cost effective LCD applications.

Universal LCD driver for low multiplex rates

PCF8566

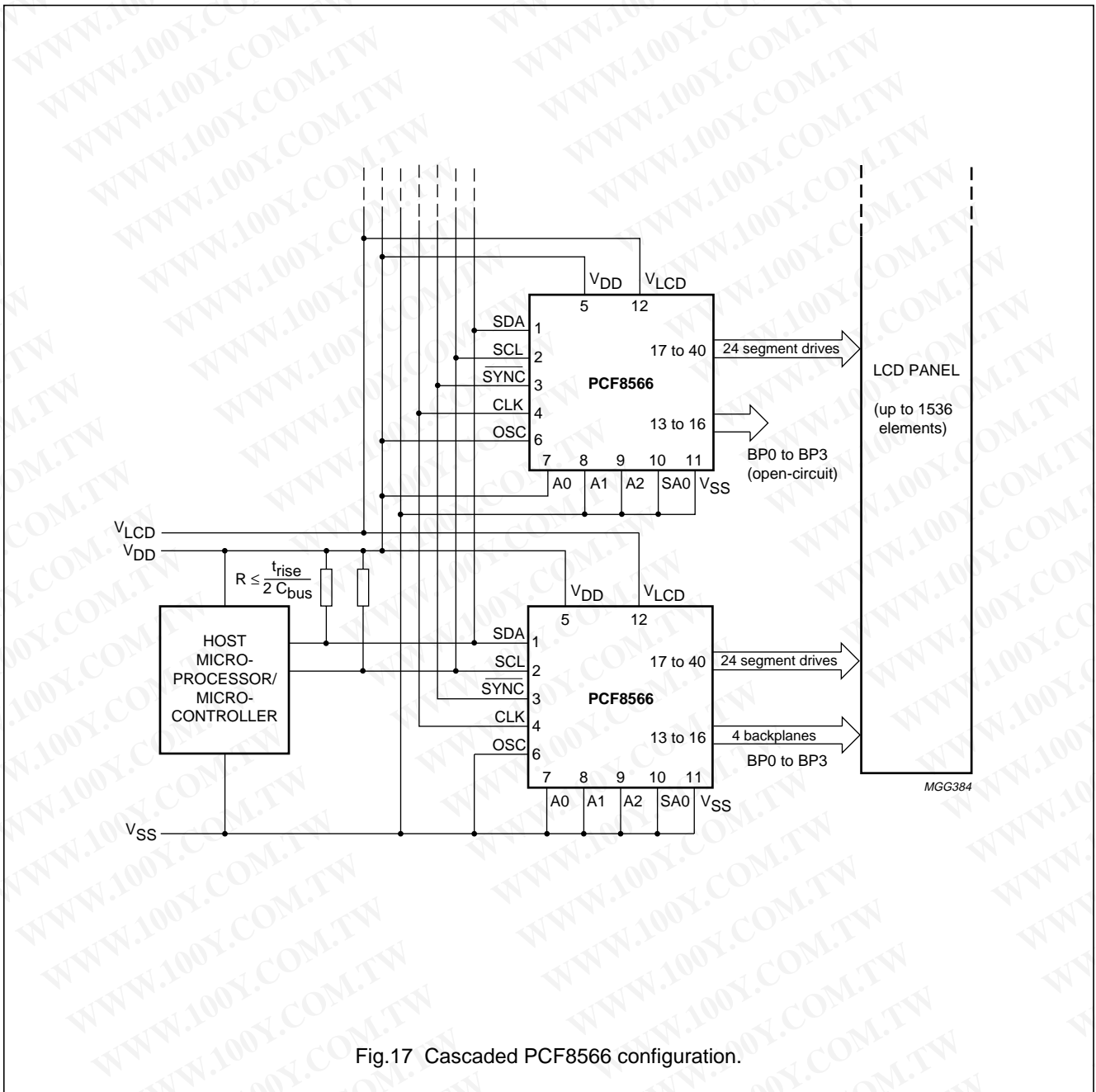
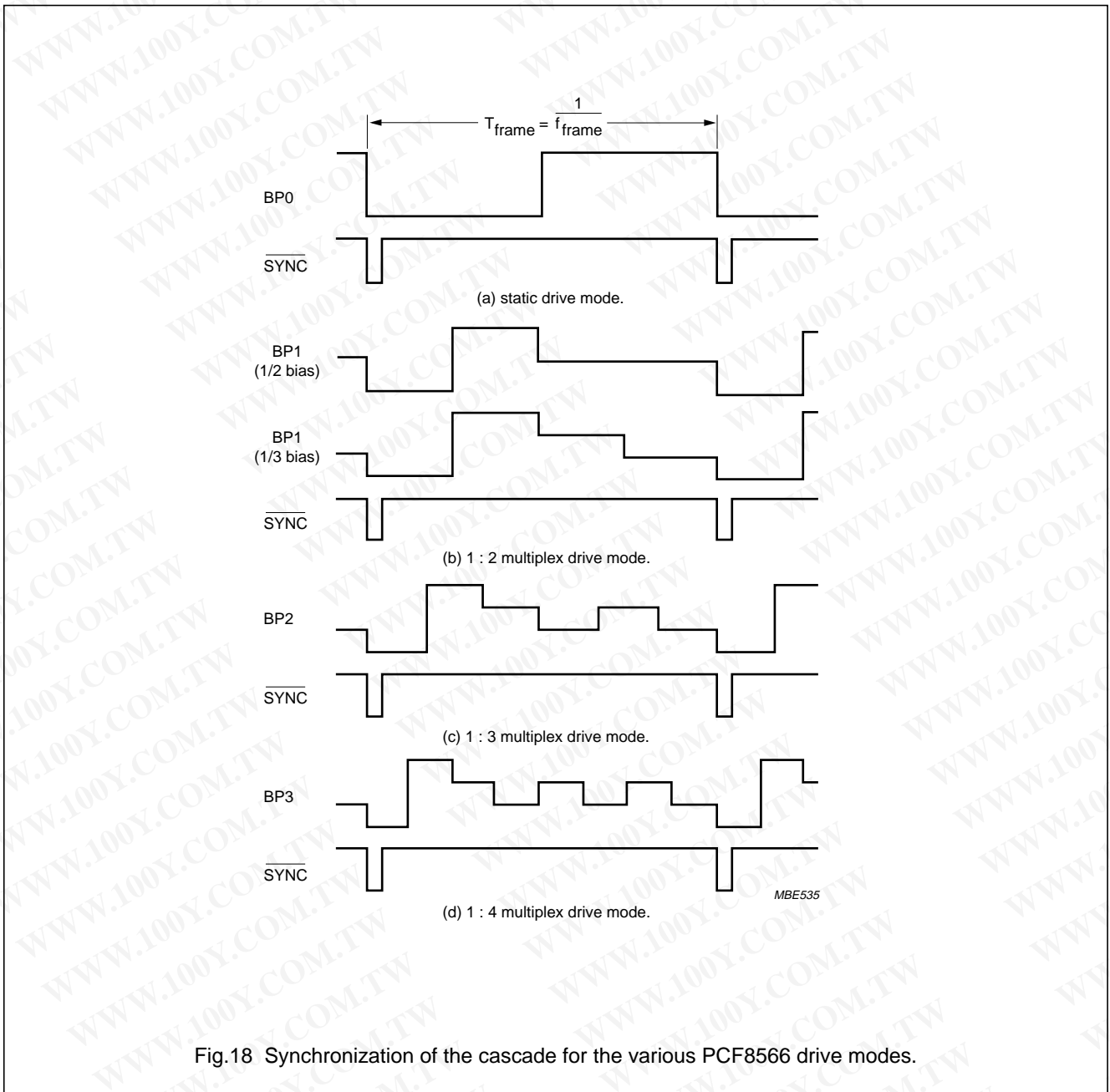


Fig.17 Cascaded PCF8566 configuration.

Universal LCD driver for low multiplex rates

PCF8566



For single plane wiring of PCF8566s, see Chapter "Application information".

Universal LCD driver for low multiplex rates

PCF8566

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|---------------------------|---|-----------------|----------------|------|
| V_{DD} | supply voltage | -0.5 | +7 | V |
| V_{LCD} | LCD supply voltage | $V_{DD} - 7$ | V_{DD} | V |
| V_I | input voltage (SCL, SDA, A0 to A2, OSC, CLK, \overline{SYNC} and SA0) | $V_{SS} - 0.5$ | $V_{DD} + 0.5$ | V |
| V_O | output voltage (S0 to S23 and BP0 to BP3) | $V_{LCD} - 0.5$ | $V_{DD} + 0.5$ | V |
| I_I | DC input current | - | ± 20 | mA |
| I_O | DC output current | - | ± 25 | mA |
| I_{DD}, I_{SS}, I_{LCD} | V_{DD}, V_{SS} or V_{LCD} current | - | ± 50 | mA |
| P_{tot} | power dissipation per package | - | 400 | mW |
| P_O | power dissipation per output | - | 100 | mW |
| T_{stg} | storage temperature | -65 | +150 | °C |

9 HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see "Handling MOS devices").

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

Universal LCD driver for low multiplex rates

PCF8566

10 DC CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $V_{DD} = 2.5\text{ to }6\text{ V}$; $V_{LCD} = V_{DD} - 2.5\text{ to }V_{DD} - 6\text{ V}$; $T_{amb} = -40\text{ to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--------------------|--|--|-----------------|----------|----------------|------------------|
| Supplies | | | | | | |
| V_{DD} | operating supply voltage | | 2.5 | – | 6 | V |
| V_{LCD} | LCD supply voltage | | $V_{DD} - 6$ | – | $V_{DD} - 2.5$ | V |
| I_{DD} | operating supply current (normal mode) | $f_{CLK} = 200\text{ kHz}$; note 1 | – | 30 | 90 | μA |
| I_{LP} | power saving mode supply current | $V_{DD} = 3.5\text{ V}$; $V_{LCD} = 0\text{ V}$; $f_{CLK} = 35\text{ kHz}$; A0, A1 and A2 tied to V_{SS} ; note 1 | – | 15 | 40 | μA |
| Logic | | | | | | |
| V_{IL} | LOW level input voltage | | V_{SS} | – | $0.3V_{DD}$ | V |
| V_{IH} | HIGH level input voltage | | $0.7V_{DD}$ | – | V_{DD} | V |
| V_{OL} | LOW level output voltage | $I_O = 0\text{ mA}$ | – | – | 0.05 | V |
| V_{OH} | HIGH level output voltage | $I_O = 0\text{ mA}$ | $V_{DD} - 0.05$ | – | – | V |
| I_{OL1} | LOW level output current (CLK and SYNC) | $V_{OL} = 1\text{ V}$; $V_{DD} = 5\text{ V}$ | 1 | – | – | mA |
| I_{OH} | HIGH level output current (CLK) | $V_{OH} = 4\text{ V}$; $V_{DD} = 5\text{ V}$ | – | – | –1 | mA |
| I_{OL2} | LOW level output current (SDA and SCL) | $V_{OL} = 0.4\text{ V}$; $V_{DD} = 5\text{ V}$ | 3 | – | – | mA |
| I_{LI} | leakage current (SA0, CLK, OSC, A0, A1, A2, SCL and SDA) | $V_I = V_{SS}\text{ or }V_{DD}$ | – | – | ± 1 | μA |
| I_{pd} | pull-down current (A0, A1, A2 and OSC) | $V_I = 1\text{ V}$; $V_{DD} = 5\text{ V}$ | 15 | 50 | 150 | μA |
| R_{puSYNC} | pull-up resistor (SYNC) | | 15 | 25 | 60 | $\text{k}\Omega$ |
| V_{ref} | power-on reset level | note 2 | – | 1.3 | 2 | V |
| t_{sw} | tolerable spike width on bus | | – | – | 100 | ns |
| C_i | input capacitance | note 3 | – | – | 7 | pF |
| LCD outputs | | | | | | |
| V_{BP} | DC voltage component (BP0 to BP3) | $C_{BP} = 35\text{ nF}$ | – | ± 20 | – | mV |
| V_S | DC voltage component (S0 to S23) | $C_S = 5\text{ nF}$ | – | ± 20 | – | mV |
| Z_{BP} | output impedance (BP0 to BP3) | $V_{LCD} = V_{DD} - 5\text{ V}$; note 4 | – | 1 | 5 | $\text{k}\Omega$ |
| Z_S | output impedance (S0 to S23) | $V_{LCD} = V_{DD} - 5\text{ V}$; note 4 | – | 3 | 7 | $\text{k}\Omega$ |

Notes

1. Outputs open; inputs at V_{SS} or V_{DD} ; external clock with 50% duty factor; I²C-bus inactive.
2. Resets all logic when $V_{DD} < V_{ref}$.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.

Universal LCD driver for low multiplex rates

PCF8566

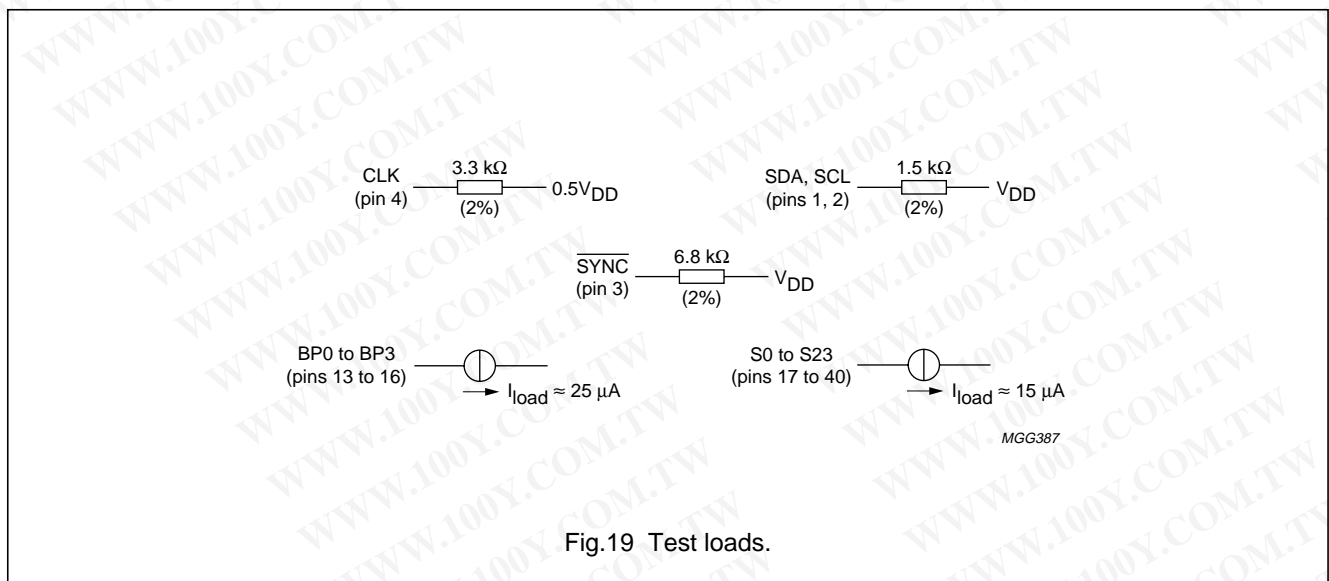
11 AC CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $V_{DD} = 2.5\text{ to }6\text{ V}$; $V_{LCD} = V_{DD} - 2.5\text{ to }V_{DD} - 6\text{ V}$; $T_{amb} = -40\text{ to }+85\text{ }^\circ\text{C}$; unless otherwise specified; note 1.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---------------------------|--|---------------------------------|------|------|------|---------------|
| f_{CLK} | oscillator frequency (normal mode) | $V_{DD} = 5\text{ V}$; note 2 | 125 | 200 | 315 | kHz |
| f_{CLKLP} | oscillator frequency (power saving mode) | $V_{DD} = 3.5\text{ V}$ | 21 | 31 | 48 | kHz |
| t_{CLKH} | CLK HIGH time | | 1 | – | – | μs |
| t_{CLKL} | CLK LOW time | | 1 | – | – | μs |
| t_{PSYNC} | $\overline{\text{SYNC}}$ propagation delay | | – | – | 400 | ns |
| t_{SYNCL} | $\overline{\text{SYNC}}$ LOW time | | 1 | – | – | μs |
| t_{PLCD} | driver delays with test loads | $V_{LCD} = V_{DD} - 5\text{ V}$ | – | – | 30 | μs |
| I²C-bus | | | | | | |
| t_{BUF} | bus free time | | 4.7 | – | – | μs |
| $t_{HD; STA}$ | START condition hold time | | 4 | – | – | μs |
| t_{LOW} | SCL LOW time | | 4.7 | – | – | μs |
| t_{HIGH} | SCL HIGH time | | 4 | – | – | μs |
| $t_{SU; STA}$ | START condition set-up time (repeated start code only) | | 4.7 | – | – | μs |
| $t_{HD; DAT}$ | data hold time | | 0 | – | – | μs |
| $t_{SU; DAT}$ | data set-up time | | 250 | – | – | ns |
| t_r | rise time | | – | – | 1 | μs |
| t_f | fall time | | – | – | 300 | ns |
| $t_{SU; STO}$ | STOP condition set-up time | | 4.7 | – | – | μs |

Notes

- All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD} .
- At $f_{CLK} < 125\text{ kHz}$, I²C-bus maximum transmission speed is derated.



Universal LCD driver for low multiplex rates

PCF8566

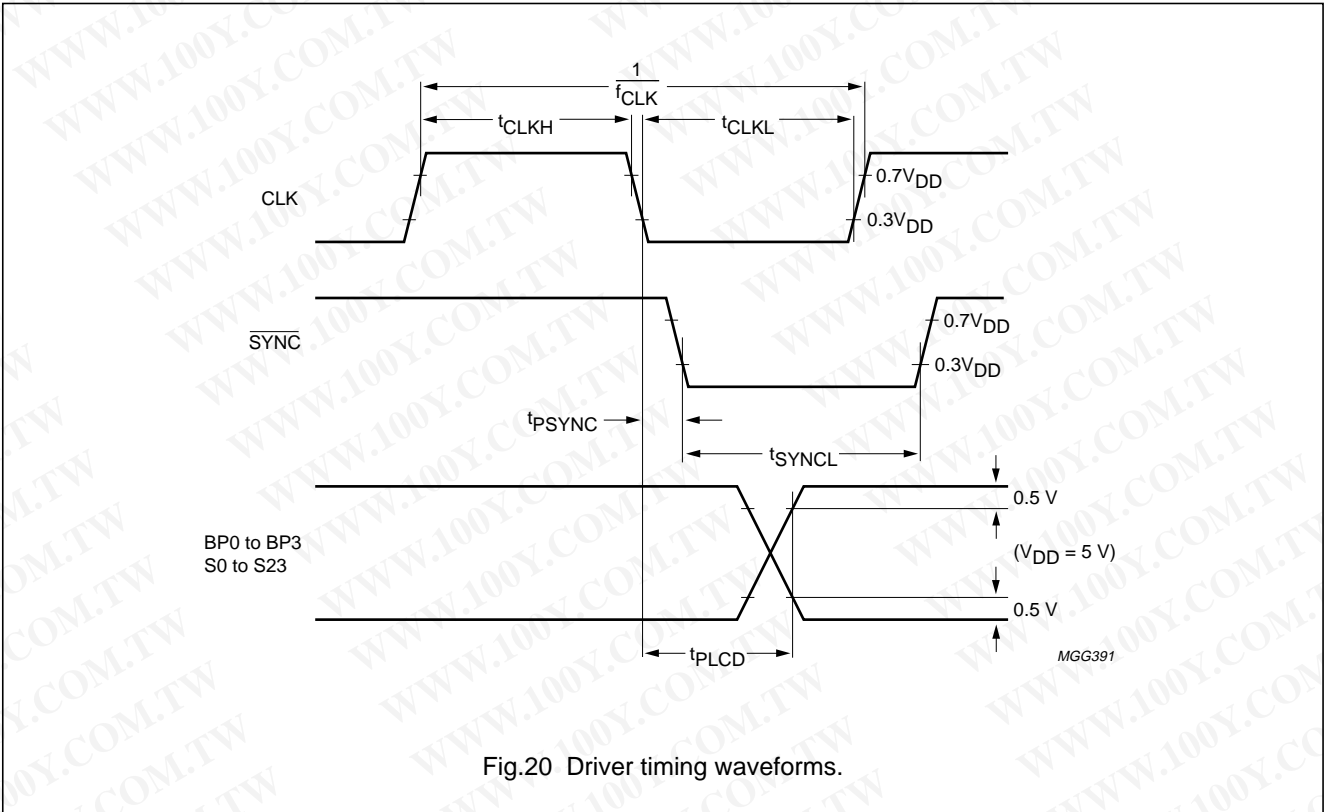


Fig.20 Driver timing waveforms.

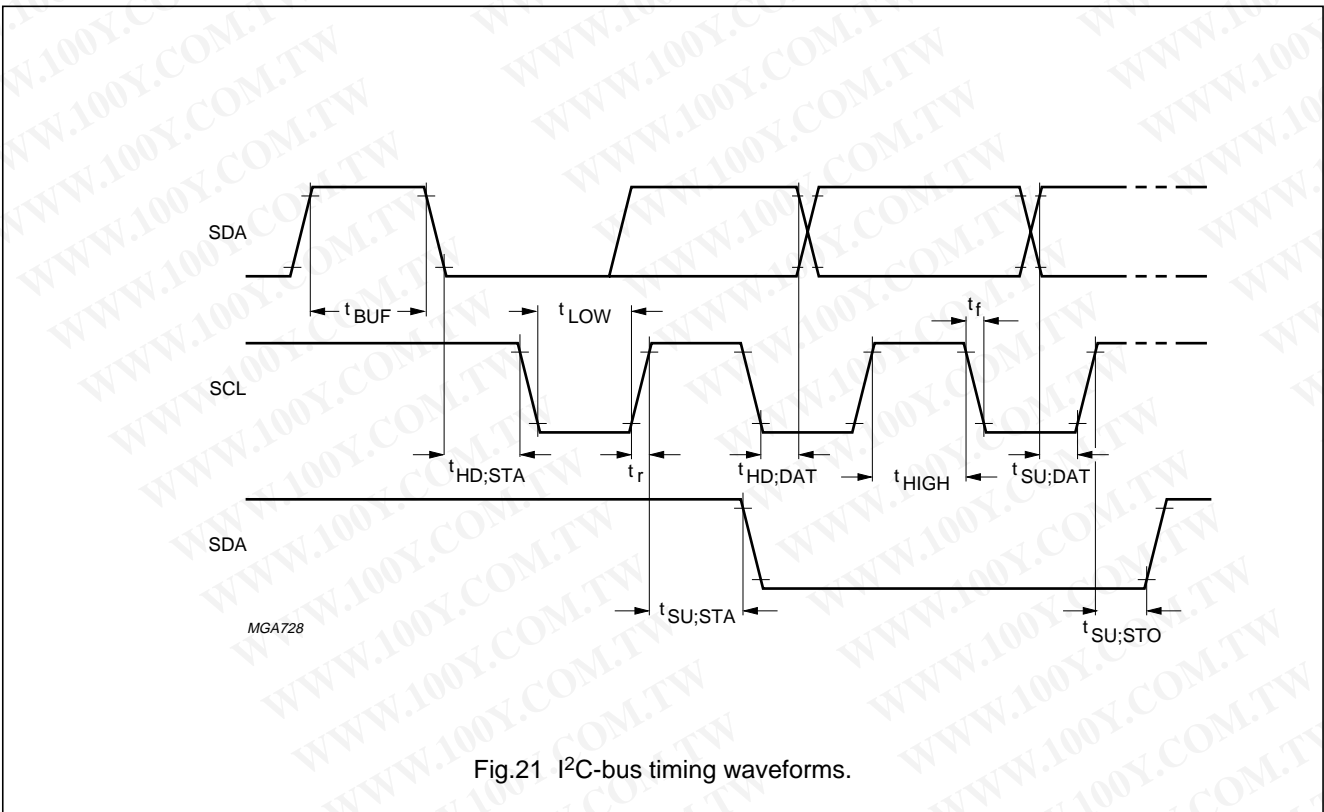
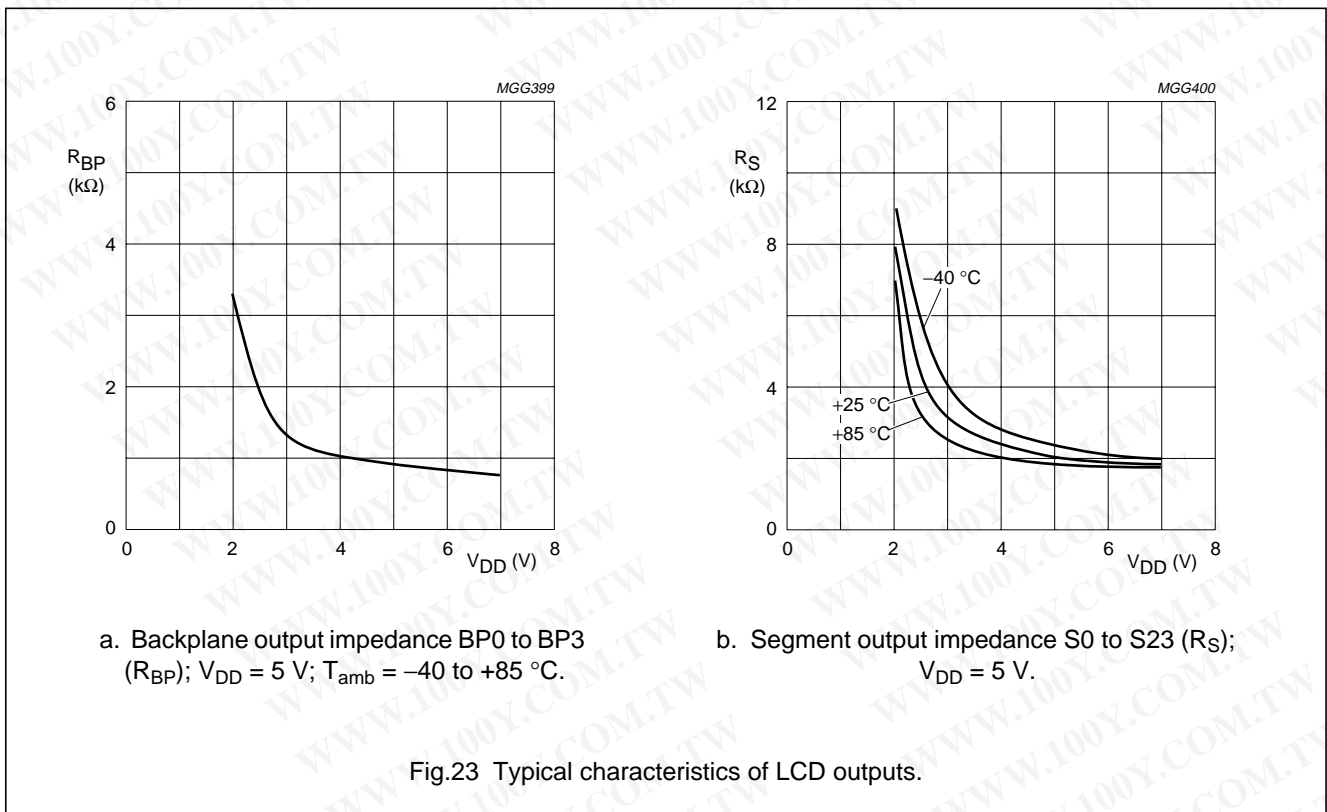
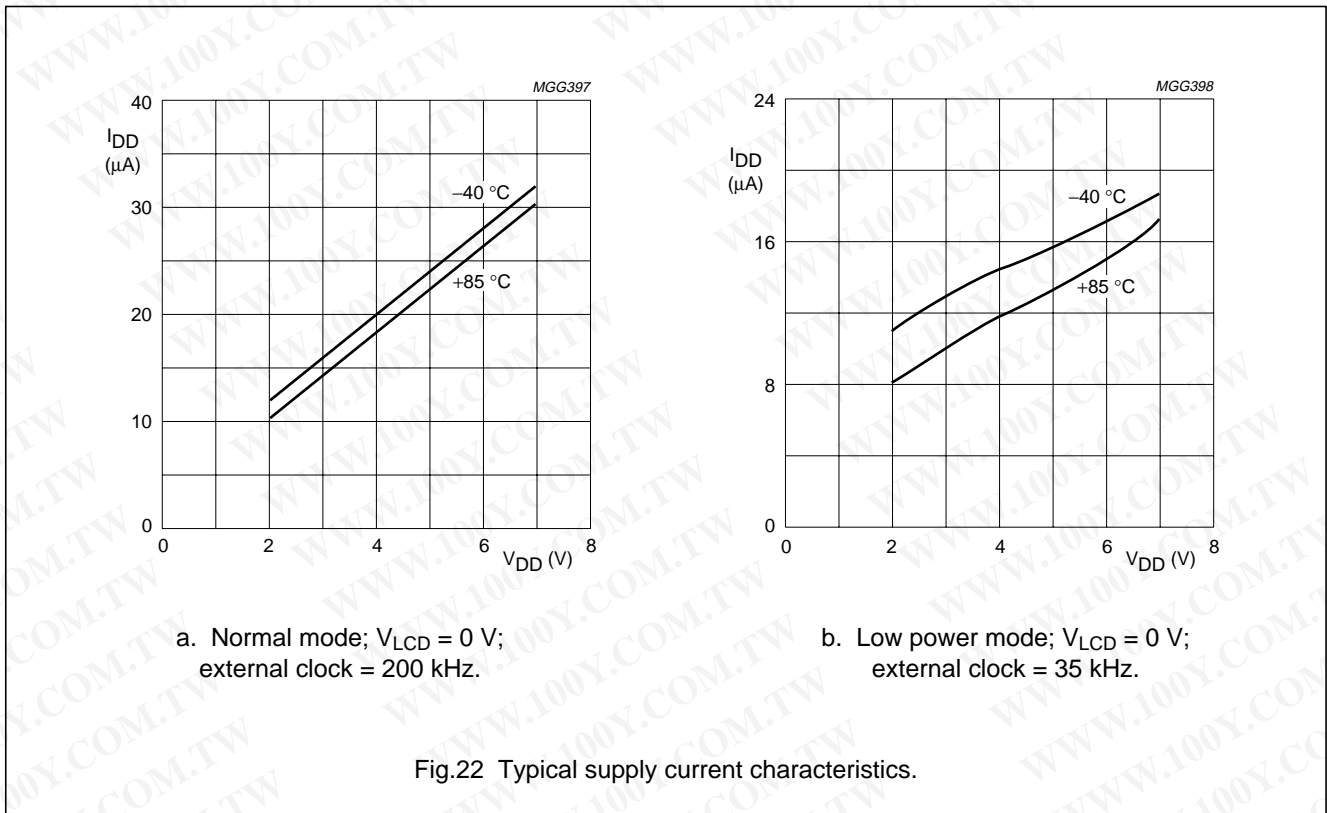


Fig.21 I²C-bus timing waveforms.

Universal LCD driver for low multiplex rates

PCF8566



Universal LCD driver for low multiplex rates

PCF8566

12 APPLICATION INFORMATION

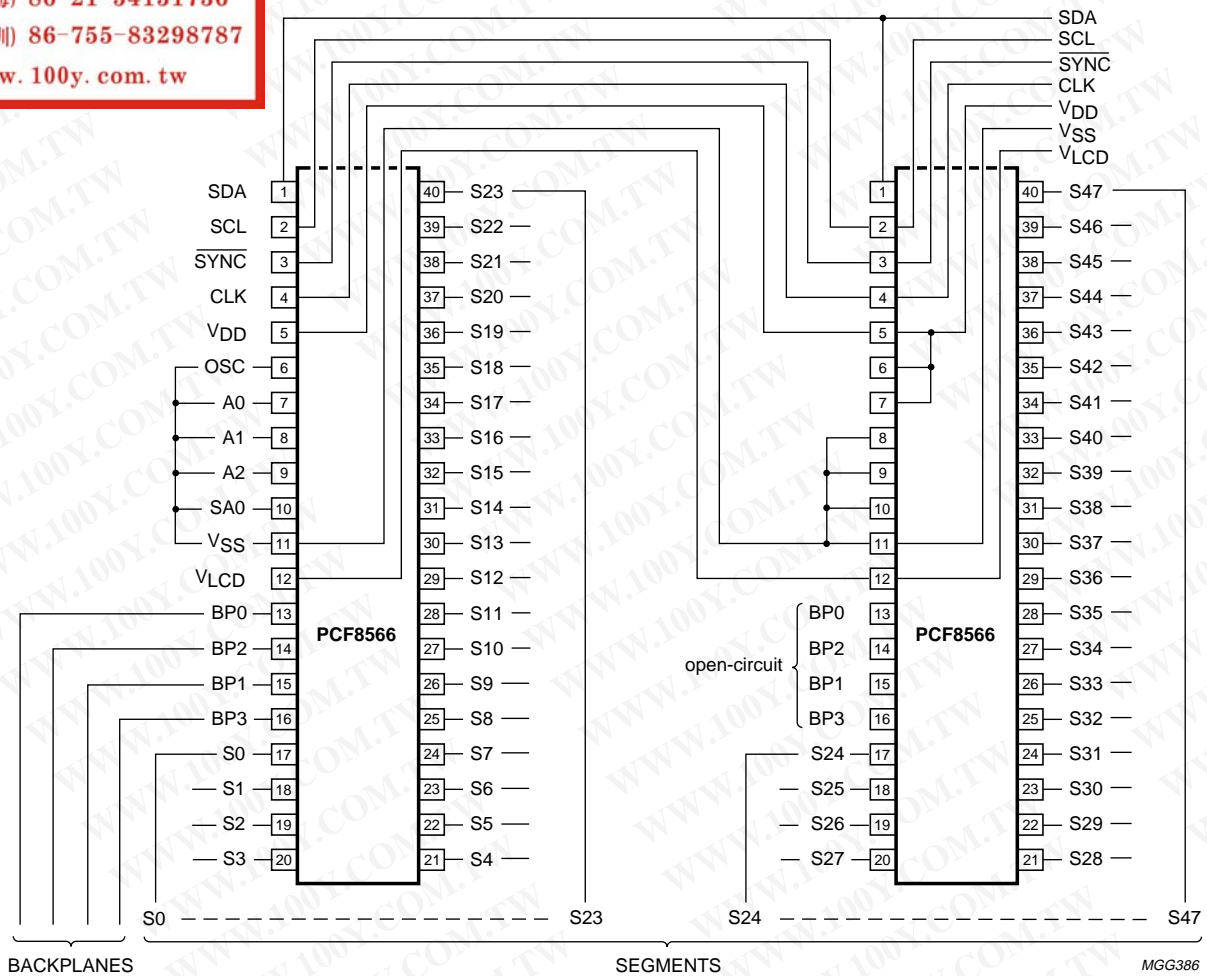


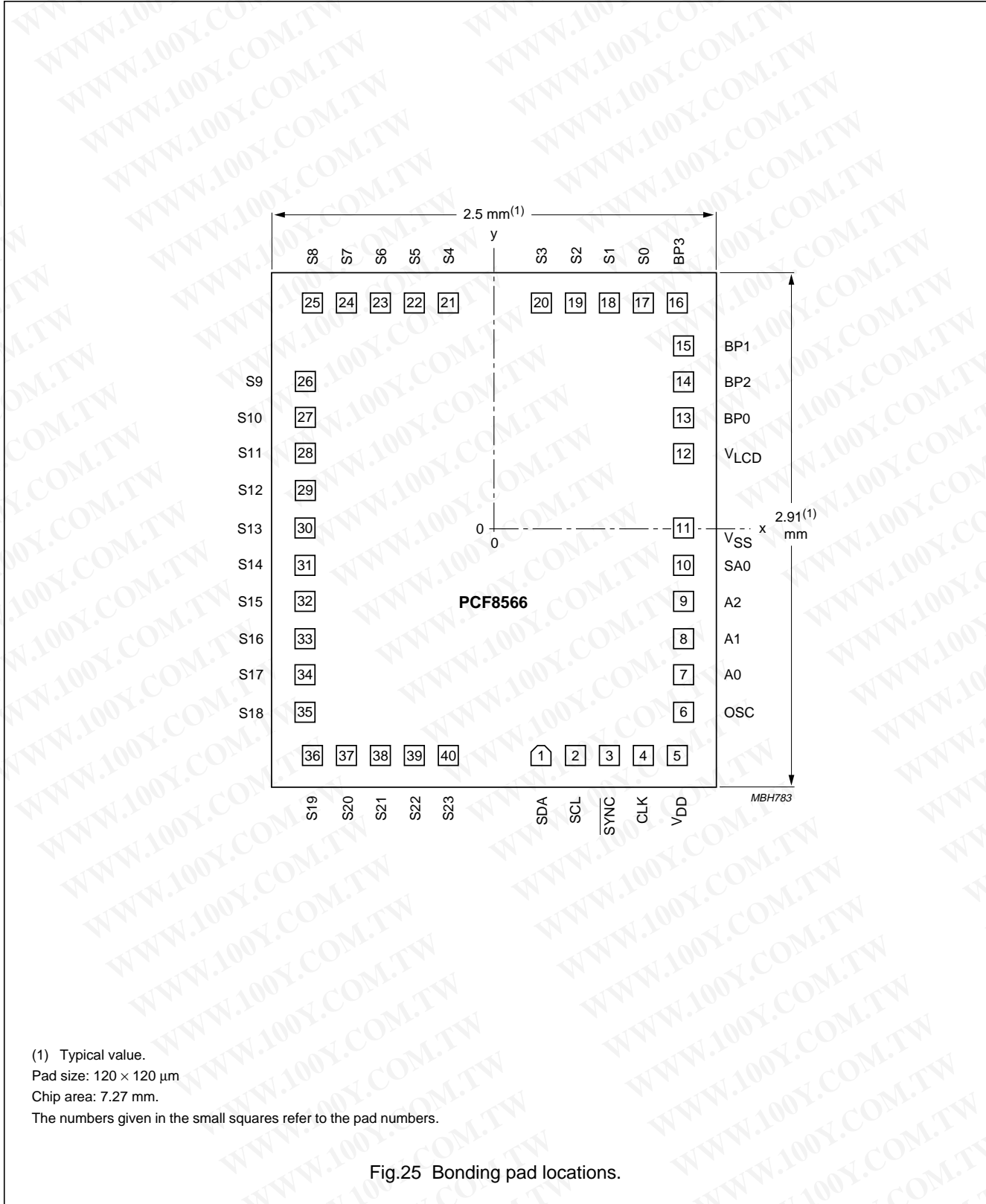
Fig.24 Single plane wiring of package PCF8566s.

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

Universal LCD driver for low multiplex rates

PCF8566

13 CHIP DIMENSIONS AND BONDING PAD LOCATIONS



(1) Typical value.
 Pad size: 120 × 120 μm
 Chip area: 7.27 mm.
 The numbers given in the small squares refer to the pad numbers.

Fig.25 Bonding pad locations.

Universal LCD driver for low multiplex rates

PCF8566

Table 16 Bonding pad locations (dimensions in mm)

All x/y coordinates are referenced to centre of chip, (see Fig.25).

| PAD NUMBER | SYMBOL | x | y | PIN |
|------------|------------------|-------|-------|-----|
| 1 | SDA | 200 | -1235 | 1 |
| 2 | SCL | 400 | -1235 | 2 |
| 3 | SYNC | 605 | -1235 | 3 |
| 4 | CLK | 856 | -1235 | 4 |
| 5 | V _{DD} | 1062 | -1235 | 5 |
| 6 | OSC | 1080 | -1025 | 6 |
| 7 | A0 | 1080 | -825 | 7 |
| 8 | A1 | 1080 | -625 | 8 |
| 9 | A2 | 1080 | -425 | 9 |
| 10 | SA0 | 1080 | -225 | 10 |
| 11 | V _{SS} | 1080 | -25 | 11 |
| 12 | V _{LCD} | 1080 | 347 | 12 |
| 13 | BP0 | 1080 | 547 | 13 |
| 14 | BP2 | 1080 | 747 | 14 |
| 15 | BP1 | 1080 | 947 | 15 |
| 16 | BP3 | 1074 | 1235 | 16 |
| 17 | S0 | 874 | 1235 | 17 |
| 18 | S1 | 674 | 1235 | 18 |
| 19 | S2 | 474 | 1235 | 19 |
| 20 | S3 | 274 | 1235 | 20 |
| 21 | S4 | -274 | 1235 | 21 |
| 22 | S5 | -474 | 1235 | 22 |
| 23 | S6 | -674 | 1235 | 23 |
| 24 | S7 | -874 | 1235 | 24 |
| 25 | S8 | -1074 | 1235 | 25 |
| 26 | S9 | -1080 | 765 | 26 |
| 27 | S10 | -1080 | 565 | 27 |
| 28 | S11 | -1080 | 365 | 28 |
| 29 | S12 | -1080 | 165 | 29 |
| 30 | S13 | -1080 | -35 | 30 |
| 31 | S14 | -1080 | -235 | 31 |
| 32 | S15 | -1080 | -435 | 32 |
| 33 | S16 | -1080 | -635 | 33 |
| 34 | S17 | -1080 | -835 | 34 |
| 35 | S18 | -1080 | -1035 | 35 |
| 36 | S19 | -1056 | -1235 | 36 |
| 37 | S20 | -830 | -1235 | 37 |
| 38 | S21 | -630 | -1235 | 38 |
| 39 | S22 | -430 | -1235 | 39 |
| 40 | S23 | -230 | -1235 | 40 |

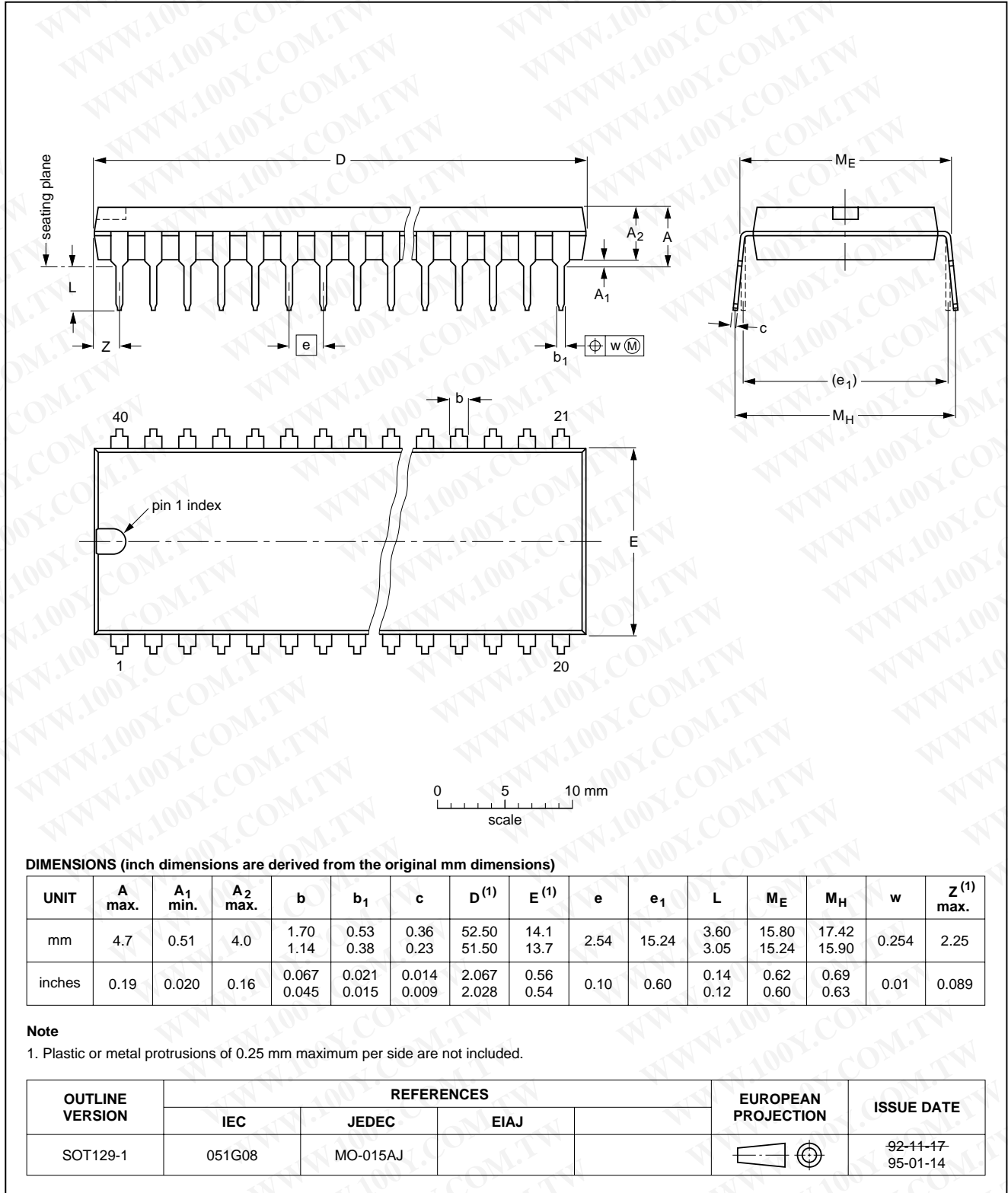
Universal LCD driver for low multiplex rates

PCF8566

14 PACKAGE OUTLINES

DIP40: plastic dual in-line package; 40 leads (600 mil)

SOT129-1

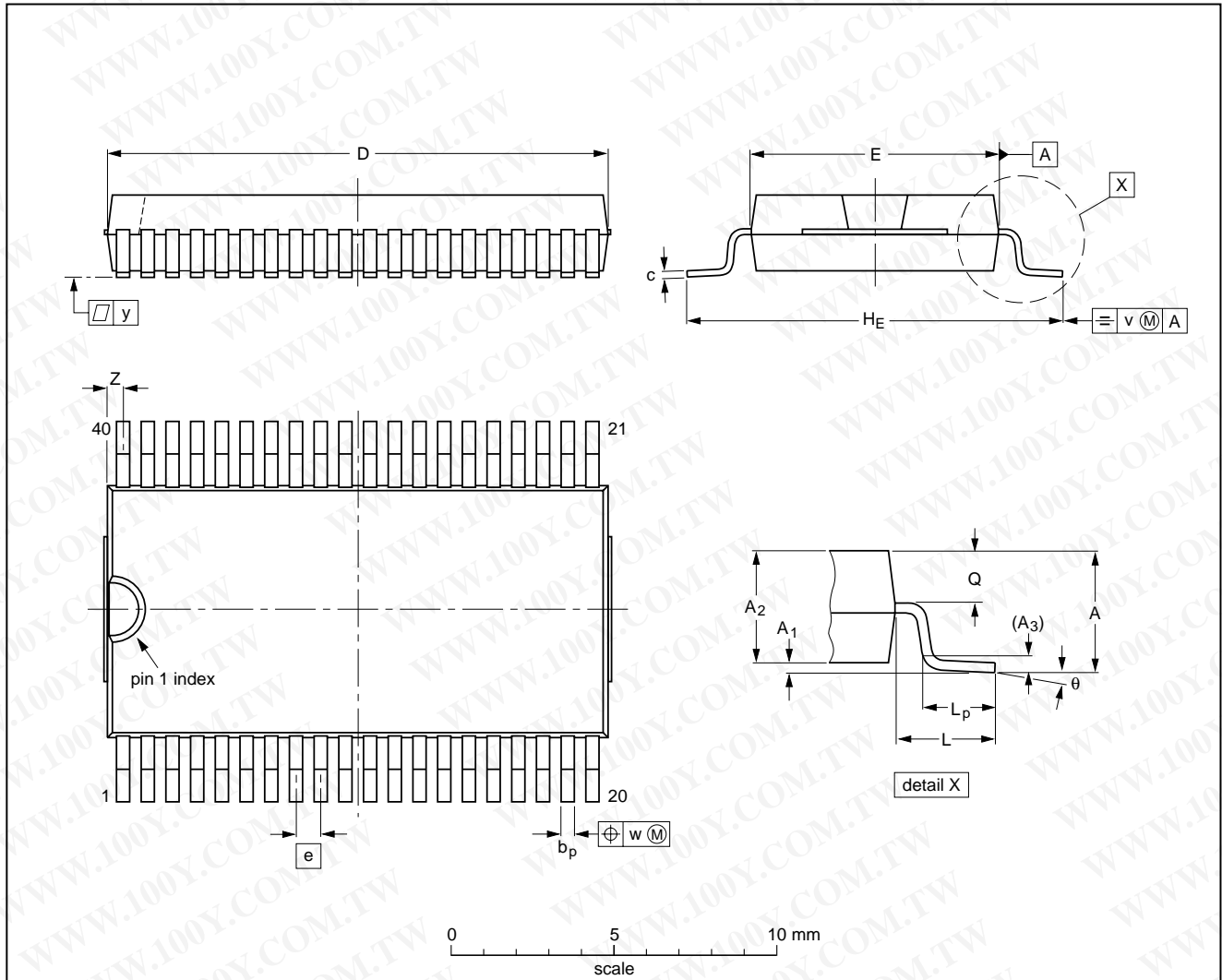


Universal LCD driver for low multiplex rates

PCF8566

VSO40: plastic very small outline package; 40 leads

SOT158-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|--------|--------|----------------|----------------|----------------|----------------|------------------|------------------|------------------|-------|----------------|-------|----------------|----------------|-------|-------|-------|------------------|----------|
| mm | 2.70 | 0.3 0.1 | 2.45 2.25 | 0.25 | 0.42 0.30 | 0.22 0.14 | 15.6 15.2 | 7.6 7.5 | 0.762 | 12.3 11.8 | 2.25 | 1.7 1.5 | 1.15 1.05 | 0.2 | 0.1 | 0.1 | 0.6 0.3 | 7° 0° |
| inches | 0.11 | 0.012 0.004 | 0.096 0.089 | 0.010 | 0.017 0.012 | 0.0087 0.0055 | 0.61 0.60 | 0.30 0.29 | 0.03 | 0.48 0.46 | 0.089 | 0.067 0.059 | 0.045 0.041 | 0.008 | 0.004 | 0.004 | 0.024 0.012 | |

Notes

1. Plastic or metal protrusions of 0.4 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|------|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | |
| SOT158-1 | | | | | 92-11-17 95-01-24 |

Universal LCD driver for low multiplex rates

PCF8566

15 SOLDERING

15.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "Data Handbook IC26; Integrated Circuit Packages" (order code 9398 652 90011).

15.2 DIP

15.2.1 SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

15.2.2 REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

15.3 SO and VSO

15.3.1 REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO and VSO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

15.3.2 WAVE SOLDERING

Wave soldering techniques can be used for all SO and VSO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.3.3 REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

Universal LCD driver for low multiplex rates

PCF8566

16 DEFINITIONS

| Data sheet status | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

17 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

18 PURCHASE OF PHILIPS I²C COMPONENTS



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

Universal LCD driver for low multiplex
rates

PCF8566

NOTES

Universal LCD driver for low multiplex
rates

PCF8566

NOTES

Universal LCD driver for low multiplex
rates

PCF8566

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax. +381 11 635 777

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: <http://www.semiconductors.philips.com>

© Philips Electronics N.V. 1998

SCA59

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

415106/1200/06/pp40

Date of release: 1998 May 04

Document order number: 9397 750 03725

勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-54151736
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

Philips
Semiconductors



PHILIPS

Let's make things better.