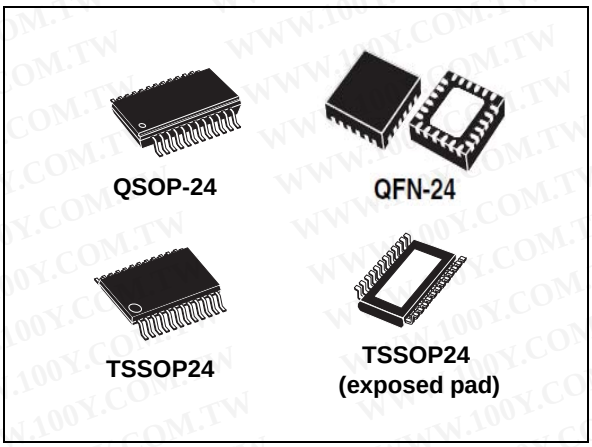
LED1642GW

16 channels LED driver with error detection current gain control and 12/16-bit PWM brightness control

Datasheet - preliminary data



Features

- 16 constant current output channels
- Output current: from 3 mA to 40 mA
- Current programmable through external resistor
- 7-bit global current gain adjustment in two ranges
- 12/16-bit PWM grayscale brightness control
- Programmable output turn-on/off time
- Error detection mode (both open and shorted-LED)
- Programmable shorted-LED detection thresholds
- Auto power saving/auto-wakeup
- Selectable SDO synchronization on the CLK falling edge
- Gradual output delay (selectable)
- Supply voltage: 3 V to 5.5 V
- Thermal shutdown and overtemperature alert
- 30 MHz 4-wires interface
- 20 V current generator rated voltage

Applications

- Full color/monochrome large displays
- LED signage

Description

The LED1642GW is a monolithic, low voltage, low current power 16-bit shift register designed for LED panel displays. The LED1642GW guarantees 20 V output driving capability allowing the user to connect several LEDs in series. In the output stage, sixteen regulated current sources provide from 3 mA to 40 mA constant current to drive the LEDs. The current is programmed through an external resistor and can be adjusted by 7-bit current gain register in two subranges.The brightness can be adjusted separately for each channel through a 12/16-bit grayscale control.

A programmable turn-on and turn-off time (four different values are available) improves the system low noise generation performances.

In the LED1642GW is available the open/short error detection mode. The auto power shutdown and auto power-on feature (this feature is selectable) allow the device to save power without any external intervention.

Thermal management is equipped with overtemperature data alert and the output thermal shutdown (170 °C). The high clock frequency is up to 30 MHz and it makes the device suitable for high data rate transmission. A selectable gradual output delay reduces the inrush current whereas the selectable SDO synchronization feature works when the device is used in daisy chain configuration. The supply voltage range is between 3 V and 5.5 V.

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Figure 1. TSSOP24, TSSOP24EP, QSOP-24 pinout

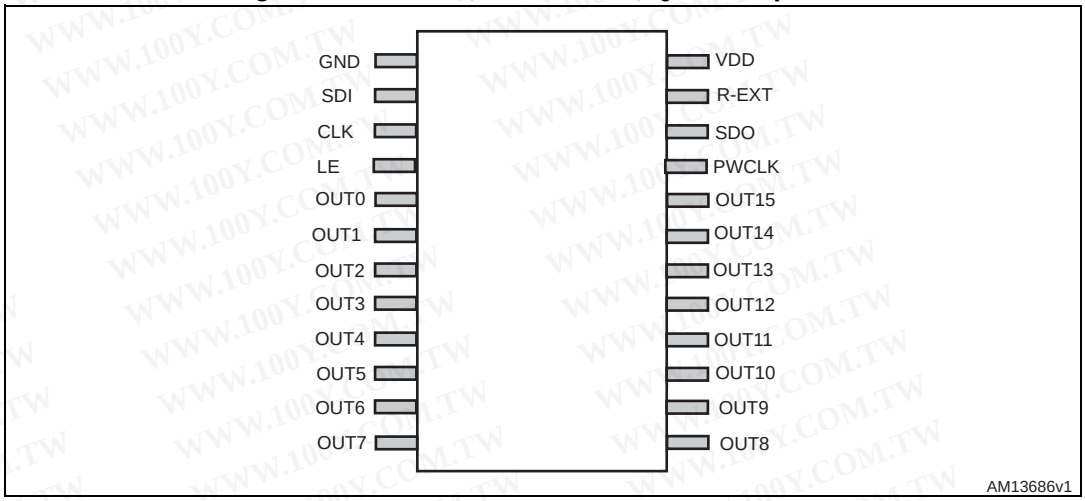


Figure 2. QFN-24 pinout

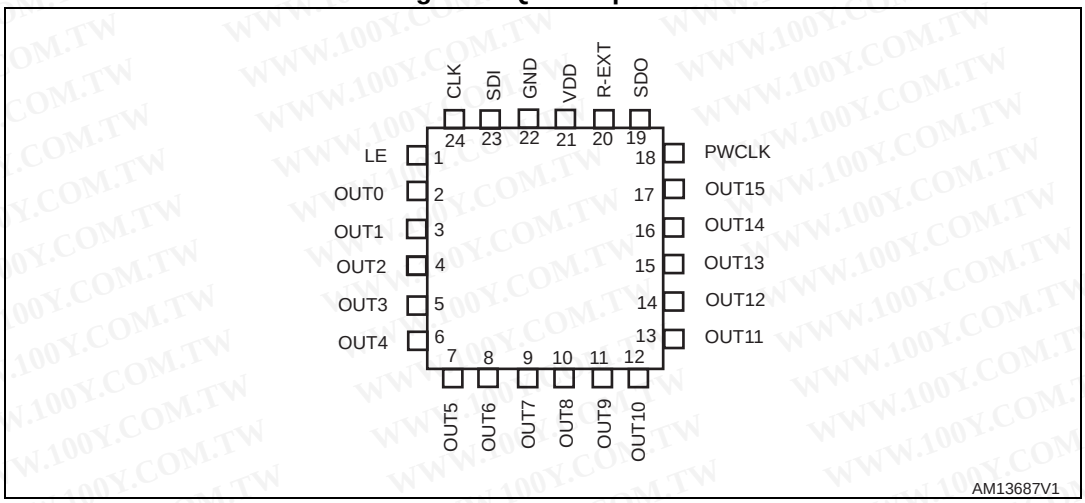


Table 1. Pin description

TSSOP24 TSSOP24EP QSOP-24	QFN-24	Symbol	Name and function
1	22	GND	Ground terminal
2	23	SDI	Serial data input terminal
3	24	CLK	Clock input terminal
4	1	LE	Latch input terminal
5-20	2-17	OUT0-OUT15	Output terminals
21	18	PWCLK	Clock input for PWM counter

Table 1. Pin description (continued)

TSSOP24 TSSOP24EP QSOP-24	QFN-24	Symbol	Name and function
22	19	SDO	Serial data output terminal
23	20	R-EXT	Terminal for external resistor for constant current programming
24	21	VDD	Supply voltage terminal

2 Absolute maximum ratings

Stressing the device above the ratings listed in the *Table 2* may cause the device permanent damage. Operating under conditions above those indicated in the operating section is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	0 to 7	V
V_{OUT}	Output voltage	-0.5 to 20	V
I_{OUT}	Output current	50	mA
V_i	Input voltage	-0.4 to V_{DD} +0.4	V
I_{GND}	GND terminal current	1400	mA
ESD	Electrostatic discharge protection HBM human body model	±2	kV

3 Thermal characteristics

Table 3. Thermal characteristics

Symbol	Parameter		Value	Unit
T_a	Operative free-air temperature range(1)		-40 to +85	°C
T_{OPR}	Operative junction temperature range		-40 to +125	
T_{STG}	Storage ambient temperature range		-55 to +150	
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	QFN-24	30	°C/W
		TSSOP24	85	
		TSSOP24EP(2)	37.5	
		QSOP-24	72	

1. This data must be considered in adequate power dissipation conditions, the junction temperature must be maintained below 125 °C.
2. The exposed pad should be soldered directly to the PCB to get the thermal benefits.

4 Electrical characteristics

V_{DD} = 3.3 V, T_j = 25 °C, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		3		5.5	V
V_{OUT}	Output voltage	Out 0 - out 15	-	-	19	
V_{IH}	Input voltage		0.7 x V_{DD}	-	V_{DD}	
V_{IL}			GND	-	0.3 x V_{DD}	
V_{OL}	Serial data output voltage (SDO)	V_{DD}= 3 to 5.5 V I = +/- 1 mA	-	-	0.4	
V_{OH}			V_{DD} -0.4	-	-	
I_{Oleak}	Output leakage current	V_{OUT} = 19 V, all outputs OFF	-	-	0.5	µA
V_{uvlo}	UVLO threshold (rising)			2.7	2.9	V
	UVLO threshold (falling)		2.2	2.3		
Hy_{uvlo}	UVLO hysteresis			400		mV

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
ΔI_{OL1}	Output current precision channel-to-channel (all outputs ON)(1)(2)	V_{OUT} = 0.1 V; (I_{OUT} = 3 mA) R_{EXT} = 11 kΩ CFG-0…CFG-5= “000000” CFG-6 = “0”	-	-	±4	%
ΔI_{OL2}		V_{OUT} = 0.5 V; (I_{OUT} = 20 mA) R_{EXT} = 11 kΩ CFG-0…CFG-5 = “011010” CFG-6 = “1”	-	-	±3	
ΔI_{OL3}		V_{OUT} = 0.8 V; (I_{OUT} = 36 mA) R_{EXT} = 11 kΩ CFG-0…CFG-5 = “111111” CFG-6 = “1”	-	-	±3	
ΔI_{OL2a}	Output current precision device-to-device (all outputs ON)(1)	V_{OUT} = 0.5 V; (I_{OUT} = 20 mA) R_{EXT}=1 1 kΩ CFG-0…CFG-5 = “011010” CFG-6 = “1”	-	-	±6	%
$\%/dV_{OUT}$	Output current vs. output voltage regulation (3)	V_{OUT} from 1 V to 3 V; (I_{OUT} = 36 mA) R_{EXT} = 11 kΩ CFG-0…CFG-5 = “111111” CFG-6 = “1”	-	±0.1	-	%/V
$\%/dV_{DD}$	Output current vs. supply voltage regulation(4)	V_{DD} from 3 V to 5.5 V V_{OUT} = 0.8 V; (I_{OUT} = 36 mA) R_{EXT} = 11 kΩ CFG-0…CFG-5 = “111111” CFG-6 = “1”	-	±1	-	
Rup	Pull-up resistor for PWCLK pin		400	500	600	KΩ
Rdw	Pull-down resistor for LE pin		400	500	600	
R_{EXT}	External current setup resistance				100	
I_{DD}(OFF1)	Supply current (OFF)	R_{EXT} = 11 kΩ OUT 0 to 15 = OFF CFG = default	-	-	6	mA
I_{DD}(ON1)	Supply current (ON)	R_{EXT} = 11 kΩ; I_{OUT} = 20 mA OUT 0 to 15 = ON CFG-0…CFG-5 = “011010” CFG-6 = “1”	-		8	
I_{DD}(ON2)		R_{EXT} = 11 kΩ; I_{OUT} = 36 mA OUT 0 to 15 = ON CFG-0…CFG-5 = “111111” CFG-6 = “1”	-		10	

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{DD} (auto OFF)	Supply current (auto OFF)	R_{EXT}= 11 kΩ; OUT 0 to 15 = OFF CFG-0…CFG-5 = “111111” CFG-6 = “1”	-	200	500	µA
T_{flg}	Thermal flag			150		°C
T_{sd}	Thermal shutdown			170		
T_{sd-hy}	Thermal shutdown hysteresis			15	20	

1. Tested with just one output loaded.
2. ((Ioutn - Ioutavg1-15)/ Ioutavg1-15) x 100.
3. $$\Delta(\%/V) = \frac{(Ioutn @ Voutn = 3.0V) - (Ioutn @ Voutn = 1.0V)}{(Ioutn @ Voutn = 1.0V)} \times \frac{100}{3-1}$$
4. $$\Delta(\%/V) = \frac{(Ioutn @ Vdd = 5.5V) - (Ioutn @ Vdd = 3.0V)}{(Ioutn @ Vdd = 3.0V)} \times \frac{100}{5.5-3}$$

Figure 3. Typical chip-to-chip accuracy

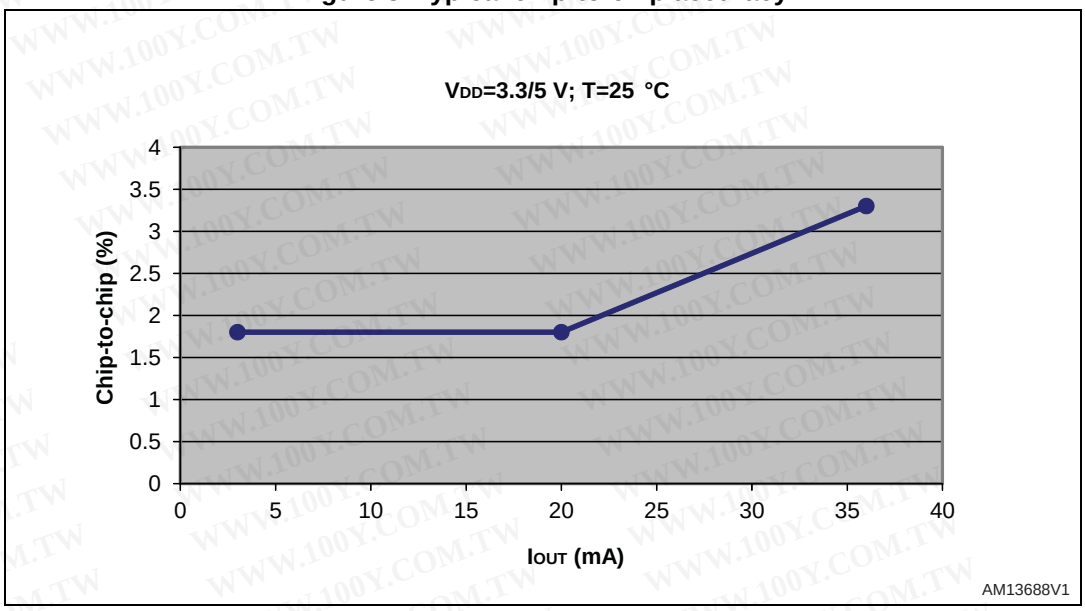
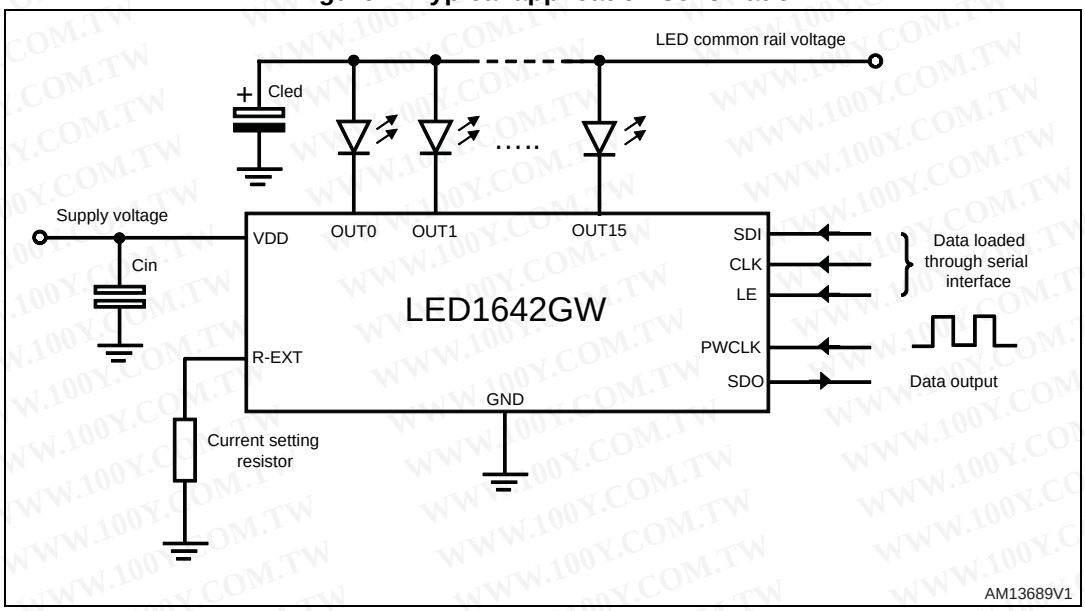


Figure 4. Typical application schematic



5 Switching characteristics

V_{DD} = 3.3 V, T_j = 25 °C, unless otherwise specified.

Table 5. Switching characteristics

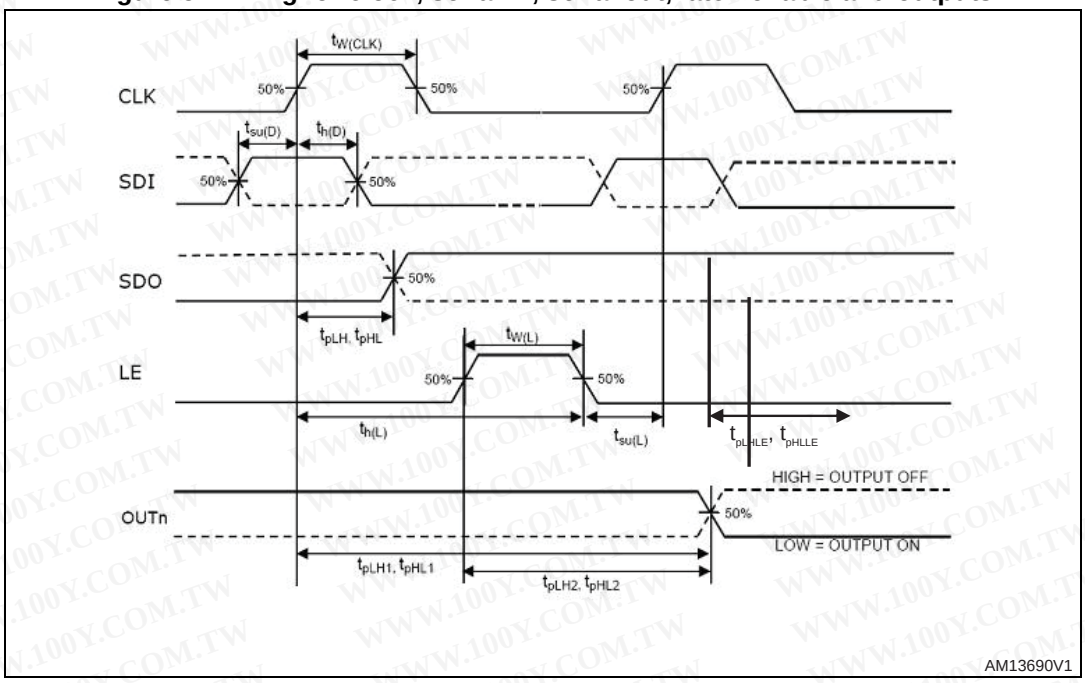
Symbol	Parameter		Conditions	Min.	Typ.	Max.	Unit
f_{clk}	Clock frequency		Cascade operation	-	-	30	MHz
f_{pwclk}	PWclock frequency			-	-	30	
$tr_{(SDO)}$	SDO rise time		R_{EXT}= 11 kΩ; I_{OUT} = 20 mA V_{OUT} = 0.8 V VIH = V_{DD}; VIL = GND RL = 3.3 KΩ; CL = 10 pF CFG-0…CFG-5 = “011010” CFG-6 = “1”	-	5	-	ns
$tf_{(SDO)}$	SDO fall time			-	5	-	
tPLHLE	LE - OUTn(1)	Propagation delay time (“L to “H”)	R_{EXT} = 11 kΩ; I_{OUT} = 20 mA V_{OUT} = 0.8 V VIH = V_{DD}; VIL = GND RL = 50 Ω; CL = 10 pF CFG-0…CFG-5 = “011010” CFG-6 = “1”	-	200	-	
tPLH	CLK - SDO CFG-13 = ‘0’			8	15	25	
tPHLLE	LE - OUTn(1)	Propagation delay time (“H” to “L”)		-	100	-	
tPHL	CLK - SDO CFG-13 = ‘0’			8	15	25	
tw(CLK)	CLK	Pulse width		20	-	-	
t_W(PWCLK)	PWCLK			20	-	-	
tw(L)	LE			20	-	-	
t_{gr-d}	Gradual delay ch-to-ch				10		
$t_{su(L)}$	Setup time for LE			5	-	-	
$t_{h(L)}$	Hold time for LE			5	-	-	
$t_{su(D)}$	Setup time for SDI			5	-	-	
$t_{h(D)}$	Hold time for SDI			10	-	-	
tclkr(2)	Maximum CLK rise time			-	-	5	µs
tclkf(2)	Maximum CLK fall time			-	-	5	
I_{out-ov}	Output current turn-on overshoot		V_{OUT} = 0.6 to 3 V CL = 10 pF; I_{OUT} = 3 to 36 mA	-	-	10	%
t_{n-err}	Normal error detection minimum output ON time			-	-	1	µs
$t_{shutdown}$	Auto power shutdown time (auto OFF)		From LE falling edge to R_{EXT} voltage reference at -10%	-	100	-	ns
t_{wakeup}	Auto-wakeup		From LE falling edge to R_{EXT} voltage reference at 90%	-	3	-	µs

1. CFG -11= 0 and CFG -12 = 0 (output tr = 30 ns; output tf = 20 ns); CFG-14=1 (no output gradual delay).
2. If devices are connected in cascade and tclkr or tclkf is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

Table 6. Programmable T_{ON}/T_{OFF} (output rise and fall time)

Configuration bits (CFG-12 - CFG-11)	Conditions	Typ. (20% to 80%)		Unit
		Turn-on	Turn-off	
0 - 0	R_{EXT} = 11 kΩ; I_{OUT} = 20 mA V_{OUT} = 0.8 V VIH= V_{DD}; VIL= GND RL = 50 Ω; CL=10pF CFG-0...CFG-5="011010" CFG-6 = "1"	30 ns	20 ns	ns
0 - 1		100 ns	40 ns	
1 - 0		140 ns	80 ns	
1 - 1		180 ns	150 ns	

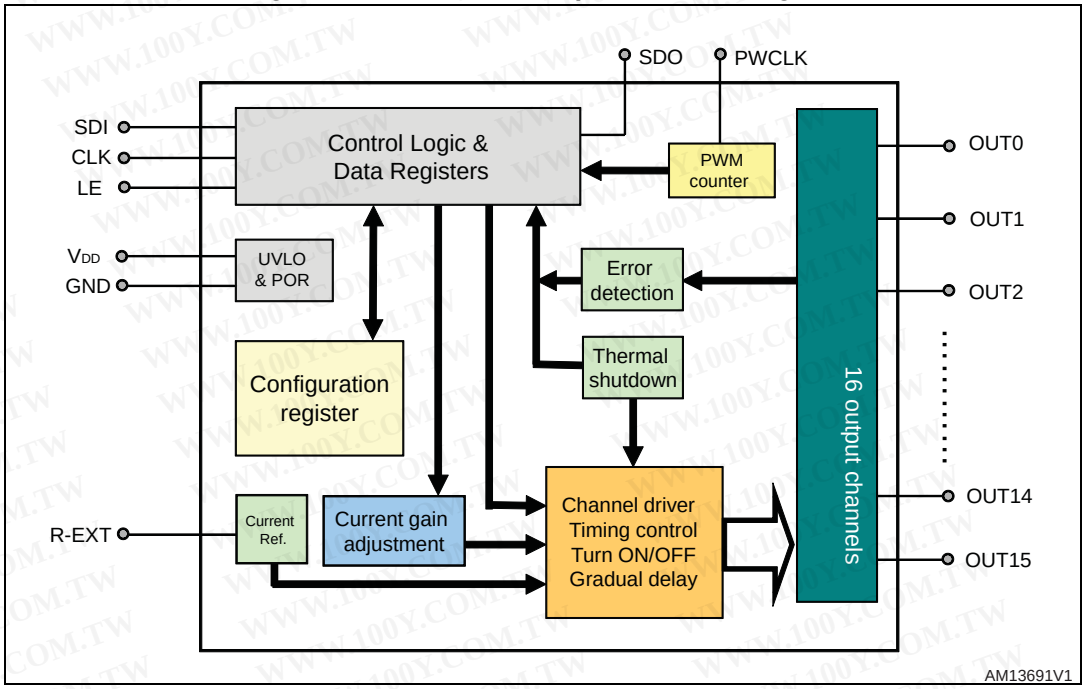
Figure 5. Timing for clock, serial in, serial out, latch enable and outputs



The correct sampling of the data depends on the stability of the data at SDI on the rising edge of the clock signal and it is assured by a proper data setup and hold time ($t_{SU(D)}$ and $t_{h(D)}$), as shown in *Figure 5*. The same figure shows the propagation delay from CLK to SDO (t_{PLH}/t_{PHL}). *Figure 5* describes also the minimum duration of CLK, LE pulses ($t_{W(CLK)}$) and $t_{W(L)}$ respectively and the propagation delay from LE to OUT_n (t_{PLHLE} and t_{PHLLE}) in the hypothesis that all channels have already been enabled by PWM counter.

6 Simplified internal block diagram

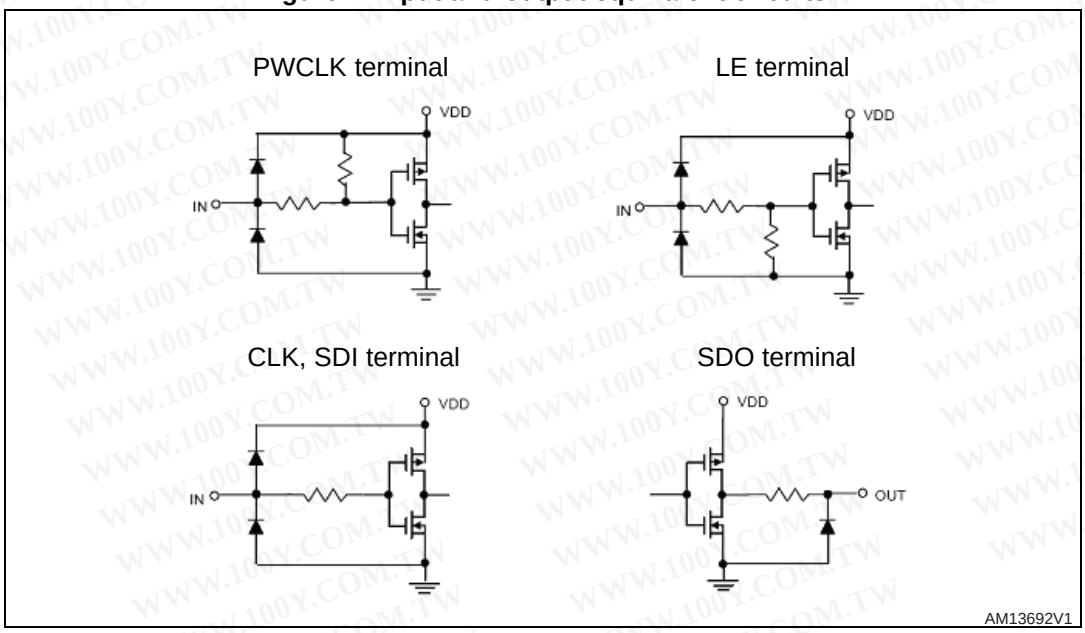
Figure 6. LED1642GW simplified block diagram



6.1 Equivalent circuits of inputs and outputs

LE and PWCLK input terminals have pull-down and pull-up connection respectively. CLK and SDI must be connected to the external circuit to fix the logic level.

Figure 7. Input and output equivalent circuits



7 Digital blocks

The data input arrives through the serial Interface at each CLK rising edge. The LE signal is used to latch the loaded data and also to address data loading to the appropriate register, thermal flag reading and error detection. The access to the different registers or functions of the device (configuration register, brightness register or current gain, error detection, etc.) is achieved by using different digital keys, defined as a number of CLK pulses during which the LE signal is asserted. The available digital keys are listed in *Table 7* and *Figure 8*. A typical channel data input is shown in *Figure 9*.

Table 7. Digital key summary

Number	# CLK rising edge when the LE is “1”	Command description
1	1 – 2	Write switch (to turn on/off output channels)
2	3 – 4	Brightness data latch
3	5 – 6	Brightness global latch
4	7	Write configuration register
5	8	Read configuration register
6	9	Start open error detection mode
7	10	Start short error detection mode
8	11	Start combined error detection mode
9	12	End error detection mode
10	13	Thermal error reading
11	14	Reserved
12	15	Reserved

Figure 8. Digital keys

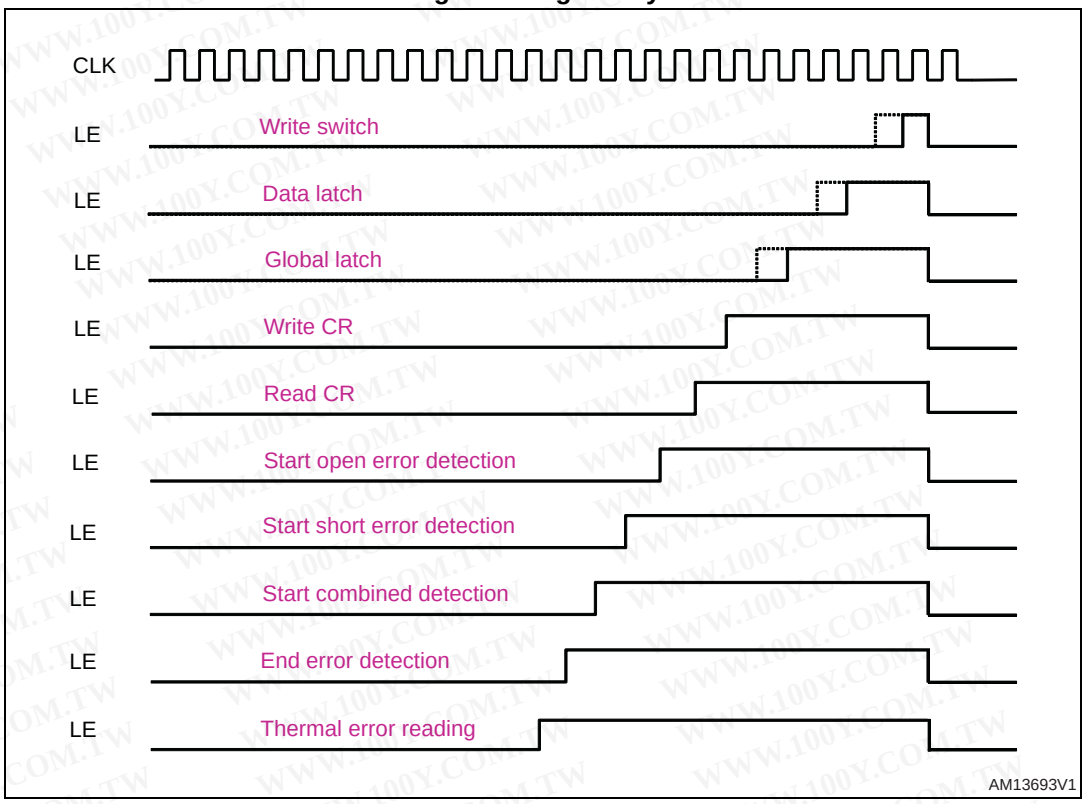
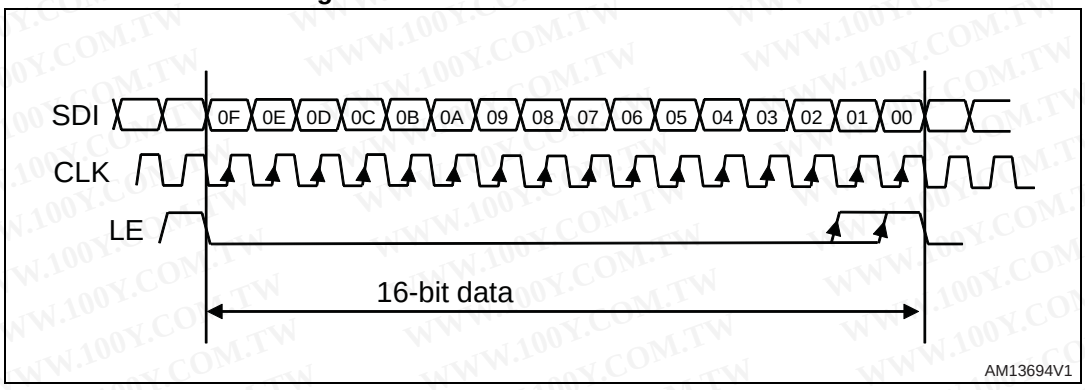


Figure 9. Channel data and write switch



8 Configuration register

The configuration register is used to enable or disable some device features, to program some parameters and to change other settings. The access to this register (read or write) is managed to find a description for each bit as described in *Table 8*. The default value of the configuration register (when the device is switched on or after a reset) is "0" for all bits. To change anything in the configuration register, a 16-bit digital word must be sent (CFG - 0 represents LSB, CFG -15 the MSB).

Table 8. Configuration register

Bit	Definition	R/W	Description				Default
CFG-0	Current gain adjustment	R/W	6-bit DAC allows adjusting the device output current in 64 steps for each range (defined by CFG-6)				0
CFG-1							0
CFG-2							0
CFG-3							0
CFG-4							0
CFG-5							0
CFG-6	Current range	R/W	”0” low current range “1” high current range				0
CFG-7	Error detection mode	R/W	“0” normal mode “1” reserved mode				0
CFG-8	Shorted-LED detection thresholds	R/W	Programmable output shorted-LED detection thresholds	CFG-9	CFG-8	Th. volt.	0
				0	0	1.8 V	
				0	1	2.5 V	
CFG-9		R/W		1	0	3 V	0
				1	1	3.5 V	
CFG-10	Auto OFF shutdown	R/W	“0” device always ON ”1” auto power shutdown active (auto OFF)				0
CFG-11	Output turn-on/off time	R/W	Programmable output rise and fall time (20% to 80%)	CFG-12	CFG-11	Turn-on	Turn-off	0
				0	0	30 ns	20 ns	
				0	1	100 ns	40 ns	
CFG-12		R/W		1	0	140 ns	80 ns	0
				1	1	180 ns	150 ns	
CFG-13	SDO delay	R/W	If “0” no delay is present on SDO If “1” the data are shifted out and they are synchronized with the falling edge of the CLK signal					0

Table 8. Configuration register (continued)

Bit	Definition	R/W	Description	Default
CFG-14	Gradual output delay	R/W	“0” a progressive delay is applied to output (10 ns per channel) ”1” no delay is applied to output	0
CFG-15	12/16 PWM counter	R/W	“0” to select 16-bit brightness register (65536 grayscale rightness steps). “1” to select 12-bit brightness register (4096 grayscale brightness steps)	0

8.1 Gain control (from CFG 0 to 5) and current ranges (CFG- 6)

The LED current can be programmed using an external resistor connected to GND from R_{EXT} pin and can be fixed using the dedicated bits of the configuration register (from CFG - 0 to CFG - 5 bits define the gain, while CFG - 6 bit defines the current range within the which the gain can be adjusted). The device can regulate the current up to 36 mA and down to 0.5 mA. The accuracy of the LED current depends on the selected range and it is guaranteed in the ranges indicated in the static electrical characteristics only (see *Table 3* and *9*). When the device is switched on, the selected current range and the resistor connected to the R_{EXT} pin fix the default LED current:

$$I_{OL\_default} = \frac{V_{REF}}{R_{EXT}} \cdot K$$

Where V_{REF}=1.23 V is the voltage of the R_{EXT} pin and K is the mirroring current ratio, whose value depends on the selected current range:

- K = 28 with low current range selected (CFG - 6 = "0")
- K = 80 with high current range selected (CFG - 6 = "1")

The relation between the programmed current and the current gain settings is the following:

$$I_{OL} = (I_{OL\_default} + G \cdot \Delta I_{step})$$

where G is the current gain value (decimal value) defined by the dedicated bits of the current gain register. The current gain is managed by 6-bits of the configuration register (CFG - 0 to CFG - 5, CFG - 0 is LSB and CFG - 5 is MSB) and can be adjusted within two ranges (selectable through the bit CFG - 6) over 64 steps. The width of each step depends on the default current ($I_{ol\_default}$) as well as the selected R_{EXT}. Finally, each step is as follows:

$$\Delta I_{step} = \frac{I_{OL\_default}}{21}$$

The *Table 9* shows an example of the current setting with an external resistance (R_{EXT}) = 11 KΩ:

Table 9. Example of current ranges

	R_{EXT} [KΩ]	CFG-6	CFG-0 to CFG-5	LED current(1) [mA]	Accuracy
Low range	11	0	000000	3.1 mA	± 4% ch-to-ch
	11	0	111111	12.5 mA	-
High range	11	1	000000	8.9 mA	
	11	1	011010	20 mA	± 3% ch-to-ch

1. The indicated values may be slightly different on the current device.

The *Table 10* shows an example of current setting and gain control with R_{EXT} = 11 kΩ, see also *Figure 10*.

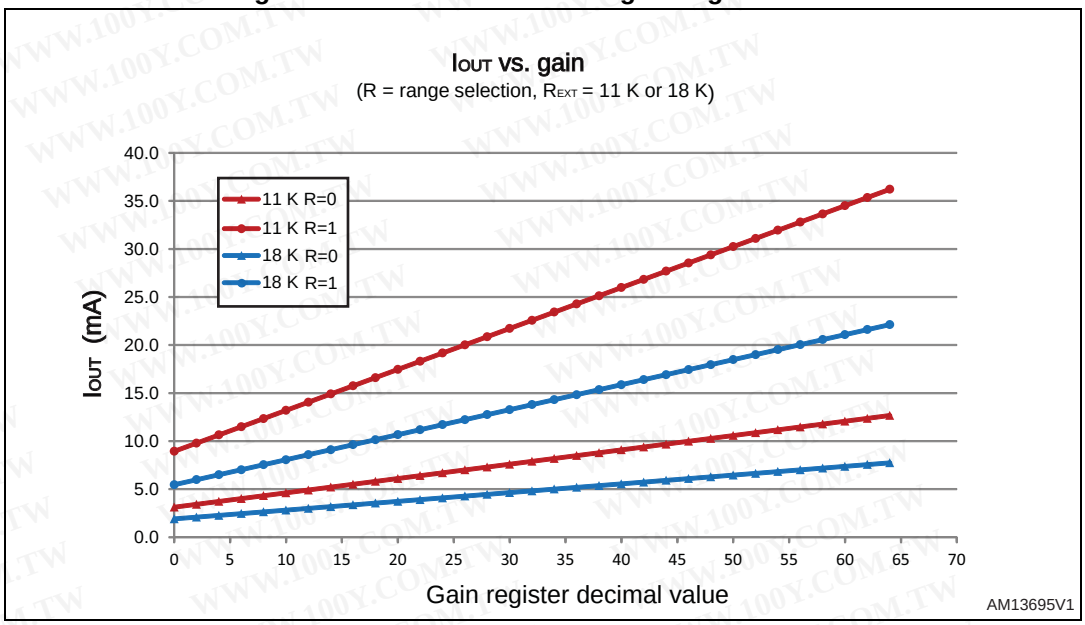
Table 10. Gain steps for the current range selected by R_{EXT} = 11 kΩ

	CFG-6	CFG(0 to 5)	LED current (1) [mA]
Low range	0	000000	3.131
	0	000001	3.280
	…	…	…
	0	111111	12.524
High range	1	000000	8.945
	1	000001	9.371
	…	…	…
	1	111111	35.78

1. The indicated values may be slightly different on the current device.

The external programming resistance must be connected as close as possible to the related device pins (R_{EXT} and GND) to reduce as minimum as possible the routing length and prevent reference noise injection and electromagnetic interferences. Moreover, a direct connection to the device GND pin reduces the possible output current variation when the total device ground current changes (load effect).

Figure 10. Channel current vs. gain register value



8.2 Error detection mode (CFG-7)

Stopping the normal activity of the display and turning on all driver channels allows the error detection to be performed and failed LED or display defects to be checked.

The error detection is active when the CFG -7 bit of the configuration register is "0". The diagnostics is performed as shown in *Figure 11*:

- The LED has to be selected turning on the relative channel on the switch register (powering on or off the output channels); the brightness register value for this channel cannot be zero.
- The normal error detection has to be selected in the configuration register (CFG-7= "0"). The appropriate digital key to choose the type of detection (open, short or combined) must be sent (see *Table 7*).
- After the error detection starts, the channel under testing has to be turned on at least 1 µs (the LED is at the nominal current). Please note that, the output power-on depends on PWCLK signal and in several applications this signal is not synchronized with the serial interface clock (CLK pin). Therefore, to be sure that, between the detection start and the detection end, the output power-on is 1 µs and moreover, that last power-on, in the interval, starts at least 0.5 µs before the detection end pattern (see *Figure 12*), it is suggested that the error detection should be performed just after the device startup (brightness counter reset) with all channels ON, before applying PWCLK signal.
- The result of the detection ("0" indicates a fault condition) is shifted out SDO, in 16 clock pulses after the "detection end command" is provided, first output bit represents channel 15 (error data can be read in a way similar to configuration register data reading as shown on *Figure 13*, *14*, *15* and *16*).

Please note that (with SDO delay off) output 15 detection result will be available just after 1st clock pulse rising edge, so it can be sampled on the rising edge of second clock pulse. In the same way output 0 detection result will be available just after 16th clock pulse rising edge, so it can be sampled on the rising edge of 17th CLK pulse.

Figure 11. Error detection action sequence

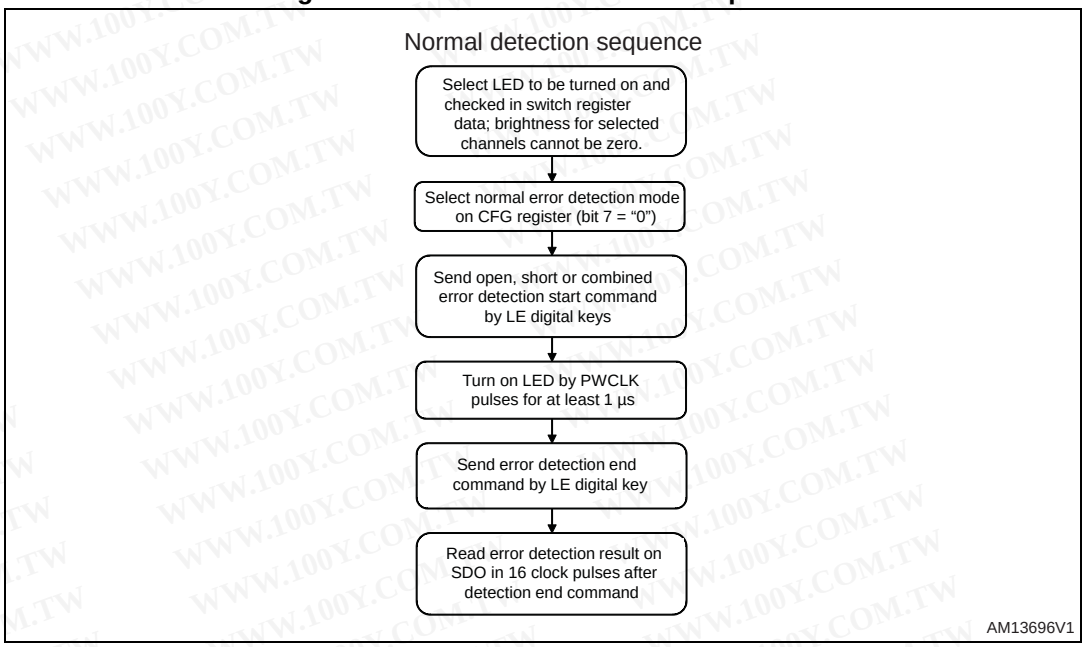


Figure 12. Error detection power-on timing

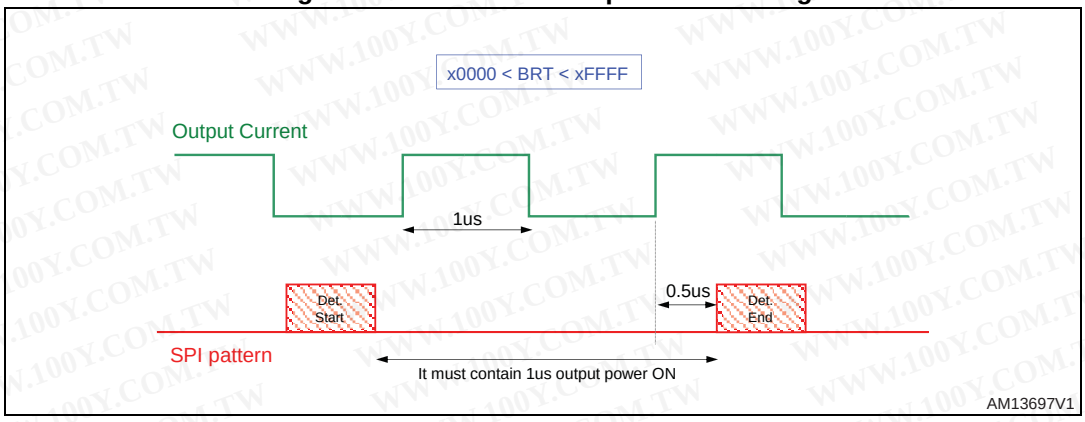


Figure 13. Configuration register reading sequence

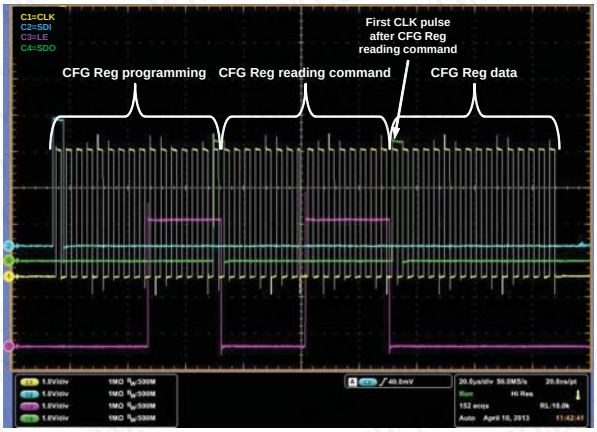


Figure 14. Configuration register reading sequence (zoom)

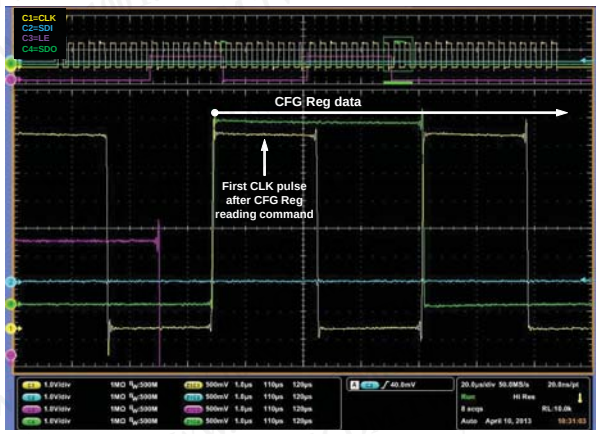


Figure 15. Configuration register reading sequence - SDO delay actives

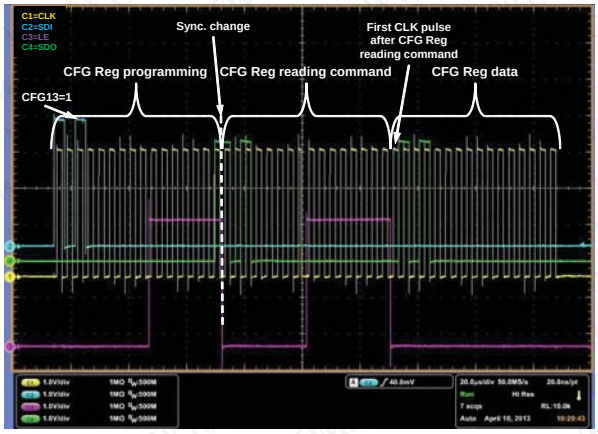
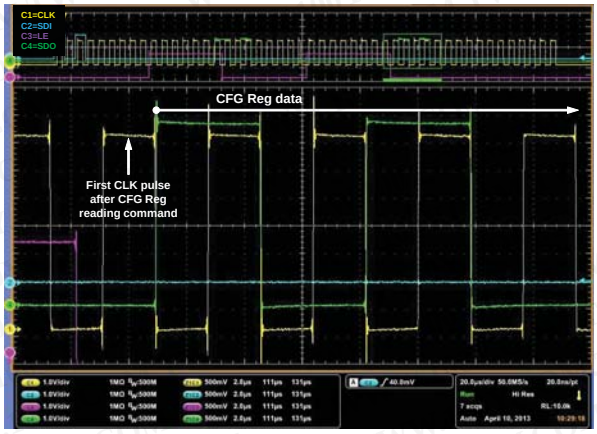


Figure 16. Configuration register reading sequence - SDO delay actives (zoom)



8.3 Error detection conditions

During the error detection phases for each channel, the following checks have to be performed:

- The output current in open detection mode (digital key: 9 CLK rising edges when LE is "1")
- The output voltage in short detection (digital key: 10 CLK rising edges when LE is "1")
- Both parameters (output voltage and current) in combined error detection mode (digital key: 11 CLK rising edges when LE is "1").

The thresholds for the error diagnostics are listed in *Table 11*:

Table 11. Diagnostic thresholds

Error detection modes		Checked malfunction	CFG-9	CFG-8	Thresholds (V)		
					Min.	Typ.	Max.
Open detection	Combined mode	Open line or output short to GND	x	x	-	$I_{OUT} \leq 0.5 \times I_{OUT}$ programmed	-
Short detection		Short on LED or short to V-LED	0	0	1.15	$V_{OUT} \geq 1.8$	2.05
			0	1	2.25	$V_{OUT} \geq 2.5$	2.75
			1	0	2.75	$V_{OUT} \geq 3.0$	3.25
			1	1	3.25	$V_{OUT} \geq 3.5$	3.80

8.4 Auto-wakeup/auto power shutdown (CFG-10)

This feature reduces the power consumption when all outputs are OFF. It is active when the CFG -10 bit of configuration register is "1". The auto power shutdown (auto OFF) starts when the data latched is "0" for all channels, and device is active again (wakeup) at the first latched data string including at least one bit = "1" (at least one channel ON). Timings for shutdown and wakeup are present in the dynamics feature table. While the auto power shutdown is active, the device ignores any other command except the channel power-on.

8.5 Programmable turn-on/turn-off time (CFG-11/12)

The device gives the possibility to program the turn-on and turn-off time of the current generators. Four different values can be selected using CFG -12 and CFG-11 bits of the configuration register (see *Table 8*) to fit the application requirements: 30/20 ns (00), 100/40 ns (01), 140/80 ns (10) and 180/150 ns (11). The selected value refers to T_{ON} (current rise time) and T_{OFF} (current fall time).

Figure 17. Output T_{ON} (current rise time) CFG - 12 = CFG - 11 = 0

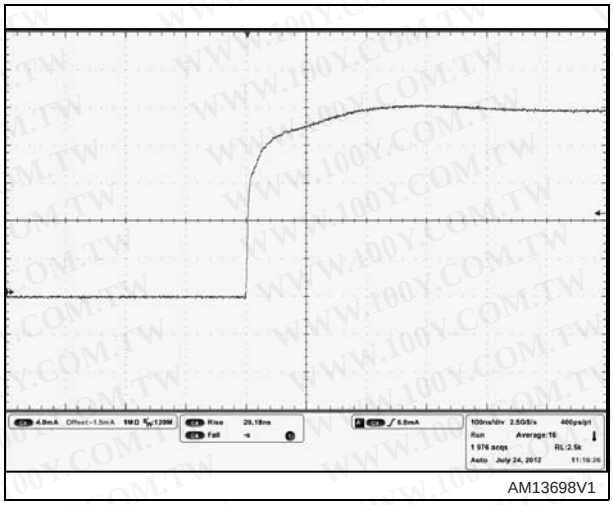


Figure 18. Output T_{OFF} (current fall time) CFG - 12 = CFG - 11 = 0

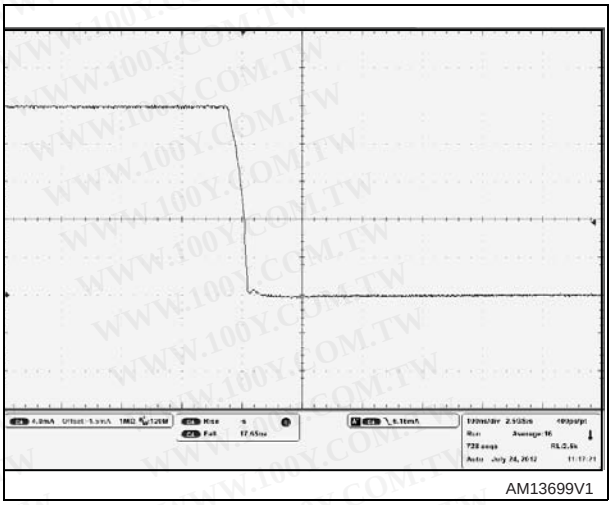


Figure 19. Output T_{ON} (current rise time) CFG - 12 = CFG - 11 = 1

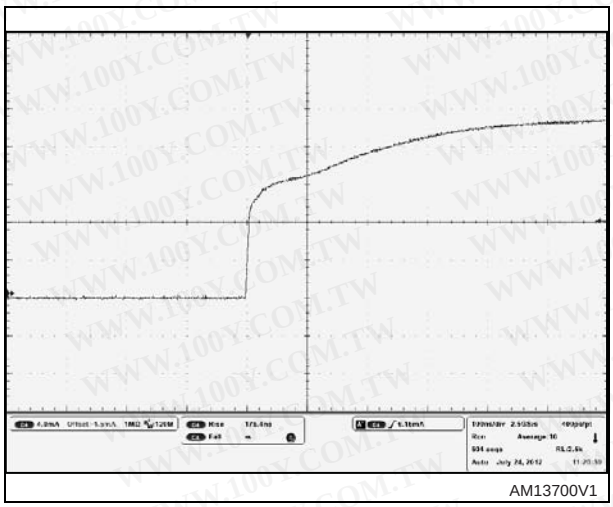
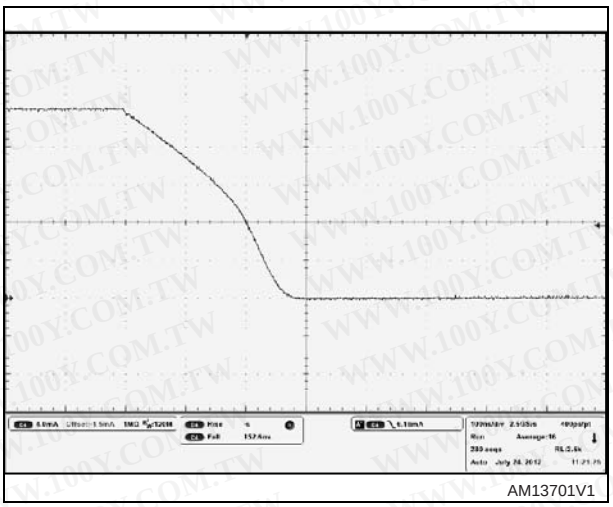


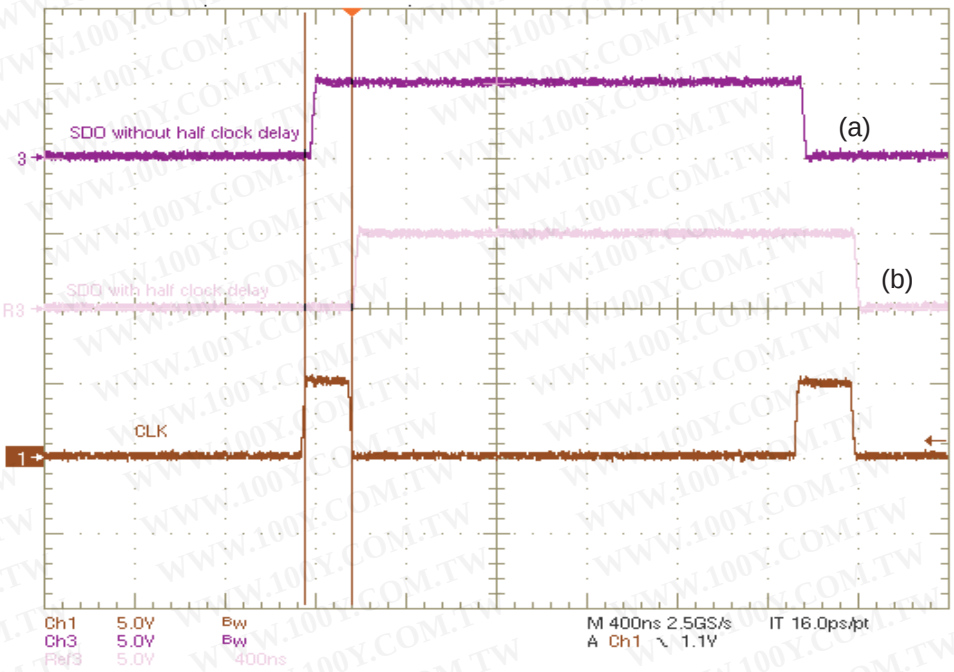
Figure 20. Output T_{OFF} (current fall time) CFG - 12 = CFG - 11 = 1



8.6 SDO delay (CFG-13)

Usually in SDO terminal, data are shifted out the rising edge of CLK signal (with a propagation delay of about 15 ns - signal (a) in *Figure 21*). The device has the possibility to shift data out the falling edge of the CLK signal (with few ns of propagation delay - signal (b) in *Figure 21*). This feature is active when CFG -13 bit of the configuration register is "1". Default setting for this bit is "0" hence the SDO delay is not activated by default. This feature is particularly useful when some devices are connected in daisy chain configuration with mismatched propagation delays, between CLK and SDO data path (board routing).

Figure 21. SDO delay



(a) Data shifted out of the SDO with the device propagation delay
(b) Data shifted out of the SDO by the falling edge of the CLK

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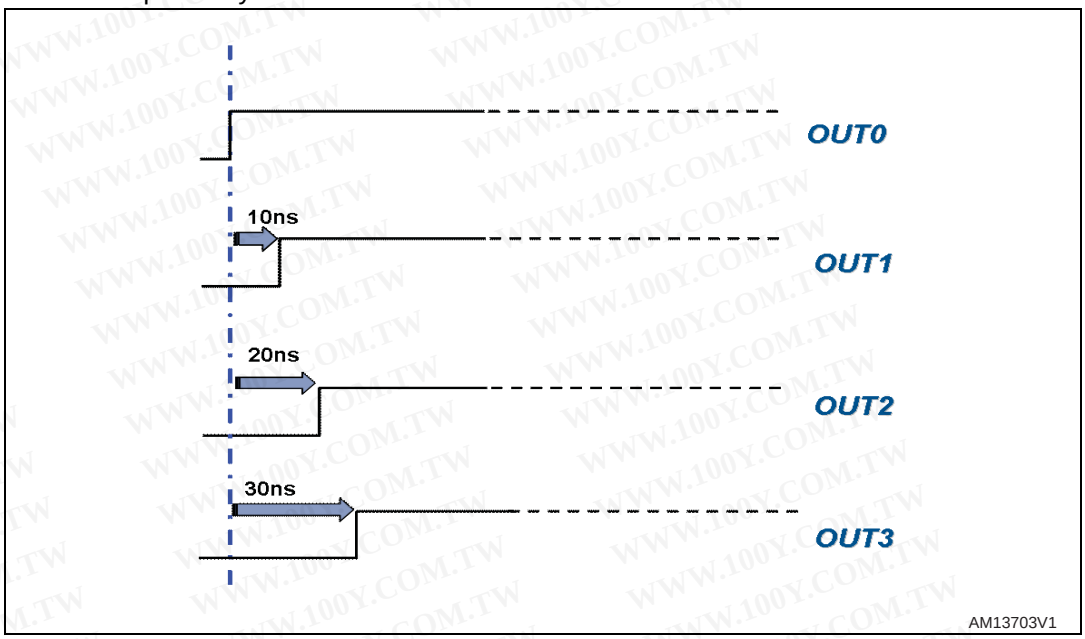
8.7 Gradual output delay (CFG-14)

The gradual output delay consists of turning on gradually the current generators avoiding to turn on all channels at the same time.

When PWM counter enables the device channels, the outputs can be turned on simultaneously or with a progressive delay. Thanks to configuration register CFG -14 bit, the user can decide to put a delay among outputs (10 ns from each channel to the next one, around 150 ns between first and last channel). The typical output timing is shown in *Figure* . This feature prevents the inrush current and reduces the bypass capacitor value.

Gradual output delay



8.8 PWM counter setting and brightness register (CFG-15)

The brightness of each channel can be adjusted through a 12/16-bit PWM grayscale brightness control according to the PWM counter selection (configuration register CFG -15 bit). Brightness data is loaded by the SDI pin in a 16-bit shift register. Once 16-bit has been loaded (first input bit of brightness word is MSB, 16th bit is LSB), the digital word is moved to the corresponding temporary buffer (first word is the brightness of channel 15, the last one is for channel 0) using the appropriate key shown in *Table 7* ("data latch"). One "data latch" key must follow each 16-bit brightness word except the last one. When the last brightness word is loaded (channel 0 brightness data), the key indicated as "global latch" in *Table 7* must be used. This action moves the word from the shift register to the temporary buffer through the OUT0 and, at the same time, transfers all data of the 16 temporary buffers (16 x16-bit string) to the corresponding brightness registers (see also *Figure 27*).

The PWM signals are generated by comparing the content of the brightness registers to a 16-bit or 12-bit counter, according to the CFG-15 bit status. The counter's clock source is provided to the PWCLK pin. In case of selection of 12-bit PWM counter, the four most significant bits of each brightness data word are ignored. However, each of sixteen brightness data words must be 16-bit long.The brightness register default value is "0", unless this value is changed, the LED brightness is minimum. *Figure 26* shows this function in the schematic.

PWCLK must be a square wave signal, duty cycle is not important but the minimum width has to be above 20 ns, max. frequency has to be 30 MHz (pay attention the minimum output ON time). Just after the device startup (brightness counter reset), before applying PWCLK signal, all channels are in power-on condition if the brightness register values are not zeroed.

Figure 22. PWCLK counter and comparator

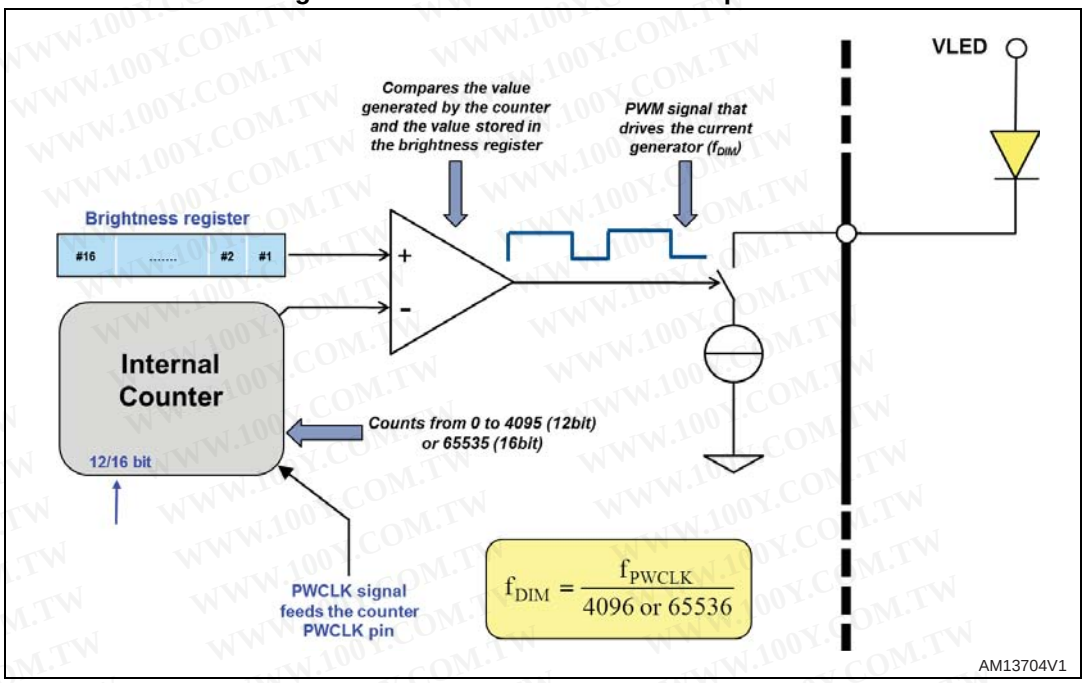
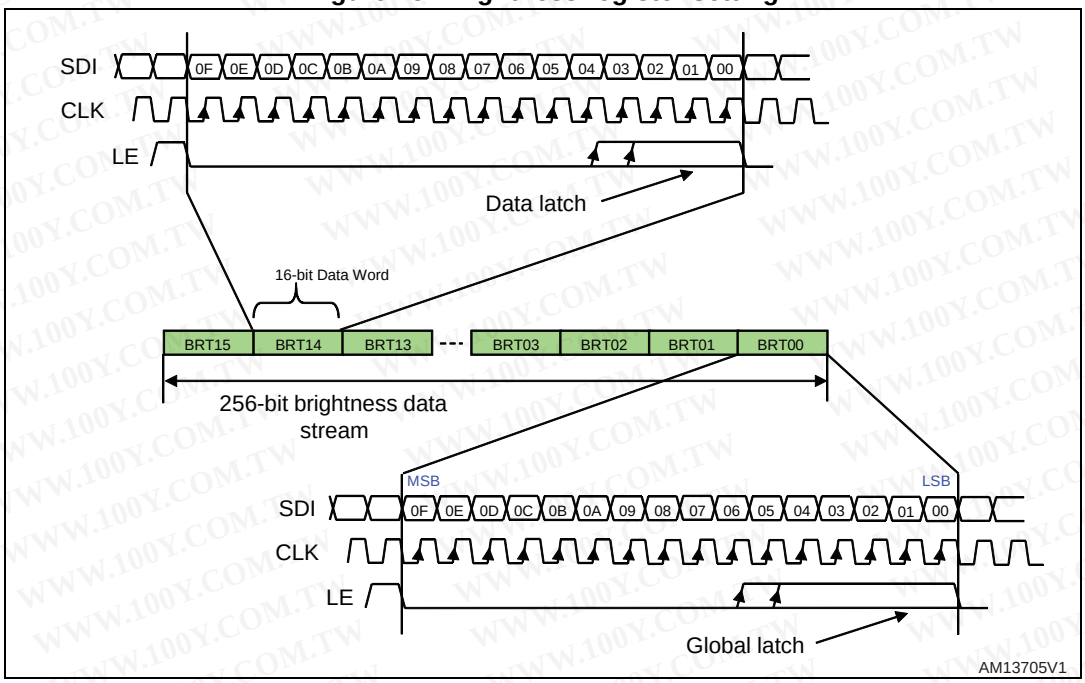


Figure 23. Brightness register setting

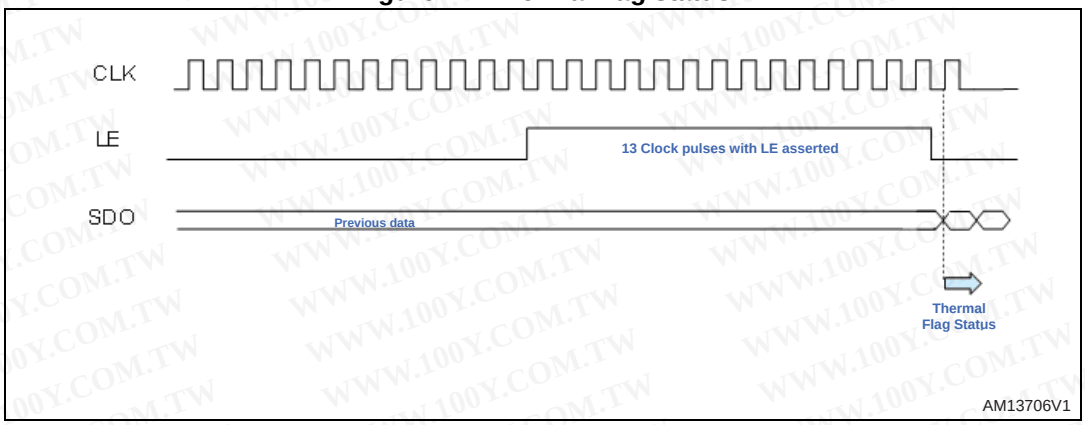


9 Thermal flag

The device has a thermal control logic providing a flag status when the internal temperature exceeds 150 °C (if temperature increases over 170 °C a thermal shutdown protects the device). This status can be read running the digital key "thermal error reading", holding the LE high for 13 CLK rising edges (see *Figure 24*). If thermal alert is asserted, a 16-bit string = "1" is sent by SDO. The error data is uploaded into EDR register and this error notification is ready to be streamed through SDO to next 16 CLK rising edges. Hence, thermal flag status can be:

Device temperature	SDO
under 150 °C	“0000 0000 0000 0000”
over 150 °C	“1111 1111 1111 1111”

Figure 24. Thermal flag status



10 Dropout voltage

In order to correctly regulate the channel current, a minimum output voltage (V_{DROP}) across each current generator must be guaranteed.

The *Figure 25* and *Table 12* show the minimum V_{DROP} related to the regulated current; these measurements have been recorded with just one output ON. When more than one output is active the drop voltage increases. At 36 mA per channel, the minimum output voltage must be increased about 200 mV.

A V_{DROP}, lower than the minimum recommended, implies the regulation of a current lower than the expected one. However an excess of V_{DROP} increases the power dissipation.

Figure 25. Typical channel dropout voltage vs. output current (V_{DD} = 3.3 V)

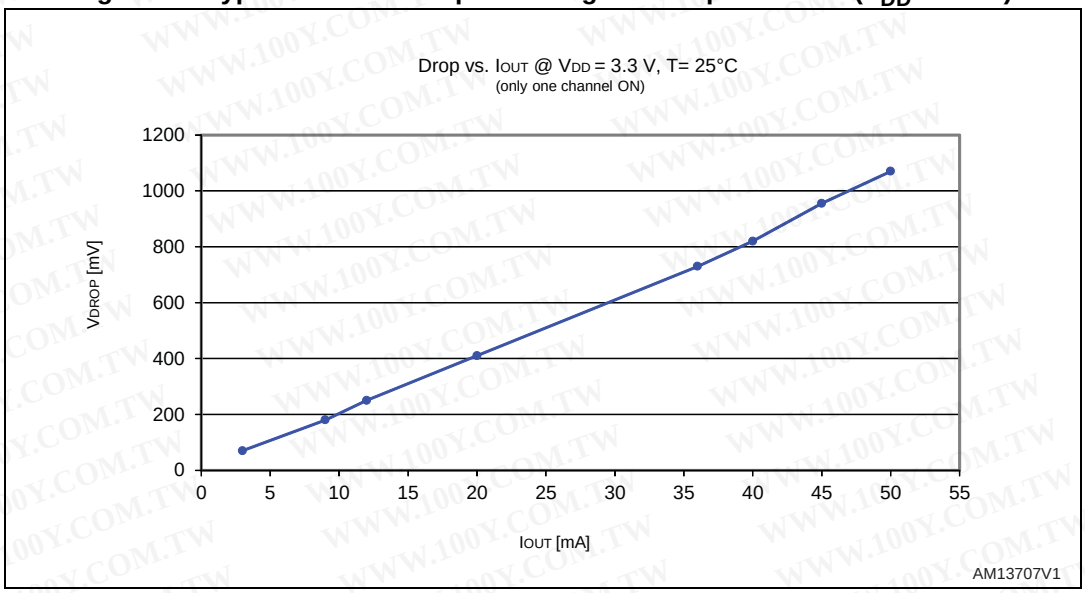


Table 12. Minimum dropout voltage for some current values

Output current [mA]	Minimum V_{DROP} @ V_{DD} = 3.3 V [mV]
3	70
9	180
12	250
20	410
36	730
40	820
45	955
50	1070

11 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 13. QSOP-24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	1.54	1.62	1.73
A1	0.1	0.15	0.25
A2		1.47	
b	0.31	0.2	
c	0.254	0.17	
D	8.56	8.66	8.76
E	5.8	6	6.2
E1	3.8	3.91	4.01
e		0.635	
L	0.4	0.635	0.89
h	0.25	0.33	0.41
<	8°	0°	

Figure 26. QSOP-24 package dimensions

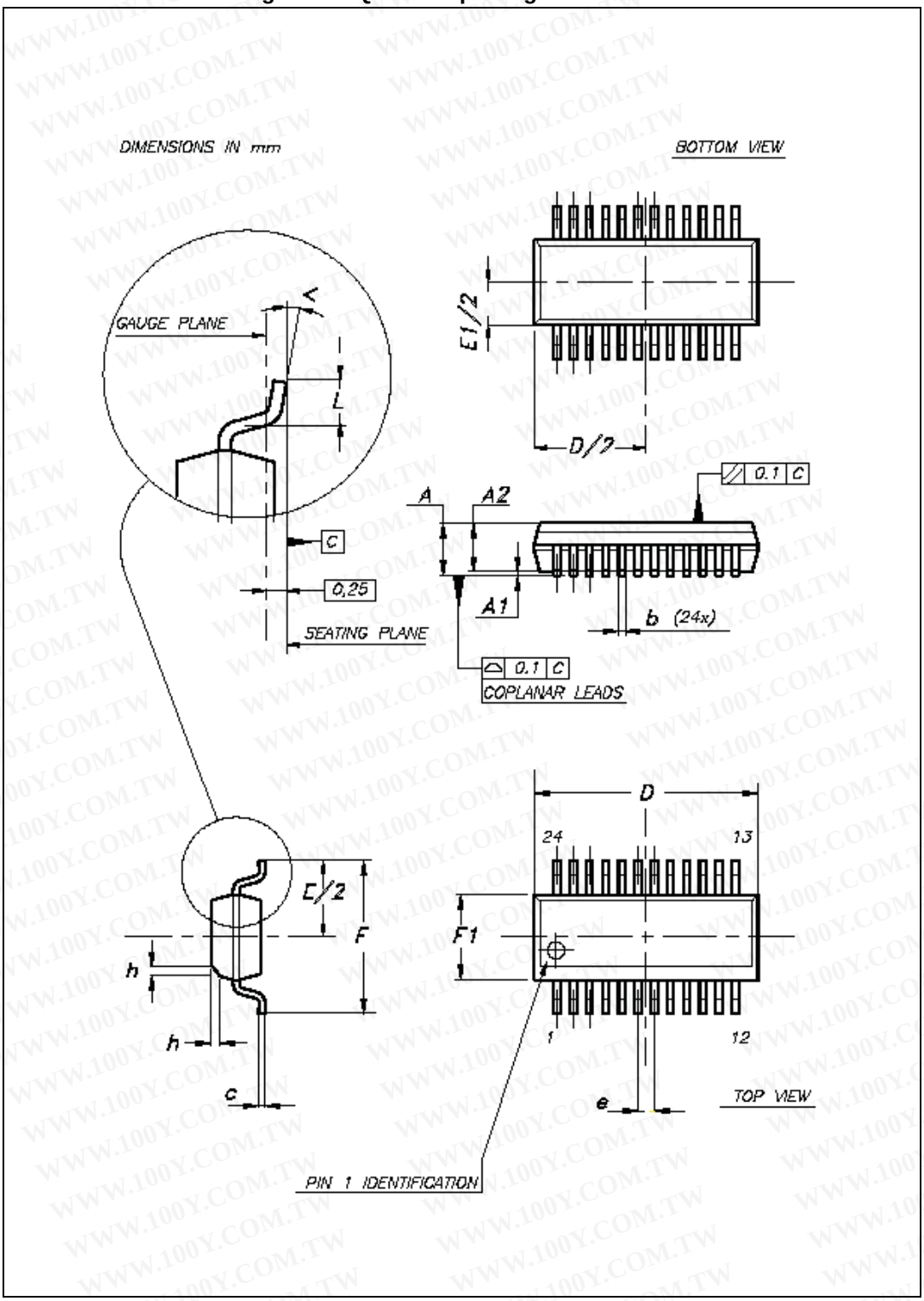


Table 14. QFN-24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20	
b	0.18	0.25	0.30
D	3.85	4.00	4.15
D2	2.00	2.15	2.25
E	3.85	4.00	4.15
E2	2.00	2.15	2.25
e		0.50	
L	0.30	0.40	0.50

Figure 27. QFN-24 package dimensions

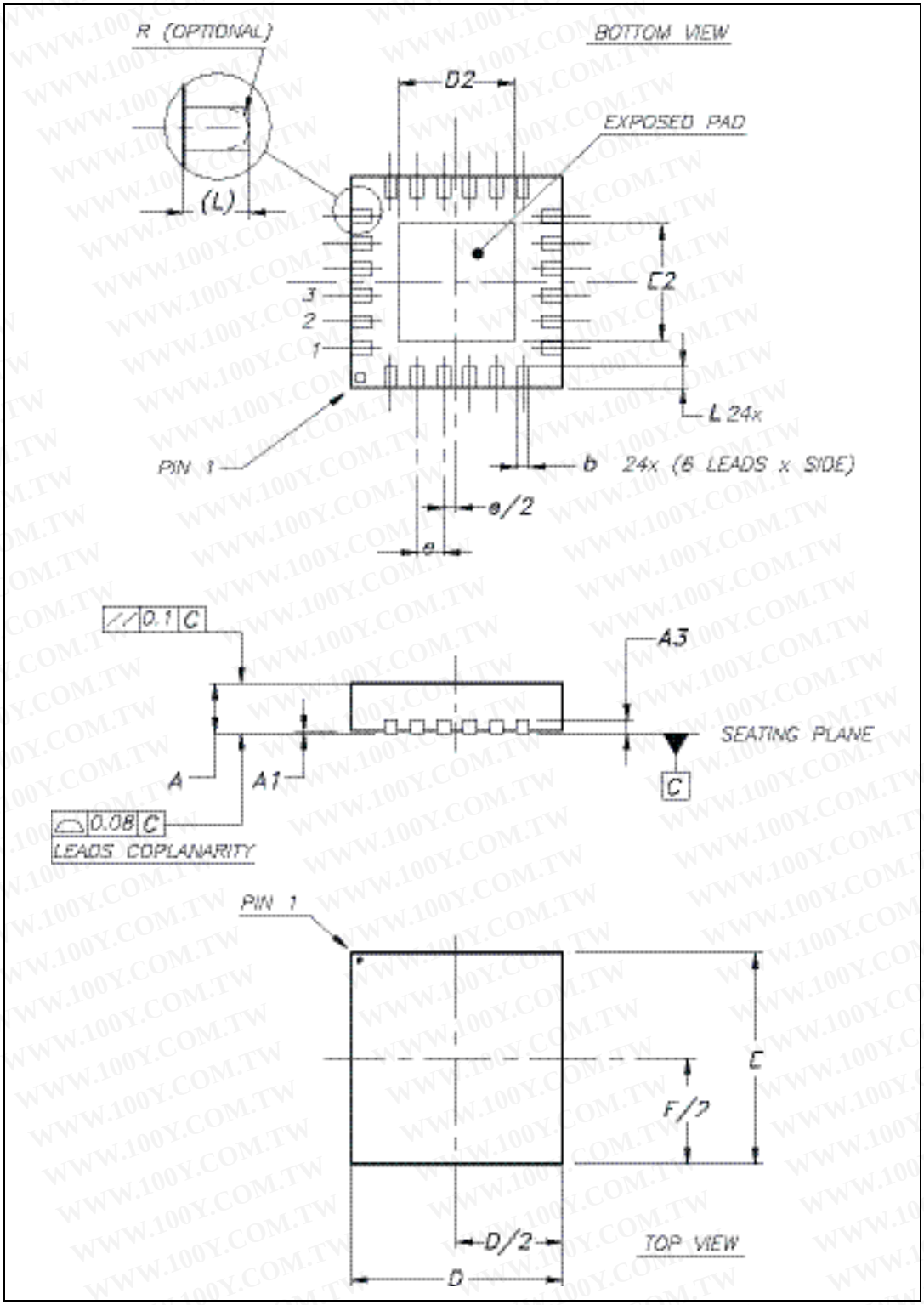


Table 15. TSSOP24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.1
A1	0.05		0.15
A2		0.9	
b	0.19		0.30
c	0.09		0.20
D	7.7		7.9
E	4.3		4.5
e		0.65 BSC	
H	6.25		6.5
K	0°		8°
L	0.50		0.70

Figure 28. TSSOP24 package dimensions

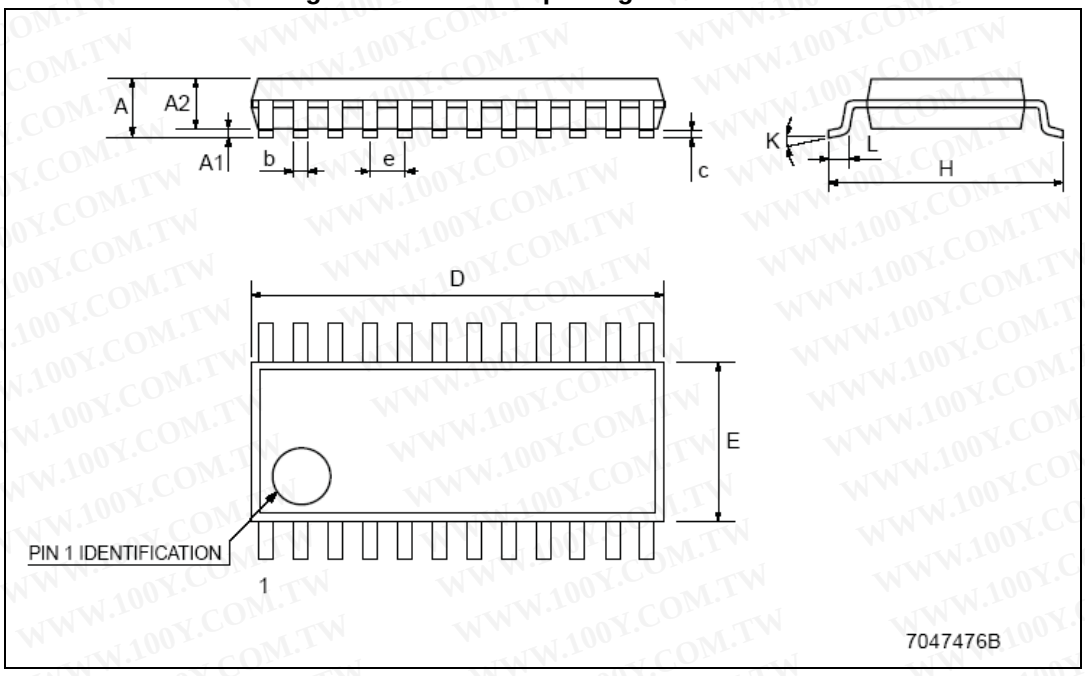
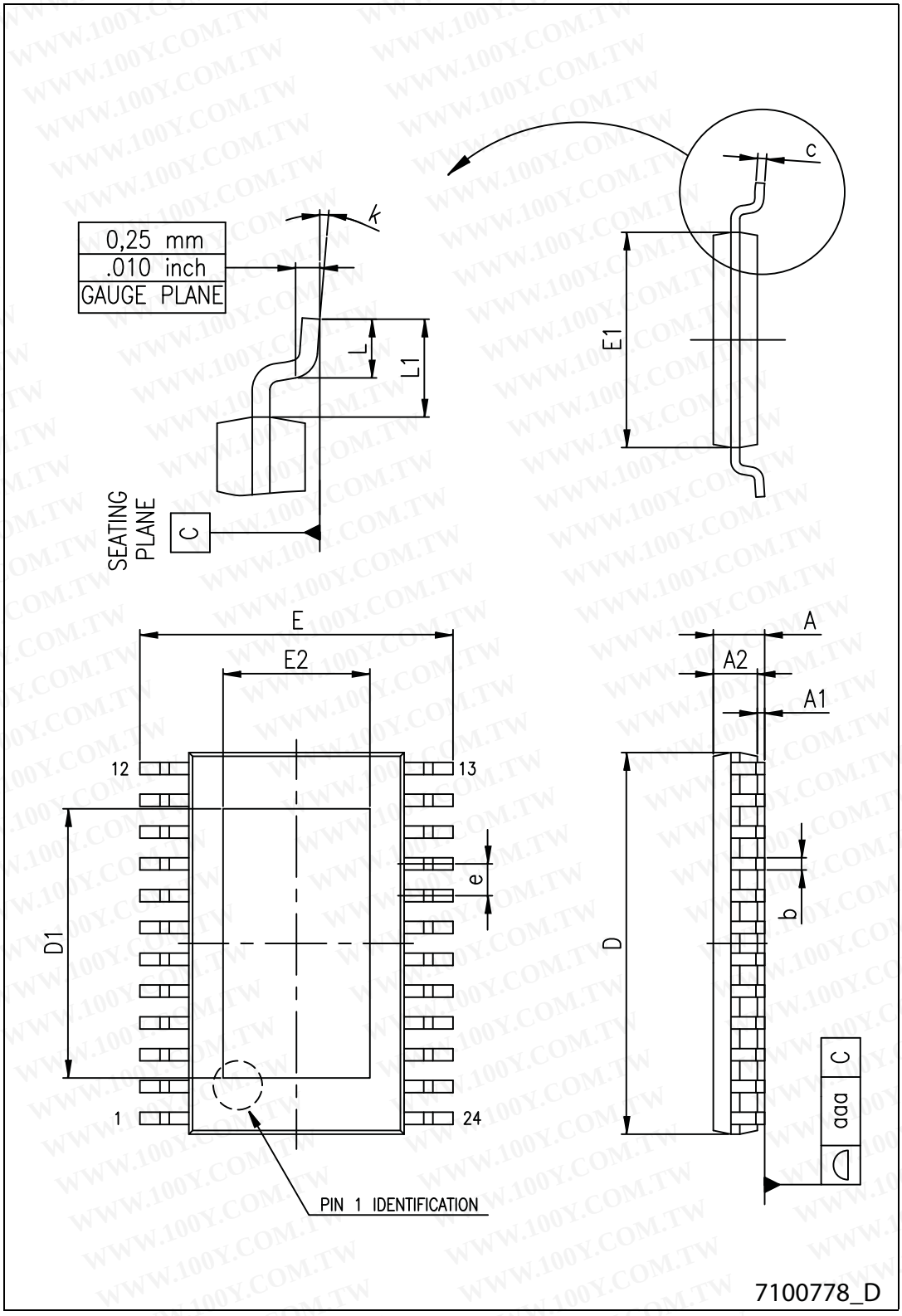


Table 16. TSSOP24 exposed pad mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.20
A1			0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	7.70	7.80	7.90
D1	2.70		
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	1.50		
e		0.65	
L	0.45	0.60	0.75
L1		1.00	
k	0		8
aaa			0.10

Figure 29. TSSOP24 exposed pad dimensions

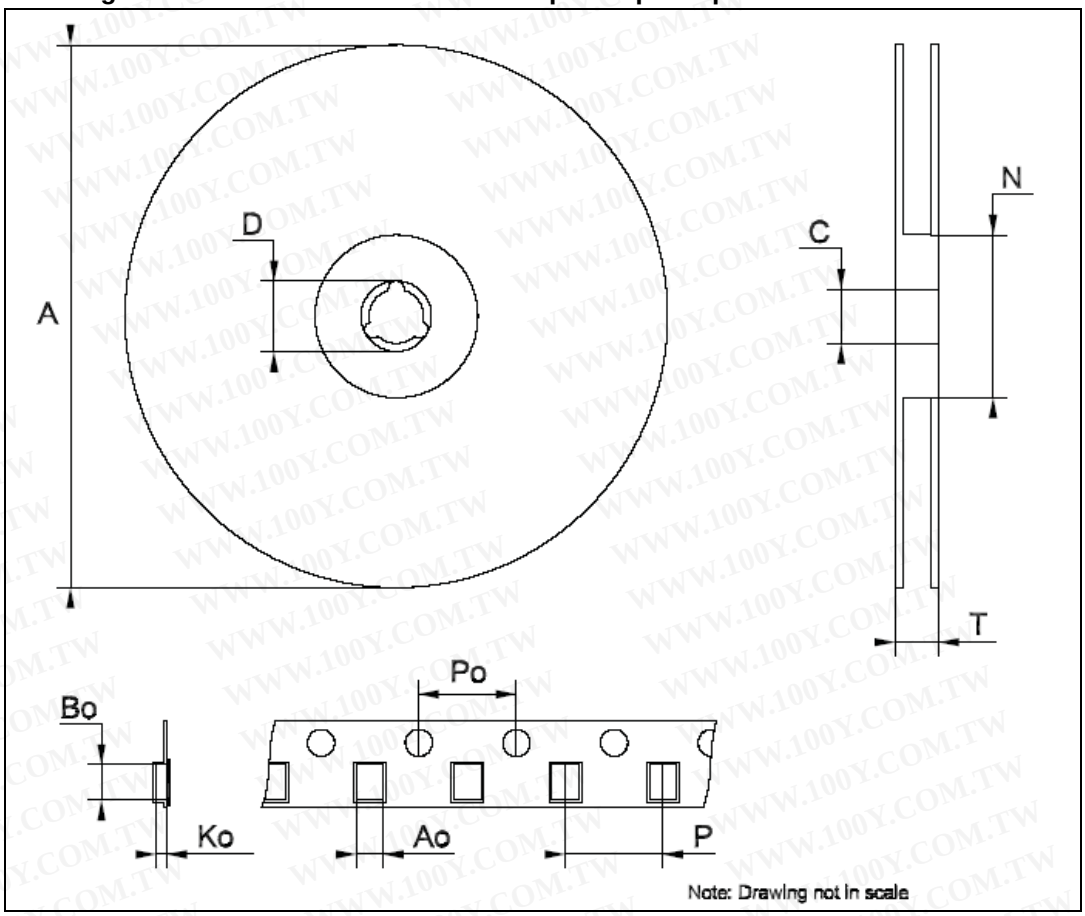


12 Packaging mechanical data

Table 17. TSSOP24 and TSSOP24 exposed pad tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A		-	330
C	12.8	-	13.2
D	20.2	-	
N	60	-	
T		-	22.4
Ao	6.8	-	7
Bo	8.2	-	8.4
Ko	1.7	-	1.9
Po	3.9	-	4.1
P	11.9	-	12.1

Figure 30. TSSOP24 and TSSOP24 exposed pad tape and reel dimensions



13 Ordering information

Table 18. Ordering information

Order code	Package	Packaging
LED1642GWPTR	QSOP-24	2500 parts per reel
LED1642GWQTR	QFN-24	4000 parts per reel
LED1642GWTTR	TSSOP24	2500 parts per reel
LED1642GWXTTR	TSSOP24 exposed pad	2500 parts per reel

14 Revision history

Table 19. Document revision history

Date	Revision	Changes
03-May-2013	1	Initial release.
06-Jun-2013	2	Updated *Table 2: Absolute maximum ratings*, *Figure 10: Channel current vs. gain register value* and *Section 8.2: Error detection mode (CFG-7)*. Added *Figure 13*, *14*, *15* and *16*. Minor text changes.
19-Aug-2013	3	Updated the Title, the Features and the Description. Modified *Table 4: Electrical characteristics*, Updated *Table 9: Example of current ranges*, *Table 10: Gain steps for the current range selected by REXT = 11 kW*, *Section 8.2: Error detection mode (CFG-7)*, *Section 8.8: PWM counter setting and brightness register (CFG-15)*.

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