

Fault-Protected RS-485 Transceivers With Extended Common-Mode Range

Check for Samples: [SN65HVD1785](#), [SN65HVD1786](#), [SN65HVD1787](#), [SN65HVD1791](#), [SN65HVD1792](#), [SN65HVD1793](#)

FEATURES

- **Bus-Pin Fault Protection to:**
 - $> \pm 70$ V ('HVD1785, 86,91,92)
 - $> \pm 30$ V ('HVD1787, 93)
- **Common-Mode Voltage Range (–20 V to 25 V) More Than Doubles TIA/EIA 485 Requirement**
- **Bus I/O Protection**
 - ± 16 kV JEDEC HBM Protection
- **Reduced Unit Load for Up to 256 Nodes**
- **Failsafe Receiver for Open-Circuit, Short-Circuit and Idle-Bus Conditions**
- **Low Power Consumption**
 - Low Standby Supply Current, 1 μ A Typ
 - I_{CC} 5 mA Quiescent During Operation
- **Power-Up, Power-Down Glitch-Free Operation**

APPLICATIONS

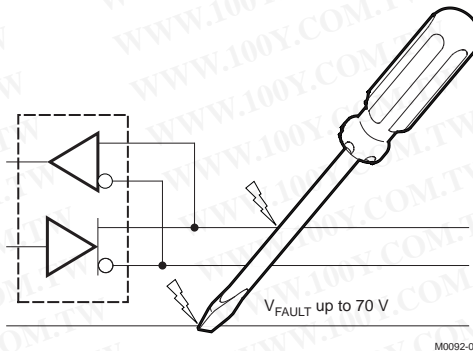
- **Designed for RS-485 and RS-422 Networks**

DESCRIPTION

These devices are designed to survive overvoltage faults such as direct shorts to power supplies, mis-wiring faults, connector failures, cable crushes, and tool mis-applications. They are also robust to ESD events, with high levels of protection to human-body model specifications.

These devices combine a differential driver and a differential receiver, which operate from a single power supply. In the 'HVD1785, 'HVD1786, and 'HVD1787, the driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. In the 'HVD1793, the driver differential outputs and the receiver differential inputs are separate pins, to form a bus port suitable for full-duplex (four-wire bus) communication. These ports feature a wide common-mode voltage range, making the devices suitable for multipoint applications over long cable runs. These devices are characterized from -40°C to 105°C .

For similar features with 3.3 V supply operation, see the SN65HVD1781 ([SLLS877](#)).



PRODUCT SELECTION GUIDE

PART NUMBER	DUPLEX	SIGNALING RATE	NODES	CABLE LENGTH
SN65HVD1785	Half	115 kbps	Up to 256	1500 m
SN65HVD1786	Half	1 Mbps	Up to 256	150 m
SN65HVD1787	Half	10 Mbps	Up to 64	50 m
SN65HVD1791	Full	115 kbps	Up to 256	1500 m
SN65HVD1792	Full	1 Mbps	Up to 256	150 m
SN65HVD1793	Full	10 Mbps	Up to 64	50 m



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION

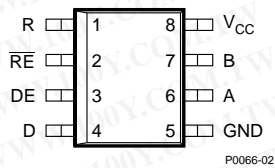
DRIVER FUNCTION TABLE

Input	Enable	Outputs		
		A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

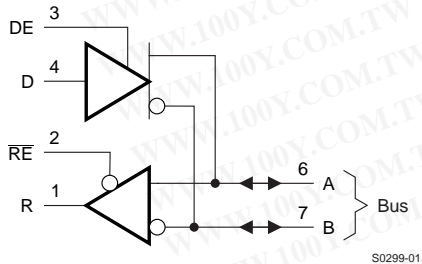
RECEIVER FUNCTION TABLE

Differential Input	Enable	Output	
$V_{ID} = V_A - V_B$	RE	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus high
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

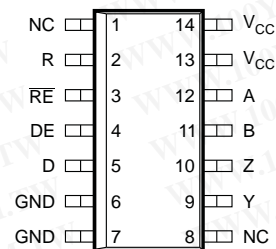
SN65HVD1785, 1786, 1787
 D or P Package
 (Top View)



Logic Diagram (Positive Logic)

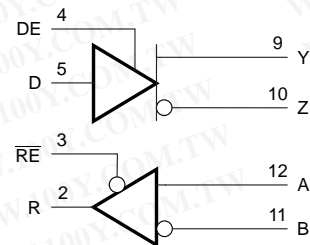


SN65HVD1791, 1792, 1793
 D Package
 (Top View)



NC - No internal connection
 Pins 6 and 7 are connected together internally.
 Pins 13 and 14 are connected together internally.

Logic Diagram (Positive Logic)



S0300-01

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

			VALUE	UNIT	
V _{CC}	Supply voltage		–0.5 to 7	V	
Voltage range at bus pins		'HVD1785, 86, 91, 92, 93	A, B pins	–70 to 70	V
		'HVD1787	A, B pins	–70 to 30	V
		'HVD1793	Y, Z pins	–70 to 30	V
Input voltage range at any logic pin			–0.3 to V _{CC} + 0.3	V	
Transient overvoltage pulse through 100 Ω per TIA-485			–100 to 100	V	
Receiver output current			–24 to 24	mA	
T _J	Junction temperature		170	°C	
Continuous total power dissipation			See Dissipation Rating Table		
IEC 60749-26 ESD (human-body model), bus terminals and GND			±16	kV	
JEDEC Standard 22, Test Method A114 (human-body model), bus terminals and GND			±16	kV	
JEDEC Standard 22, Test Method A114 (human-body model), all pins			±4	kV	
JEDEC Standard 22, Test Method C101 (charged-device model), all pins			±2	kV	
JEDEC Standard 22, Test Method A115 (machine model), all pins			±400	V	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE DISSIPATION RATINGS

PACKAGE	JEDEC THERMAL MODEL	T _A < 25°C RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 85°C RATING	T _A = 105°C RATING
SOIC (D) 8-pin	High-K	905 mW	7.25 mW/°C	470 mW	325 mW
	Low-K	516 mW	4.1 mW/°C	268 mW	186 mW
SOIC (D) 14-pin	High-K	1315 mW	10.5 mW/°C	684 mW	474 mW
	Low-K	744 mW	6 mW/°C	387 mW	268 mW
PDIP (P) 8-pin	High-K	2119 mW	16.9 mW/°C	1100 mW	763 mW
	Low-K	976 mW	7.8 mW/°C	508 mW	352 mW

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.5	5	5.5	V
V _I	Input voltage at any bus terminal (separately or common mode) ⁽¹⁾		–20		25	V
V _{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)		2		V _{CC}	V
V _{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)		0		0.8	V
V _{ID}	Differential input voltage		–25		25	V
I _O	Output current, driver		–60		60	mA
	Output current, receiver		–8		8	mA
R _L	Differential load resistance		54	60		Ω
C _L	Differential load capacitance			50		pF
1/t _{UI}	Signaling rate	HVD1785, HVD1791			115	kbps
		HVD1786, HVD1792			1	Mbps
		HVD1787, HVD1793			10	
T _A	Operating free-air temperature (see application section for thermal information)		–40		105	°C
T _J	Junction temperature		–40		150	°C

(1) By convention, the least positive (most negative) limit is designated as minimum in this data sheet.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
V _{OD}	Driver differential output voltage magnitude	RS-485 with common-mode load, V _{CC} > 4.75 V, see Figure 1	T _A ≤ 85°C	1.5			V	
			T _A ≤ 105°C	1.4				
		R _L = 54 Ω, 4.75 V ≤ V _{CC} ≤ 5.25 V	1.5	2				
		R _L = 100 Ω, 4.75 V ≤ V _{CC} ≤ 5.25 V	2	2.5				
Δ V _{OD}	Change in magnitude of driver differential output voltage	R _L = 54 Ω	-0.2	0	0.2	V		
V _{OC(SS)}	Steady-state common-mode output voltage		1	V _{CC} /2	3	V		
ΔV _{OC}	Change in differential driver output common-mode voltage		-100	0	100	mV		
V _{OC(PP)}	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω load resistors, See Figure 2		500		mV		
C _{OD}	Differential output capacitance			23		pF		
V _{IT+}	Positive-going receiver differential input voltage threshold			-100	-10	mV		
V _{IT-}	Negative-going receiver differential input voltage threshold	V _{CM} = -20 V to 25 V		-200	-150	mV		
V _{HYS}	Receiver differential input voltage threshold hysteresis (V _{IT+} - V _{IT-})			30	50	mV		
V _{OH}	Receiver high-level output voltage	I _{OH} = -8 mA		2.4	V _{CC} - 0.3		V	
		I _{OH} = -400 μA		4				
V _{OL}	Receiver low-level output voltage	I _{OL} = 8 mA	T _A ≤ 85°C		0.2	0.4	V	
			T _A ≤ 105°C		0.2	0.5		
I _I	Driver input, driver enable, and receiver enable input current			-100	100	μA		
I _{OZ}	Receiver output high-impedance current	V _O = 0 V or V _{CC} , RE at V _{CC}		-1	1	μA		
I _{OS}	Driver short-circuit output current			-250	250	mA		
I _I	Bus input current (disabled driver)	V _{CC} = 4.5 to 5.5 V or V _{CC} = 0 V, DE at 0 V	85, 86, 91, 92	V _I = 12 V		75	125	μA
				V _I = -7 V	-100	-40		
			87, 93	V _I = 12 V			500	
				V _I = -7 V	-400			
I _{CC}	Supply current (quiescent)		Driver and receiver enabled	DE = V _{CC} , RE = GND, no load		4	6	mA
			Driver enabled, receiver disabled	DE = V _{CC} , RE = V _{CC} , no load		3	5	
			Driver disabled, receiver enabled	DE = GND, RE = GND, no load		2	4	
			Driver and receiver disabled	DE = GND, D = open RE = V _{CC} , no load		0.5	5	μA
Supply current (dynamic)		See TYPICAL CHARACTERISTICS section						

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER (HVD1785 AND HVD1791)						
t_r, t_f	Driver differential output rise/fall time	$R_L = 54 \Omega, C_L = 50 \text{ pF}$, See Figure 3	0.4	1.7	2.6	μs
t_{PHL}, t_{PLH}	Driver propagation delay			0.8	2	μs
$t_{SK(P)}$	Driver differential output pulse skew, $ t_{PHL} - t_{PLH} $			20	250	ns
t_{PHZ}, t_{PLZ}	Driver disable time	Receiver enabled Receiver disabled	See Figure 4 and Figure 5	0.1	5	μs
t_{PZH}, t_{PZL}	Driver enable time			0.2	3	μs
				3	12	μs
DRIVER (HVD1786 AND HVD1792)						
t_r, t_f	Driver differential output rise/fall time	$R_L = 54 \Omega, C_L = 50 \text{ pF}$, See Figure 3	50		300	ns
t_{PHL}, t_{PLH}	Driver propagation delay				200	ns
$t_{SK(P)}$	Driver differential output pulse skew, $ t_{PHL} - t_{PLH} $				25	ns
t_{PHZ}, t_{PLZ}	Driver disable time	Receiver enabled Receiver disabled	See Figure 4 and Figure 5		3	μs
t_{PZH}, t_{PZL}	Driver enable time				300	10
		Receiver enabled	$V_{CM} > V_{CC}$	500		ns
DRIVER (HVD1787 AND HVD1793)						
t_r, t_f	Driver differential output rise/fall time	$R_L = 54 \Omega, C_L = 50 \text{ pF}$, See Figure 3	3		30	ns
t_{PHL}, t_{PLH}	Driver propagation delay				50	ns
$t_{SK(P)}$	Driver differential output pulse skew, $ t_{PHL} - t_{PLH} $				10	ns
t_{PHZ}, t_{PLZ}	Driver disable time	Receiver enabled Receiver disabled	See Figure 4 and Figure 5		3	μs
t_{PZH}, t_{PZL}	Driver enable time				300	9
		Receiver enabled	$V_{CM} > V_{CC}$	500		ns
RECEIVER (ALL DEVICES UNLESS OTHERWISE NOTED)						
t_r, t_f	Receiver output rise/fall time	$C_L = 15 \text{ pF}$, See Figure 6		4	15	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time		85, 86, 91, 92	100	200	ns
			87, 93		70	
$t_{SK(P)}$	Receiver output pulse skew, $ t_{PHL} - t_{PLH} $		85, 86, 91, 92	6	20	ns
		87, 93		5		
t_{PLZ}, t_{PHZ}	Receiver disable time	Driver enabled, See Figure 7		15	100	ns
$t_{PZL(1)}, t_{PZH(1)}$ $t_{PZL(2)}, t_{PZH(2)}$	Receiver enable time	Driver enabled, See Figure 7		80	300	ns
		Driver disabled, See Figure 8		3	9	μs

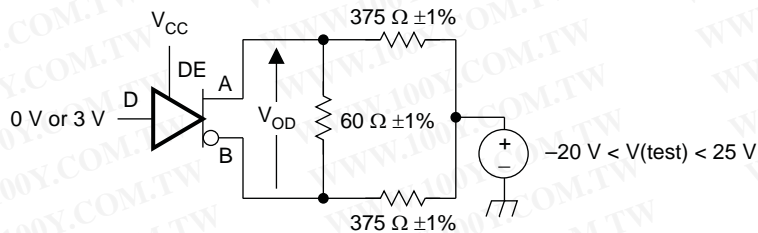
THERMAL INFORMATION

PARAMETER		TEST CONDITIONS	VALUE	UNIT	
R _{θJA}	Junction-to-ambient thermal resistance (no airflow)	SOIC-8	JEDEC high-K model	138	°C/W
			JEDEC low-K model	242	
	DIP-8	JEDEC high-K model	59		
		JEDEC low-K model	128		
	SOIC-14	JEDEC high-K model	95		
		JEDEC low-K model	168		
R _{θJB}	Junction-to-board thermal resistance	SOIC-8	62	°C/W	
		DIP-8	39		
		SOIC-14	40		
R _{θJC}	Junction-to-case thermal resistance	SOIC-8	61	°C/W	
		DIP-8	61		
		SOIC-14	44		
P _D	Power dissipation	85, 91	V _{CC} = 5.5 V, T _J = 150°C, R _L = 300 Ω, C _L = 50 pF (driver), C _L = 15 pF (receiver) 5-V supply, unterminated ⁽¹⁾	290	mW
		85, 91	V _{CC} = 5.5 V, T _J = 150°C, R _L = 100 Ω, C _L = 50 pF (driver), C _L = 15 pF (receiver) 5-V supply, RS-422 load ⁽¹⁾	320	
		86			
		87	V _{CC} = 5.5 V, T _J = 150°C, R _L = 54 Ω, C _L = 50 pF (driver), C _L = 15 pF (receiver) 5-V supply, RS-485 load ⁽¹⁾	400	
		85, 91			
		86			
87					
T _{SD}	Thermal-shutdown junction temperature		170	°C	

(1) Driver and receiver enabled, 50% duty cycle square-wave signal at signaling rate: HVD1785, 1791 at 115 kbps, HVD1786 at 1 Mbps, HVD1787 at 10 Mbps)

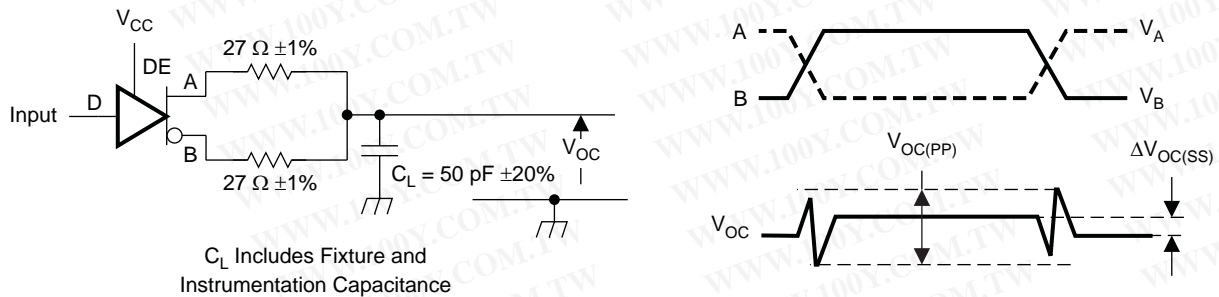
PARAMETER MEASUREMENT INFORMATION

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50 Ω.



S0301-01

Figure 1. Measurement of Driver Differential Output Voltage With Common-Mode Load



S0302-01

Figure 2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

PARAMETER MEASUREMENT INFORMATION (continued)

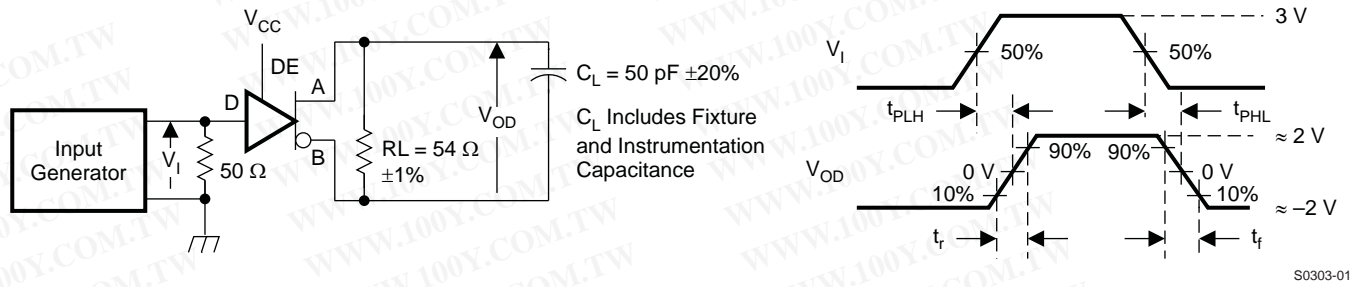
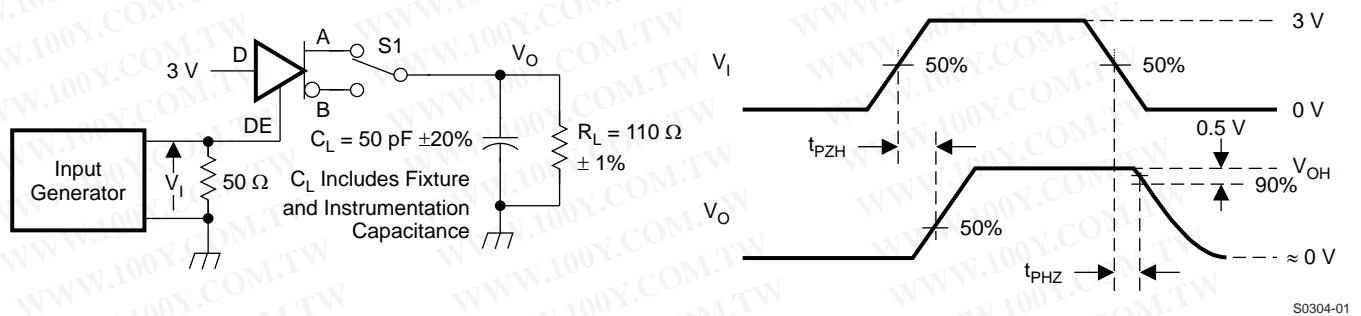
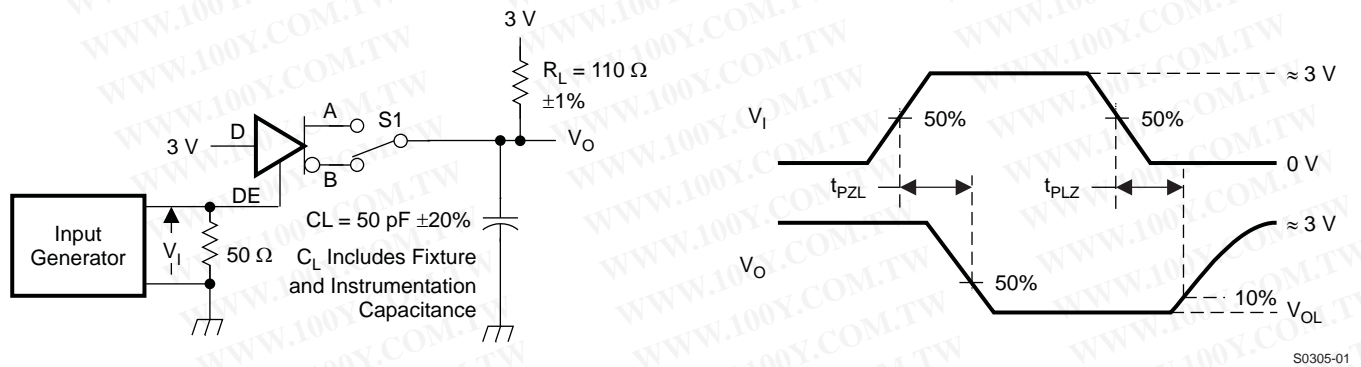


Figure 3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



NOTE: D at 3 V to test non-inverting output, D at 0 V to test inverting output.

Figure 4. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load



NOTE: D at 0 V to test non-inverting output, D at 3 V to test inverting output.

Figure 5. Measurement of Driver Enable and Disable Times With Active-Low Output and Pullup Load

PARAMETER MEASUREMENT INFORMATION (continued)

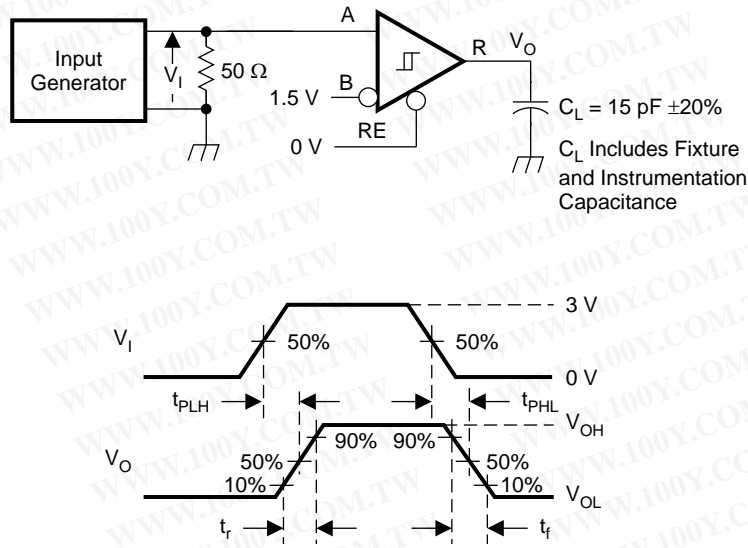


Figure 6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

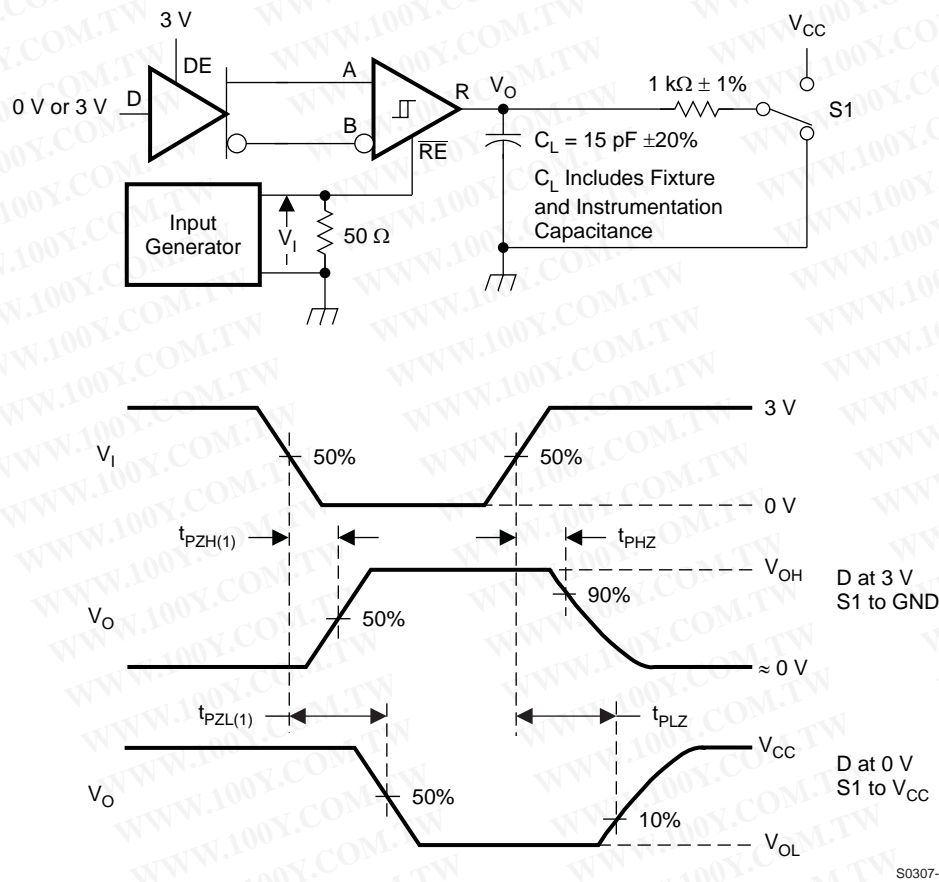


Figure 7. Measurement of Receiver Enable/Disable Times With Driver Enabled

PARAMETER MEASUREMENT INFORMATION (continued)

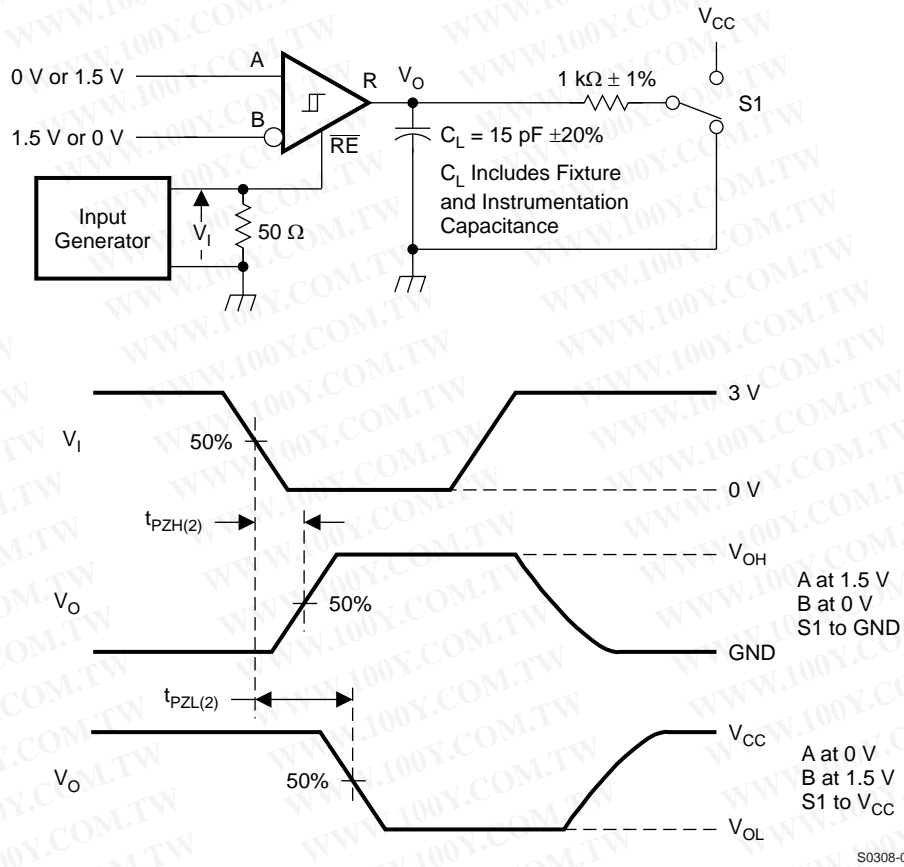


Figure 8. Measurement of Receiver Enable Times With Driver Disabled

TYPICAL CHARACTERISTICS

**DRIVER OUTPUT CURRENT
 vs
 SUPPLY VOLTAGE**

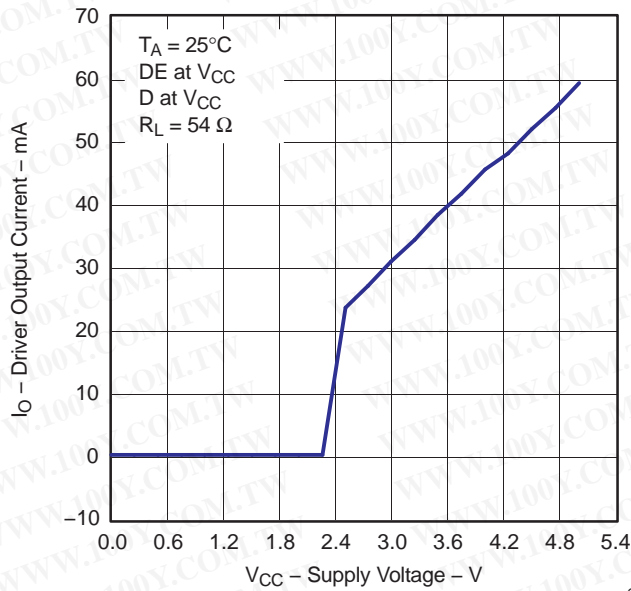


Figure 9.

**HVD1787 RMS SUPPLY CURRENT
 vs
 SIGNALING RATE**

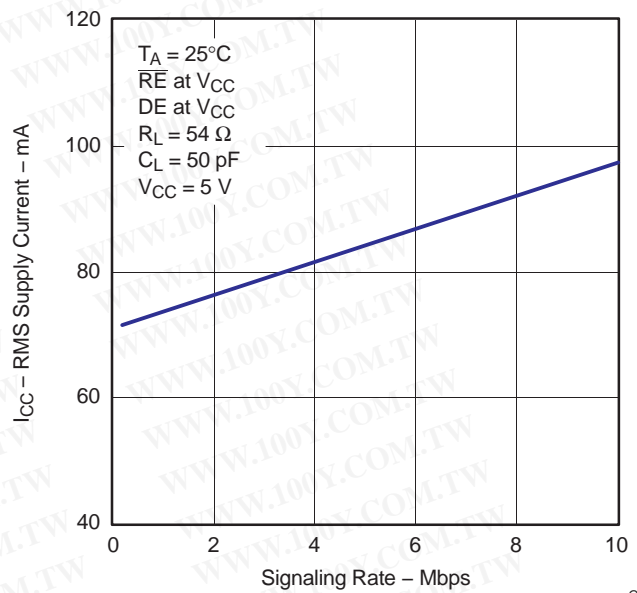


Figure 10.

**BUS PIN CURRENT
 vs
 BUS PIN VOLTAGE**

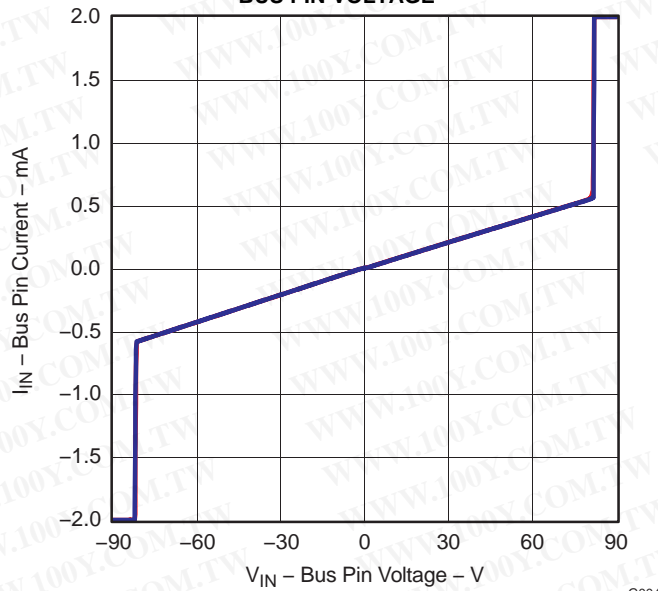


Figure 11.

TYPICAL CHARACTERISTICS (continued)

DIFFERENTIAL OUTPUT VOLTAGE
 VS
 DIFFERENTIAL LOAD CURRENT

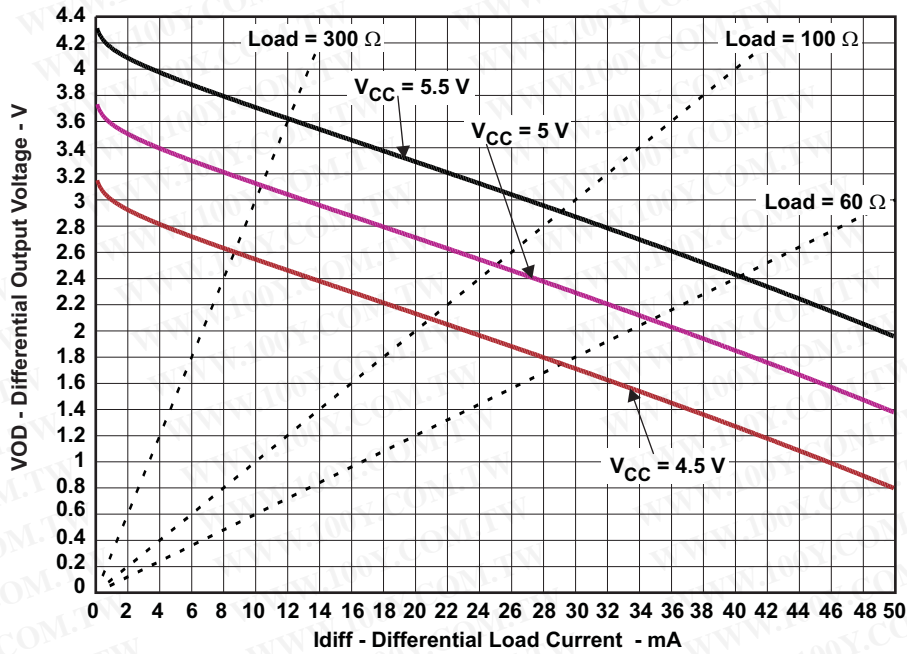


Figure 12.

ADDITIONAL OPTIONS

The SN65HVD17xx family also has options for J1708 applications, for always-enabled full-duplex versions (industry-standard SN65LBC179 footprint) and for inverting-polarity versions, which allow users to correct a reversal of the bus wires without re-wiring. Contact your local Texas Instruments representative for information on these options.

PART NUMBER	SN65HVD17xx		
	SLOW	MEDIUM	FAST
Half-duplex (176 pinout)	85	86	87
Full-duplex no enables (179 pinout)	88	89	90
Full-duplex with enables (180 pinout)	91	92	93
Half-duplex with cable invert	94	95	96
Full-duplex with cable invert and enables	97	98	99
J1708	08	09	10

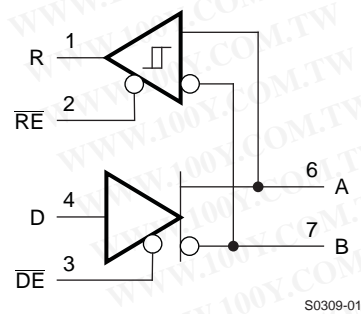
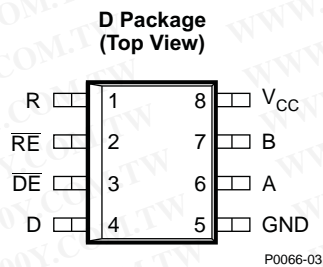


Figure 13. SN65HVD1708E Transceiver for J1708 Applications

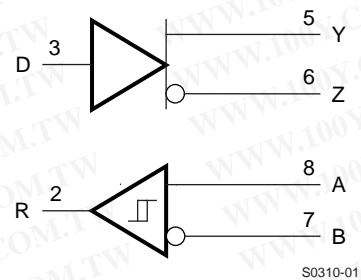
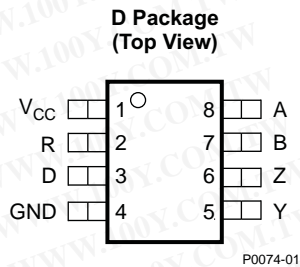


Figure 14. SN65HVD17xx Always-Enabled Driver Receiver

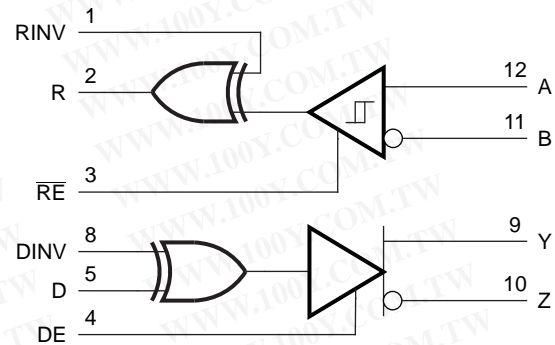
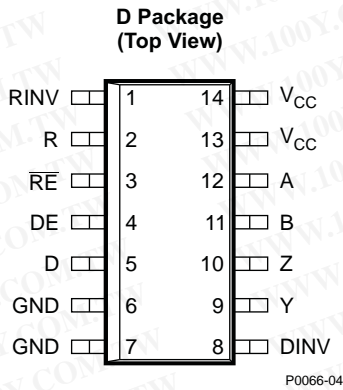
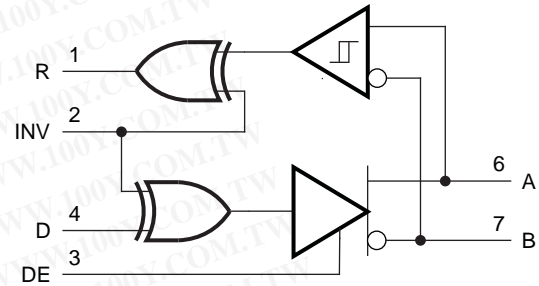
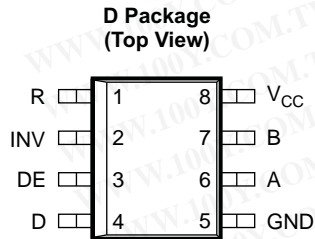


Figure 15. SN65HVD17xx Options With Inverting Feature to Correct for Miswired Cables

APPLICATION INFORMATION

Hot-Plugging

These devices are designed to operate in "hot swap" or "hot pluggable" applications. Key features for hot-pluggable applications are power-up, power-down glitch free operation, default disabled input/output pins, and receiver failsafe. As shown in Figure 9, an internal Power-On Reset circuit keeps the driver outputs in a high-impedance state until the supply voltage has reached a level at which the device will reliably operate. This ensures that no spurious transitions (glitches) will occur on the bus pin outputs as the power supply turns on or turns off.

As shown in the device **FUNCTION TABLE**, the *ENABLE* inputs have the feature of default disable on both the driver enable and receiver enable. This ensures that the device will neither drive the bus nor report data on the R pin until the associated controller actively drives the enable pins.

Receiver Failsafe

The differential receiver is “failsafe” to invalid bus states caused by:

- open bus conditions such as a disconnected connector,
- shorted bus conditions such as cable damage shorting the twisted-pair together,
- or idle bus conditions that occur when no driver on the bus is actively driving.

In any of these cases, the differential receiver outputs a failsafe logic High state, so that the output of the receiver is not indeterminate.

In the HVD17xx family of RS-485 devices, receiver failsafe is accomplished by offsetting the receiver thresholds so that the “input indeterminate” range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input V_{ID} is more positive than 200 mV, and must output a Low when the V_{ID} is more negative than -200 mV. The HVD17xx receiver parameters which determine the failsafe performance are V_{IT+} and V_{IT-} and V_{HYS} . In the *Electrical Characteristics* table, V_{IT-} has a typical value of -150 mV and a minimum (most negative) value of -200 mV, so differential signals more negative than -200 mV will always cause a Low receiver output. Similarly, differential signals more positive than 200 mV will always cause a High receiver output, because the typical value of V_{IT+} is -100mV, and V_{IT+} is never more positive than -10 mV under any conditions of temperature, supply voltage, or common-mode offset.

When the differential input signal is close to zero, it will still be above the V_{IT+} threshold, and the receiver output will be High. Only when the differential input is more negative than V_{IT-} will the receiver output transition to a Low state. So, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value V_{HYS} (the separation between V_{IT+} and V_{IT-}) as well as the value of V_{IT+} .

For the HVD17xx devices, the typical noise immunity is typically about 150 mV, which is the negative noise level needed to exceed the V_{IT-} threshold (V_{IT-} TYP = -150 mV). In the worst case, the failsafe noise immunity is never less than 40 mV, which is set by the maximum positive threshold (V_{IT+} MAX = -10mV) plus the minimum hysteresis voltage (V_{HYS} MIN = 30 mV).

70-V Fault-Protection

The SN65HVD17xx family of RS-485 devices is designed to survive bus pin faults up to $\pm 70V$. The devices designed for fast signaling rate (10 Mbps) will not survive a bus pin fault with a direct short to voltages above 30V when:

1. the device is powered on AND
 - 2a. the driver is enabled (DE=HIGH) AND D=HIGH AND the bus fault is applied to the A pin OR
 - 2b. the driver is enabled (DE=HIGH) AND D=LOW AND the bus fault is applied to the B pin

Under other conditions, the device will survive shorts to bus pin faults up to 70V. [Table 1](#) summarizes the conditions under which the device may be damaged, and the conditions under which the device will not be damaged.

Table 1. Device Conditions

POWER	DE	D	A	B	RESULTS
OFF	X	X	$-70V < V_A < 70V$	$-70V < V_B < 70V$	Device survives
ON	LO	X	$-70V < V_A < 70V$	$-70V < V_B < 70V$	Device survives
ON	HI	L	$-70V < V_A < 70V$	$-70V < V_B < 30V$	Device survives
ON	HI	L	$-70V < V_A < 70V$	$30V < V_B$	Damage may occur
ON	HI	H	$-70V < V_A < 30V$	$-70V < V_B < 30V$	Device survives
ON	HI	H	$30V < V_A$	$-70V < V_B < 30V$	Damage may occur

REVISION HISTORY

Changes from Original (January 2008) to Revision A	Page
• Changed Features Bullet From: Low Standby Supply Current, 2 μ A Max To: Low Standby Supply Current, 1 μ A Typ	1
• Deleted columns to the PRODUCT SELECTION GUIDE for Package Options and Status.	1
• Added text: For similar features with 3.3 V supply operation... ..	1
• Changed the Product Selection Guide Signaling Rate for SN65HVD1787 From 20 Mbps To: 10 Mbps	1
• Changed the Product Selection Guide Signaling Rate for SN65HVD1793 From 20 Mbps To: 10 Mbps	1
• Deleted The Competitive Comparison table.	2
• Added $ V_{OD} $ RS-485 with common-mode load $T_A \leq 85^\circ\text{C}$ and $T_A \leq 105^\circ\text{C}$	4
• Changed ΔV_{OC} From min = -0.2 mV and max 0.2 mV To: min = -100 mV and max 100 mV	4
• Changed HVD1785/1791 Driver differential output rise/fall time max value From 2.5 μ s To: 2.6 μ s.	5
• Changed HVD1787/1793 Driver differential output rise/fall time max value From 1.5 ns To: 30 ns.	5
• Changed Receiver propagation delay max value From 50 ns To: 70 ns.	5
• Changed t_{PLZ} , t_{PHZ} Receiver disable time From 3000 ns To 100 ns.	5
• Deleted graph DIFFERENTIAL OUTPUT VOLTAGE vs DIFFERENTIAL LOAD CURRENT.	10
Changes from Revision A (March 2008) to Revision B	Page
• Added $T_A \leq 85^\circ\text{C}$ and $T_A \leq 105^\circ\text{C}$ conditions and values to the Receiver low-level output voltage.	4
• Changed the max value for Supply Current (quiescent) Driver and receiver disabled, From 1 μ A To 5 μ A.	4
Changes from Revision B (March 2008) to Revision C	Page
• Changed Rec Op Table. Signaling rate, HVD1787, HVD1793 From: 20 Mbps max to 10 Mbps max.	3
Changes from Revision C (March 2008) to Revision D	Page
• Added Features Bullet: Power-Up, Power-Down Glitch-Free Operation	1
• Changed (Preview) to part number SN65HVD1791 in the Product Selection Guide	1
• Changed Receiver disabled by default - Enable from X to OPEN. Output from OPEN to Z	2
• Changed SN65HVD1791, 1792, 1793 pin out. Pin 11 from A to B, Pin 12 from B to A.	2
• Added section - APPLICATION INFORMATION	13
Changes from Revision D (June 2008) to Revision E	Page
• Changed - Removed Product Preview label	1
• Changed SN65HVD1792 Removed Product Preview label	1
• Changed SN65HVD1793 Removed Product Preview label	1
Changes from Revision E (July 2008) to Revision F	Page
• Added to Title: With Extended Common-Mode Range	1
• Added Receiver enabled $V_{CM} > V_{CC}$ condition and values to the Driver enabled time	5
• Added Figure 12	11

Changes from Revision F (November 2008) to Revision G	Page
• Added Notes for pin connections.	2
• Added $I_{OH} = -400 \mu A$ conditions and values to the Receiver high-level output voltage	4
• Added Receiver enabled $V_{CM} > V_{CC}$	5
• Added Receiver Failsafe information.	13
• Changed the Receiver Failsafe section	14

Changes from Revision G (April 2009) to Revision H	Page
• Deleted 70-V from the data sheet title	1
• Changed first Features Bullet From: Bus-Pin Fault Protection to $> \pm 70 V$ To: Bus-Pin Fault Protection to: $> \pm 70 V$ ('HVD1785, 86,91,92), $> \pm 30 V$ ('HVD1787, 93)	1
• Changed Voltage range at A and B inputs in the ABS MAX RATINGS table, adding separate conditions for the different devices	3
• Changed From: Voltage input range, transient pulse, A and B, through 100Ω To: Transient overvoltage pulse through 100Ω per TIA-485	3
• Changed Figure 14 From: PW Package (Top View) To: D Package (Top View)	12
• Added the 70-V Fault-Protection section	14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD1785D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1785	Samples
SN65HVD1785DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1785	Samples
SN65HVD1785DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1785	Samples
SN65HVD1785DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1785	Samples
SN65HVD1785P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 105	65HVD1785	Samples
SN65HVD1786D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1786	Samples
SN65HVD1786DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1786	Samples
SN65HVD1786DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1786	Samples
SN65HVD1786DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1786	Samples
SN65HVD1786P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 105	65HVD1786	Samples
SN65HVD1787D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1787	Samples
SN65HVD1787DG4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 105		Samples
SN65HVD1787DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1787	Samples
SN65HVD1787DRG4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 105		Samples
SN65HVD1787P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 105	65HVD1787	Samples
SN65HVD1791D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1791	Samples
SN65HVD1791DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1791	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD1791DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1791	Samples
SN65HVD1791DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1791	Samples
SN65HVD1792D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1792	Samples
SN65HVD1792DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1792	Samples
SN65HVD1793D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1793	Samples
SN65HVD1793DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1793	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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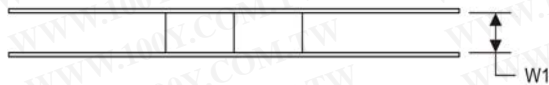
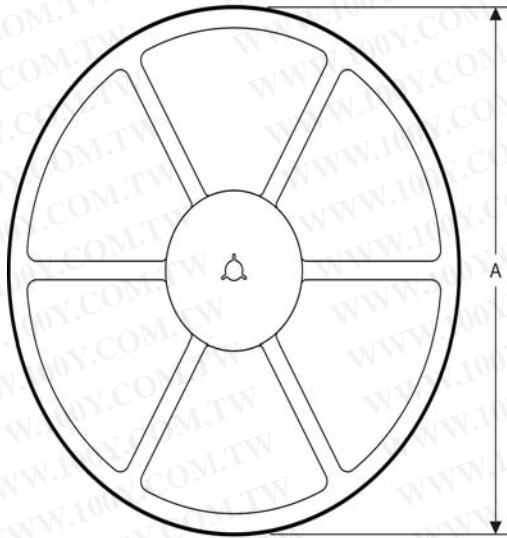
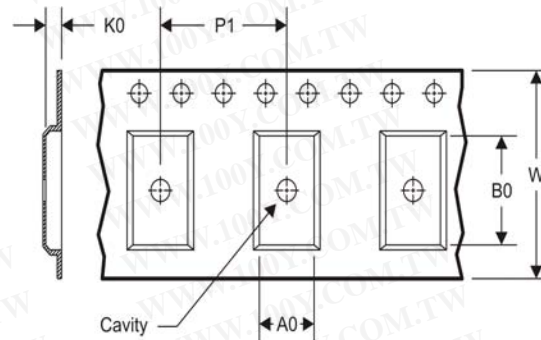
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OTHER QUALIFIED VERSIONS OF SN65HVD1792 :

- Enhanced Product: [SN65HVD1792-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

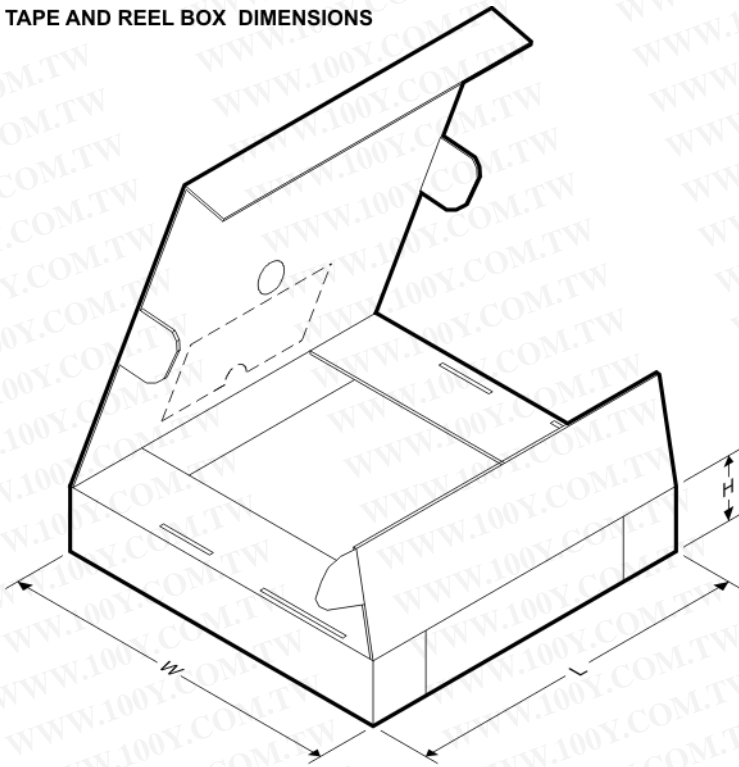
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1785DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD1786DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD1787DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD1791DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65HVD1792DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65HVD1793DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

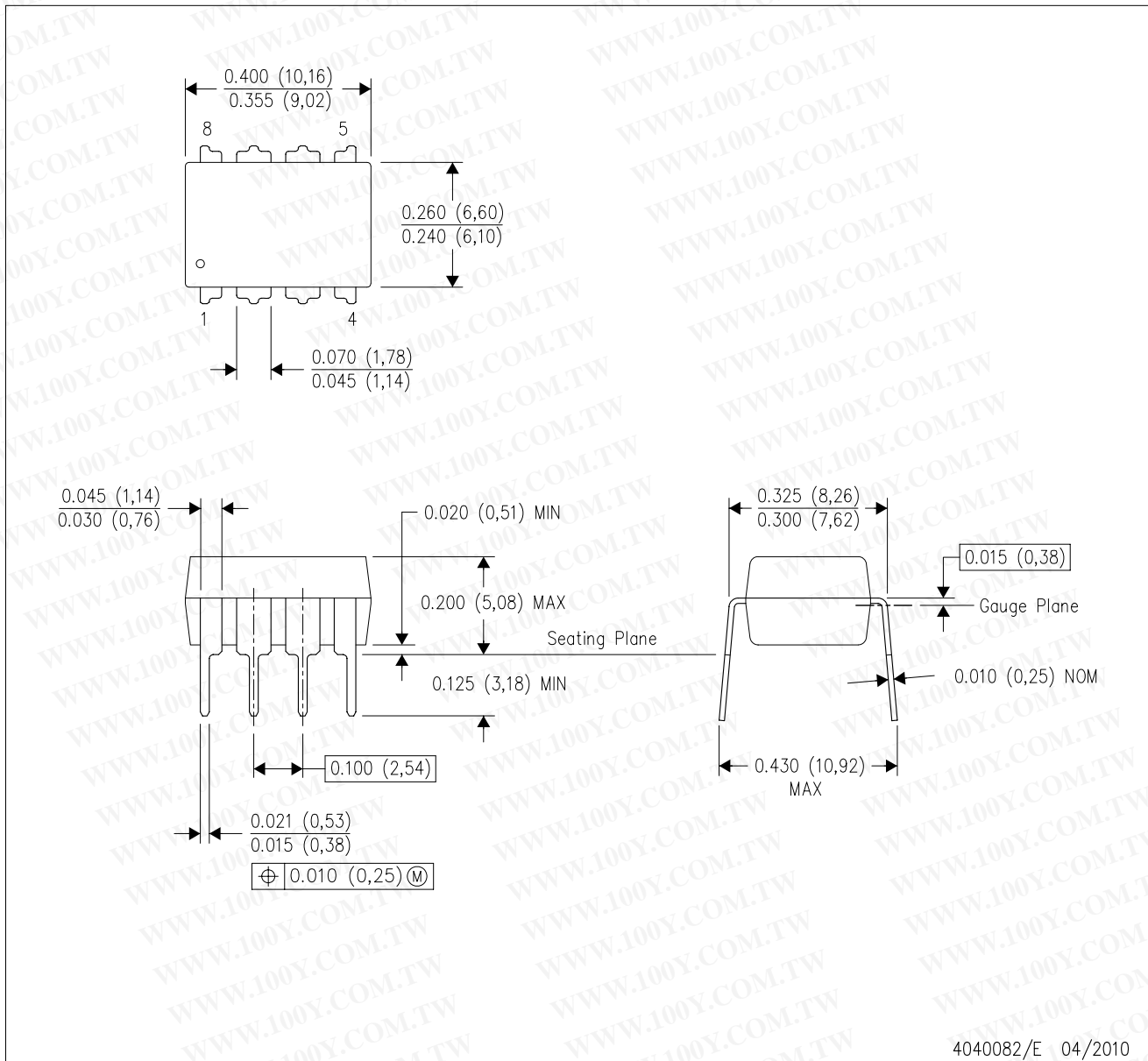
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1785DR	SOIC	D	8	2500	367.0	367.0	35.0
SN65HVD1786DR	SOIC	D	8	2500	367.0	367.0	35.0
SN65HVD1787DR	SOIC	D	8	2500	367.0	367.0	35.0
SN65HVD1791DR	SOIC	D	14	2500	367.0	367.0	38.0
SN65HVD1792DR	SOIC	D	14	2500	367.0	367.0	38.0
SN65HVD1793DR	SOIC	D	14	2500	367.0	367.0	38.0

P (R-PDIP-T8)

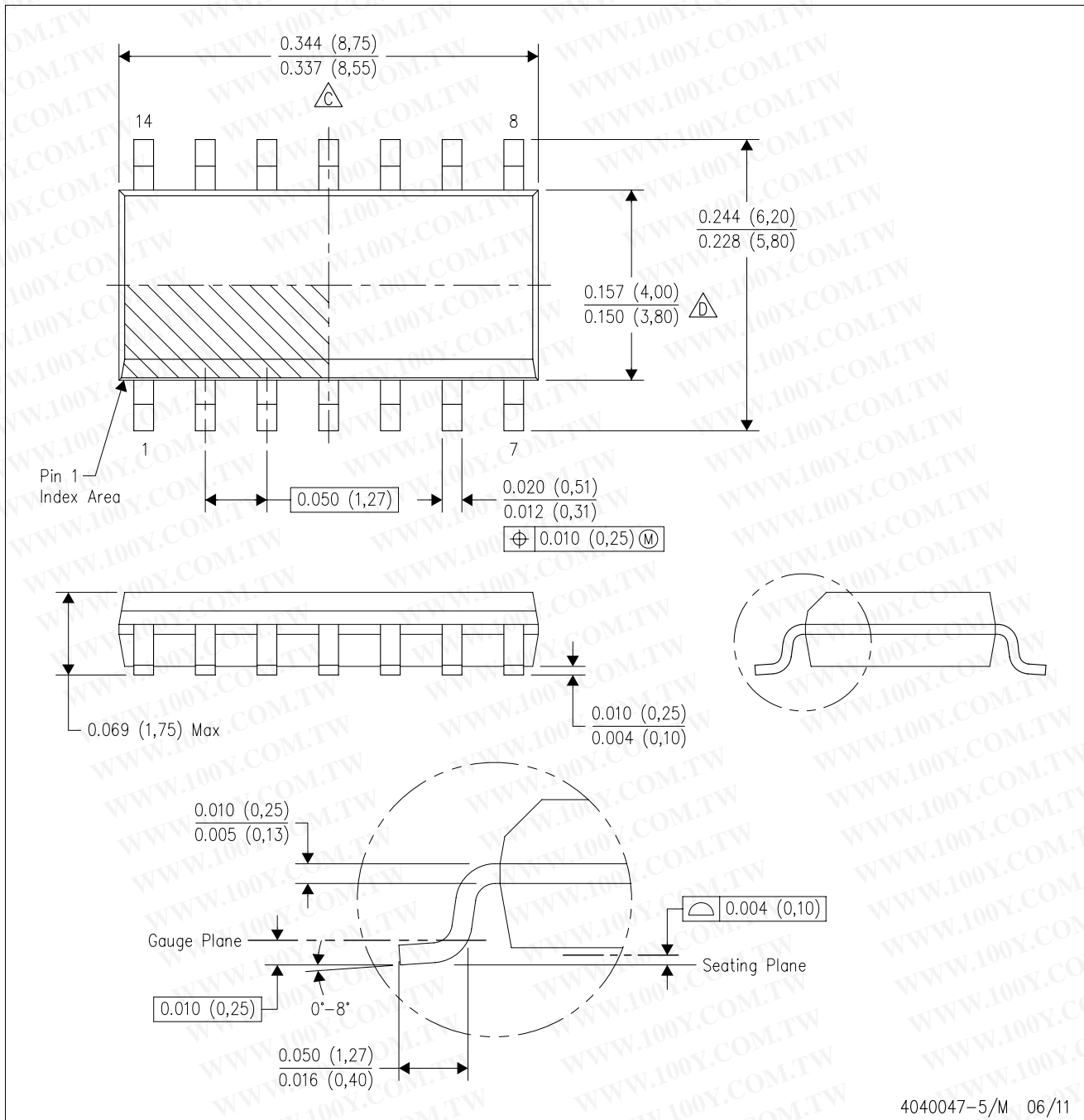
PLASTIC DUAL-IN-LINE PACKAGE



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D (R-PDSO-G14)

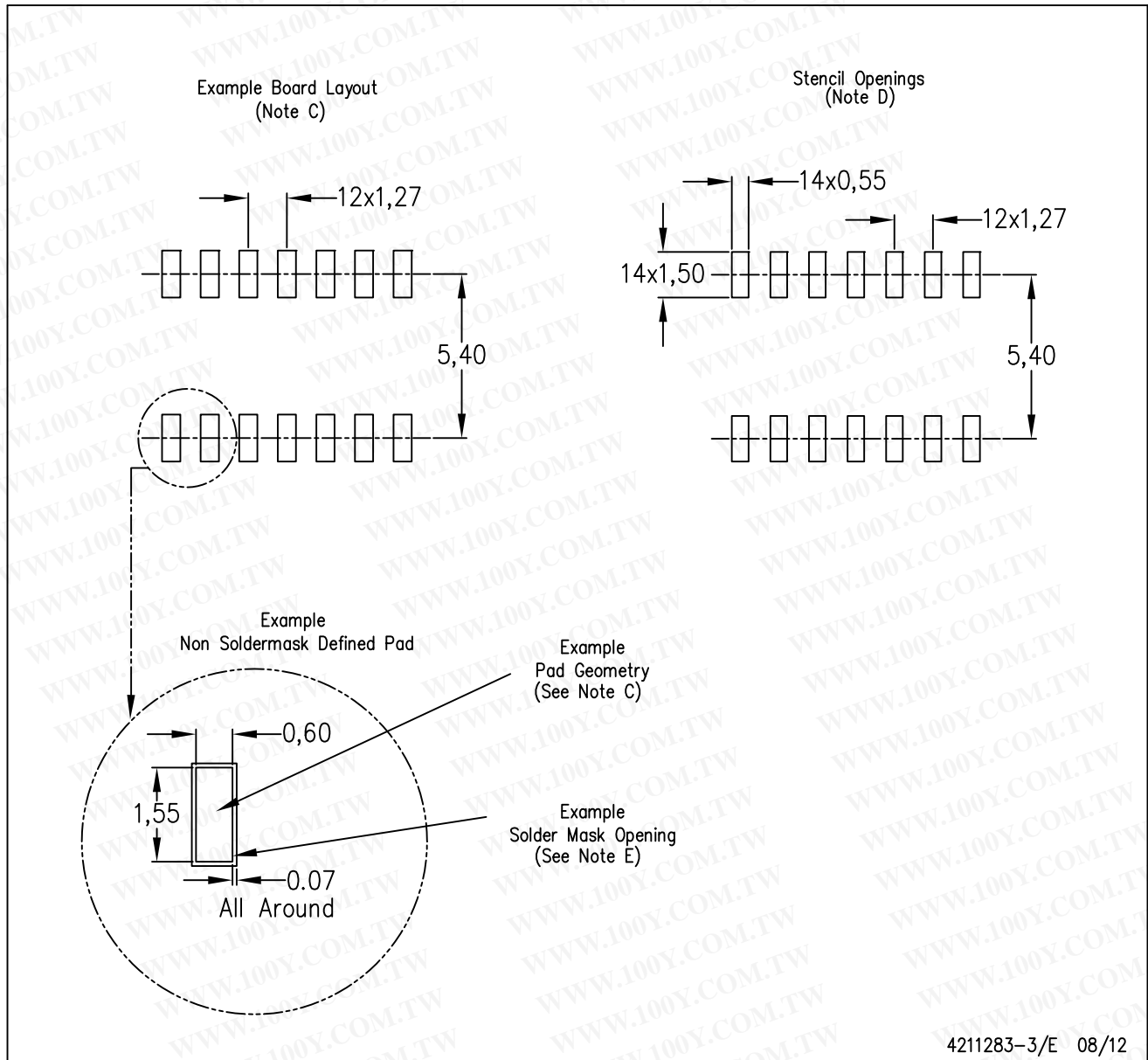
PLASTIC SMALL OUTLINE



- NOTES:
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 - (C) Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - (D) Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

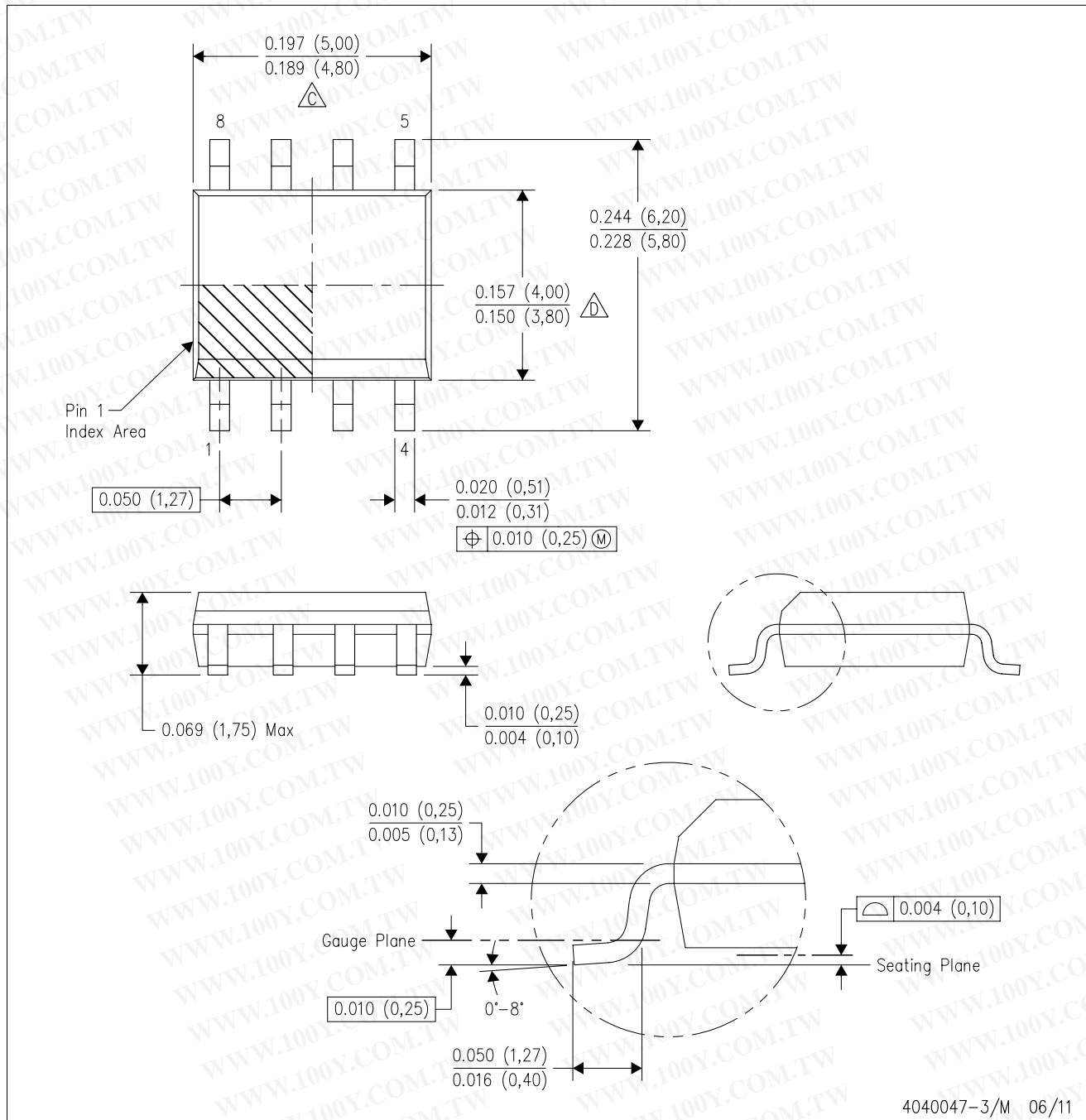


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 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

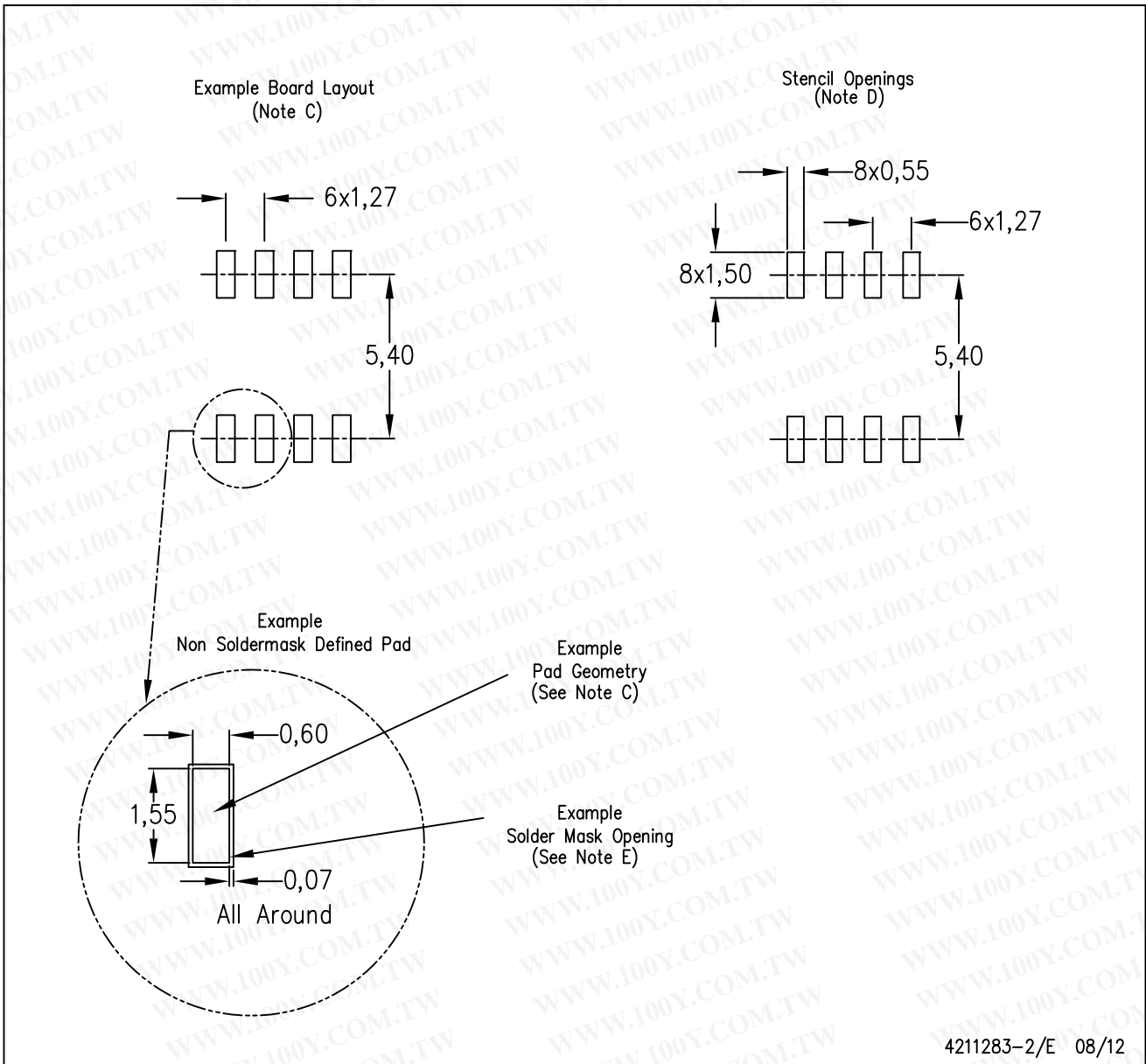
PLASTIC SMALL OUTLINE



- NOTES:
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 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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