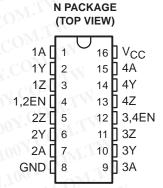
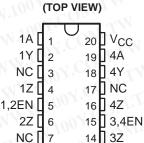
- Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B and RS-485
- **High-Speed Advanced Low-Power Schottky** Circuitry
- Designed for up to 20-Mbit/s Operation in **Both Serial and Parallel Applications**
- **Designed for Multipoint Transmission on** Long Bus Lines in Noisy Environments
- **Low Supply Current Requirements** 55 mA Max
- Wide Positive and Negative Input/Output **Bus Voltage Ranges**
- Driver Output Capacity . . . ±60 mA
- Thermal-Shutdown Protection
- **Driver Positive- and Negative-Current** Limiting
- **Functionally Interchangeable With SN75174**

description

The SN75ALS174A is a quadruple line driver with 3-state differential outputs. It is designed to meet requirements of ANSI Standards EIA/TIA-422-B and RS-485. This device is optimized for balanced multipoint bus transmission at rates of up to 20 Mbit/s. Each driver features wide positive and negative common-mode output voltage ranges that make them suitable for party-line applications in noisy environments.





13 NC

11 3A

12 3Y

DW PACKAGE

NC - No internal connection

2Y 🛮

2A

GND L

The SN75ALS174A provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C.

The SN75ALS174A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each driver)

INPUT	ENABLES	OUT	PUTS
Α	ENABLES	Y	Z
Н	Н	H 1	00 F.
L	H W	L	H
X	L «	Z	Z

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

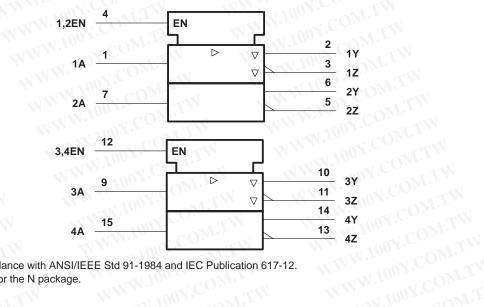
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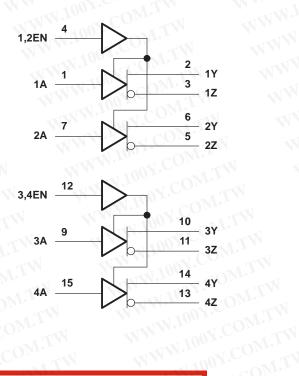
logic symbol† W.100Y.COM.TW



WWW.100Y.COM. †This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the N package.

logic diagram (positive logic)

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Pin numbers shown are for the N package.

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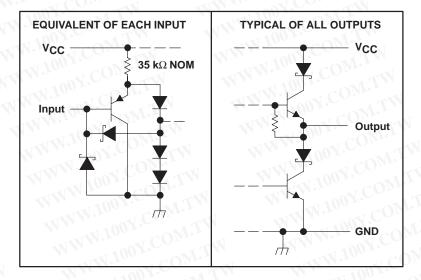


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SN75ALS174A QUADRUPLE DIFFERENTIAL LINE DRIVER

SLLS122E - JULY 1991 - REVISED APRIL 1998

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage, V _I	
Output voltage range, V _O	
Continuous total dissipation	See Dissipation Rating Table
Storage temperature range, T _{Stq}	—65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25^{\circ}C$ POWER RATING	DERATING FACTOR	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

MAN'IL CA'COM.	MAIN W. TAN	MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}	MAN. TO STORY	4.75	5	5.25	VC
High-level input voltage, VIH	M. 100 COM: 1.	2		1.11	V
Low-level input voltage, V _{IL}	WW. TIOOY.		W.	0.8	V
Common-mode output voltage, VOC	WWW.100Y.COM.T	N	W	12 -7	100
High-level output current, IOH	W. 1001.			-60	mA
Low-level output current, IOL	MM 100X.CO	IN		60	mA
Operating free-air temperature, TA	N. W. CO.	0		70	°C
MMM.100X.COM.1	M MAM. 100 X.COV	VTV		W	MM



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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

O_{Mrr}	PARAMETER	TEST CO	ONDITIONS	MIN	TYP [†]	MAX	UNIT
VIK	Input clamp voltage	I _I = -18 mA	TANN TOO TO)NI.		-1.5	V
Vo	Output voltage	IO = 0	W. 1001.	0	4	6	V
V _{OD1}	Differential output voltage	I _O = 0	MM. 1001.6	1.5		6	V
IV _{OD2} I	Differential output voltage	R _L = 100 Ω	See Figure 1	1/2V _{OD1} or 2‡	N		V
M.CO	TW WW 1005	$R_L = 54 \Omega$	1/1/1/1005	1.5	2.5	5	
V _{OD3}	Differential output voltage	See Note 2	WWW	1.5	W	5	V
Δ V _{OD}	Change in magnitude of differential output voltage§	$R_L = 54 \Omega \text{ or } 100 \Omega,$	See Figure 1	M.COM	I.TW	±0.2	V
Voc	Common-mode output voltage¶	$R_L = 54 \Omega \text{ or } 100 \Omega,$	See Figure 1	100 X CC	M.TV	3 -1	V
Δ V _{OC}	Change in magnitude of common-mode output voltage§	$R_L = 54 \Omega \text{ or } 100 \Omega,$	See Figure 1	100 Y.C	$O_{M',r}$	±0.2	V
lo	Output current with power off	$V_{CC} = 0$,	$V_0 = -7 \text{ V to } 12 \text{ V}$	N. COV.	COn	±100	μΑ
loz	High-impedance-state output current	$V_0 = -7 \text{ V to } 12 \text{ V}$		W.Inc	CO_{M_1}	±100	μΑ
lін	High-level input current	V _I = 2.7 V	I.M.	100		20	μΑ
ĮΣ	Low-level input current	V _I = 0.4 V	W	100	V.C.	-100	μΑ
los	Short-circuit output current	$V_0 = -7 \text{ V to } 12 \text{ V}$	W. W.	MW.	N.Ct	±250	mA
1	Cumply assurant (all drivers)	No load	Outputs enabled	M.In	36	55	A
ICC	Supply current (all drivers)	No load	Outputs disabled	VI TIN 1	16	30	mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^{\circ}\text{C}$.

NOTE 2: See EIA Standard RS-485, Figure 3-5, Test Termination Measurement 2.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 pF$

	PARAMETER	TEST C	ONDITIONS	MIN	TYP [†]	MAX	UNIT
td(OD)	Differential output delay time	$R_L = 54 \Omega$,	See Figure 2	9	15	22	ns
^t PZH	Output enable time to high level	$R_L = 110 \Omega$,	See Figure 3	30	45	70	ns
tPZL	Output enable time to low level	$R_L = 110 \Omega$,	See Figure 4	25	40	65	ns
t _{PHZ}	Output disable time from high level	$R_L = 110 \Omega$,	See Figure 3	10	20	35	ns
t _{PLZ}	Output disable time from low level	$R_L = 110 \Omega$,	See Figure 4	10	30	45	ns

WWW.100Y.COM.TW [†] All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^{\circ}\text{C}$.

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[‡] The minimum V_{OD2} with a 100- Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.

^{§ ∆|}V_{OD}| and ∆|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

[¶] In ANSI Standard EIA/TIA-422-B, VOC, which is the average of the two output voltages with respect to ground, is called output offset voltage, Vos.

PARAMETER MEASUREMENT INFORMATION

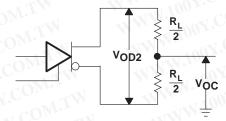
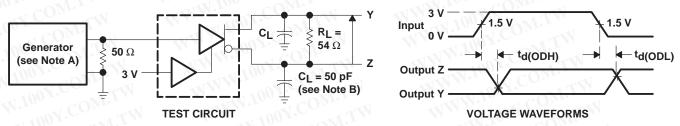
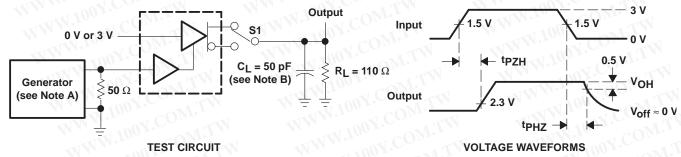


Figure 1. Differential and Common-Mode Output Voltages



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, $Z_0 = 50 \Omega$, duty cycle = 50%, $t_f \le 5$ ns, $t_r \le 5$ ns.
 - B. CL includes probe and stray capacitance.

Figure 2. Differential-Output Test Circuit and Delay and Transition Times Voltage Waveforms

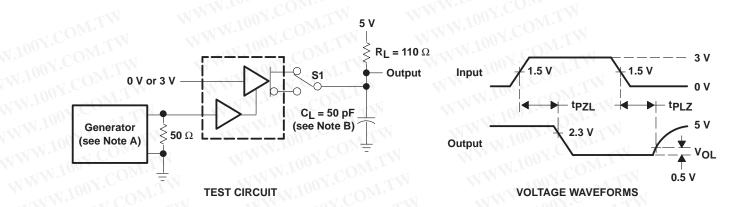


- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, $Z_O = 50 \Omega$, duty cycle = 50%, $t_f \le 5$ ns.
 - B. C_L includes probe and stray capacitance.

Figure 3. Test Circuit and Voltage Waveforms, tpzH and tpHZ

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PR = 1 MHz, $Z_O = 50 \Omega$, duty cycle = 50%, $t_f \le 5 \text{ ns}$, $t_r \le 5 \text{ ns.}$

B. C_L includes probe and stray capacitance.

Figure 4. Test Circuit and Voltage Waveforms, tpzL and tpLZ

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PACKAGE OPTION ADDENDUM



10-May-2007

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins I	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp (3)
SN75ALS174ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS174ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS174ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS174ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS174ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS174ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS174AN	ACTIVE	PDIP	Y. N X COM	16	25	Pb-Free (RoHS)	CU NIPD	N / A for Pkg Type
SN75ALS174ANE4	ACTIVE	PDIP	NO	16	25	Pb-Free (RoHS)	CU NIPD	N / A for Pkg Type

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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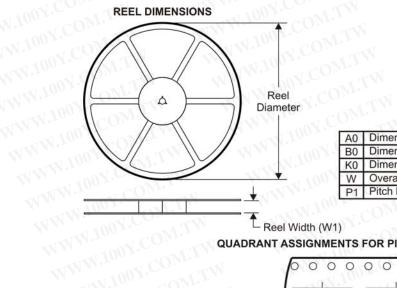
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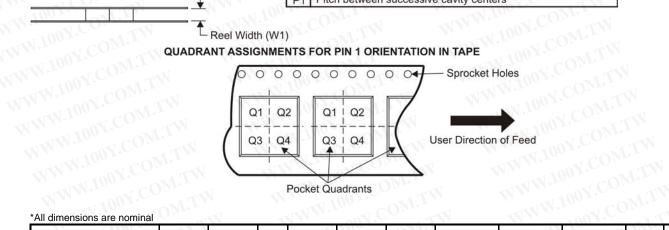


TAPE AND REEL INFORMATION



TAPE DIMENSIONS → K0 ←P1→ 0 $\Phi \Phi \Phi \Phi$ 0 Φ 0 0 B₀ → A0 ← Cavity -

		Dimension designed to accommodate the component width
Ŋ	B0	Dimension designed to accommodate the component length
7		Dimension designed to accommodate the component thickness
¥	W	Overall width of the carrier tape
	P1	Pitch between successive cavity centers



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dimensions are nomina Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadran
SN75ALS174ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.1	2.65	12.0	24.0	Q1

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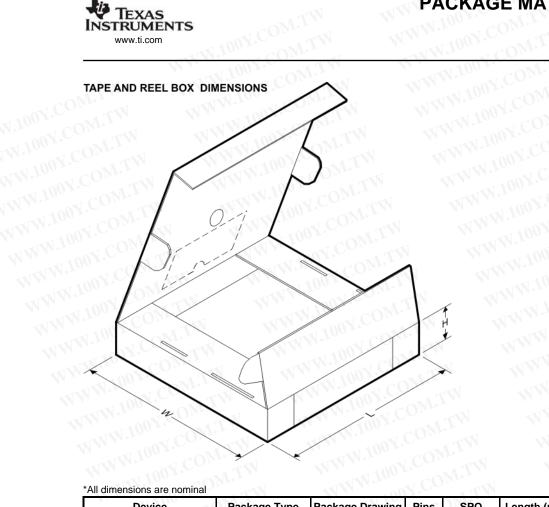
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*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
N75ALS174ADWR	SOIC	DW	20	2000	346.0	346.0	41.0

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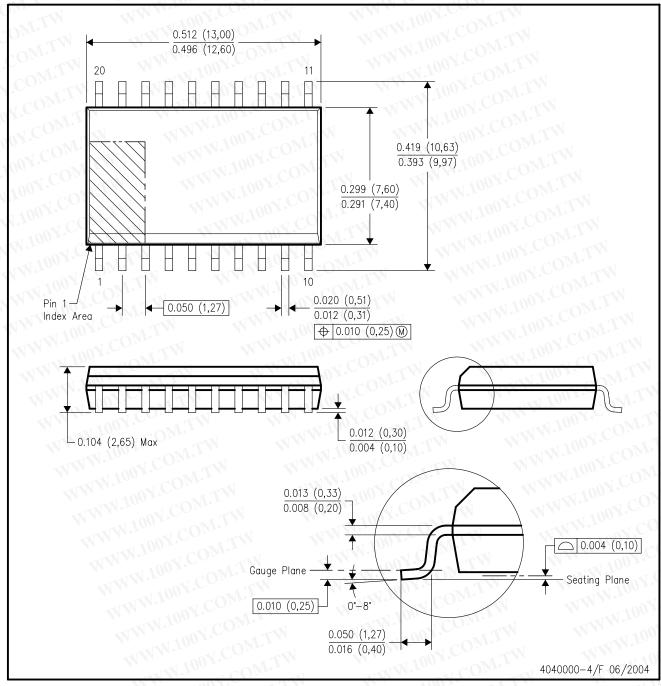
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DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A.

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.

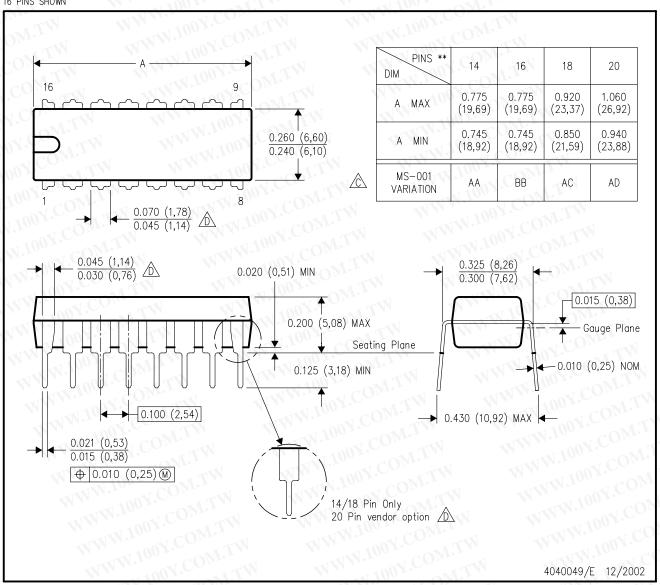


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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- ⚠ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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