TC358768AXBG

Functional Specification

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HISTORY

Revision	Date	Note
Rev 0.1	02/24/2012	Initial Release 1. Command parameters increases to ~1KB 2. Modify bit 0x0004[6] to turn on/off Parallel port properly with register 0x0032[15:14] 3. Remove PClk toggle requirement when RefClk is used 4. No need to toggle RefClk to get out of reset 5. Add register bit 0x0032[0] to control Hsync Polarity 6. Update Revision ID to 0x01
Rev 0.2	04/19/2012	1. Rename Register 0x00E0 and its fields to reflect the meaning better 2. Section 3.6.3 modified to add step #12 for commands > 8 parameters 3. Update Figure 4-3, removing toggling requirement 4. Correct register 0x0030 typo to 0x0032 5. Update section 3.7.3 for proper stopping/starting parallel video stream sequence to prevent 768A from hanging 6. Replace TC358768 with TC358768A
Rev 0.3	07/01/2012	1. Typo Correction 2. Update Register 0x00E0 field description 3. Long Command steps updated 4. Remove bit 0x0002[1], sleep bit 5. Update Registers 0x0140 – 0x0150 6. Update Table 5-1 to indicate registers' addressability 7. Remove Tentative

REFERENCES

1. MIPI DSI, "mipi_DSI_specification_v01-02-00, June 28, 2010"
2. MIPI DCS “DRAFT mipi_DCS_specification_v01-02-00_r0-02, December 2008”
3. MIPI D-PHY, “mipi_D-PHY_specification_v01-00-00, May 14, 2009"
4. I2C bus specification, version 2.1, January 2000, Philips Semiconductor

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1 Overview

The Parallel Port to MIPI DSI (TC358768AXBG) is a bridge device that converts RGB to DSI. All internal registers can be access through I2C or SPI. .

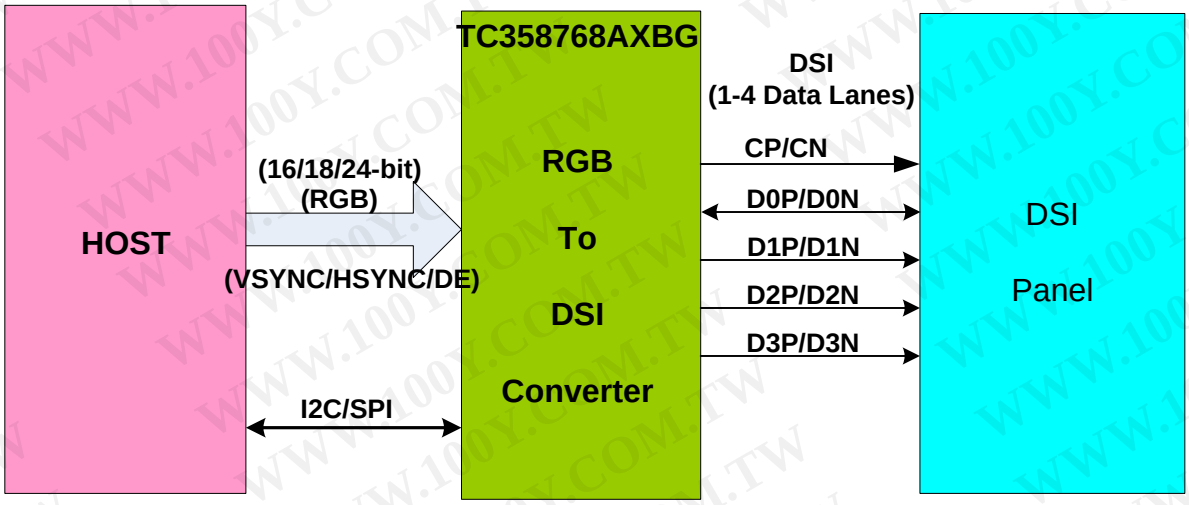


Figure 1-1 System Overview with TC358768AXBG in RGB to DSI-TX

2 Features

Below are the main features supported by TC358768AXBG.

DSI-TX Interface

- ✧ MIPI DSI compliant (Version 1.02.00 – June 28, 2010)
  - Support DSI Video Mode data transfer
  - DCS Command for panel register access
- ✧ Supports up to 1 Gbps per data lane
- ✧ Supports 1,2,3 or 4 data lanes
- ✧ Supports video data formats
  - RGB888/666/565

RGB Interface

- ✧ Supports data formats
  - ➢ 24-bit data bus
    - ✧ RGB888/666/565 data formats
- ✧ Up to 166 MHz input clock
- ✧ Support VSYNC/HSYNC polarity option (default LOW)
- ✧ Support DE polarity option (default High)

I2C/SPI Slave Interface (Option to select either I2C or SPI interface)

- ✧ I2C Interface (when CS=L)
  - Support for normal (100KHz), fast mode (400 KHz) and Special mode (1 MHz)
  - Configure all TC358768AXBG internal registers
  - Writing to DCS registers will trigger DCS Command transmits over DSI
- ✧ SPI interface (when CS =H)
  - SPI interface support for up to 25 MHz operation.
  - Configure all TC358768AXBG internal registers
  - Writing to DCS registers will trigger DCS Command transmits over DSI

GPIO signals

- ✧ 2 GPIO signals
  - Two GPIO signals can be configured as SPI signals (SPI_SS and SPI_MISO)
  - Or One GPIO signal can be configured as Interrupt output signal (INT).

System

- ✧ Clock and power management support to achieve low power states.

Power supply inputs

- ✧ Core and MIPI D-PHY: 1.2V
- ✧ I/O: 1.8V – 3.3V

Power Consumption

- ✧ 720P @60fps: Pixel Clk: 74.25 MHz, DSIClk: 219.6 MHz ➔ 52.4 mW
- ✧ 1080P @60fps: Pixel Clk: 148.5 MHz, DSIClk: 471.6 MHz ➔ 91.3 mW

3 External Pins

TC358768AXBG resides in BGA72 pin packages. The following table gives the signals of TC358768AXBG and their function.

Table 3-1 TC358768AXBG Functional Signal List

Group	Pin Name	I/O	Type	Initial	Function	Note
System: Reset & Clock (4)	RESX	I	Sch	-	System reset input, active low	
	REFCLK	I	N	-	Reference clock input (6MHz – 40MHz)	
	MSEL	I	N	-	Mode Select 1'b0: Test mode 1'b1: Normal mode	
	CS	I	N	-	Configuration Select - When CS=L, enable I2C interface - When CS=H, enable SPI interface	
MIPI-DSI (10)	MIPI_CP		PHY		MIPI-DSI clock positive	
	MIPI_CN		PHY		MIPI-DSI clock negative	
	MIPI_D0P		PHY		MIPI-DSI Data 0 positive	
	MIPI_D0N		PHY		MIPI-DSI Data 0 negative	
	MIPI_D1P		PHY		MIPI-DSI Data 1 positive	
	MIPI_D1N		PHY		MIPI-DSI Data 1 negative	
	MIPI_D2P		PHY		MIPI-DSI Data 2 positive	
	MIPI_D2N		PHY		MIPI-DSI Data 2 negative	
	MIPI_D3P		PHY		MIPI-DSI Data 3 positive	
	MIPI_D3N		PHY		MIPI-DSI Data 3 negative	
I2C (2)	I2C_SCL	OD	Sch		I2C serial clock or SPI_SCLK	4mA
	I2C_SDA	OD	Sch		I2C serial data or SPI_MOSI	4mA
Parallel Port (28)	PD[23:0]	I	N		Parallel Port Input Data Note: PD[23:16] can be config to be GPIO[10:3]	
	VSYNC	I	N		Parallel port VSYNC signal	
	HSYNC	I	N		Parallel port HSYNC signal	
	DE	I	N		Parallel Port DE signal	
	PCLK	I	N		Parallel Port Clock signal	
GPIOx (2)	GPIO[2:1]	I/O	N		GPIO[2:1] signals - (GPIO[1] option to become SPI_SS or INT signal) - (GPIO[2] option to become SPI_MISO signal)	4mA
POWER (9)	VDDC (1.2V)	NA			VDD for Internal Core (3)	
	VDDIO (1.8V – 3.3V)	NA			VDDIO is for IO power supply (4)	
	VDD_MIPI (1.2V)	NA			VDD for the MIPI (2)	
Ground (17)	VSS	NA			Ground	

3.1 TC358768AXBG BGA72 Pin Count Summary

Table 3-2 BGA72 Pin Count Summary

Group Name	Pin Count	Notes
SYSTEM	4	
DSI IF	10	
I2C	2	
GPIOx	2	
Parallel Port IF	28	
POWER	9	IO, MIPI and Core Power
GROUND	17	
TOTAL	**72**	

3.2 Pin Layout

A1	**A2**	**A3**	**A4**	**A5**	**A6**	**A7**	**A8**	**A9**
VSS	PD17	PD19	PD21	PD23	GPIO2	I2C_SCL	MSEL	VSS
B1	**B2**	**B3**	**B4**	**B5**	**B6**	**B7**	**B8**	**B9**
VDDC	PD16	PD18	PD20	PD22	GPIO1	I2C_SDA	RESX	VDDIO
C1	**C2**	**C3**	**C4**	**C5**	**C6**	**C7**	**C8**	**C9**
PD15	PD14	VSS	VSS	VSS	VSS	VDD_MIPI	MIPI_D3P	MIPI_D3N
D1	**D2**	**D3**				**D7**	**D8**	**D9**
PD13	PD12	VSS				VSS	MIPI_D2P	MIPI_D2N
E1	**E2**	**E3**				**E7**	**E8**	**E9**
VSS	VSS	VDDC				VDD_MIPI	MIPI_CP	MIPI_CN
F1	**F2**	**F3**				**F7**	**F8**	**F9**
VSS	VSS	VSS				VSS	MIPI_D1P	MIPI_D1N
G1	**G2**	**G3**	**G4**	**G5**	**G6**	**G7**	**G8**	**G9**
PD11	PD10	VDDIO	VSS	VSS	VDDIO	VDDIO	MIPI_D0P	MIPI_D0N
H1	**H2**	**H3**	**H4**	**H5**	**H6**	**H7**	**H8**	**H9**
VDDC	PD8	PD6	PD4	PD2	PD0	PCLK	DE	CS
J1	**J2**	**J3**	**J4**	**J5**	**J6**	**J7**	**J8**	**J9**
VSS	PD9	PD7	PD5	PD3	PD1	REFCLK	VSYNC	HSYNC

Figure 3-1 TC358768AXBG 72-Pin Layout

3.3 System Overview

TC358768AXBG received the data/controls from RGB then transmits them out to MIPI DSI TX. Host uses I2C/SPI interface to configure all TC358768AXBG internal registers.

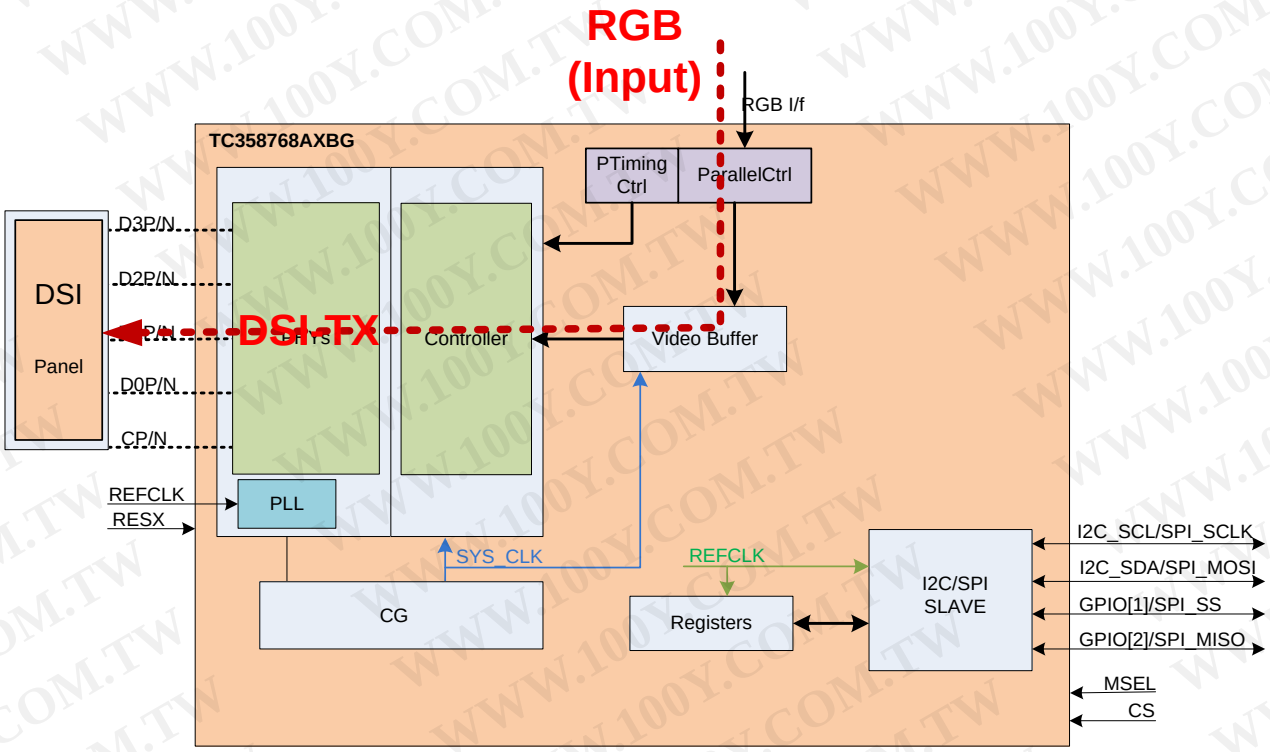


Figure 3-2 TC358768AXBG Data/Controls Flow in RGB to DSI-TX

3.4 DSI TX Protocol

Table below shows all the data types that supported in TC358768AXBG.

Table 3-3 Supports Data Types

Data Type	Description	Packet Size
0x01	Sync Event, V Sync Start	Short
0x11	Sync Event, V Sync End	Short
0x21	Sync Event, H Sync Start	Short
0x31	Sync Event, H Sync End	Short
0x08	End of Transmission packet (EoTp)	Short
0x02	Color Mode (CM) Off Command	Short
0x12	Color Mode (CM) On Command	Short
0x22	Shut Down Peripheral Command	Short
0x32	Turn On Peripheral Command	Short
0x03	Generic Short WRITE, no parameters	Short
0x13	Generic Short WRITE, 1 parameter	Short
0x23	Generic Short WRITE, 2 parameters	Short
0x04	Generic READ, no parameters	Short
0x14	Generic READ, 1 parameter	Short
0x24	Generic READ, 2 parameters	Short
0x05	DCS Short WRITE, no parameters	Short
0x15	DCS Short WRITE, 1 parameter	Short
0x06	DCS READ, no parameters	Short
0x37	Set Maximum Return Packet Size	Short
0x29	Generic Long Write (Max 8 byte for register access)	Long
0x39	DCS Long Write (Max 8 byte for register access)	Long
0x0E	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
0x1E	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x2E	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x3E	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long

3.4.1 Video Mode Transmission

In Video mode, TC358768AXBG transmits all video timing events and pixel data in proper sequence and time. Video timing events are transmitted in these DSI short packets: VSYNC Start, VSYNC End, HSYNC Start, and HSYNC End. They are multiplexed with null (or blank) packets (or transitioned to LP idle cycle) and pixel data packets in the DSI serial link such that their reception at the chip will reflect in signal transition on VSYNC and HSYNC at proper timing for the receiving display panel. Pixel data is expected to be transmitted using Pixel Stream packet types (Data Type ID = 0x0E, 0x1E, 0x2E or 0x3E.).

VSYNC Start, VSYNC End, HSYNC Start and HSYNC End are trigger by RGB VSYNC and HSYNC pulse. Refer to Figure 3-6 for more information.

Video Line byte count must be configs into Word Count Register 1 (WordCnt1) before starting transfer video over RGB.

3.4.2 Pixel Format

The chip supports RGB-565, RGB-666 packed or loose, and RGB-888 pixel formats in video data packets.

In video mode transmission, pixel format is differentiated by the data type ID in the header of pixel stream packets received. Data type ID must be configured into DSITX_DT register before starting video transmission.

3.5 DSI TX Video Packet Operation

Below describes the TC358768AXBG sequence for transmit out the video data onto DSI TX.

1) Configures all registers.
2) Enable Parallel Input port.
3) Detects VSYNC transition
    a. If detect VSYNC transition from HIGH to LOW. Transmits VSYNC Start packet.
    b. Detect HSYNC pulse (generate Hsync Start, Hsync End packets accordingly)
    c. If detect VSYNC transition from LOW to HIGH. Transmits VSYNC End packet. Go to step “4”
4) Detect HSYNC pulse (generate Hsync Start, Hsync End packets accordingly). Once detect DE transition from LOW to HIGH then go to step “5”.
5) Wait for the Video buffer reaches the programmable “FIFO Level” go to step “6”
6) Transmits Video packet (one line) then go to step “7”
7) Detects HSYNC pulse (generate Hsync Start, Hsync End packets accordingly). If detect DE transition from LOW to HIGH then go to step “5”
    a. If detect VSYNC transition from HIGH to LOW. Transmits VSYNC Start packet, go to step “3”

Note: Assume VSYNC/HSYNC are active LOW.

3.6 DSI TX Command Packet Operation

Below describes the TC358768AXBG sequence for transmitting out DSI, including DCS, Command over DSI TX. Host can use either I2C or SPI interface to access to TC358768AXBG registers.

By programming the following registers, TC358768AXBG will generate/transmit DSI command packets. ECC and CRC are generated and attached automatically by the hardware.

- DSICMD_TX (Register 0x0600)
  - Contains DSI Command Packet Start Transmit bit.
- DSICMD_TYPE (Register 0x0602)
  - Contains DSI (short or long) CommandPacket Type
  - Contains DSI Packet Data ID
- DSICMD_WC (Register 0x0604)
  - Contains DSI Command Packet Word Count
- DSICMD_WD0, DSICMD_WD1, DSICMD_WD2, DSICMD_WD3 (0x0610 – 0x0616)
  - Contains DSI Command Packet Data Bytes (total 8 bytes)

3.6.1 TX Short Packet (DCS) Write Command

The relationship/assembly of a short DSI packet respect to the DSICMD_** registers are illustrated in Figure 3-3. The command code, either DCS command or Panel specific command, is stored in Data Byte 0 while Data Byte1 contains either command parameter or “0x00”.

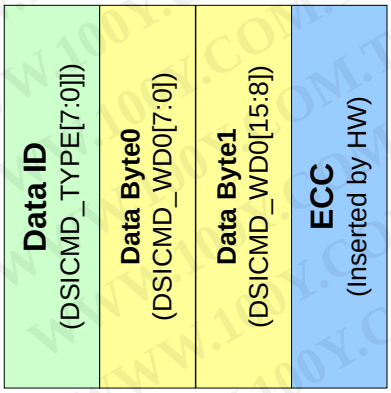


Figure 3-3 DSI Short Command Packet Assembly

The step-by-step procedure is listed below with two examples:

1 Set register DSICMD_TYPE[PkType] = 0x10 for DSI short packet.

2 Choose desired DCS Short Write Command in register DSICMD_TYPE[DATA_ID] = 0x05 or 0x15 for DCS Command without parameter or with 1 parameter, respectively.

3 Be sure to set 0x0000 in DSICMD_WC register.

4 Program DCS command code (as specified in MIPI DCS Command Spec in DSICMD_WD0[7:0].

5 If DSICMD_TYPE[DATA_ID] = 0x15, set DCS Command Parameter in DSICMD_WD0[15:8]. Otherwise set “0x00” in DSICMD_WD0[15:8].

6 Set DSICMD_TX = 0x01 to start DCS Write Short packet.

Example1: TX DCS Short Command: Exit_Sleep_Mode (0x11), no parameter

0x0602 = 0x1005 (Short packet, Data ID = 0x05)
0x0604 = 0x0000 (WC1,WC0=0 for DSC short write)
0x0610 = 0x0011 (Data1= 0,DCS Command)
0x0600 = 0x0001 (Start transfer)

Example2: TX DCS Short Command: Set_Pixel_Format (0x3A), 1 parameter (RGB888)

0x0602 = 0x1015 (Short packet, Data ID = 0x15)
0x0604 = 0x0000 (WC1,WC0=0 for DSC short write)
0x0610 = 0x703A (RGB888,DCS Command)
0x0600 = 0x0001 (Start transfer)

3.6.2 TX Long Packet Write Command (limited to 8-byte in length)

The relationship/assembly of a long DSI packet respect to the DSICMD_** registers are illustrated in Figure 3-4. The command code, either DCS command or Panel specific command, is stored in Data Byte 0 while Data Byte1 to Data 7contains either command parameters. The maximum word count for DSI Long Command is limited to 8 bytes. For a single byte command code, the maximum parameters length can be 7 bytes.

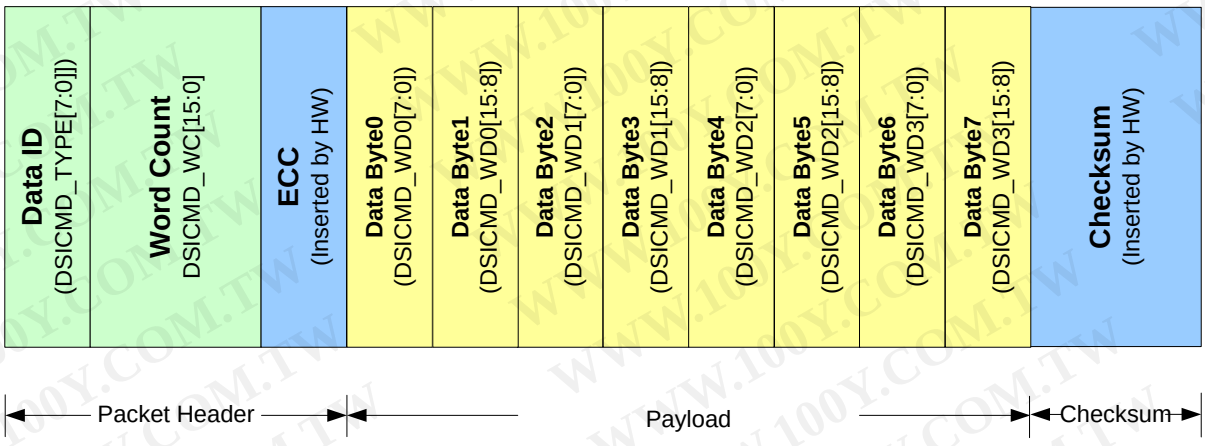


Figure 3-4 DSI Long Command Packet Assembly

The step-by-step procedure is listed below with an examples:

1 Set register DSICMD_TYPE[PkType] = 0x40 for DSI long packet.
2 Choose desired DSI Long Write Packet/Command, ex, 0x19 for Generate Long Write Packet, in register DSICMD_TYPE[DATA_ID] field.
3 Set DSICMD_WC register to the correct word count, number of data bytes in the packet.
4 Fill update to 8-bytes of data in registers DSICMD_WD0, 1, 2 & 3 in sequence.
5 For DCS Long Write Command, the command code should be set at register DSICMD_WD0[7:0].
6 Set DSICMD_TX = 0x01 to start DCS Write Short packet.

Example: TX Generic Long Write Packet with 4 bytes of Data: 0x12, 0x34, 0x56, 0x78

0x0602 = 0x4029 (DSI Long Command/Packet, Data ID = 0x29)
0x0604 = 0x0004 (WC1,WC0)
0x0610 = 0x3412 (Data1,Data0)
0x0612 = 0x7856 (Data3,data2)
0x0600 = 0x0001 (Start transfer)

3.6.3 TX Long Packet Write Command (Up to 1024-byte in length)

In order to support user defined DCS commands, which require more than 7 bytes of parameters. TC358768A provides a method to use its video buffer to store the command and its parameters before sending out via DSI link.

- Since video buffer is used to store the command and its parameters, these long commands can only be issued when there is no video data being transferred.
- Please make sure the number of “command plus parameters” are in multiple of 4-byte, padding with “0x00” at the end to achieve this requirement.

The step-by-step procedure is listed below with an examples:

1 0x0008 = 0x0001 (Use DataID specified in register 0x0050)
2 0x0050 = 0x0039 (DataID = 0x39)
3 0x026C = 0x000a (10 bytes, 1-byte command + 9-byte param, to be sent)
4 0x00e0 = 0x8000 (Enable Write into video buffer via I2C/SPI bus)
5 0x00e8 = 0x00d5 (Command = 0xd5, 1st param = 0x00)
6 0x00e8 = 0x7666 (2nd param = 0x66, 3rd param = 0x76)
7 0x00e8 = 0x0204 (4th param = 0x04, 5th param = 0x02)

8 0x00e8 = 0x4202 (6th param = 0x02, 7th param = 0x42)

9 0x00e8 = 0x0302 (8th param = 0x02, 9th param = 0x03)

10 0x00e8 = 0x0000 (Padding to make 12 bytes total)

11 0x00e0 = 0xE000 (Start DSI Tx command transfer)

(wait for Command finishes by estimating the number of bytes to be transferred)

12 0x00e0 = 0x2000 (Keep Mask High to prevent short packets send out)

13 0x00e0 = 0x0000 (Stop DSI Tx command transfer)

3.6.4 TX (Short) Packet Read Command

All the DSI Read packet are short packets. After issuing any read command, TC358768A will automatically performs bus turn around and the data returned will be stored in register DSICMD_RDFIFO for Application Processor to read. DSICMD_RDFIFO is a 32 x 8 FIFO, which means TC35768 can accept up to 32 byte of data per DSI Read command. TC35768 is expected to send DSI "Set Maximum Return Packet Size" short packet (Data ID = 0x37) to the DSI Rx to indicate how many bytes it needs to read in the following read command(s). The sequence are:

1 Inform DSI Rx the desired bytes to read by sending "Maximum Return Packet Size" short packet

0x0602 = 0x1037 (Short packet, Data ID = 0x37)
0x0604 = 0x0000 (WC1,WC0=0 for Short Packet)
0x0610 = 0x0008 (Read 8-byte of Data, 2 parameters)
0x0600 = 0x0001 (Start transfer)

2 Issue a DCS Read Command get_power_mode (0x0A)

0x0602 = 0x1006 (Short packet, Data ID = 0x06, DCS Read, no parameter)
0x0604 = 0x0000 (WC1,WC0=0 for DSC Short Packet)
0x0610 = 0x000A (Data1, DCS Command)
0x0600 = 0x0001 (Start transfer)

3 TC35768 performs Bus Turn Around (BTA) automatically to let DSI Rx to send one byte of data.

a. The received data will be pushed into DSICMD_RDFIFO (0x0430), where Host can read the data from

b. Host can monitor registers bit RDFIFO_STATUS[5] when asserted data arrived.

c. Host needs to track the data which is read into DSICMD_RDFIFO if multiple read commands were issued before it fetch the data.

TC358768A does not extract data out of each LP packets received from DSIRx, a whole packet is stored into DSICMD_RXFIFO, packed into 32-bit boundary as shown in Figure 3-5 below. It is up to the Host to fetch and interpret the data.

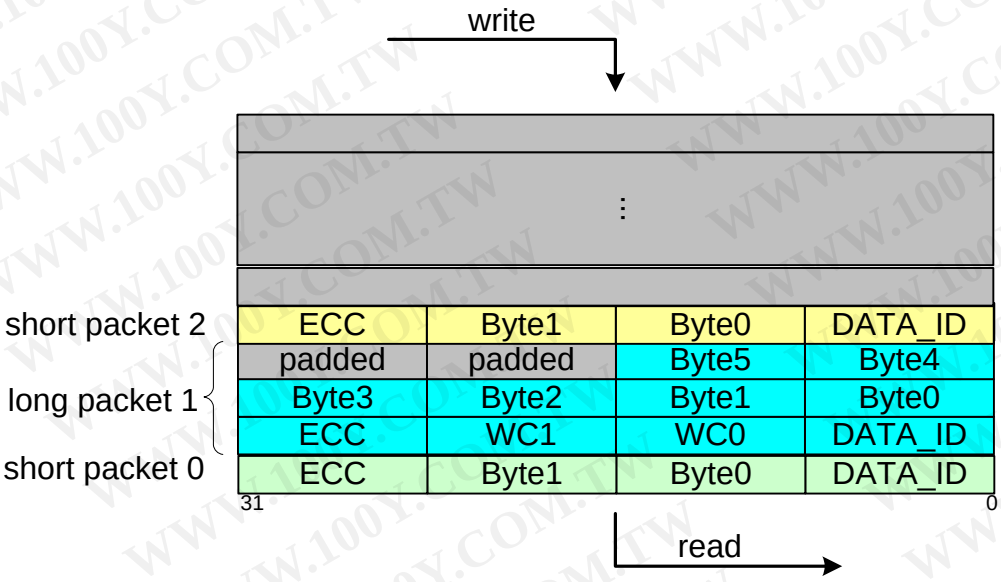


Figure 3-5 DSICMD_RXFIFO Data Arrangement

3.7 Parallel Input (RGB)

3.7.1 Overview

24-bit parallel input interface is capable to transfer various types of data formats (RGB888/666/565). The signal connections for these types are shown in below Table.

Table 3-4 24-bit Unpacked Data bus

Data Type	Mode	Pin Usage	
		PD[23:0]	Comment
RGB888	0	{R[7:0],G[7:0],B[7:0]}	1 pixel/PClk
RGB888	1	{R[1:0]G[1:0],B[1:0],R[7:2],G[7:2],B[7:2]}	1 pixel/PClk
RGB666	0	{2'b0,R[5:0],2'b0,G[5:0],2'b0,B[5:0]}	1 pixel/PClk
RGB666	1	{6'b0,R[5:0],G[5:0],B[5:0]}	1 pixel/PClk
RGB565	0	{2'b0,R[4:0],3'b0,G[5:0],2'b0,B[4:0],1'b0}	1 pixel/PClk
RGB565	1	{3'b0,R[4:0],2'b0,G[5:0],3'b0,B[4:0]}	1 pixel/PClk
RGB565	2	{8'b0,R[4:0],G[5:0],B[4:0]}	1 pixel/PClk

The Parallel Input controller received the video data from external RGB transmitter. It then packed these into 32-bit data format then transfers the packed data into the Video buffer. The 32-bit data format is showed in Table 3-5.

Parallel Input controller is operated with PCLK only. All asynchronous logic is handled inside Video buffer Controller

3.7.2 Timing Diagrams for Video signals (Vsync and Hsync)

Below Figures show the timing relationship between HSYNC, VSYNC, DE and DSI-TX. Please note the leading edge of first Hsync is expected to lineup with that of VSync's.

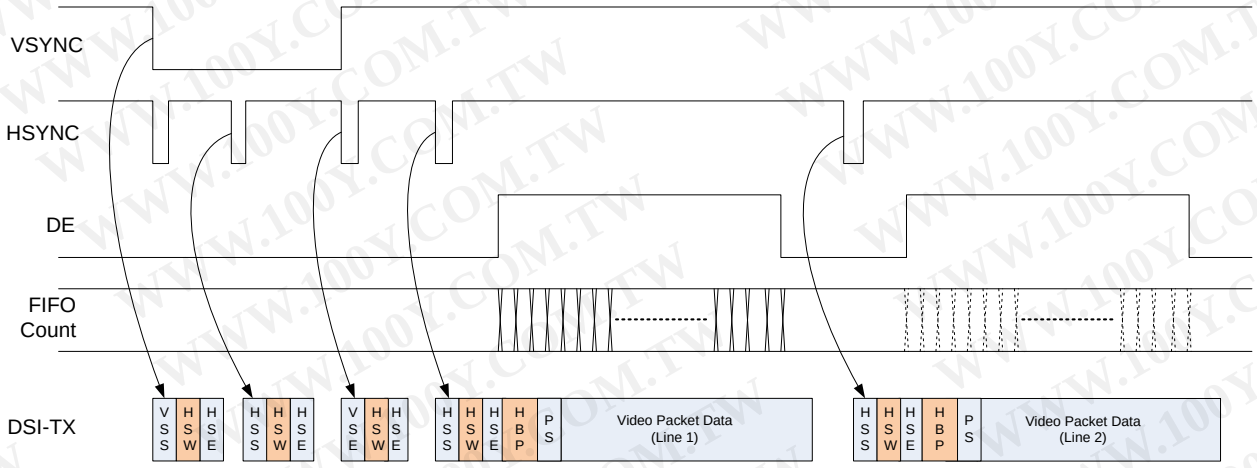


Figure 3-6 VSYNC/HSYNC/DE Timing Diagram – Pulse mode

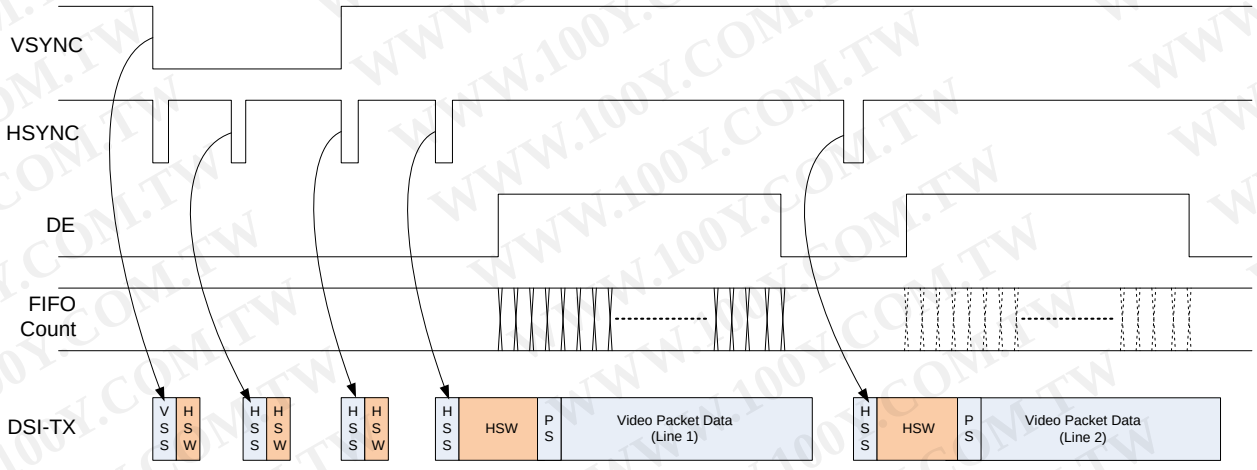


Figure 3-7 VSYNC/HSYNC/DE Timing Diagram – Event mode

3.7.3 Enable and Disable Parallel Input (Video)

While TC358768A is running, the following procedures need to perform in order to stop and re-start video operation without reset. Otherwise, TC358768A might be hung, which needs to be reset.

Three registers bits, 0x0032[15] (FrmStop), 0x0032[14] (RstPtr) and 0x0004[6] (PP_En) needs to be programmed sequentially.

To stop TC358768A (video):

1 Set FrmStop to 1'b1, wait for at least one frame time for TC358768A to stop properly
2 Clear PP_En to 1'b0
3 Set RstPtr to 1'b1
4 Stop Video to TC358768A (optional)

To re-start TC358768A (video):

1 Start Video to TC358768A
2 Clear RstPtr and FrmStop to 1'b0
3 Set PP_En to 1'b1

3.8 I2C Slave Interface

3.8.1 Overview

TC358768AXBG supports an I2C slave function. The I2C module supports the following features:

- Fail safe I2C pad operation
- Up to 400 KHz fast mode operation or 1MHz for special mode operation.
- Supports 7 bit slave addresses recognition (slave address=7'b0000_111X)
- No support for general call address
- Supports 16 bit index value for TC358768AXBG I2C slave access

The I2C slave function supports a fixed slave address only and does not support general call address. The I2C slave function does not require any programmable configuration parameters.

3.8.2 I2C Write Access Translation

Registers in TC358768AXBG are 16 bit aligned. This implies that I2C accesses to registers should always be done on 16 bit boundaries. The I2C slave will update an internal 16-bit write data register indexed by the lsb of the internal address index. Write access to TC358768AXBG registers over the register interface is performed when a byte of data has been received and the internal address index has hit a 16-bit boundary. This mechanism allows 16-bit aligned registers to be updated simultaneously based on the register address value presented on the I2C bus interface. Note that data transferred on the I2C bus is sent MSB first.

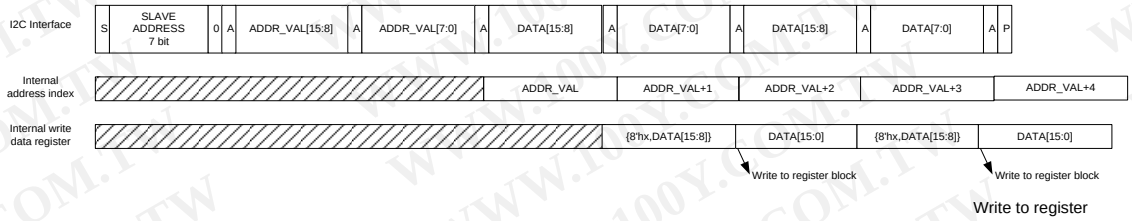


Figure 3-8 I2C Write Transfers Translated to Register Write Accesses

3.8.3 I2C Read Access Translation

Registers in TC358768AXBG are 16 bit aligned. This implies that I2C accesses to registers should always be done on 16 bit boundaries. The I2C slave will update an internal 16-bit read data register when it received the I2C read command or when a byte transfer has completed and the internal address index has hit a 16-bit boundary. Data from the internal read register indexed by the lsb of the internal address index is then transferred over the I2C bus. This mechanism allows 16-bit aligned registers to be read without any side effects. Note that data transferred on the I2C bus is sent MSB first.

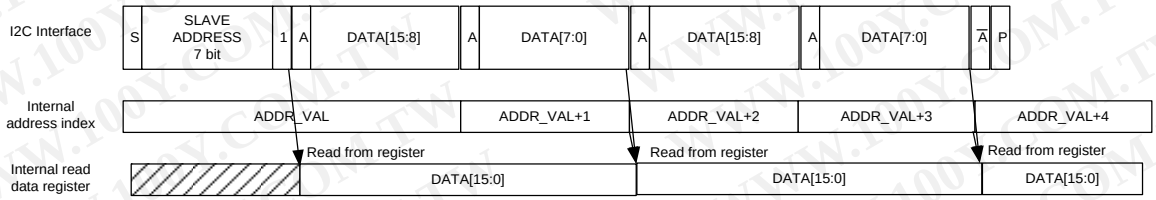


Figure 3-9 I2C Read Transfers to Register Read Accesses

3.9 SPI Slave Interface

The TC358768AXBG Bridge Chip incorporates a SPI Slave Interface port which Host can drive to configure registers in the chip.

The following features are supported:

- Slave select pin supported
- Clock Polarity and Phase selectable
- Transfer Frame size of 32 bits
- Slave speed is up to 25 MHz
- Supports 16 bit index value for TC358768AXBG SPI slave access

The basic operation of SPI interface is shown below where the standard 4-wire interface is used for transactions between the Host (SPI Master) and TC358768AXBG (SPI Slave).
The Host asserts (active low) the Slave Select signal (SPI_SS) when it wants to initiate a read or write transaction. This is followed by the Host sending 32 pulses on the SPI Clock signal (SPI_SCK). In this spec., the bit slots are assumed numbered 31 to 0 from left to right.
Once the intended 16 bits (for TC358768AXBG register address and command) and the additional data bits have been transferred, the Host de-asserts the Slave Select signal (SPI_SS) to indicate end of frame transfer.
This is shown in a simplistic way in the figure below (16 bits transfer size shown in the figure).

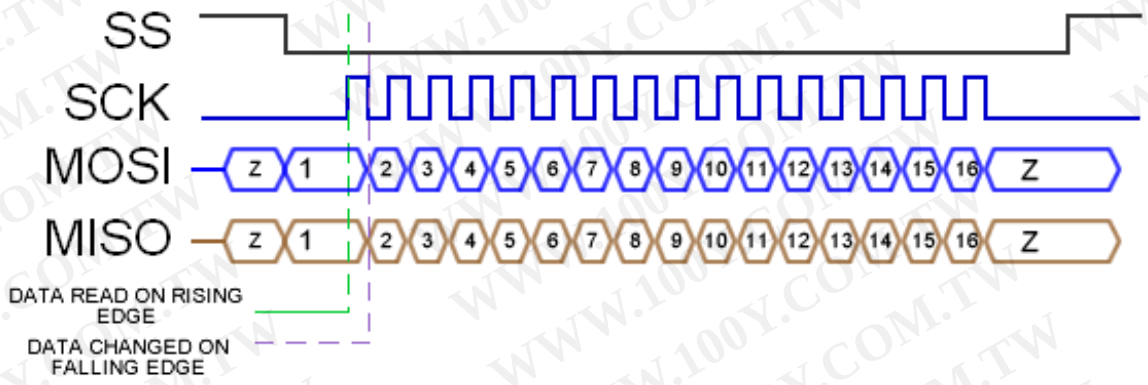


Figure 3-10 SPI basic operation

3.9.1 Clocking Modes

The SPI slave function supports one clocking mode which shown below.

Table 3-5 SPI Clocking modes

Mode	SPOL	SPHA	Drive Edge	Sample Edge	Comments
3	1	1	negedge	posedge	Master/Slave drive first data on first active clock edge

3.9.1.1 Timing Diagram

In this transfer format, the first bit value is captured on the second clock edge. This will be on a rising edge. The levels on the MOSI and MISO signals always change with the inactive clock edges on SCLK. The inactive clock edge will be the falling edge. It will idle high.

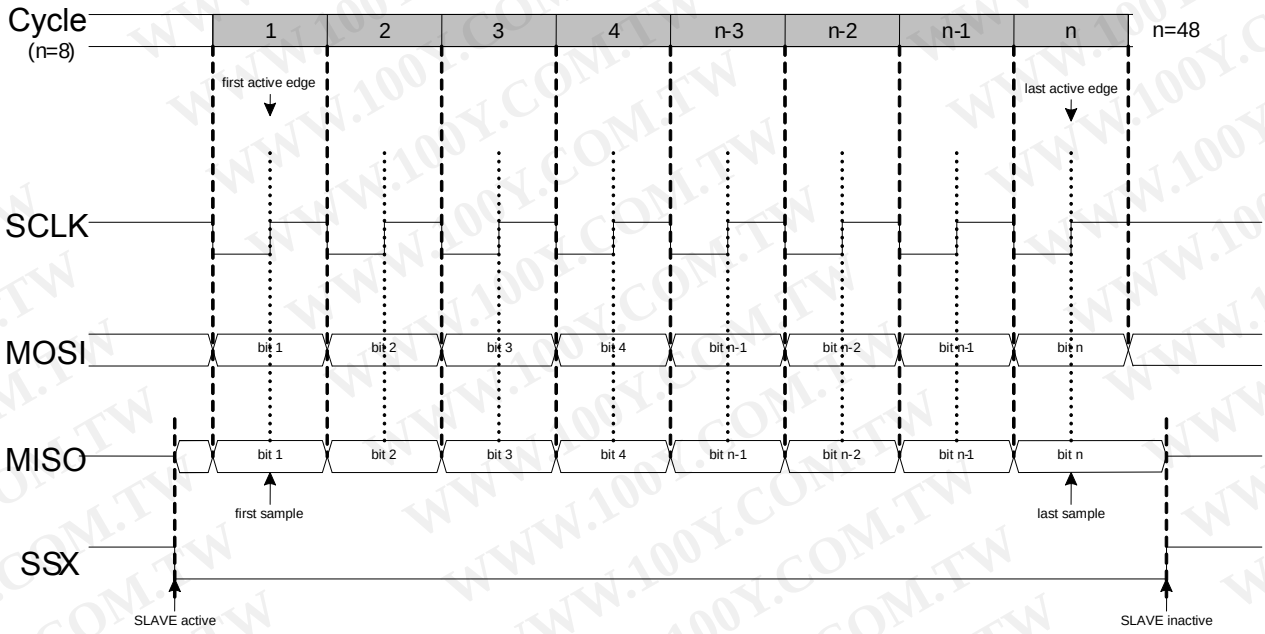


Figure 3-11 SPI transfer

3.9.1.2 Providing Register Address over SPI Interface

The SPI transactions are performed in 32 bits wide frames. The SPI master drives the command and address of the TC358768AXBG register to be accessed. The first 15 bits provide the register address bits 15 to 1. The 16th bit of a frame is the command: 0=Write / 1=Read. Meaning of rest of the bits is based on transaction type. This frame structure is shown in the figure below for a write transaction.

Figure 3-12 Register Write Transfer over SPI (transfer size=32 bits)

CMD = Command: 1=Read / 0=Write
SPI slave function supports random write and read accesses.

3.9.1.3 SPI Write Access Translation

Registers in TC358768AXBG are 16 bit aligned. This implies that SPI accesses to registers should always be done on 16 bit boundaries. The SPI slave will update an internal 16-bit write data register indexed by the address in the SPI frame. The data in bit slots 15 to 0 (after the first 16 bits of address and command) on MOSI line is used as the write data for these writes. Write access to TC358768AXBG registers over the register interface is performed when a frame transfer is completed with command bit set to 0. During the write transaction, the data on the MISO line is not related to the write transaction. How to handle the data on MISO line during write transactions is discussed more in section on full-duplex mode.

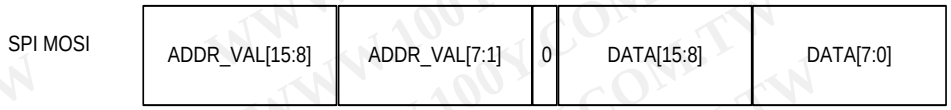


Figure 3-13 Register Write Transfer over SPI (transfer size=32 bits)

3.9.1.4 SPI Read Access Translation

Registers in TC358768AXBG are 16 bit aligned. This implies that SPI accesses to registers should always be done on 16 bit boundaries. The SPI slave will access an internal 16-bit data register indexed by the address in the SPI frame.

Read access to TC358768AXBG registers is completed in two frames. The first frame is similar to a write frame (as shown above) but with the 16 bits of data on MOSI line ignored by TC358768AXBG. This step provides the 15 bits index address of the TC358768AXBG register to be accessed. The only difference in this step from Write frame is that the command bit is set to 1 (Read command). During the second frame period, the TC358768AXBG stuffs the read data into the bit slots 15 to 0 based on the data from the TC358768AXBG register indexed by the read command address in the first frame as shown below. Handling of MISO line during first frame period and MOSI line during the second frame period is discussed further in full-duplex mode section.

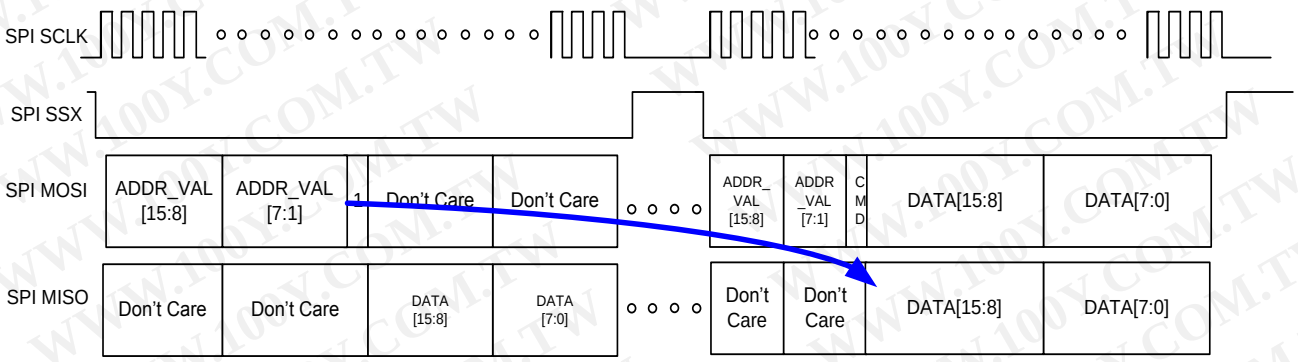


Figure 3-14 Register Read (Normal) Transfer over SPI (transfer size=32 bits)

3.9.2 Full Duplex

All above transactions are considered as full duplex by TC358768AXBG by default. During any frame, TC358768AXBG inserts the data from the TC358768AXBG register that was last addressed by the read command from the SPI master into the bit slots 15 to 0 of the frame on MISO line. During any frame, the bits on the MOSI line bit slots 31 to 17 are considered as the address with the bit slot 16 providing the command. Data on MOSI line during bit slots 15 to 0 are used as write data.

The data on MISO line during bit slots 15 to 0 always corresponds to the previous frame's read command and can be ignored by the SPI Master if the previous frame command was a read command.

The data on MOSI line during bit slots 31 to 17 always provides the address for the TC358768AXBG register for the current frame command.

The data on MOSI line during bit slots 15 to 0 will always be written into the TC358768AXBG register addressed by current frame's address bits (bit slots 31 to 17) if the command in the current frame is a write command.

Four scenarios are possible for back to back transactions as explained below.

3.9.2.1 Back-2-back writes

In this case, the data on the MOSI line is always valid during both back-2-back frames and used for TC358768AXBG register writes. The data on the MISO line in first frame might correspond to a read command issued in the previous frame. Data on the MISO line in 2nd frame is redundant (corresponds to the TC358768AXBG register addressed by the last read command some frames ago).

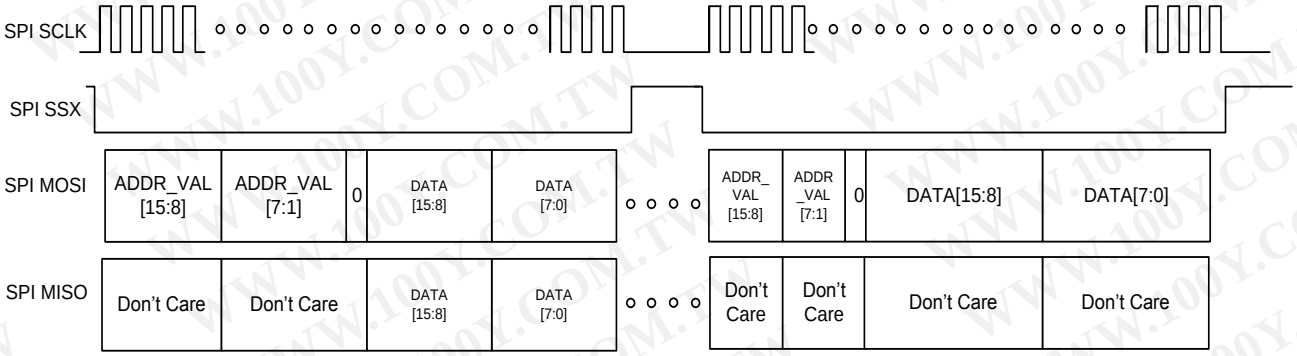


Figure 3-15 Back-2-Back Write Transfers over SPI

3.9.2.2 Back-2-back reads

In this case, the data on the MOSI line is always valid only during first 16 bits (bit slots 31 to 16) in both back-2-back frames and used for TC358768AXBG register reads. The data on the MISO line in first frame might correspond to a read command issued in the previous frame. Data on the MISO line in 2nd frame corresponds to the TC358768AXBG register addressed by the read command in 1st frame. The read data corresponding to the register addressed by the read command in 2nd frame shall be available in the next (3rd) frame on MISO line.

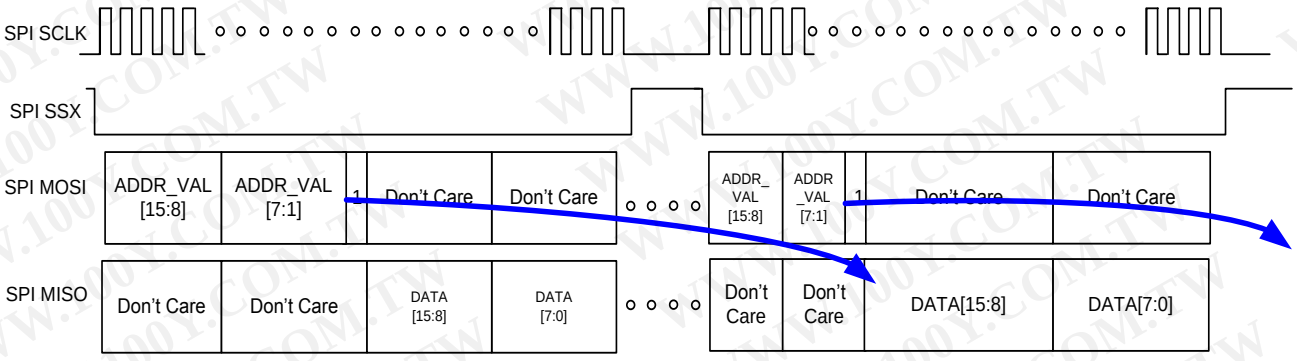


Figure 3-16 Back-2-Back Read Transfers over SPI

3.9.2.3 Write-after-Read

In this case, the handling of data on MISO and MOSI lines during first frame is similar to the "Back-to-Back reads" case. Data on the MOSI line during first 16 bits (bit slots 31 to 16) in 2nd frame provides the address and command for the write (write-after-read). Data on the MOSI line during bit slots 15 to 0 in 2nd frame provides the write data for the write command. Data on the MISO line in 2nd frame corresponds to the TC358768AXBG register addressed by the read command in 1st frame.

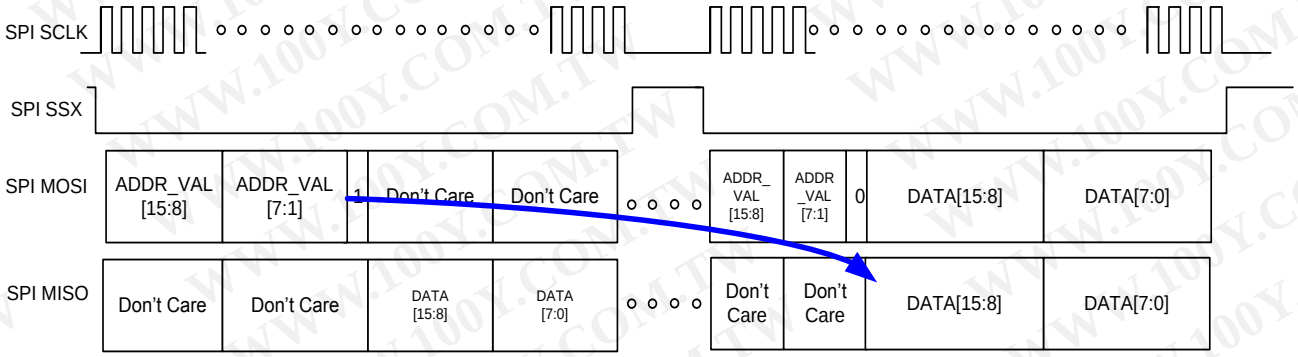


Figure 3-17 Write-after-Read Transfer over SPI

3.9.2.4 Read-after-Write

In this case, the handling of data on MISO and MOSI lines during first frame is similar to the "Back-to-Back writes" case. Data on the MOSI line during first 16 bits (bit slots 31 to 16) in 2nd frame provides the address and command for the read (read-after-write). Data on the MOSI line during bit slots 15 to 0 in 2nd frame is redundant. Data on the MISO line in 2nd frame is redundant. The read data corresponding to the register addressed by the read command in 2nd frame shall be available in the next (3rd) frame on MISO line.

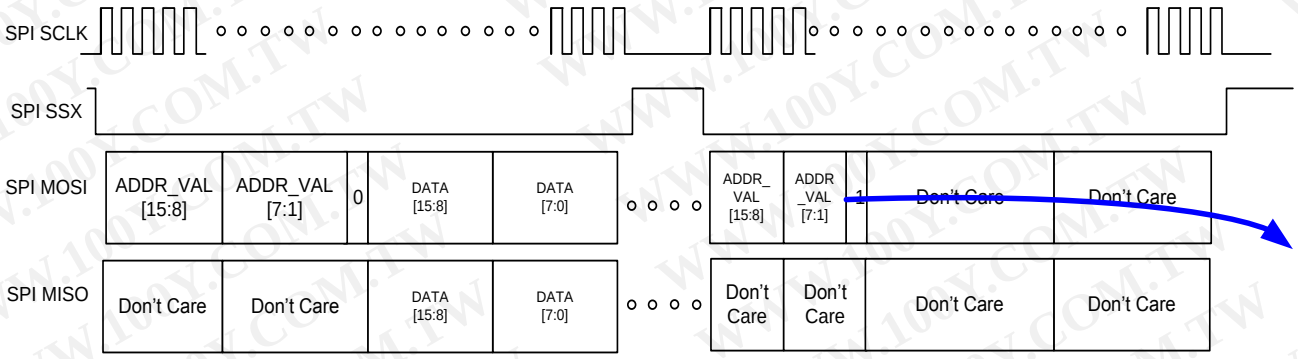


Figure 3-18 Read-after-Write Transfer over SPI

3.9.2.5 NOP-after-Read

In this case, where there is a read alone followed by no more immediate request, the handling of data on MISO and MOSI lines during first frame is similar to the “Back-to-Back reads” case. Data on the MOSI line during first 16 bits (bit slots 31 to 16) in 2nd frame should contain all 1’s to point to a dummy address for SPI and command for the write. Data on the MOSI line during bit slots 15 to 0 in 2nd frame is redundant. Data on the MISO line in 2nd frame corresponds to the TC358768AXBG register addressed by the read command in 1st frame. The write on MOSI line in 2nd frame points to a dummy address (all 1’s) and so redundant.

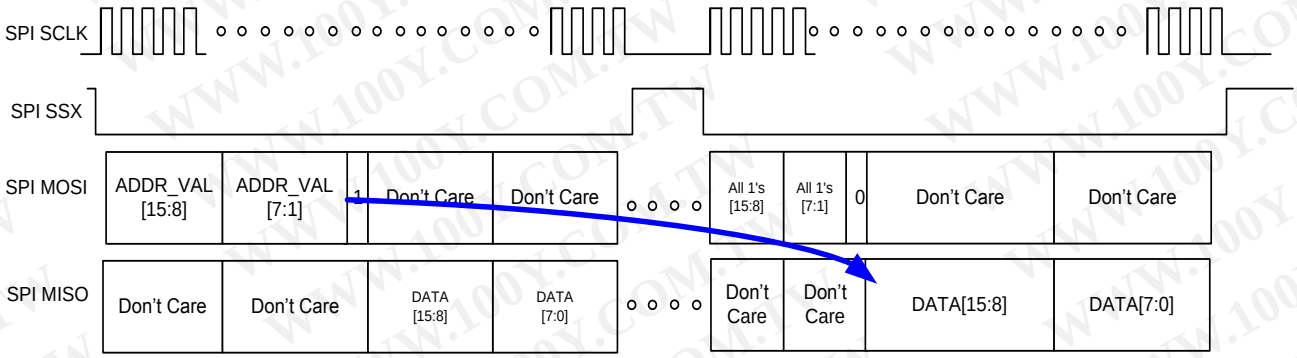


Figure 3-19 NOP-after-Read Transfer over SPI

4 Clock and System

The clock generation unit (CG) makes use of a single PLL. PLL Clock output frequency is same as DSITX Bit clock frequency. DSITX Byte clock will be used for DSITX controller and Video Buffer controller. PCLK input will be used for Parallel port input controller. Rest of the modules use either REFCLK or PCLK/4.

PLL uses either an external input clock REFCLK (6MHz to 40 MHz) or PCLK/4 to generate PLL Refclk as shown in Figure 4-1. After reset, if REFCLK is not present on the system, automatically TC358768AXBG will select PCLK/4 as the clock source. However, REFCLK needs to be toggle at least two cycles, Figure 4-3, a GPIO from host controller can be used to achieve this purpose.

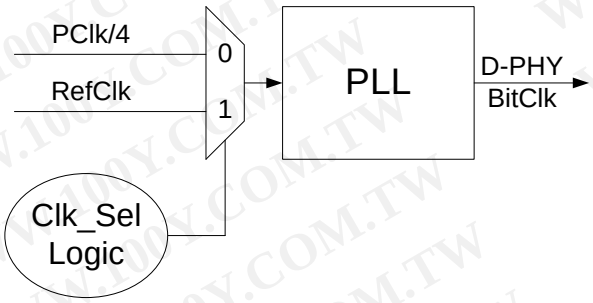


Figure 4-1 D-PHY PLL with its Clock Sources

4.1.1 Example of PLL Generated Clock Frequency

The possible clock frequencies generated from the PLL are achieved by varying the values in registers PLLFBD and PLLDiv.

*pll_clk = RefClk * [(FBD + 1)/ (PRD + 1)] * [1 / (2^FRS)]*

or

*pll_clk = (PCLK/4) * [(FBD + 1)/ (PRD + 1)] * [1 / (2^FRS)]*

Table 4-1 provides possible frequencies that may be used in TC358768AXBG.

Table 4-1 Possible PLL parameters

Reference clock (MHz) (REFCLK or PCLK/4)	FBD	PRD	FRS	pll_clk (MHz)
16.6	255	7	1	265.60
	319	5	2	221.33
	319	6	2	189.71

	319	7	2	166.00

Table 4-2 Controllers' Operating Frequency

Controllers	Operating Frequency		Source
	min (MHz)	max (MHz)	
VB controller (Write port)	10	166	Input PCLK
VB controller (Read port)	---	125	DSI Byte clock (PLL)
Parallel Input controller	---	166	Input PCLK
SPI/I2C controller	6	40	Input REFCLK
Register module	6	40	Input REFCLK

4.1.2 TC358768AXBG Power Up Procedure

The following sequence should happen before TC358768AXBG is able to operate properly:

1. Provide voltage and clock sources to TC358768AXBG.
2. For voltage source, it is desired to turn on core power (1.2) source first, then Analog PHY and IO power as shown in Figure 4-2 Power On Sequence.
3. RefClk, PClk/4, clock source can be from 6 MHz to 40 MHz.
4. The timing parameters for Figure 4-2 are tabulated in Table 4-3.

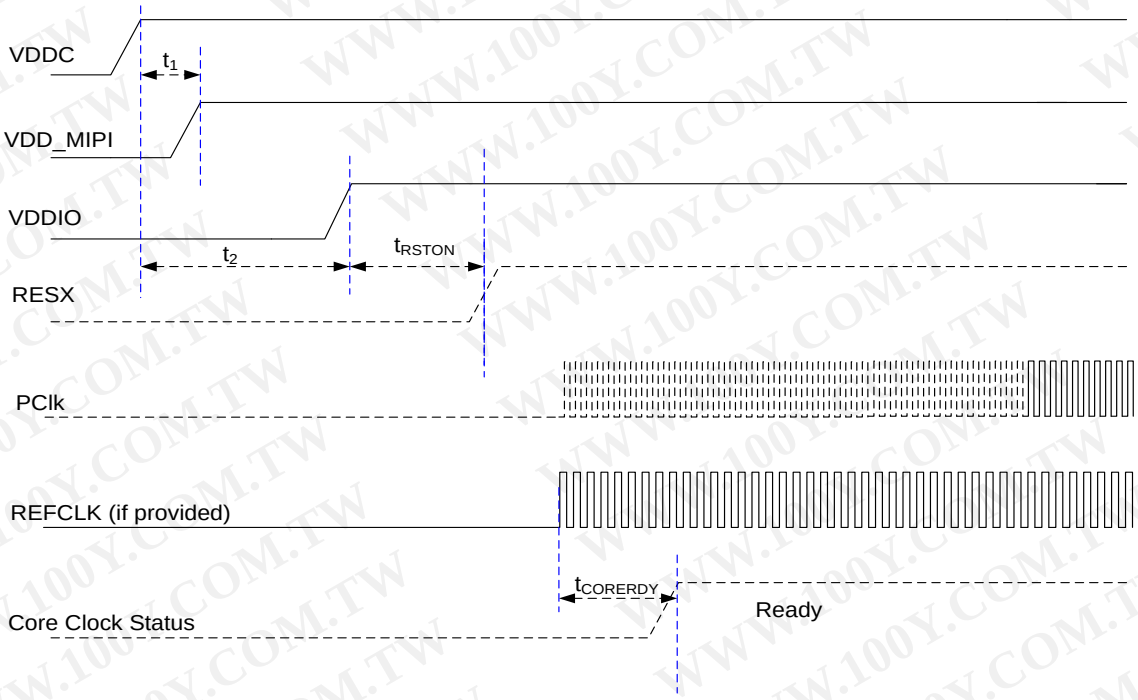


Figure 4-2 Power On Sequence With External RefClk Running

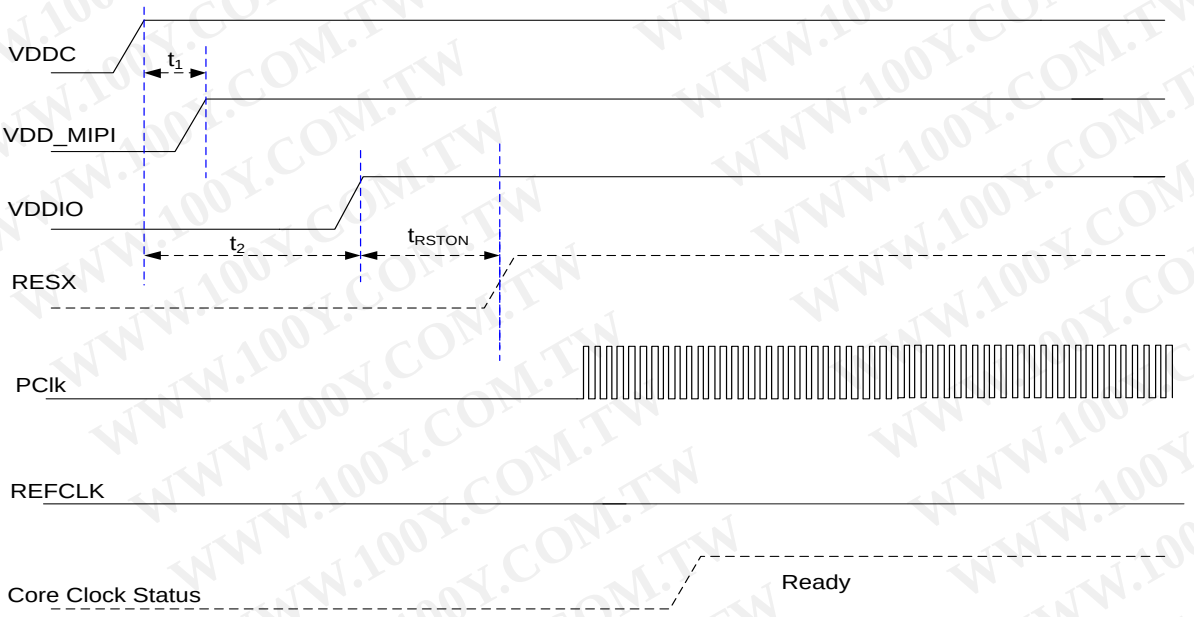


Figure 4-3 Power On Sequence Without External RefClk Running

Table 4-3 Power On Sequence Timing

Parameters	Description	Min.	Typ.	Max.	Units
RefClk	Reference clock frequency	6	---	40	MHz
t_1	VDD_MIPI on delay from VDDC.	0	---	10	msec
t_2	VDDIO on delay from VDDC	0	---	10	msec
t_{RSTON}	RESET width period	200	---	---	nsec
$t_{CORERDY}$	Period after reset de-assertion when TC358768AXBG clocks are stable (Dependent on REFCLK frequency)	.7	---	1	msec

4.1.3 TC358768AXBG Power Down Procedure

Figure 4-4 Power Down Sequence

Table 4-4 Power Down Sequence Timing

Parameters	Description	Min.	Typ.	Max.	Units
t_1	VDD_MIPI off delay from VDDIO off	0	---	10	msec
t_2	VDDC off delay from VDD_MIPI off	0	---	10	msec

5 RegFile Block

Host accesses TC358768AXBG RegFile block to read status and/or write control registers through the I2C or SPI slave interface.

Registers in Group Global and DSITX_CTL (Table 5-1) can be accessed as 16-bit registers. While the others have to be written as 32-bit registers, even if the upper 16-bits are all zeros.

5.1 Register Map

The control and status registers in TC358768AXBG is provided in Table 5-1.

Table 5-1 Register Map

Group	Address	Register	Description
Global (16-bit addressable)	0x0000	ChipID	TC358768AXBG Chip and Revision ID
	0x0002	SysCtl	System Control Register
	0x0004	ConfCtl	Configuration Control Register
	0x0006	VSDly	Video Delay Register
	0x0008	DataFmt	Data Format Control Register
	0x000E	GPIOEn	GPIO Enable Control Register
	0x0010	GPIODir	GPIO Pin Direction Control Register
	0x0012	GPIOIn	GPIO Input Pin Value
	0x0014	GPIOOut	GPIO Output Pin Value
	0x0016	PLLCtl0	PLL control Register 0
	0x0018	PLLCtl1	PLL control Register 1
	0x0032	PP_MISC	Parallel Input Port Miscellaneous Register
	0x0050	DSITX_DT	DSITX Data Type Register
	0x00F8	FiFoStatus	FiFo Underflow/Overflow Status
TX PHY (32-bit addressable)	0x0100	CLW_DPHYCONTTX	Clock Lane DPHY Tx Control register
	0x0104	D0W_DPHYCONTTX	Data Lane0 DPHY Tx Control register
	0x0108	D1W_DPHYCONTTX	Data Lane1 DPHY Tx Control register
	0x010C	D2W_DPHYCONTTX	Data Lane2 DPHY Tx Control register
	0x0110	D3W_DPHYCONTTX	Data Lane3 DPHY Tx Control register
	0x0114 – 0x013F	Reserved	
	0x0140	CLW_CNTRL	Clock Lane DPHY Control Register
	0x0144	D0W_CNTRL	Data Lane 0 DPHY Control Register
	0x0148	D1W_CNTRL	Data Lane 1 DPHY Control Register
	0x014C	D2W_CNTRL	Data Lane 2 DPHY Control Register
	0x0150	D3W_CNTRL	Data Lane 3 DPHY Control Register
TX PPI (32-bit addressable)	0x0200	Reserved	
	0x0204	STARTCNTRL	DSITX Start Control Register
	0x0208	STATUS	DSITX Status Register
	0x020C	Reserved	
	0x0210	LINEINITCNT	DSITX Line Initialization Control Register
	0x0214	LPTXTIMECNT	SYSLPTX Timing Generation Counter
	0x0218	TCLK_HEADERCNT	TCLK_ZERO and TCLK_PREPARE Counter
	0x021C	TCLK_TRAILCNT	TCLK_TRAIL Counter
	0x0220	THS_HEADERCNT	THS_ZERO and THS_PREPARE Counter
	0x0224	TWAKEUP	TWAKEUP Counter
	0x0228	TCLK_POSTCNT	TCLK_POST Counter
	0x022C	THS_TRAILCNT	THS_TRAIL Counter
	0x0230	HSTXVREGCNT	TX Voltage Regulator setup Wait Counter
	0x0234	HSTXVREGEN	Voltage regulator enable for HSTX Data Lanes
	0x0238	TXOPTIONCNTRL	TX Option Control

	0x023C	BTACNTRL1	BTA Control
TX CTRL (32-bit addressable)	0x0400-0x0408	Reserved	
	0x040C	DSI_CONTROL	DSI Configuration Read Register
	0x0410	DSI_STATUS	DSI Status Register
	0x0414	DSI_INT	DSITX – Presents interrupts currently being held
	0x0418	DSI_INT_ENA	DSITX – Enables DSI_INT interrupt source
	0x0430	DSICMD_RDFIFO	DSI Command Read Data FIFO
	0x0434	DSI_ACKERR	DSITX – acknowledge error packet
	0x0438	DSI_ACKERR_INTENA	DSITX – acknowledge error packet interrupt enable
	0x043C	DSI_ACKERR_HALT	DSITX – stop on error bit set in the DSI_ACKERR register
	0x0440	DSI_RXERR	DSITX – internal error while receiving by the previous BTA
	0x0444	DSI_RXERR_INTENA	DSITX – interrupt enable bits of the DSI_RXERR register
	0x0448	DSI_RXERR_HALT	DSITX – stop on error bit set in the DSI_RXERR register
	0x044C	DSI_ERR	DSITX – transfer general errors
	0x0450	DSI_ERR_INTENA	DSITX – interrupt enable bits of the DSI_ERR register
	0x0454	DSI_ERR_HALT	DSITX – stop on error bit set in the DSI_ERR register
	0x0500	DSI_CONFW	DSI TX Configure Write Register
	0x0504	DSI_RESET	DSITX – reset he module and the Receive FIFO content
	0x050C	DSI_INT_CLR	DSITX – Clears particular bits of the DSI_INT register
	0x0518	DSI_START	DSI – Starts DSI-TX operation
DSITX CTRL(16-bit addressable)	0x0600	DSICMD_TX	DSI Command Packet Start register
	0x0602	DSICMD_TYPE	DSI Command Packet Type register
	0x0604	DSICMD_WC	DSI Command Packet Word Count
	0x0610	DSICMD_WD0	DSI Command Packet Data register 0
	0x0612	DSICMD_WD1	DSI Command Packet Data register 1
	0x0614	DSICMD_WD2	DSI Command Packet Data register 2
	0x0616	DSICMD_WD3	DSI Command Packet Data register 3
	0x0620	DSI_EVENT	DSI Hsync Event Mode
	0x0622	DSI_VSW	DSI Vsync Width register
	0x0624	DSI_VBPR	DSI Vsync Back Porch lines register
	0x0626	DSI_VACT	DSI Vsync Active lines register
	0x0628	DSI_HSW	DSI Hsync Width register
	0x062A	DSI_HBPR	DSI Hsync Back Porch register
	0x062C	DSI_HACT	DSI Hsync Active Piels register
Debug (16-bit addressable)	0x00e0	VBufCtl	VBuffer Control (ColorBar, or Command) Register
	0x00e2	DBG_WIDTH	Debug Setting for Line Width
	0x00e4	DBG_VBlank	Debug Setting for Vertical Blank lines
	0x00e8	DBG_Data	Debug Setting for Data Written into FIFO

5.2 Register Description

The following sections provide a detailed description of the registers.

5.2.1 Chip and Revision ID (ChipID: 0x0000)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	ChipID							
Type	RO							
Default	0x44							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	RevID							
Type	RO							
Default	0x01							

Table 5-2 Chip and Revision ID

Register Field	Bit	Default	Description
ChipID	[15:8]	0x44	**Chip ID** Chip ID assigned for this device by Toshiba.
RevID	[7:0]	0x01	**Revision ID** Revision ID for this device assigned by Toshiba.

5.2.2 System Control Register (SysCtl:0x0002)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							SReset
Type	RO							R/W
Default	0x0							0x0

Table 5-3 System Control Register

Register Field	Bit	Default	Description
Reserved	[15:1]	0x0	
SReset	0	0x0	**Software Reset (Active high)** This bit is set to force TC358768AXBG logic to reset state except all configuration registers content (regFile) and I2C slave module. 0: Normal operation 1: Reset operation Software needs to clear SReset when set.

5.2.3 Input Control Register (InputCtl: 0x0004)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved		INTEn2	Reserved			PDataF	
Type	RO		R/W	RO			R/W	
Default	0x0		0x0	0x0			0x0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved	PPEn	VsyncP	DEP	Reserved	Auto	Reserved	

Type	RO	R/W	R/W	R/W	RO	R/W	RO
Default	0x0	0x0	0x0	0x0	0x0	0x1	0x0

Table 5-4 Input Control Register

Register Field	Bit	Default	Description
Reserved	[15:14]	0x0	Reserved
INTEn2	13	0x0	**INT Output Enable 2** 0: Normal (Default to GPIO1 function) 1: Enable (output INT to GPIO1)
Reserved	[12:10]	0x0	Reserved
PDataF	[9:8]	0x0	**Parallel Data Format Option** 2'b00: Mode 0 2'b01: Mode 1 2'b10: Mode 2 2'b11: Reserved Note: See Table 3-4 for more information
Reserved	7	0x0	Reserved
PPEn	6	0x0	**Parallel Port Enable** 0: Parallel Port Disable 1: Parallel Port Enable
VsyncP	5	0x0	**VSync Polarity Control** 0: Active low 1: Active high Note: Hsync Polarity is defined in register bit 0x0032[0]
DEP	4	0x0	**DE Polarity Control** 0: Active high 1: Active low
Reserved	3	0x0	Reserved
Auto	2	0x1	**I2C slave index increment** 0: I2C address index does not increment on every data byte transfer 1: I2C address index increments on every data byte transfer Note: For I2C interface only
Reserved	[1:0]	0x0	Reserved

Note: All Reserved bits must program "0"

5.2.4 VSDly Register (VSDly: 0x0006)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						VSDly[9:8]	
Type	RO						R/W	
Default	0x0						0x0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	VSDly[7:0]							
Type	R/W							
Default	0x1							

Table 5-5 VSDly Register

Register Field	Bit	Default	Description
Reserved	[15:10]	0x0	Reserved

Register Field	Bit	Default	Description
VSDly	[9:0]	0x1	**V/HSync Delay Value** This field determines Video Starts. After detecting VSync/HSync at parallel inputs, DSI Tx waits for the delay (counted in ByteClk) plus ~40 cycles (internal latency delay) before sending out VSS/HSS. Note: If this value is set too small, the chip will waits for data available in the video buffer before starting video output.

5.2.5 Data Format Control Register (DataFmt: 0x0008)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	PDFormat				spmode_en	rdswap_en	dsitx_en	txdt_en
Type	R/W				R/W	R/W	R/W	R/W
Default	0x0				0x0	0x0	0x0	0x0

Table 5-6 Data Format Control Register

Register Field	Bit	Default	Description
Resserved	[15:8]	0x0	Reserved
PDFormat	[7:4]	0x0	Peripheral Data Format 0000: User Define 0001: Reserved 0010: Reserved 0011: RGB888 0100: RGB666 0101: RGB565 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011 – 1111: Reserved Notes: This field used for parallel input port packing logic
spmode_en	[3]	0x0	Special mode enable 0: Normal 1: RGB666: select Loosely pack Note: Only valid when rdswap_en=1
rdswap_en	[2]	0x0	RGB Swap R & B enable **Note: Must program to "1"**
dsitx_en	[1]	0x0	DSITX i/f enable 0: Disable 1: Enable
txdt_en	[0]	0x0	DSITX Data Type ID enable **Must program to "1"**

Register Field	Bit	Default	Description
			DSITX: Use Data Type ID defined in DSITX_DT register

5.2.6 GPIO Enable Register (GPIOEn: 0x000E)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	GPIOEn[10:3]							
type	R/W							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							
type	RO							
Default	0x0							

Table 5-7 GPIO Direction Register

Register Field	Bit	Default	Description
GPIOEn	[15:8]	0x0	**GPIO Enable** 0: Disable (GPIOx function depend on mode of operation) 1: Enable (GPIOx function depend on GPIODir)
Resserved	[7:0]	0x0	Reserved

5.2.7 GPIO Direction Register (GPIODir: 0x0010)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	GPIODir[10:3]							
type	R/W							
Default	0xFF							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					GPIODir[2:1]		Reserved
type	R/W					R/W		R/W
Default	0x1F					0x3		0x1

Table 5-8 GPIO Direction Register

Register Field	Bit	Default	Description
GPIODir	[15:8]	0x0	**GPIO[10:3] Pin Direction**
Resserved	[7:3]	0x1F	Do not change default value
GPIODir	[2:1]	0x3	**GPIO[2:1] Pin Direction** 0: GPIO Pin is set to Output Mode 1: GPIO Pin is set to Input Mode
Resserved	[0]	0x1	Do not change default value

5.2.8 GPIO Pin Value Register (GPIOPin: 0x0012)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	GPIOIn[10:3]							
type	RO							
Default	0x??							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					GPIOIn[2:1]		Reserved
type	RO					RO		RO
Default	0x??					0x??		0x??

Table 5-9 GPIO Pin Value Register

Register Field	Bit	Default	Description
GPIOPin	[15:8]	0x??	**GPIO[10:3] Pin Value**
Reserved	[7:3]	0x??	
GPIOPin	[2:1]	0x??	**GPIO[2:1] Pin Value**
Reserved	[0]	0x??	

5.2.9 GPIO Output Value Register (GPIOOut: 0x0014)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	GPIOOut[10:3]							
type	R/W							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					GPIOOut[2:1]		Reserved
type	R/W					R/W		R/W
Default	0x00					0x0		0x0

Table 5-10 GPIO Output Value Register

Register Field	Bit	Default	Description
GPIOOut	[15:8]	0x0	**GPIO[10:3] Output Register Value**
Reserved	[7:3]	0x0	
GPIOOut	[2:1]	0x0	**GPIO[2:1] Output Register Value**
Reserved	[0]	0x0	

5.2.10 PLL Control Register 0 (PLLCtl0: 0x0016)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	PLL_PRD				Reserved			PLL_FBD[8]
Type	R/W				RO			R/W
Default	0x4				0x00			0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	PLL_FBD[7:0]							
Type	R/W							
Default	0x63							

Table 5-11 PLL Control Register 0

Register Field	Bit	Default	Description
PLL_PRD	[15:12]	0x4	Input divider setting Division ratio = (PRD3..0) + 1
Reserved	[11:9]	0x0	
PLL_FBD	[8:0]	0x063	Feedback divider setting Division ratio = (FBD8…0) + 1

5.2.11 PLL Control Register 1 (PLLCtl1: 0x0018)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				PLL_FRS		PLL_LBWS	
Type	RO				R/W		R/W	
Default	0x0				0x1		0x2	

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Revsd	LFBREN	BYPCKEN	CKEN	Reserved		RESETB	PLL_EN
Type	RO	R/W	R/W	R/W	RO		R/W	R/W
Default	0x0	0x0	0x0	0x0	0x0		0x0	0x0

Table 5-12 PLL Control Register 1

Register Field	Bit	Default	Description
Reserved	[15:12]	0x0	
PLL_FRS	[11:10]	0x1	Frequency range setting (post divider) for HSCK frequency 2'b00: 500MHz – 1GHz HSCK frequency 2'b01: 250MHz – 500MHz HSCK frequency 2'b10: 125 MHz – 250MHz HSCK frequency 2'b11: 62.5MHz – 125MHz HSCK frequency
PLL_LBWS	[9:8]	0x2	Loop bandwidth setting 2'b00: 25% of maximum loop bandwidth 2'b01: 33% of maximum loop bandwidth 2'b10: 50% of maximum loop bandwidth (default) 2'b11: maximum loop bandwidth
Reserved	[7]	0x0	
PLL_LFBREN	[6]	0x0	Lower Frequency Bound Removal Enable 1'b0: REFCLK toggling –> normal operation, REFCLK stops -> no oscillation 1'b1: REFCLK toggling -> normal operation, REFLCK stops -> free running PLL
PLL_BYPCKEN	[5]	0x0	Bypass clock enable 1'b0: Normal operation 1'b1: bypass mode, REFCLK is used instead of PLL_VCO output
PLL_CKEN	[4]	0x0	Clock enable 1'b0: clocks switched off (output LOW) 1'b1: clocks switched on
Reserved	[3:2]	0x0	
PLL_RESETB	[1]	0x0	PLL Reset 1'b0: Reset 1'b1: Normal operation

PLL_EN	[0]	0x0	PLL Enable 1'b0: PLL off 1'b1: PLL on

5.2.12 Parallel In Miscellaneous Register (PP_MISC: 0x0032)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	FrmStop	RstPtr	Reserved					
Type	R/W	R/W	RO					
Default	0x0	0x0	0x00					
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							HsyncP
Type	RO							R/W
Default	0x00							0

Table 5-13 DSITX Data Type Register

Register Field	Bit	Default	Description
FrmStop	15	0x0	**Frame Stop** When this bit is asserted, TC358768A will stop outputting at the next Vsync
RstPtr	14	0x0	**Reset Pointers** When this bit is asserted, TC358768A resets its write/read pointers to Video Buffer
Reserved	[13:1]	0x00	
HsyncP	0	0x0	**Hsync Polarity Control** 0: Active low 1: Active high

Please refer to section 3.7.3 for the usage of bits [15:14].

5.2.13 DSITX Data Type Register (DSITX_DT: 0x0050)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	dsitx_dt[7:0]							
Type	R/W							
Default	0x30							

Table 5-14 DSITX Data Type Register

Register Field	Bit	Default	Description
dsitx_dt	[7:0]	0x30	DSITX Data Type ID This field uses for DSITX Data Type ID when txdt_en = 1;

5.2.14 FIFO Status Register (FIFOSTATUS: 0x00F8)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved						Vb_uflow	Vb_oflow
Type	RO						RO	RO
Default	0x00						0x0	0x0

Table 5-15 FIFO Status Register

Register Field	Bit	Default	Description
Reserved	[15:2]		
vb_uflow	1	0	VB Under Flow Status 0: Normal 1: Under flow Read this register will clear the status
vb_oflow	0	0	VB Over Flow Status 0: Normal 1: Over flow Read this register will clear the status

5.2.15 Clock Lane DPHY TX Control register (CLW_DPHYCONTTX: 0x0100)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						CLW_CAP1	CLW_CAP0
Type	RO	RO	RO	RO	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DLYCNTRL3	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	Reserved		CLW_LPTXCURR1EN	CLW_LPTXCURR0EN
Type	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0

Table 5-16 Clock Lane DPHY TX Control register

Register Field	Bit	Default	Description
Reserved	[31:10]	0x0	
CLW_CAP1	[9]	0x1	Selection bit 1 of different HSTX output capacitors for Clock Lane

Register Field	Bit	Default	Description
CLW_CAP0	[8]	0x0	Selection bit 0 of different HSTX output capacitors for Clock Lane (CAP1,CAP0): = (00): 0 [pF] (CAP1,CAP0): = (01): 2.8 [pF] (CAP1,CAP0): = (10): 3.2 [pF] (CAP1,CAP0): = (11): 3.6 [pF]
DLYCNTRL[3:0]	[7:4]	0x0	Tuning of transmit window position. The High Speed Clock output can be delayed according to the setting. The recommended value is determined by evaluating the LSI in which this module is implemented. Typical delay for rising/falling edge is about DLYCNTRL x 24ps/27ps. Rising edge : DLYCNTRL x 24ps, Falling edge : DLYCNTRL x 27ps.
Reserved	[3:2]	0x0	
CLW_LPTXCURR1EN	[1]	0x1	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for clock Lane.
CLW_LPTXCURR0EN	[0]	0x0	Selection bit-0 for LPTX output current (TRLP/TFLP tuning) for clock Lane. 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current The default value is “10”. However, if “00” is set, the rise/fall time will become later and if “11” is set, the rise/fall time will become earlier.

5.2.16 Data Lane 0 DPHY TX Control register (D0W_DPHYCONTTX:0x0104)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						D0W_CAP1	D0W_CAP0
Type	RO	RO	RO	RO	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	DLYCNTRL3	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	Reserved	Reserved	D0W_LPTXCURR1EN	D0W_LPTXCURR0EN
Type	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W

Default	0	0	0	0	0	0	1	0

Table 5-17 Data Lane 0 DPHY TX Control register

Register Field	Bit	Default	Description
Reserved	[15:10]	0x0	
D0W_CAP1	[9]	0x1	Selection bit 1 of different HSTX output capacitors for Data Lane 0.
D0W_CAP0	[8]	0x0	Selection bit 0 of different HSTX output capacitors for Data Lane 0. (CAP1,CAP0): = (00): 0 [pF] (CAP1,CAP0): = (01): 2.8 [pF] (CAP1,CAP0): = (10): 3.2 [pF] (CAP1,CAP0): = (11): 3.6 [pF]
DLYCNTRL[3:0]	[7:4]	0x0	Tuning of transmit window position. The High Speed Data output can be delayed according to the setting. The recommended value is determined by evaluating the LSI in which this module is implemented. Typical delay for rising/falling edge is about DLYCNTRL x 24ps/27ps. Rising edge : DLYCNTRL x 24ps, Falling edge : DLYCNTRL x 27ps.
Reserved	[3:2]	0x0	
D0W_LPTXCURR1EN	[1]	0x1	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 0.
D0W_LPTXCURR0EN	[0]	0x0	Selection bit-0 for LPTX output current (TRLP/TFLP tuning) for Data Lane 0. 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current The default value is “10”. However, if “00” is set, the rise/fall time will become later and if “11” is set, the rise/fall time will become earlier.

5.2.17 Data Lane 1 DPHY TX Control Register (D1W_DPHYCONTTX: 0x0108)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						D1W_CAP1	D1W_CAP0
Type	RO	RO	RO	RO	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DLYCNTRL3	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	Reserved		D1W_LPTXCURR1EN	D1W_LPTXCURR0EN
Type	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0

Table 5-18 Data Lane 1 DPHY TX Control Register

Register Field	Bit	Default	Description
Reserved	[15:10]	0x0	
D1W_CAP1	[9]	0x1	Selection bit 1 of different HSTX output capacitors for Data Lane 1.
D1W_CAP0	[8]	0x0	Selection bit 0 of different HSTX output capacitors for Data Lane 1. (CAP1,CAP0): = (00): 0 [pF] (CAP1,CAP0): = (01): 2.8 [pF] (CAP1,CAP0): = (10): 3.2 [pF] (CAP1,CAP0): = (11): 3.6 [pF]
DLYCNTRL[3:0]	[7:4]	0x0	Tuning of transmit window position. The High Speed Clock output can be delayed according to the setting. The recommended value is determined by evaluating the LSI in which this module is implemented. Typical delay for rising/falling edge is about DLYCNTRL x 24ps/27ps. Rising edge : DLYCNTRL x 24ps, Falling edge : DLYCNTRL x 7ps.
Reserved	[3:2]	0x0	
D1W_LPTXCURR1EN	[1]	0x1	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 1.
D1W_LPTXCURR0EN	[0]	0x0	Selection bit-0 for LPTX output current (TRLP/TFLP tuning) for Data Lane 1. 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current The default value is “10”. However, if “00” is set, the rise/fall time will become later and if “11” is set, the rise/fall time will become earlier.

5.2.18 Data Lane 2 DPHY TX Control Register (D2W_DPHYCONTTX: 0x010C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8

Name	Reserved						D2W_CAP1	D2W_CAP0
Type	RO	RO	RO	RO	RO	RO	RO	R/W
Default	0	0	0	0	0	0	1	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DLYCNTRL3	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	Reserved		D2W_LPTXCURR1EN	D2W_LPTXCURR0EN
Type	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0

Table 5-19 Data Lane 2 DPHY TX Control Register

Register Field	Bit	Default	Description
Reserved	[15:10]	0x0	
D2W_CAP1	[9]	0x1	Selection bit 1 of different HSTX output capacitors for Data Lane 2.
D2W_CAP0	[8]	0x0	Selection bit 0 of different HSTX output capacitors for Data Lane 2. (CAP1,CAP0): = (00): 0 [pF] (CAP1,CAP0): = (01): 2.8 [pF] (CAP1,CAP0): = (10): 3.2 [pF] (CAP1,CAP0): = (11): 3.6 [pF]
DLYCNTRL[3:0]	[7:4]	0x0	Tuning of transmit window position. The High Speed Clock output can be delayed according to the setting. The recommended value is determined by evaluating the LSI in which this module is implemented. Typical delay for rising/falling edge is about DLYCNTRL x 24ps/27ps. Rising edge : DLYCNTRL x 24ps, Falling edge : DLYCNTRL x 27ps.
Reserved	[3:2]	0x0	
D2W_LPTXCURR1EN	[1]	0x1	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 2.
D2W_LPTXCURR0EN	[0]	0x0	Selection bit-0 for LPTX output current (TRLP/TFLP tuning) for Data Lane 2. 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current The default value is “10”. However, if “00” is set, the rise/fall time will become later and if “11” is set, the rise/fall time will become earlier.

5.2.19 Data Lane 3 DPHY TX Control Register (D3W_DPHYCONTTX: 0x0110)

Bit	B15	B14	B13	B12	B11	B10	B9	B8

Name	Reserved						D3W_CAP1	D3W_CAP0
Type	RO	RO	RO	RO	RO	RO	RO	R/W
Default	0	0	0	0	0	0	1	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DLYCNTRL3	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	Reserved		D3W_LPTXCURR1EN	D3W_LPTXCURR0EN
Type	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0

Table 5-20 Data Lane 2 DPHY TX Control Register

Register Field	Bit	Default	Description
Reserved	[15:10]	0x0	
D3W_CAP1	[9]	0x1	Selection bit 1 of different HSTX output capacitors for Data Lane 3.
D3W_CAP0	[8]	0x0	Selection bit 0 of different HSTX output capacitors for Data Lane 3. (CAP1,CAP0): = (00): 0 [pF] (CAP1,CAP0): = (01): 2.8 [pF] (CAP1,CAP0): = (10): 3.2 [pF] (CAP1,CAP0): = (11): 3.6 [pF]
DLYCNTRL[3:0]	[7:4]	0x0	Tuning of transmit window position. The High Speed Clock output can be delayed according to the setting. The recommended value is determined by evaluating the LSI in which this module is implemented. Typical delay for rising/falling edge is about DLYCNTRL x 24ps/27ps. Rising edge : DLYCNTRL x 24ps, Falling edge : DLYCNTRL x 27ps.
Reserved	[3:2]	0x0	
D3W_LPTXCURR1EN	[1]	0x1	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 3.

Register Field	Bit	Default	Description
D3W_LPTXCURR0EN	[0]	0x0	Selection bit-0 for LPTX output current (TRLP/TFLP tuning) for Data Lane 3. 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current The default value is “10”. However, if “00” is set, the rise/fall time will become later and if “11” is set, the rise/fall time will become earlier.

5.2.20 Clock Lane DPHY Control Register (CLW_CNTRL: 0x0140)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							CLW_LaneDisable
Type	RO							R/W
Default	0x00							0

Table 5-21 Clock Lane DPHY Control Register

Register Field	Bit	Default	Description
Reserved	[15:1]	0x0	
CLW_LaneDisable	[0]	0x0	Force Lane Disable for Clock Lane. 1’b1: Force Lane Disable 1’b0: Bypass Lane Enable from PPI Layer enable. When SCANTESTMODE=1, this register is disabled. When SCANMODE=0, this register is always enabled.

5.2.21 Data Lane 0 DPHY Control Register (D0W_CNTRL: 0x0144)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**

Name	Reserved	CLW_LaneDisable
Type	RO	R/W
Default	0x00	0

Table 5-22 Data Lane 0 DPHY Control Register

Register Field	Bit	Default	Description
Reserved	[15:1]	0x0	
D0W_LaneDisable	[0]	0x0	Force Lane Disable for Data Lane 0. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable from PPI Layer enable. When SCANTESTMODE=1, this register is disabled. When SCANMODE=0, this register is always enabled.

5.2.22 Data Lane 1 DPHY Control Register (D1W_CNTRL: 0x0148)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							D1W_LaneDisable
Type	RO							R/W
Default	0x00							0

Table 5-23 Data Lane 1 DPHY Control Register

Register Field	Bit	Default	Description
Reserved	[15:1]	0x0	
D1W_LaneDisable	[0]	0x0	Force Lane Disable for Data Lane 0. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable from PPI Layer enable. When SCANTESTMODE=1, this register is disabled. When SCANMODE=0, this register is always enabled.

5.2.23 Data Lane 2 DPHY Control Register (D2W_CNTRL: 0x014C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							

Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							D2W_LaneDisable
Type	RO							R/W
Default	0x00							0

Table 5-24 Data Lane 2 DPHY Control Register

Register Field	Bit	Default	Description
Reserved	[15:1]	0x0	
D2W_LaneDisable	[0]	0x0	Force Lane Disable for Data Lane 2. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable from PPI Layer enable. When SCANTESTMODE=1, this register is disabled. When SCANMODE=0, this register is always enabled.

5.2.24 Data Lane 3 DPHY Control Register (D3W_CNTRL: 0x0150)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							D3W_LaneDisable
Type	RO							R/W
Default	0x00							0

Table 5-25 Data Lane 3 DPHY Control Register

Register Field	Bit	Default	Description
Reserved	[15:1]	0x0	
D3W_LaneDisable	[0]	0x0	Force Lane Disable for Data Lane 3. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable from PPI Layer enable. When SCANTESTMODE=1, this register is disabled. When SCANMODE=0, this register is always enabled.

5.2.25 STARTCNTRL (STARTCNTRL: 0x0204)

Bit	B15	B14	B13	B12	B11	B10	B9	B8

Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							START
Type	RO	RO	RO	RO	RO	RO	RO	WO
Default	0	0	0	0	0	0	0	0

Table 5-26 STARTCNTRL

Register Field	Bit	Default	Description
Reserved	[15:1]	0x0	
START	[0]	0x0	START control bit of PPI-TX function. By writing 1 to this bit, PPI starts function. 0: Stop function. (default). Writing 0 is invalid and the bit can be set to zero by system reset only. 1: Start function. The following registers are set to appropriate value before starting any transmission by START bit in STARTCTRL register. Once START bit is set to high, the change of the register bits does not affect to function. In order to change the values, initialization by RESET_N is necessary.

5.2.26 STATUS (STATUS: 0x0208)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							BUSY
Type	RO	RO	RO	RO	RO	RO	RO	R
Default	0	0	0	0	0	0	0	0

Table 5-27 STATUS

Register Field	Bit	Default	Description
Reserved	[15:1]	0x0	
BUSY	[0]	0x0	After writing 1 to the START bit in the STARTCNTRL register, this bit is set until RESET_N is asserted. 0: Not Busy. (default) 1: Busy.

5.2.27 LINEINITCNT (LINEINITCNT: 0x0210)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	LINEINITCNT[15:8]							
Type	R/W							
Default	0x20							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	LINEINITCNT[7:0]							
Type	R/W							
Default	0x8E							

Table 5-28 LINEINITCNT

Register Field	Bit	Default	Description
Reserved	[31:16]		
LINEINITCNT	[15:0]	0x208e	Line Initialization Wait Counter This counter is used for line initialization. **Set this register before setting [STARTCNTRL].START = 1.** MIPI specification requires that the slave device needs to observe LP-11 for 100 us and ignore the received data before the period at initialization time. The count value depends on HFCLK and the value needs to be set to achieve more than 100 us. The counter starts after the START bit of the STARTCNTRL register is set. The Master device needs to output LP-11 for 100 us in order for the slave device to observe LP-11 for the period. For example, in order to set 100 us when the period of HFCLK is 12 ns, the counter value should be more than 8333.3 = 0x208D (100 us / 12 ns). Default is 0x208E.

5.2.28 LPTXTIMECNT (LPTXTIMECNT: 0x0214)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					LPTXTIMECNT[10:8]		
Type	RO					R/W		
Default	0x00					0x0		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	LPTXTIMECNT[7:0]							
Type	R/W							
Default	0x01							

Table 5-29 LPTXTIMECNT

Register Field	Bit	Default	Description
Reserved	[15:11]	0x0	
LPTXTIMECNT	[10:0]	0x1	SYSLPTX Timing Generation Counter The counter generates a timing signal for the period of LPTX. This counter is counted using the HSByteClk (the Main Bus clock), and the value of (setting + 1) * HSByteClk Period becomes the period LPTX. Be sure to set the counter to a value greater than 50 ns.

Set this register before setting [STARTCNTRL].START = 1.

5.2.29 TCLK_HEADERCNT (TCLK_HEADERCNT: 0x0218)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	TCLK_ZEROCNT[7:0]							
Type	R/W							
Default	0x01							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved	TCLK_PREPARECNT[6:0]						
Type	RO	R/W						
Default	0	0x01						

Table 5-30 TCLK_HEADERCNT

Register Field	Bit	Default	Description
TCLK_ZEROCNT	[15:8]	0x1	**TCLK_ZERO Counter** This counter is used for Clock Lane control in the Master mode. In order to satisfy the timing parameter TCLK-PREPARECNT + TCLK-ZERO for Clock Lane, this counter is used. This counter is counted by HSBYTECLk. Set this register in order to set the minimum time (TCLK-PREPARECNT + TCLK-ZERO) to a value greater than 300 ns. The actual value is ((1 to 2) + (TCLK_ZEROCNT + 1)) x HSByteClkCycle + (PHY output delay). The PHY output delay is about (0 to 1) x HSByteClkCycle in the ByteClk conversion performed during RTL simulation, and is about (2 to 3) x MIPIBitClk cycle in the BitClk conversion.
Reserved	[7]	0x0	

Register Field	Bit	Default	Description
TCLK_PREPARECNT	[6:0]	0x1	**TCLK_PREPARE Counter** This counter is used for Clock Lane control in the Master mode. In order to satisfy the timing parameter TCLK-PREPARE for Clock Lane, this counter is used. This counter is counted by HSBYTECLK. Set TCLK-PREPARE period that is greater than 38 ns but less than 95 ns. Calculating formula (TCLK_PREPARECNT + 1) x HSByteClkCycle

Set this register before setting [STARTCNTRL].START = 1.

5.2.30 TCLK_TRAILCNT (TCLK_TRAILCNT: 0x021C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	TCLKTRAILCNT[7:0]							
Type	R/W							
Default	0x01							

Table 5-31 TCLK_TRAILCNT

Register Field	Bit	Default	Description
Reserved	[15:8]	0x0	
TCLK_TRAILCNT	[7:0]	0x1	**TCLK_TRAIL Counter** This counter is used for Clock Lane control in Master mode. In order to satisfy the timing parameter about TCLK-TRAIL and TEOT for Clock Lane, this counter is used. This counter is counted by HSBYTECLK. Set this register in order to set TCLK-TRAIL to a value greater than 60 ns and TEOT to a value less than 105 ns + 12 x UI The actual value is (TCLK_TRAILCNT + (1 to 2)) x HSByteClkCycle + (2+(1 to 2)) * HSBYTECLKCycle - (PHY output delay). The PHY output delay is about (0 to 1) x HSByteClkCycle in the ByteClk conversion performed during RTL simulation, and is about (2 to 3) x MIPIBitClk cycle in the BitClk conversion.

Set this register before setting [STARTCNTRL].START = 1.

5.2.31 THS_HEADERCNT (THS_HEADERCNT: 0x0220)

Bit	B15	B14	B13	B12	B11	B10	B9	B8

Name	Reserved	THS_ZEROCNT[6:0]						
Type	RO	R/W						
Default	0	0x01						
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	B0
Name	Reserved	THS_PREPARECNT[6:0]						
Type	RO	R/W						
Default	0	0x01						

Table 5-32 THS_HEADERCNT

Register Field	Bit	Default	Description
THS_ZEROCNT	[14:8]	0x1	**THS_ZERO Counter** This counter is used for Data Lane control in Master mode. In order to satisfy the timing parameter about THS-PREPARE + THS-ZERO for Data Lane, this counter is used. This counter is counted by HSBYTECLK. Set this register to set the (THS-PREPARE + THS-ZERO) period, which should be greater than (145 ns + 10 x UI) results. The actual value is ((1 to 2) + 1 + (TCLK_ZEROCNT + 1) + (3 to 4)) x ByteClk cycle + HSByteClk x (2+(1 to 2)) +(PHY delay). The PHY output delay is about (1 to 2) x HSByteClkCycle in the ByteClk conversion performed during RTL simulation, and is about (8+(5 to 6)) x MIPIBitClk cycle in BitClk conversion.
Reserved	[7]	0x0	
THS_PREPARECNT	[6:0]	0x1	**THS_PREPARE Counter** This counter is used for Data Lane control in Master mode. In order to satisfy the timing parameter about THS-PREPARE for Data Lane, this counter is used. This counter is counted by HSBYTECLK. Set this register in order to set the THS-PREPARE period, which should be greater than (40 ns + 4xUI) and less than (8 5 ns + 6xUI) results. Calculating Formula: (THS_PREPARECNT + 1) x HSByteClkCycle

Set this register before setting [STARTCNTRL].START = 1.

5.2.32 TWAKEUP (TWAKEUP: 0x0224)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	TWAKEUPCNT[15:8]							
Type	R/W							
Default	0x4E							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	B0
Name	TWAKEUPCNT[7:0]							
Type	R/W							

Default	0x20

Table 5-33 TWAKEUP

Register Field	Bit	Default	Description
Reserved	[31:16]		
TWAKEUPCNT	[15:0]	0x4e20	TWAKEUP Counter This counter is used to exit ULPS state. Ultra-Low Power State is exited by means of a Mark-1 state with a length TWAKEUP followed by a Stop state. This counter is counted by the unit of LPTXTIMECNT.

Set this register before setting [STARTCNTRL].START = 1.

5.2.33 TCLK_POSTCNT (TCLK_POSTCNT: 0x0228)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					TCLK_POSTCNT[10:8]		
Type	RO					R/W		
Default	0x00					0x2		
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	TCLK_POSTCNT[7:0]							
Type	R/W							
Default	0x00							

Table 5-34 TCLK_POSTCNT

Register Field	Bit	Default	Description
Reserved	[15:11]	0x0	
TCLK_POSTCNT	[10:0]	0x200	**TCLK_POST Counter** This counter is used for Clock Lane control in Master mode. This counter is counted by the HSByteClk. Set a value greater than (60 ns + 52 x UI) results. The actual value is ((1 to 2) + (TCLK_POSTCNT + 1)) x HSByteClk cycle + (1) x HSBYTECLK cycle.

Set this register before setting [STARTCNTRL].START = 1.

5.2.34 THS_TRAILCNT (THS_TRAILCNT: 0x022C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				THS_TRAILCNT[3:0]			
Type	RO				R/W			
Default	0x0				0x2			

Table 5-35 THS_TRAILCNT

Register Field	Bit	Default	Description
Reserved	[15:4]	0x0	
THS_TAILCNT	[3:0]	0x2	**THS_TRAIL Counter** This counter is used for Data Lane control in Master mode. This counter is counted by HSBYTECLK. Set a value greater 8 x UI or (60 ns + 4 x UI) and less than TEOT which is 105 ns + 12 x UI results. The actual value is (1 + THS_TRAILCNT) x ByteClk cycle + ((1 to 2) + 2) x HSBYTECLK cycle - (PHY output delay). The PHY output delay is about (1 to 2) x HSByteClkCycle in ByteClk conversion performed during RTL simulation and is about (8+(5 to 6)) x MIPIBitClk cycle in BitClk conversion.

Set this register before setting [STARTCNTRL].START = 1.

5.2.35 HSTXVREGCNT (HSTXVREGCNT: 0x0230)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	HSTXVREGCNT[15:8]							
Type	R/W							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	HSTXVREGCNT[7:0]							
Type	R/W							
Default	0x20							

Table 5-36 HSTXVREGCNT

Register Field	Bit	Default	Description

HSTXVREGCNT	[15:0]	0x0020	TX Voltage Regulator setup Wait Counter This counter is used for all lanes of HSTXVREG commonly. Counter value is counted by HFCLK. The counter starts when START bit is set. After the counter is counted up, PPI-TX can change the line from LP mode to HS mode. If the counter value is set to zero, there is no wait by the counter. Recommended counter value will be decided by evaluation. LINEINCNT is 100 us, so any value less than that will not affect the value of this counter. The value 1 us is used in the example setting.

Set this register before setting [STARTCNTRL].START = 1.

5.2.36 HSTXVREGEN (HSTXVREGEN: 0x0234)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	B0
Name	Reserved			D3M_HSTX VREGEN	D2M_HSTX VREGEN	D1M_HST XVREGEN	D0M_HST XVREGEN	CLM_HST XVREGEN
Type	RO	RO	RO	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Table 5-37 HSTXVREGEN

Register Field	Bit	Default	Description
Reserved	[15:5]	0x0	
D3M_HSTXVREGEN	[4]	0x0	Voltage regulator enable for HSTX Data Lane 3. In order to reduce power consumption, set to be “disable” when PPI-TX is not used. 0: Disable (Default) 1: Enable
D2M_HSTXVREGEN	[3]	0x0	Voltage regulator enable for HSTX Data Lane 2. In order to reduce power consumption, set to be “disable” when PPI-TX is not used. 0: Disable (Default) 1: Enable
D1M_HSTXVREGEN	[2]	0x0	Voltage regulator enable for HSTX Data Lane 1. In order to reduce power consumption, set to be “disable” when PPI-TX is not used. 0: Disable (Default) 1: Enable

Register Field	Bit	Default	Description
D0M_HSTXVREGEN	[1]	0x0	Voltage regulator enable for HSTX Data Lane 0. In order to reduce power consumption, set to be “disable” when PPI-TX is not used. 0: Disable (Default) 1: Enable
CLM_HSTXVREGEN	[0]	0x0	Voltage regulator enable for HSTX Clock Lane. In order to reduce power consumption, set to be “disable” when PPI-TX is not used. 0: Disable (Default) 1: Enable

Set this register before setting [STARTCNTRL].START = 1.

5.2.37 TXOPTIONCNTRL (TXOPTIONCNTRL: 0x0238)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							CONTCLK MODE
Type	RO	RO	RO	RO	RO	RO	RO	R/W
Default	0	0	0	0	0	0	0	0

Table 5-38 TXOPTIONCNTRL

Register Field	Bit	Default	Description
Reserved	[15:1]	0x0	
CONTCLKMODE	[0]	0x0	Set Continuous Clock Mode Writing “1” to this bit will set the Clock Lane to the Continuous Clock mode regardless of the PPI interface signal and will maintain the Clock Lane output. 0: Non-continuous clock mode. Transitions into the LP11 state in coordination with the Data Lane operation. 1: Continuous clock mode. Maintains the Clock Lane output regardless of the Data Lane operation.

This bit can be rewritten when [STATUS].BUSY is set.
Set this register before setting [STARTCNTRL].START = 1. Do not change this register after START = 1 is set.

5.2.38 BTACNTRL1 (BTACNTRL1: 0x023C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved					TXTAGOCNT[10:8]		
Type	RO	RO	RO	RO	RO	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	TXTAGOCNT[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	1	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					RXTASURECNT[10:8]		
Type	RO	RO	RO	RO	RO	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	RXTASURECNT[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	1	0	0	0

Table 6-29 BTACNTRL1

Register Field	Bit	Default	Description
Reserved	[31:27]	0x0	
TXTAGOCNT	[26:16]	0x8	The TTA-GO period (LP-00 drive period) when drive privileges are released by BTA is set by the setting of this counter. The period for driving LP-00 for the TTA-GO period is 4 x (TXTAGOCNT + 1) x (HSByteClk cycle). Set so that the TTA-GO period (4 x TLPX) described in the MIPI D-PHY specifications results.
Reserved	[15:11]	0x0	
RXTASURECNT	[10:0]	0x8	The timing for starting driving of LP-00 in the TTA-SURE period when drive privileges are obtained by BTA is set by the setting of this counter. The drive start timing is (RXTASURECNT + (3 or 2)) x (HSByteClk cycle) cycle. Set so as to be within the TTA-SURE period (Min TLPX, Max 2 x TLPX) range described in the MIPI D-PHY specifications.

Set this register before setting [STARTCNTRL].START = 1.

5.2.39 DSI Control Register (DSI_CONTROL: 0x040C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	dsi_mode	Reserved	PrToEn	TaToEn	LrxToEn	HtxToEn	CntDis	EccDis
Type	RO	RO	RO	RO	RO	RO	RO	RO

Default	1	0	1	1	1	1	1	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	TxMd	CrcDis	HsCkMd	Reserved		NOL[1:0]		EoTDis
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 5-39 DSI Configuration Register

Register Field	Bit	Default	Description
dsi_mode	15	0x1	**DSI Mode Selection** 0: DSI Mode 1: Reserved
PrToEn	13	0x1	**PR_TO_EN** 0: Disables the PR_TO timer. 1: Enables the PR_TO timer.
TaToEn	12	0x1	**TA_TO_EN** 0: Disables the TA_TO timer. 1: Enables the TA_TO timer.
LrxToEn	11	0x1	**LPRX_TO_EN** 0: Disables the LRX-H_TO timer. 1: Enables the LRX-H _TO timer.
HtxToEn	10	0x1	**HSTX_TO_EN** 0: Disables the HTX_TO timer. 1: Enables the HTX_TO timer.
CntDis	9	0x1	**CONTENTION_DIS** This bit disables contention detection.
EccDis	8	0x0	**ECC_DISABLE** This bit sets operation for when there are multiple-bit ECC errors in the received data. If multiple-bit ECC errors are detected, the ECC Error multi bit (bit 9) bit of the DSI_RXERR register is asserted to “1” regardless of this bit’s setting. In the case of ECC single-bit errors, the setting of this bit has no effect on the operation. Single-bit errors can be corrected, so the corrected data can be stored in the Receive FIFO regardless of this bit’s setting. At this time, the ECC Error single bit (bit 8) bit of the DSI_RXERR is asserted to “1”, and the settings of the DSI_ERR_HALT, and DSI_ERR_INTENA registers are valid. 0: If there are multiple-bit ECC errors in the received data, subsequent processes including the fetching of data from the peripheral interface are terminated and wait for the LP Stop state. Loading to the Receive FIFO of the corresponding packets is not performed. 1: Even if multiple-bit ECC errors are detected in the received data, subsequent processes including the fetching of data from the peripheral interface continue. Either the packet in which multiple bit ECC errors were detected is loaded into the Receive FIFO or the corresponding package waits for a valid Data Type. If the Data Type is invalid, the DSI Data Type no recognized (bit 11) bit of the DSI_RXERR register is set to “1” and the packet is discarded. If a valid Data Type is recognized, the packet is stored

			in the Receive FIFO. In the case of a long packet, processing continues up to the reception of the data payload.
TxMd	7	0x0	**TXMODE** 0: Low power transfer is performed to Tx. 1: High-Speed data transfer is performed to Tx.
CrcDis	6	0x0	**CRC_DISABLE** Operation for when a CRC error was found in the received data is set. (For long packets only) 0: CRC checking of received long packets is performed. If CRC errors exist in the received data, the CRC Error bit (bit 10) of the DSI_RXERR register is asserted to "1". Transfers to the Receive FIFO for the received data are performed. 1: CRC checking of received long packets is not performed. Even if there are CRC errors in the received data, no notification is made to the DSI_RXERR register. The CRC errors are ignored and transfers to the Receive FIFO for the received data are performed.
HsCkMd	5	0x0	**HSCLOCKMODE** 0: Operation is in the discontinuous clock mode. 1: Operation is in the continuous clock mode.
Reserved	[4:3]	0x0	
NOL	[2:1]	0x0	**NOL** This field specifies the number of HS lanes. This field is also used as the LP Lane Enable setting. Data Lane 0 is used as the Enable for LP communication and ULPS. Data Lane 1 or higher is used as the Enable for ULPS. This setting can only be made during initial setup or during reset. 00: Only Data Lane 0 is used. 01: Data Lanes 0 and 1 are used. 10: Data Lanes from 0 to 2 are used. 11: Data Lanes 0 to 3 are used.
EoTDis	0	0x0	**EOT_DISABLE** 0: The EOT packet is automatically granted at the end of HS transfer then is transmitted. 1: The EOT packet is not automatically granted at the end of HS transfer and is not transmitted.

Only indirect writing, i.e. write to DSI_CONFW with [Addr] = 0x03.

5.2.40 DSI STATUS Register (DSI_STATUS: 0x0410)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						TxAct	RxAct
Type	RO						RO	RO
Default	0xX						0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	RxAF	RxAE	RxEm	Reserved				Hlt
Type	RO	RO	RO	RO				RO
Default	0	1	0	0x0X				0

Table 5-40 DSI STATUS Register

Register Field	Bit	Default	Description
Reserved	[15:10]	X	
TxAct	9	0	**Transmitter Active** This bit indicates that the DSI-TX module is in the Transmit mode.
RxAct	8	0	**Receiver Active** This bit indicates that the DSI-TX module is in the Receive mode.
RxAF	7	0x0	**FIFO_ALMOSTFULL** This bit indicates that the Receive FIFO is almost full (has less than 3 empty slots).
RxAE	6	0x1	**FIFO ALMOST EMPTY** This bit indicates that the Receive FIFO is almost empty (has less than 2 entries).
RxEm	5	0x0	**FIFO EMPTYn** This bit indicates that the Receive FIFO is **not** empty.
Reserved	[4:1]	X	
Hlt	0	0	**Halted** The DSI-TX module is stopped by either an error or a pause request.

5.2.41 DSI_INT Register (DSI_INT: 0x0414)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved					IntAck	Reserved	
Type	RO					RO	RO	
Default	0x00					0	0x00	
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved				IntHlt	IntEr	IntRxEr	IntAkEr
Type	RO				RO	RO	RO	RO
Default	0x00				0	0	0	0

Table 5-41 DSI_INT Register

Register Field	Bit	Default	Description
Reserved	[31:19]	0x0	
IntAk	18	0x0	**INT_ACK**

Register Field	Bit	Default	Description
			This bit indicates that the Acknowledge trigger has been received.
Reserved	[17:4]	0x0	
IntHlt	3	0x0	**INT_HALTED** The DSI-TX module was stopped by an error or a pause request.
IntEr	2	0x0	**INT_DSI_ERR** An interrupt was requested by a DSI_ERR register error.
IntRxEr	1	0x0	**INT_DSI_RXERR** An interrupt was requested by a DSI_RXERR register error.
IntAkEr	0	0x0	**INT_DSI_ACKERR** An interrupt was requested by a DSI_ACKERR register error.

Each bit can indirectly clear a register value either when "1" is written to the bit of each corresponding DSI_INT_CLR register.

5.2.42 DSI_INT_ENA Register (DSI_INT_ENA: 0x0418)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved					IEnAk	Reserved	
Type	RO					RO	RO	
Default	0x00					0	0x0	
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved				IEnHlt	IEnEr	IEnRxEr	IEnAkEr
Type	RO				RO	RO	RO	RO
Default	0x0				0	0	0	0

Table 5-42 DSI_INT_ENA Register

Register Field	Bit	Default	Description
Reserved	[31:19]	0x0	
IEnAk	18	0x0	**INTENA_ACK** This bit enables interrupt notification by INT_ACK sources.
Reserved	[17:4]	0x0	
IEnHlt	3	0x0	**INTENA_HALTED** This bit enables interrupt notification by INT_HALTED sources.
IEnEr	2	0x0	**INTENA_DSI_ERR** This bit enables interrupt notification by INT_DSI_ERR sources.

Register Field	Bit	Default	Description
IEnRxEr	1	0x0	**INTENA_DSI_RXERR** This bit enables interrupt notification by INT_DSI_RXERR sources.
IEnAkEr	0	0x0	**INTENA_DSI_ACKERR** This bit enables interrupt notification by INT_DSI_ACKERR sources.

Only indirect writing, i.e. write to DSI_CONFW with [Addr] = 0x06.

5.2.43 DSI Command Read Data FIFO Register (DSICMD_RDFIFO: 0x0430)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	RDDATA[31:24]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	RDDATA[23:16]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	RDDATA[15:8]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	RDDATA[7:0]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 5-43 DSI Command Read Data FIFO Register

Register Field	Bit	Default	Description
RDDATA	[31:0]	0x0	**RDDATA** Data received from the peripheral interface via the DSI link is written to this register.

The data received via a DSI link was written to this register.

5.2.44 DSI_ACKERR Register (DSI_ACKERR: 0x0434)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	ACKERR_REPORT[15:8]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACKERR_REPORT[7:0]							

Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 6-29 ACKERR_REPORT Register

Register Field	Bit	Default	Description
Reserved	[31:16]	0x0	
ACKERR_REPORT	[15:0]	0x0	**ACKERR_REPORT** The content of the Acknowledge packet with report of the last error received is held.

The content of the DSI_ACKERR register is cleared when the register is read.

5.2.45 DSI_ACKERR_INTENA Register (DSI_ACKERR_INTENA: 0x0438)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	DSI_ACKERR_INTENA[15:8]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DSI_ACKERR_INTENA[7:0]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 5-44 DSI_ACKERR_INTENA Register

Register Field	Bit	Default	Description
Reserved	[31:16]	0x0	
DSI_ACKERR_INTENA	[15:0]	0x0	**DSI_ACKERR_INTENA** This field sets the generation of interrupts when an acknowledge packet with error report is received. Setting each bit in this field enables generation of the DSI_ACKERR_INT interrupt which corresponds to the DSI_ACKERR register error.

Only indirect writing, i.e. write to DSI_CONFW with [Addr] = 0x0E.

5.2.46 DSI_ACKERR_HALT Register (DSI_ACKERR_HALT: 0x043C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	DSI_ACKERR_HALT[15:8]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DSI_ACKERR_HALT[7:0]							

Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 5-45 DSI_ACKERR_HALT Register

Register Field	Bit	Default	Description
Reserved	[31:16]	0x0	
DSI_ACKERR_HALT	[15:0]	0x0	**DSI_ACKERR_HALT** This field controls operation of the DSI-TX module when an acknowledge packet with error report is received. The DSI-TX module halts command processes when an error is received for which the corresponding bit in the DSI_ACKERR_INTENA and DSI_ACKERR_HALT registers is set.

Only indirect writing, i.e. write to DSI_CONFW with [Addr] = 0x0F.

5.2.47 DSI_RXERR Register (DSI_RXERR: 0x0440)

Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved			TATo	RxHTo	Reserved	FOvrFlw	Reserved
Type	RO			RO	RO	RO	RO	RO
Default	0			0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved		InCmplTx	Reserved	DTErr	CRCErr	ECCSErr	ECCMErr
Type	RO		RO	RO	RO	RO	RO	RO
Default	0		0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	LPCtlErr	Reserved	LPSyncErr	EscErr	Reserved		
Type	RO	RO	RO	RO	RO	RO		
Default	0	0	0	0	0	0		

Table 6-29 DSI_RXERR Register

Register Field	Bit	Default	Description
Reserved	[31:21]	0x0	
TATo	20	0x0	**TA_TO** This bit indicates direction change acknowledgement timeouts.
RxHTo	19	0x0	**LRX-H_TO** This bit indicates LP-RX host processor timeouts.
Reserved	18	0x0	
FOvrFlw	17	0x0	**FIFO_OVERFLOW** This bit indicates Receive FIFO overflows.
Reserved	[16:14]	0x0	
InCmplTx	13		Incomplete Tx

Reserved	12	0x0	
DTErr	11		DSI packet Data Type is not reconized
CRCErr	10		CRC Error
ECCSErr	9		ECC Error, Single bit
ECCMErr	8		ECC Error, Multi- bits
Reserved	7	0x0	
CtlErr	6		False Control Error
Reserved	5		
LPSyncErr	4		LP Sync Error
EscErr	3		Escape Mode Entry Error
Reserved	[2:0]	0x0	

The content of the DSI_RXERR register is cleared when the register is read.

5.2.48 DSI_RXERR_INTENA Register (DSI_RXERR_INTENA: 0x0444)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved			DSI_RXERR_INTENA[20:16]				
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	DSI_RXERR_INTENA[15:8]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DSI_RXERR_INTENA[7:0]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 5-46 DSI_RXERR_INTENA Register

Register Field	Bit	Default	Description
Reserved	[31:21]	0x0	
DSI_RXERR_INTENA	[20:0]	0x0	**DSI_RXERR_INTENA** This field controls generation of interrupts when the DSI_RXERR register is notified of an error. Each bit in this field enables generation of the DSI_RXERR_INT interrupt which corresponds to the DSI_RXERR register error.

Only indirect writing, i.e. write to DSI_CONFW with [Addr] = 0x11.

5.2.49 DSI_RXERR_HALT Register (DSI_RXERR_HALT: 0x0448)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved			DSI_RXERR_HALT[20:16]				
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	DSI_RXERR_HALT[15:8]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DSI_RXERR_HALT[7:0]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 5-47 DSI_RXERR_HALT Register

Register Field	Bit	Default	Description
Reserved	[31:21]	0x0	
DSI_RXERR_HALT	[20:0]	0x0	**DSI_RXERR_HALT** This field controls DSI-TX operation for when an error has been reported to the DSI_RXERR register. The DSI-TX module stops command processing when it receives an error corresponding to the set bits in the DSI_RXERR_INTENA and DSI_RXERR_HALT registers.

Only indirect writing, i.e. write to DSI_CONFW with [Addr] = 0x12.

5.2.50 DSI_ERR Register (DSI_ERR: 0x044C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						InEr	WCEr
Type	RO						RO	RO
Default	0x00						0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SynTo	RxFRdEr	TeEr	QUnk	QWrEr	HTxTo	HTxBrk	Cntn

Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 6-29 DSI_ERR Register

Register Field	Bit	Default	Description
Reserved	[31:10]	0x0	
InEr	9	0x0	**INTERNAL_ERROR** This bit indicates that another internal error occurred.
WCEr	8	0x0	**WC_ERROR** This bit indicates that more bytes than expected were received from the PDIF. Because distinguishing the current data from the next payload data of continuous transfers is difficult when the last payload data is 4-byte aligned, this error is not detected.
SynTo	7	0x0	**SYNC_TO** This bit indicates that a synchronous wait timeout occurred.
RxFRdEr	6	0x0	**RXFIFO_RDERR** This bit indicates that an empty Receive FIFO was read.
TeEr	5	0x0	**TE_ERROR** This bit indicates that the peripheral interface did not transmit the tearing trigger the DSI-TX module is expecting.
QUnk	4	0x0	**CQ_UNKNOWN** This bit indicates that an unknown command or incorrect parameter was detected by the command queue.
QWrEr	3	0x0	**CQ_WRERR** This bit indicates that Write access to a full command queue occurred.
HTxTo	2	0x0	**HTX_TO** This bit indicates that a High-Speed TX timeout occurred.
HTxBrk	1	0x0	**HSTX_BROKEN** This bit indicates that the byte stream was disrupted during High-Speed transfer.
Cntn	0	0x0	**CONTENTION** This bit indicates that a contention was detected during lower power transfer.

The content of the DSI_ERR register is cleared by reading it out.

5.2.51 DSI_ERR_INTENA (DSI_ERR_INTENA: 0x0450)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						DSI_ERR_INTENA[9:8]	
Type	RO						RO	
Default	0x00						0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	DSI_ERR_INTENA[7:0]							
Type	RO							
Default	0x00							

Table 5-48 DSI_ERR_INTENA Register

Register Field	Bit	Default	Description

Reserved	[31:10]	0x0	
DSI_ERR_INTENA	[9:0]	0x0 (??)	**DSI_ERR_INTENA** This field controls interrupt generation for when an error has been reported to the DSI_ERR register. Generation of the DSI_ERR_INT interrupt which corresponds to the DSI_ERR register error is enabled.

Only indirect writing, i.e. write to DSI_CONFW with [Addr] = 0x14.

5.2.52 DSI_ERR_HALT Register (DSI_ERR_HALT: 0x0454)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						DSI_ERR_HALT[9:8]	
Type	RO						RO	
Default	0x00						0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	DSI_ERR_HALT[7:0]							
Type	RO							
Default	0x00							

Table 5-49 DSI_ERR_HALT Register

Register Field	Bit	Default	Description
Reserved	[31:10]	0x0	
DSI_ERR_HALT	[9:0]	0x0 (??)	**DSI_ERR_HALT** This field controls DSI-TX operation for when an error is reported to the DSI_ERR register. The DSI-TX module stops command processing when it receives an error corresponding to the set bits in the DSI_ERR_INTENA and DSI_ERR_HALT registers. (??)

Only indirect writing, i.e. write to DSI_CONFW with [Addr] = 0x15.

5.2.53 DSI Configuration Register (DSI_CONFW: 0x0500)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	MODE			Address				
Type	WO	WO	WO	WO	WO	WO	WO	WO
Default	0	0	0	0	0	0	0	0
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved[23:16]							
Type	WO	WO	WO	WO	WO	WO	WO	WO
Default	0	0	0	0	0	0	0	0
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	DATA[15:8]							
Type	WO	WO	WO	WO	WO	WO	WO	WO

Default	0	0	0	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	DATA[7:0]							
Type	WO	WO	WO	WO	WO	WO	WO	WO
Default	0	0	0	0	0	0	0	0

Table 5-50 DSI Configuration Write Register

Register Field	Bit	Default	Description
MODE	[31:29]	0x0	**Set or Clear AddrReg (register specified in Address field) Bits** 3'b101: Set Register Bits in AddReg as indicated in DATA field 3'b110: Clear Register Bits in AddReg as indicated in DATA field Others: Reserved
Address	[28:24]	0x0	**Address Field** 0x03: DSI_Control, 0x040C, Register 0x06: DSI_INT_ENA, 0418, Register 0x0E: DSI_ACKERR_INTENA, 0x0438, Register 0x0F: DSI_ACKERR_HALT, 0x043C, Register 0x11: DSI_RXERR_INTENA, 0x0444 Register 0x12: DSI_RXERR_ HALT, 0x0448, Register 0x14: DSI_ERR_INTENA, 0x0450, Register 0x15: DSI_ERR_ HALT, 0x0454, Register Others: Reserved
Reserved	[23:16]	0x0	
DATA	[15:0]	0x0	**DATA Field** When location DATA[n] is set to '1', the corresponding bit at AddrReg [n] will be cleared or set depending on MODE bits described above. Multiples bits can be set simultaneously

Note: Write to DSI_CONFW Register results to changes in corresponding bit changed in Addressed Register.

5.2.54 DSI LP Command (DSI_LPCMD: 0x0500)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	LP Command							
Type	WO	WO	WO	WO	WO	WO	WO	WO
Default	0	0	1	1	0	0	0	0
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved[23:16]							
Type	WO							
Default	0xXX							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[15:8]							
Type	WO							
Default	0xXX							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**

Name	LANE_ENA					LP_Code
Type	WO	WO	WO	WO	WO	WO
Default	0	0	0	0	0	0

Note: This command share the same register as DSI_CONFW. It is in LP command mode when [31:24] = 0x 30

Table 5-51 DSI Configuration Write Register

Register Field	Bit	Default	Description
LPCommand	[31:24]	0x0	**LP Command Mode Selection** 8'h30: Set Register Bits to this value to enable LP Command mode Others: Reserved
Reserved	[23:8]	0x0	Reserved
LANE_ENA	[7:3]	0x0	**LANE Enable Field** This Lane Enable is only used by LPC_CODE 000 (ULPS transition) and 001 (LP Stop transition). Select the following Lanes within the range of Lanes set to "Enable" by DSI_CONTROL[NOL]. Do not set ULPS transition and LP Stop transition for Lanes that have not been set to "Enable" by the NOL bit. LANE_ENA[3]: Select Clock Lanes LANE_ENA[4]: Select Lane 0 LANE_ENA[5]: Select Lane 1 LANE_ENA[6]: Select Lane 2 LANE_ENA[7]: Select Lane 3
LP_CODE	[2:0]	0x0	000: The Lane indicated by LANE_ENA transitions to ULPS (the ultra low power state). 001: The Lane indicated by LANE_ENA transitions to the LP stop state. 010: A remote application reset trigger is transmitted to Lane 0. Then, Lane 0 returns to the LP stop state. The state of other Lanes is not affected. 011: Bus direction change (BTA) is executed on Lane 0. After BTA, Lane 0 returns to the LP Stop state. Other Lanes are not affected. Others: Reserved

Note: Setting 0x0500 = 0x300000F8 will put the clock lane and all the data lanes into ULPS mode. While sending any packet during ULPS mode will cause DSI link to exit ULPS mode.

5.2.55 DSI_RESET Register (DSI_RESET: 0x0504)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			RstRxF	Reserved		RstCnf	RstMdl
Type	RO			R/W	RO		R/W	R/W
Default	0			0	0		0	0

Table 5-52 DSI_RESET Register

Register Field	Bit	Default	Description
Reserved	[31:5]	0x0	
RstRxF	4	0x0	**RST_RXFIFO** 0: Operation is not affected. 1: The Receive FIFO is reset.
Reserved	[3:2]	0x0	Reserved
RstCnf	1	0x0	**RST_CONF** 0: Operation is not affected.

			1: The setting register is reset.
RstMdl	0	0x0	**RST_MODULE** Do not set this bit to "1". Perform a hardware reset when a DSITX block reset is necessary. Use this bit when resetting the sub modules inside this block (DSI layer). The PHY layer or the application layer blocks are not reset. 0: Operation is not affected. 1: Modules inside the DSI layer are reset.

5.2.56 DSI_INT_CLR Register (DSI_INT_CLR: 0x050C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved					ICrAk	Reserved	
Type	RO					WO	RO	
Default	0x00					0	0x0	
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved				ICrHlt	ICrEr	ICrRxEr	ICrAkEr
Type	RO				WO	WO	WO	WO
Default	0x0				0	0	0	0

Table 5-53 DSI_INT_CLR Register

Register Field	Bit	Default	Description
Reserved	[23:19]	0x0	
ICrAk	18	0x0	**INTCLR_ACK** 0: Operation is not affected. 1: The INT_ACK interrupt is cleared.
Reserved	[17:4]	0x0	Reserved
ICrHlt	3	0x0	**INTCLR_HALTED** 0: Operation is not affected. 1: The INT_HALTED interrupt is cleared.
ICrEr	2	0x0	**INTCLR_DSI_ERR** 0: Operation is not affected. 1: The INT_DSI_ERR interrupt is cleared.
ICrRxEr	1	0x0	**INTCLR_DSI_RXERR** 0: Operation is not affected. 1: The INT_DSI_RXERR interrupt is cleared.

Register Field	Bit	Default	Description
ICrAkEr	0	0x0	**INTCLR_DSI_ACKERR** 0: Operation is not affected. 1: The INT_DSI_ACKERR interrupt is cleared.

5.2.57 DSI START Register (DSI_START: 0x0518)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[15:8]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved[7:1]							Strt
Type	RO	RO	RO	RO	RO	RO	RO	WO
Default	0	0	0	0	0	0	0	0

Table 5-54 DSI_START

Register Field	Bit	Default	Description
Reserved	[15:1]	0x0	
Strt	0	0x0	**DSI_START** 0: The clock is not supplied to modules other than CONIF. 1: The clock is supplied to all modules. When “1” is written to this bit, the clock is supplied to modules other than the DSI-TX CONIF. To start DSI-TX operation, set this bit to “1” after a reset is performed. This bit must be set to “1” even when accessing registers other than DSI_START. Once this bit is set to “1”, writing of “0” is not allowed. Perform a reset to change this bit from “1” to “0”.

5.2.58 DSI Command Packet Start Transmit Register (DSICMD_TX: 0x0600)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							dc_start
type	RO							R/W
Default	0x0							0x0

Table 5-55 DSI Command Packet Start Transmit Register

Register Field	Bit	Default	Description
Reserved	[15:1]	0x0	Reserved
dc_start	[0]	0x0	**DCS Command Start** 1’b0: Idle

Register Field	Bit	Default	Description
			1'b1: Start DCS Command transfer Note: This bit will be reset after DCS command send out to DSITX

5.2.59 DCS Command Type Register (DSICMD_TYPE: 0x0602)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	PktType							
type	R/W							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Data ID							
type	R/W							
Default	0x0							

Table 5-56 DSI Command Packet Type Register

Register Field	Bit	Default	Description
PktType	[15:8]	0x0	**DSI Short or Long Packet Type** There are only two valid values: 0x10: DSI Short Packet 0x40: DSI Long Packet Others : Reserved
DataID	[7:0]	0x0	**DSI Packet Data ID** Please refer to MIPI DSI specification

5.2.60 DSI Command Packet Word Count Register (DSICMD_WC: 0x0604)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved				dc_wc			
type	RO				R/W			
Default	0x0				0x0			

Table 5-57 DSI Command Packet Word Count Register

Register Field	Bit	Default	Description
Reserved	[15:4]	0x0	
dc_wc	[3:0]	0x0	**DSI Command Packet Word Count**

5.2.61 DSI Command Packet Data Register 0 (DSICMD_WD0: 0x0610)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	dc_word1							
type	R/W							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	dc_word0							
type	R/W							
Default	0x0							

Table 5-58 DSI Command Packet Data Register 0

Register Field	Bit	Default	Description
dc_word1	[15:8]	0x0	Word 1 - DSI Command Packet Data Byte 1
dc_word0	[7:0]	0x0	Word 0 - DSI Command Packet Data Byte 0 Word 0 = {Byte1, Byte0}

5.2.62 DSI Command Packet Data Register 1 (DSICMD_WD1: 0x0612)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	dc_word3							
type	R/W							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	dc_word2							
type	R/W							
Default	0x0							

Table 5-59 DSI Command Packet Data Register 1

Register Field	Bit	Default	Description
dc_word3	[15:8]	0x0	Word 3 - DSI Command Packet Data Byte 3
dc_word2	[7:0]	0x0	Word 2 - DSI Command Packet Data Byte 2

5.2.63 DSI Command Packet Data Register 2 (DSICMD_WD2: 0x0614)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	dc_word5							
type	R/W							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	dc_word4							
type	R/W							
Default	0x0							

Table 5-60 DSI Command Packet Data Register 2

Register Field	Bit	Default	Description
dc_word5	[15:8]	0x0	Word 5 - DSI Command Packet Data Byte 5
dc_word4	[7:0]	0x0	Word 4 - DSI Command Packet Data Byte 4

5.2.64 DSI Command Packet Data Register 3 (DSICMD_WD3: 0x0616)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	dc_word7							
type	R/W							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	dc_word6							

type	R/W
Default	0x0

Table 5-61 DSI Command Packet Data Register 3

Register Field	Bit	Default	Description
dc_word7	[15:8]	0x0	Word 7 - DSI Command Packet Data Byte 7
dc_word6	[7:0]	0x0	Word 6 - DSI Command Packet Data Byte 6

5.2.65 DSI Event Mode Register (DSI_EVENT: 0x0620)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							tx_msel
type	RO							R/W
Default	0x0							0x0

Table 5-62 DSI Event Mode Register

Register Field	Bit	Default	Description
Reserved	[15:1]	0x0	
tx_msel	[0]	0x0	**DSI Hsync Tx Mode select** 0: Pulse mode 1: Event mode

5.2.66 DSI Vsync Width Register 1 (DSI_VSW: 0x0622)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						tx_vsw	
type	RO						R/W	
Default	0x0						0x0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	tx_vsw							
type	R/W							
Default	0x0							

Table 5-63 DSI Vsync Width Register

Register Field	Bit	Default	Description
Reserved	[15:10]	0x0	
tx_vsw	[9:0]	0x0	**Blank Line during Vertical blank** 0: illegal 1: 1 blank line **…** Note: if enable Event mode, this blank includes Vertical Back porch

5.2.67 DSI VBPR Register (DSI_VBPR: 0x0624)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						tx_vbp	
type	RO						R/W	
Default	0x0						0x0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	tx_vbp							
type	R/W							
Default	0x0							

Table 5-64 DSI VBPR Register

Register Field	Bit	Default	Description
Reserved	[15:10]	0x0	
tx_vbp	[9:0]	0x0	**Vertical Blank Back Porch in Pulse Mode** 0: 0 blank line 1: 1 blank line … Note: In Event mode, VBPR is included DSI_VSW register, this register is not used

5.2.68 DSI Vertical Active Register (DSI_VACT: 0x0626)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				tx_val			
type	RO				R/W			
Default	0x0				0x0			
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	tx_val							
type	R/W							
Default	0x0							

Table 5-65 DSI VACT Register

Register Field	Bit	Default	Description
Reserved	[15:12]	0x0	
tx_val	[11:0]	0x0	**Vertical Active Line** 0: illegal 1: 1 active line …

5.2.69 DSI Hsync Width Register (DSI_HSW: 0x0628)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	tx_hsw							
Type	R/W							
Default	0x01							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	tx_hsw							

Type	R/W
Default	0x00

Table 5-66 DSI Hsync Width Register

Register Field	Bit	Default	Description
tx_hsw	[15:0]	0x0	**Horizontal Blank Width Count** tx_hsw = INT{ ((hsw in pixel * ByteClk_freq) / PCLK_freq) * DSI #Data lane} Note: In Event mode, this count includes Horizontal Back porch

5.2.70 DSI HBPR Register (DSI_HBPR: 0x062A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	tx_hbp							
Type	R/W							
Default	0x01							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	tx_hbp							
Type	R/W							
Default	0x0							

Table 5-67 DSI HBPR Register

Register Field	Bit	Default	Description
tx_hbp	[15:0]	0x0	**Horizontal Back Porch Count in Pulse Mode** tx_hbp = INT{ ((hbp in pixel * HSByteCLK_freq) / PClk_freq) * DSI #Data lane} Note: In Event mode, HBPR is included DSI_HSW register, this register is not used

5.2.71 DSI Horizontal Active Register (DSI_HACT: 0x062C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	tx_hal							
type	R/W							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	tx_hal							
type	R/W							
Default	0x0							

Table 5-68 DSI Horizontal Active Register

Register Field	Bit	Default	Description
tx_hal	[15:0]	0x0	**Horizontal Active Line Word Count** tx_hal = (hal in pixel * #byte per pixel) Note: tx_hal indicates byte count (count by HS Byte clock)

Note: 768 output number of bytes depending on values programmed in this register.

*e.g. To transfer 1366-pixel RGB666 input with "packed" RGB666 video packets, please program 1368*18/8 = 3078 = 0x0C06 for 768 to send out 1368 pixels/line with the last two dummy pixels*

5.2.72 VBuffer Control Register (VBufCtl: 0x00E0)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	VBuf_en	Tx_en	mask	Reserved			alcnt[9:8]	
Type	R/W	R/W	R/W	RO			R/W	
Default	0x0	0x0	0x0	0x0			0x1	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	alcnt[7:0]							
Type	R/W							
Default	0x0							

Debug Active Video Line Count Register

Register Field	Bit	Description
VBuf_en	[15]	**Enable Video Buffer for I2C/SPI Write** 0: normal 1: enable I2C/SPI write to VB sram
Tx_en	[14]	**Transmit Enable** 0: Normal mode 1: Enable Tx logic
mask	[13]	**Short Packets Mask Bit** 0: Normal mode 1: Mask Out Short Pkt, such FS, FE generation for Command Mode Operation
Reserved	[12:10]	
alcnt	[9:0]	Active Line Count 10'h0: 1 line 10'h1: 2 line .. 10'h3FF: 1024 line

5.2.73 Debug Line Width Register (DBG_Width: 0x00E2)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				Db_width[11:8]			
Type	RO				R/W			
Default	0x0				0x1			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Db_awcnt[7:0]							
Type	R/W							
Default	0x0							

Debug Video Line Word Count Register

Register Field	Bit	Description
Reserved	[15:12]	
Db_width	[11:0]	Debug Total byte count in a line (include blank period) 12'h0: 1 byte 12'h1: 2 bytes .. 12'hFFE: 4095 bytes

Register Field	Bit	Description
		12'hFFF: Reserved, Do not use

5.2.74 Debug Vertical Blank Line Count Register (DBG_VBlank: 0x00E4)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved	Db_vb[6:0]						
Type	RO	R/W						
Default	0x0	0x10						

Debug Vertical Blank Register

Register Field	Bit	Description
Reserved	[15:7]	
Db_vb	[6:0]	Debug Vertical Blank line 7'h0: 1 line 7'h1: 2 line .. 7'7F:128 line

5.2.75 Debug Video Data Register (DBG_Data: 0x00E8)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Db_data[15:8]							
Type	WO							
Default	0xX							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Db_data[7:0]							
Type	WO							
Default	0xX							

Debug Video Data Register

Register Field	Bit	Description
Db_data	[15:0]	Data will be written into Video FIFO in continuous. Note: must be in multiple of 4 bytes

6 Package

The packages for TC358768AXBG are described in the figures below.

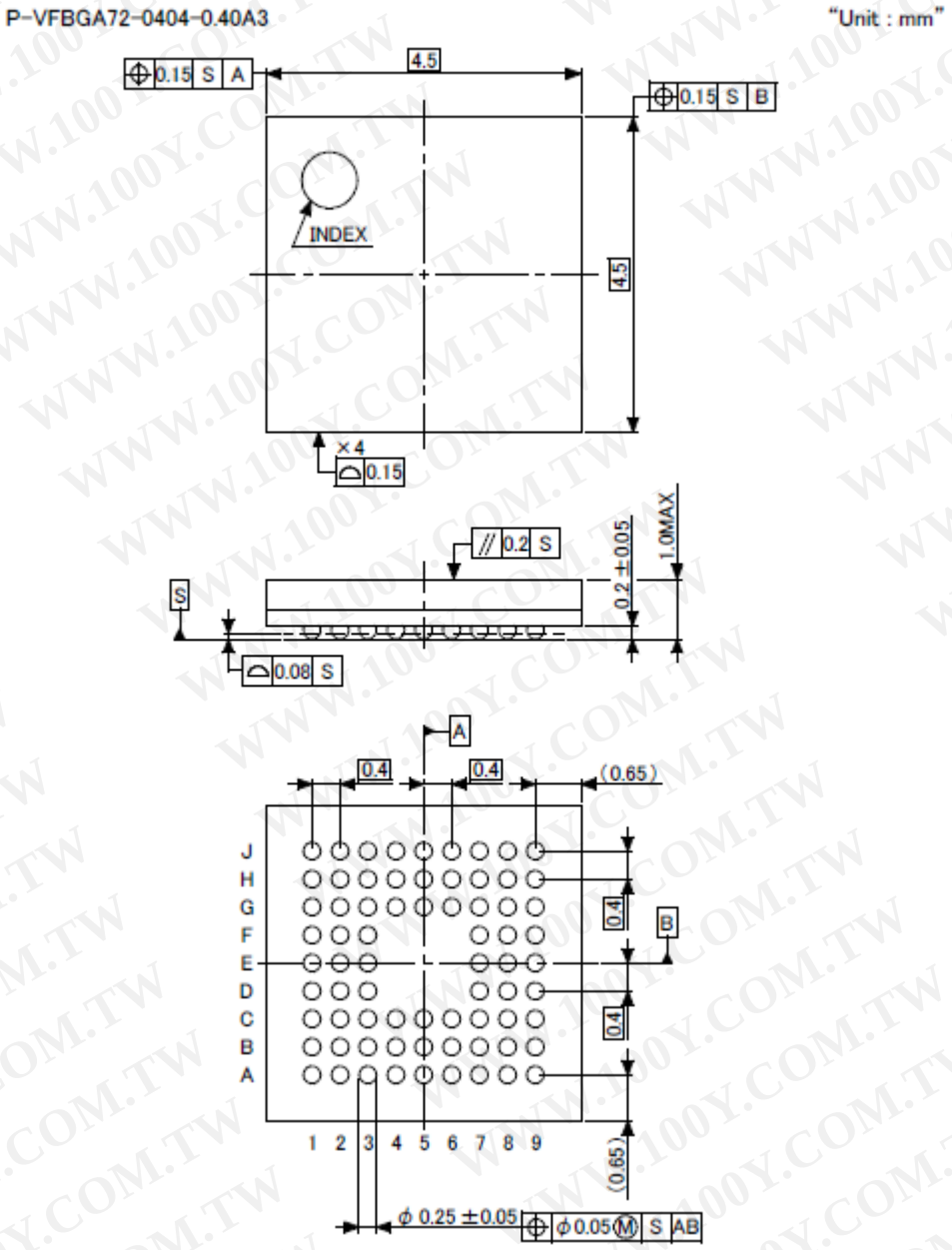


Figure 6-1 P-VFBGA72-0404-0.40A3 package

Table 6-1 P-VFBGA72-0404-0.40A3 Mechanical Dimension

Dimension	Min.	Typ.	Max.
Solder ball pitch	---	0.4 mm	---
Solder ball height	0.15 mm	0.2 mm	0.205 mm
Package dimension	---	4.5 x 4.5 mm^2	---
Package height	---	---	1.0 mm

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

VSS= 0V reference

Parameter	Symbol	Rating	Unit
Supply voltage (1.8V - Digital IO)	VDDIO	-0.3 ~ +3.9	V
Supply voltage (1.2V – Digital Core)	VDDC	-0.3 ~ +1.8	V
Supply voltage (1.2V – MIPI PHY)	VDD_MIPI	-0.3 ~ +1.8	V
Input voltage (DSI IO)	V_{IN_DSI}	-0.3 ~ VDD_MIPI+0.3	V
Output voltage (DSI IO)	V_{OUT_DSI}	-0.3 ~ VDD_MIPI+0.3	V
Input voltage (Digital IO)	V_{IN_IO}	-0.3 ~ VDDIO+0.3	V
Output voltage (Digital IO)	V_{OUT_IO}	-0.3 ~ VDDIO+0.3	V
Juntion temperature	Tj	125	^{o}C
Storage temperature	Tstg	-40 ~ +125	^{o}C

7.2 Recommended Operating Condition

VSS= 0V reference

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (1.8V – Digital IO)	VDDIO	1.65	1.8	1.95	V
Supply voltage (3.3V – Digital IO)	VDDIO	3.0	3.3	3.6	V
Supply voltage (1.2V – Digital Core)	VDDC	1.1	1.2	1.3	V
Supply voltage (1.2V – MIPI PHY)	VDD_MIPI	1.1	1.2	1.3	V
Operating temperature (ambient temperature with voltage applied)	Ta	-30	+25	+85	^{o}C
Supply Noise Voltage	V_{SN}			100	mV_{pp}

7.3 DC Electrical Specification

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input voltage, High level input Note1	V_{IH}	0.7 VDDIO		VDDIO	V
Input voltage, Low level input Note1	V_{IL}	0		0.3 VDDIO	V
Input voltage High level CMOS Schmitt Trigger Note1,2	V_{IHS}	0.7 VDDIO		VDDIO	V
Input voltage Low level CMOS Schmitt Trigger Note1,2	V_{ILS}	0		0.3 VDDIO	V

Output voltage High level (Condition: I_{OH} = -0.4mA) Note1, Note2	V_{OH}	0.8 VDDIO		VDDIO	V
Output voltage Low level (Condition: IOL = 2mA) Note1, Note2	V_{OL}	0		0.2 VDDIO	V
Input leak current, High level (Normal IO or Pull-up IO) (Condition: V_{IN} = +VDDIO, VDDIO = 3.6V)	I_{ILH1} Note3	-10	-	10	uA
Input leak current, High level (Pull-down IO) (Condition: V_{IN} = +VDDIO, VDDIO = 3.6V)	I_{ILH2} Note3	-	-	100	uA
Input leak current, Low level (Normal IO or Pull-down IO) (Condition: V_{IN} = 0V, VDDIO = 3.6V)	I_{ILL1} Note4	-10	-	10	uA
Input leak current, Low level (Pull-up IO) (Condition: V_{IN} = 0V, VDDIO = 3.6V)	I_{ILL2} Note4	-	-	200	uA

Note1 : Each power source is operating within recommended operation condition.

Note2 : Current output value is specified to each IO buffer individually. Output voltage changes with output current value.

Note3 : Normal pin or Pull-up IO pin applied VDDIO supply voltage to Vin (input voltage)

Note4 : Normal pin or Pull-down IO pin applied VSSIO (0V) to Vin (input voltage)

8 Timing Definitions

8.1 MIPI – 2 Timings

Timing specification below has been ported from Draft MIPI Alliance specification for D-PHY version 0.91.00 r0.01. Timing defined in Draft MIPI Alliance specification for D-PHY version 0.91.00 r0.01 has precedence over timing described in the sections below.

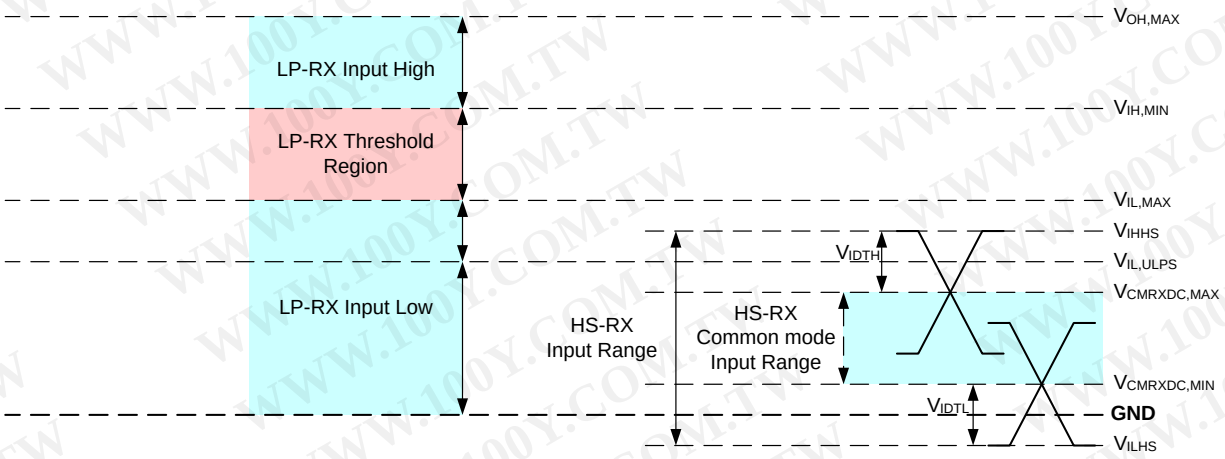


Figure 8-1 Signaling and voltage levels

Table 8-1 DC specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{PIN}	Pin signal voltage range	-50		1350	mV	
$V_{PIN(absmax)}$	Transient pin voltage	-0.15		1.45	V	
$T_{VPIN(absmax)}$	Maximum transient time above $V_{PIN(absmax)}$ or below $V_{PIN(absmax)}$.			20	ns	3
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	
V_{IH}	Logic 1 input voltage	880			mV	
V_{IL}	Logic 0 input voltage, not in ULP State			550	mV	
$V_{IL-ULPS}$	Logic 0 input voltage, ULP State			300	mV	
$V_{CMRX(DC)}$	Common-mode voltage HS receiver mode	70		330	mV	1,2
V_{IDTH}	Differential input high threshold			70	mV	
V_{IDTL}	Differential input low threshold	-70			mV	
V_{IHHS}	Single-ended input high voltage			460	mV	1

V_{ILHS}	Single-ended input low voltage	-40			mV	1

Notes:

1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
2. This table value included a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz.
3. The voltage undershoot or overshoot beyond V_{PIN} is only allowed during a single 20 ns window after any LP-0 LP-1 transition or vice versa. For all other situations it must stay within the V_{PIN} range.

Table 8-2 High Speed AC specifications

Parameter	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450MHz			100	mV	2
$\Delta V_{CMRX(LF)}$	Common-mode interference 50MHz- 450MHz	-50		50	mV	1,3

Notes:

1. Excluding `static' ground shift of 50mV
2. $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.
3. Voltage difference compared to the DC average common-mode potential.

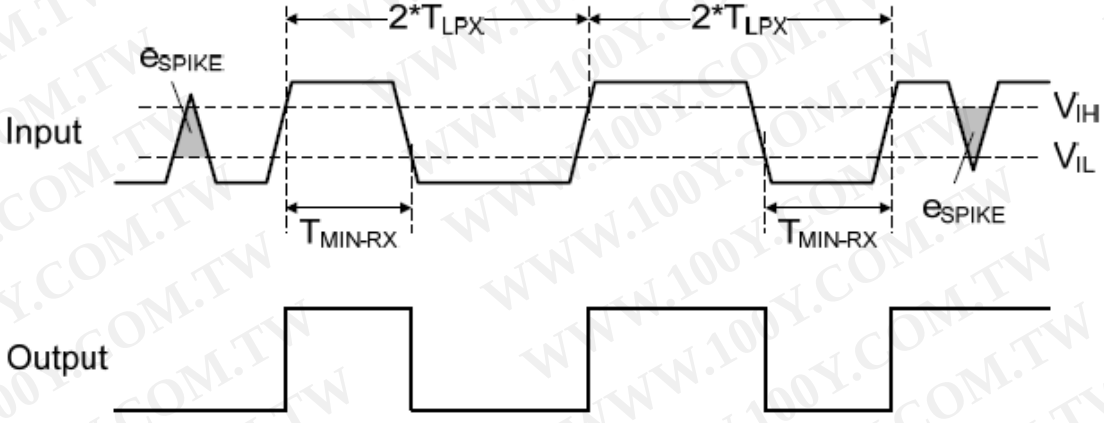


Figure 8-2 Input Glitch Rejection

Table 8-3 Low Power AC characteristics

Parameter	Description	Min	Nom	Max	Units	Notes
e_{SPIKE}	Input pulse rejection			300	V.ps	1,2,3
T_{MIN-RX}	Minimum pulse width response	20			ns	4

V_{INT}	Peak interference amplitude			200	mV	
F_{INT}	Interference frequency	450			MHz	
T_{LPX}	Length of any Low Power state period	50			ns	

Notes:

1. Time-voltage integration of a spike above V_{IL} when being in LP-0 or below V_{IH} when being in LP-1 state.
2. An impulse less than this will not change the receiver state.
3. In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
4. An input pulse greater than this shall toggle the output.

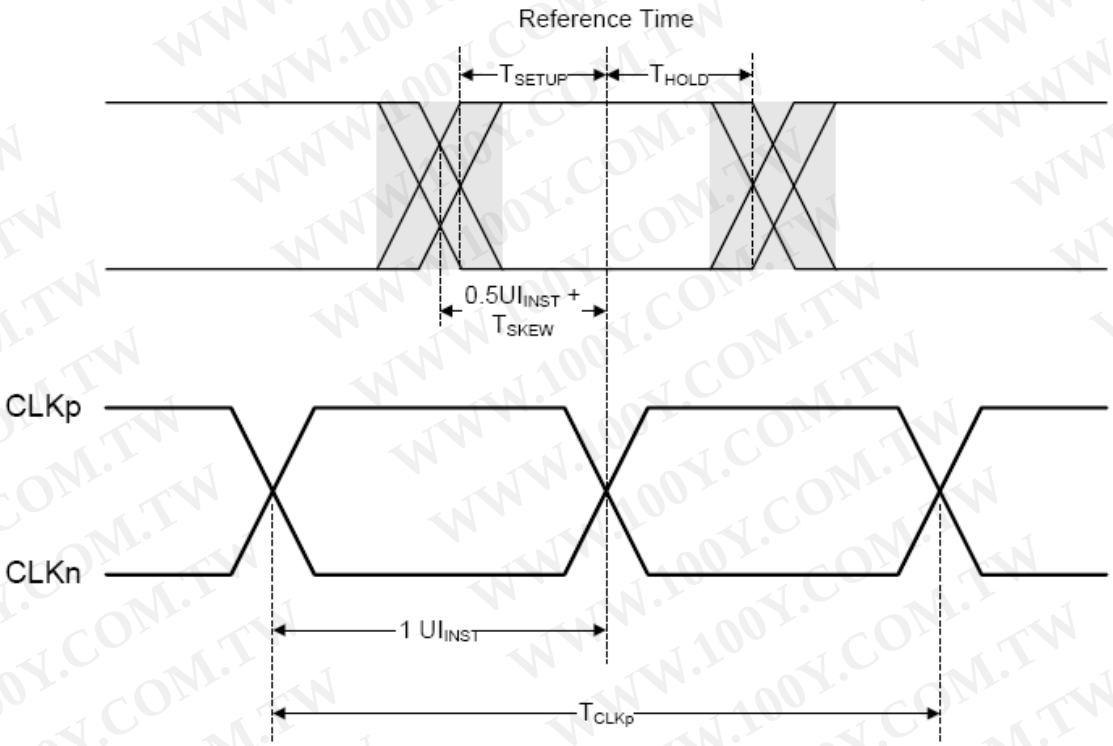


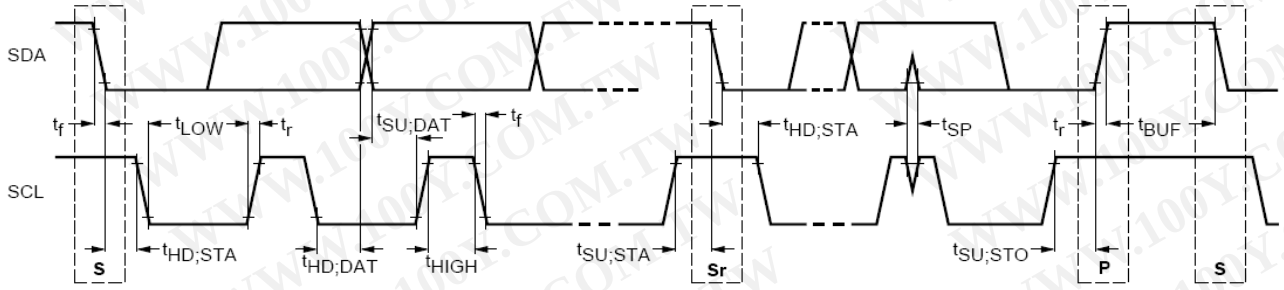
Figure 8-3 Data to clock timing reference

Table 8-4 Data-Clock timing specification

Parameter	Description	Min	Nom	Max	Units	Notes
T_{SKEW}	Data to clock skew measured at the transmitter	-0.15		0.15	UI_{INST}	
T_{SETUP}	Data to clock setup time at	0.15			UI_{INST}	

	receiver					
T_{HOLD}	clock to data hold time at receiver	0.15			UI_{INST}	
UI_{INST}	1 Data bit time (instantaneous)			12.5	ns	
T_{CLKp}	Period of dual data rate clock	2	2	2	UI_{INST}	

8.2 I2C Timings



Item	Symbol	Min	Max	Unit
SCL clock frequency	f_{SCL}	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	-	µs
LOW period of the SCL clock	t_{LOW}	1.3	-	µs
HIGH period of the SCL clock	t_{HIGH}	0.6	-	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	-	µs
Data hold time: for I2C-bus devices	$t_{HD;DAT}$	0	0.9	µs
Data set-up time	$t_{SU;DAT}$	100	-	ns
Rise time of both SDA and SCL signals	t_r	20+0.1Cb	300	ns
Fall time of both SDA and SCL signals	t_f	20+0.1Cb	300	ns

Set-up time for STOP condition	$t_{SU;STO}$	0.6	-	µs
Bus free time between a STOP and START condition	t_{BUF}	1.3	-	µs

Note: Cb = Capacitive load for each bus line (400pF max.)

8.3 Parallel Port Input Timings

Table 8-5 Parallel Input timing

Parameter	Description	Min.	Typ.	Max.	Units
$T_{pd:SU}$	Setup time of data	2	-	-	ns
$T_{pd:HD}$	Hold time of data	1	-	-	ns
$T_{pd:CLK}$	Clock period	6	-	-	ns

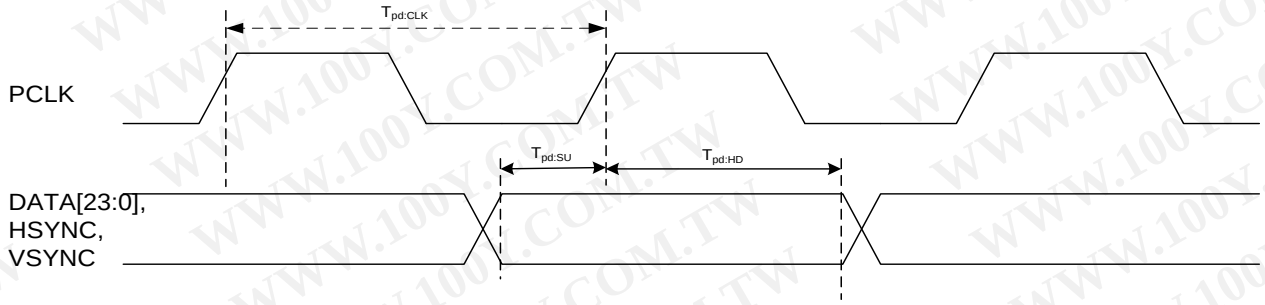


Figure 8-4 Parallel Input timing

Table 8-6 Parallel Vertical timing

Parameter	Description	Min.	Typ.	Max.	Units
T_{VP}	Vertical Sync Period	2	-	-	Lines
T_{VBP}	Vertical Back Porch	2	-	-	Lines
T_{VAFP}	Vertical Active Frame Period	16	-	4096	Lines
T_{VFP}	Vertical Front Porch	2	-	-	Lines

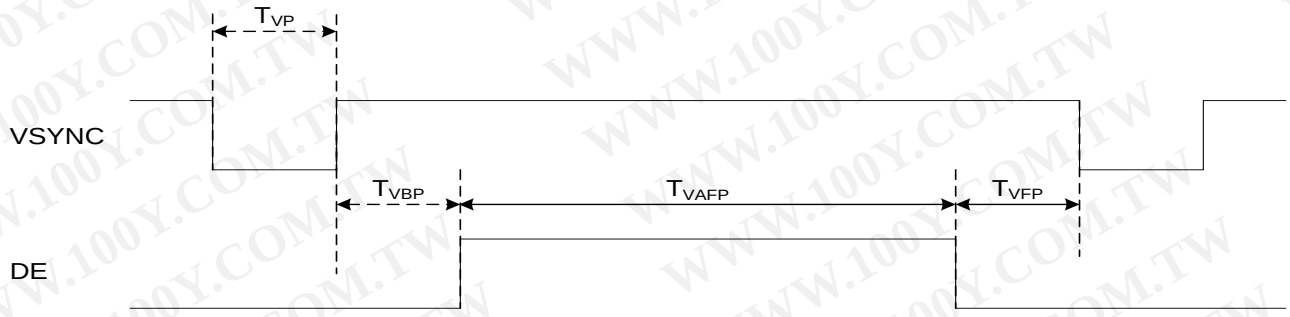


Figure 8-5 Parallel Vertical timing

Table 8-7 Parallel Horizontal timing

Parameter	Description	Min.	Typ.	Max.	Units
T_{HP}	Horizontal Sync Period	2	-	-	PCLK
T_{HBP}	Horizontal Back Porch	2	-	-	PCLK
T_{HAFP}	Horizontal Active Line Period	16	-	1920	PCLK
T_{HFP}	Horizontal Front Porch	2	-	-	PCLK

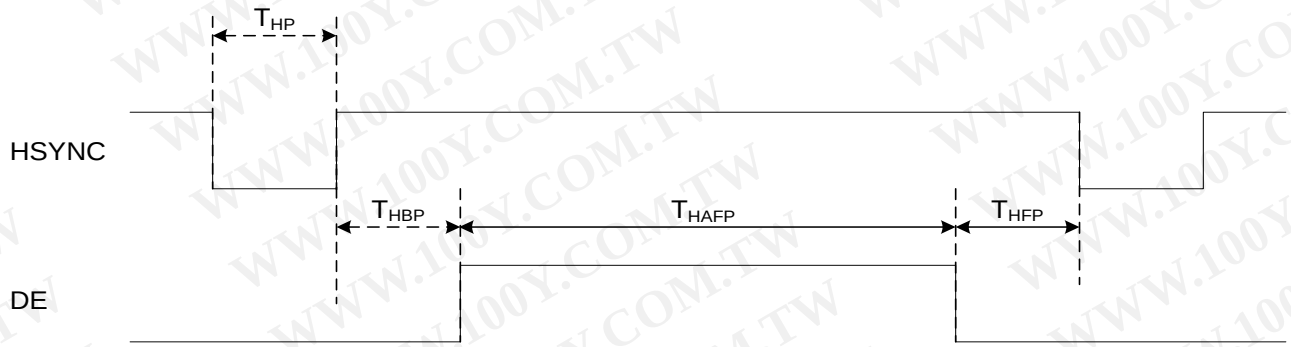


Figure 8-6 Parallel Horinzontal timing

8.4 SPI Input/Output Timings

Table 8-8 SPI timing

Parameter	Symbol	Min	Typ	Max	Unit
SPI Clock Frequency	f_{SEIS}	—	—	25	MHz
Clock to Data (MISO) Valid Time	t_{SOD}	—	—	15	ns
Clock to Data (MISO) Invalid Time	t_{SOH}	0	—	—	ns
Data in (MOSI) Setup Time	t_{SIS}	5	—	—	ns
Data in (MOSI) Hold Time	t_{SIH}	5	—	—	ns
Slave Select to Data (MISO) Valid Time	t_{SSDV}	—	—	25[1]	ns
Slave Select to Clock	t_{SSTC}	$3/f_{SYS}$	—	—	ns
Consecutive Transfer Delay Time	t_{CTDT}	$1/f_{SEIS}$	—	—	ns
Load on SEI Interface Signals	C_{IF}	—	—	10	pF

Notes: Maximum loading of MISO is 10pF

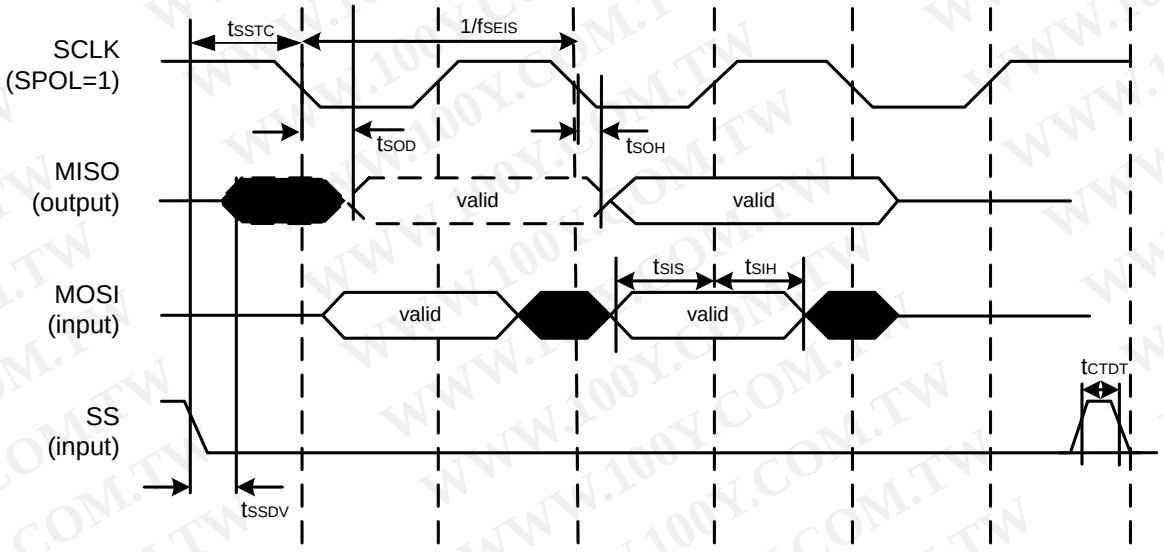


Figure 8-7 SPI timing (data valid on second active clock edge)

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