



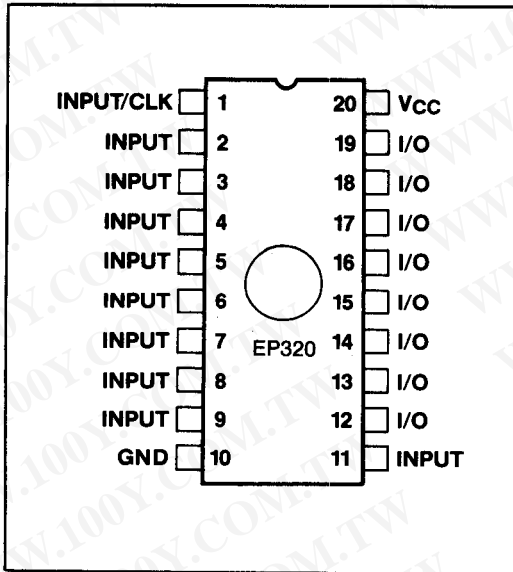
8 MACROCELL EPLD

EP320

FEATURES

- User-Configurable replacement for TTL, 74HC and 20 pin PAL Family.
- Advanced CMOS EPROM technology allows erase and reprogram.
- "Zero Power" (typically 10 $\mu$ A standby).
- High speed, tpd = 30ns.
- User-Configurable I/O architecture allows output and feedback paths to be configured for registered or combinatorial modes, active high or active low.
- 100% generically testable—provides 100% programming yield.
- Programmable "Security Bit" allows total protection of proprietary designs.
- Advanced software support allows convenience of 4 different design entry methods, complete Boolean minimization and automatic fitting into an EP320.

CONNECTION DIAGRAM



GENERAL DESCRIPTION

The Altera EP320 Erasable Programmable Logic Device may be used as a replacement for TTL and 74HC. It also provides a high speed, low power "plug compatible" replacement for fuse-based programmable logic devices.

The EP320 can accommodate up to 18 inputs and up to 8 outputs. The 20 pin, 300 mil package contains 8 Macrocells, each of which utilizes a programmable AND fixed OR structure. This AND-OR structure yields 8 product terms for the logic function as well as an individual product term for Output Enable.

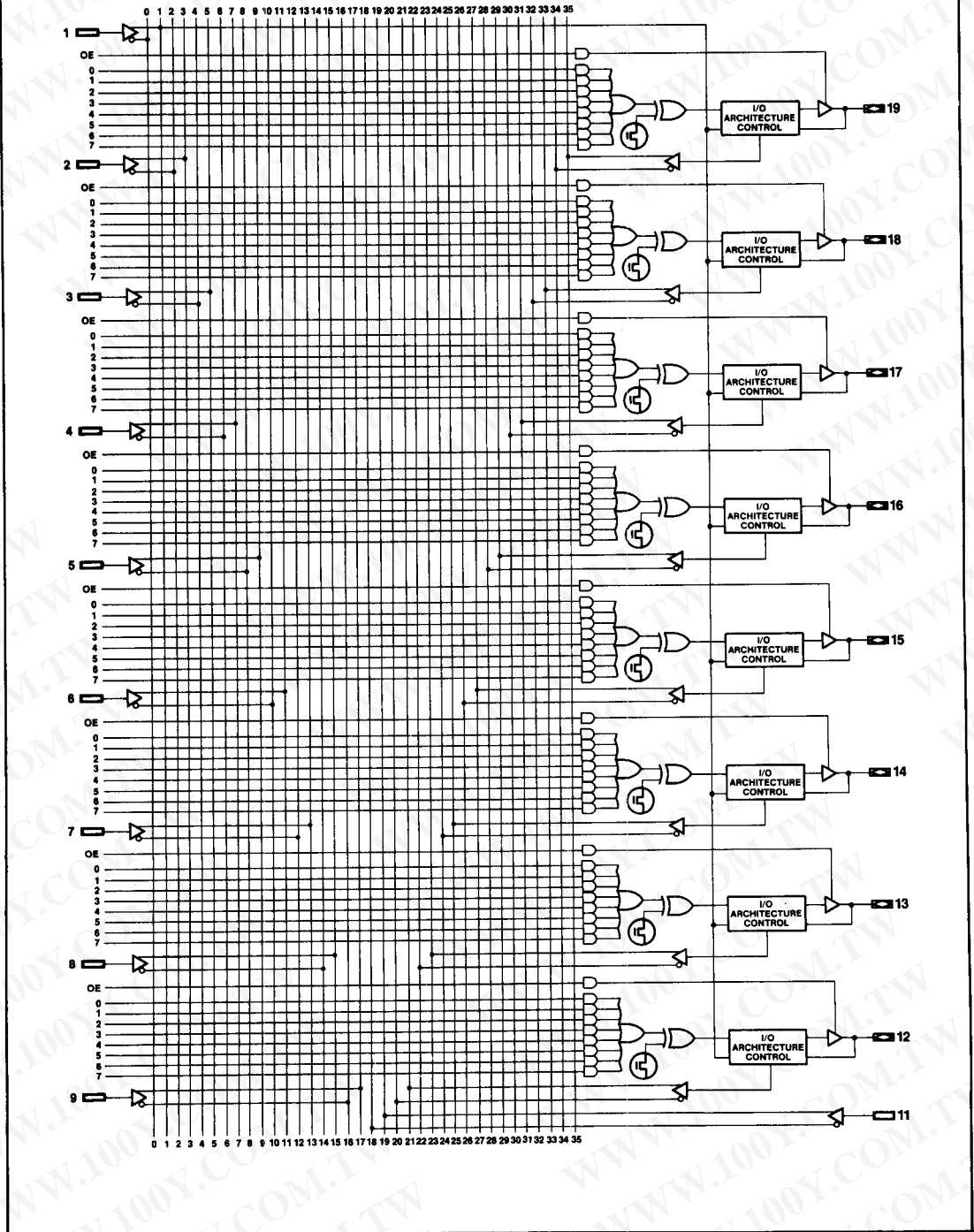
The Altera proprietary programmable I/O architecture allows the EP320 user to configure output and feedback paths for combinatorial or registered operation, active high or active low. As a result, the EP320 may be configured as a drop in replacement for PAL devices such as the 16R8 and 16L8.

In addition to architectural flexibility, performance characteristics allow the EP320 to be used in the widest possible range of applications. The CMOS EPROM technology helps make the EP320 a zero power device at standby as well as allowing for an active power consumption of less than 20% of equivalent bipolar devices without sacrifice in speed performance. This technology also facilitates 100% generic testability as well as UV erasability. As a result, designs and design modifications may be quickly implemented upon a given EP320 without the need for post programming testing.

Programming the EP320 is made easy with the Altera A+PLUS development software (A+PLUS version 4.5 or later release). Using A+PLUS, the user may enter his logic design using schematic capture, netlist entry, Boolean equations and state machine entry. Once the design is entered, A+PLUS performs automatic translation into logical equations, complete Boolean minimization and design fitting directly to an EP320. The device can then be programmed to achieve customized working silicon within minutes at the designer's own desktop.

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Figure 1. EP320 Block Diagram



### FUNCTIONAL DESCRIPTION

The EP320 is an Erasable Programmable Logic Device (EPLD) in which CMOS EPROM technology is utilized in order to configure connections in a programmable AND logic array. EPROM connections are also used as a means to control the desired output/feedback options (such as registered or combinatorial, active high or active low).

Externally, the EP320 provides 10 dedicated inputs (one of which may be used as a synchronous clock input) and 8 I/O pins which may be configured for input, output or bi-directional operation.

Figure 1 shows the complete EP320 block diagram, while Figure 2 shows the basic EP320 macrocell. The internal architecture is organized with the familiar sum of products (AND-OR) structure. Inputs to the programmable AND array (seen running vertically in Figure 2) come from two sources: a) the true and complement of the 10 dedicated input pins and; b) the true and complement of 8 feedback signals, each one originating from an I/O Architecture Control Block. The 36 input AND array encompasses a total of 72 product terms distributed equally among the 8 Macrocells. Each product term (seen running horizontally in Figure 1) represents a 36 input AND gate.

As seen in Figure 1, the outputs of 8 product terms are "ORed" together, then the output of the OR gate is fed as an input to an XOR gate. The purpose for this XOR function is to allow the user to specify the polarity of the output signal by using the "Invert Select" EPROM CELL. (Active high if EPROM cell is programmed,

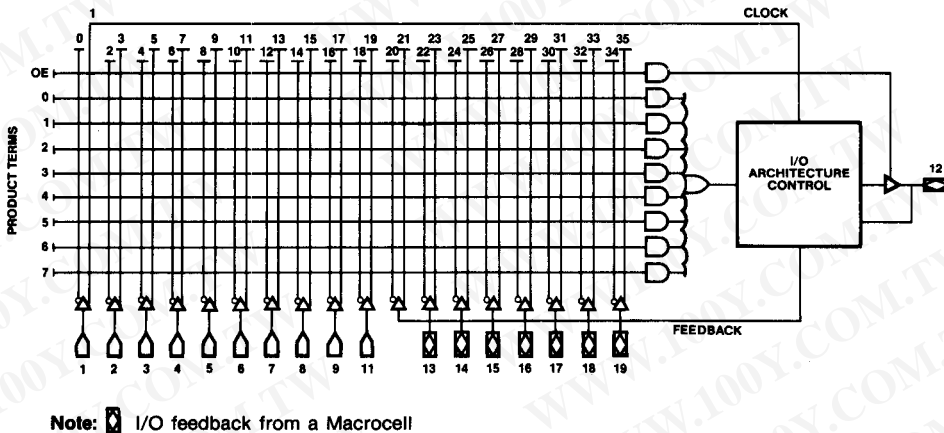
active low if not programmed.) The XOR output then feeds the I/O Architecture Control Block where the output is configured for registered or combinatorial operation. In a registered mode, the output will be registered via a positive edge-triggered D-type flipflop. Under this condition, the feedback signal going back to the array is also registered, coming directly from the output of the D-type flipflop. In a combinatorial mode, the output is non-registered and the feedback signal comes directly from the I/O pin. In the erased state, the EP320 contains the same architectural characteristics as the PAL 16L8.

### OUTPUT ENABLE PRODUCT TERM

The Output Enable (OE) product term determines whether an output signal is allowed to propagate to the output pin. If the output of the OE product term is high, output is enabled to the pin. If the output of the OE product term is low, then the output buffer becomes a high impedance node, thus inhibiting the output signal from reaching the output pin. For combinatorial modes, this OE product term can be used to allow for true bi-directional operation.

The EP320 contains 8 separate OE product terms, one per I/O pin. If the user desires all outputs to be enabled or disabled simultaneously, he may do so by using an identically programmed product term at each of the outputs. If different outputs are to be enabled under different conditions, the user may define a different OE product term for each specific output.

Figure 2. Logic Array Macrocell



This diagram shows one of the eight Macrocells within the EP320.

**I/O ARCHITECTURE**

Figure 3 shows the different output configurations that can be chosen for any of the 8 I/O pins on the EP320. Because of the individuality of each I/O Architecture Control Block, users may choose to have both registered and combinatorial outputs on the same EP320.

In the combinatorial mode, the user may choose either active high or active low output polarity, with an option for pin feedback or no feedback at all.

In the registered mode, the user again has control over output polarity and may choose to use the internal registered feedback path or no feedback at all.

Any I/O pin can be configured as a dedicated input

by choosing no output and pin feedback.

In the erased state, the I/O architecture is configured for combinatorial active low output, with pin feedback.

**PAL COMPATIBILITY**

Figures 4A and 4B show the user how an EP320 can be configured as a drop in replacement for two commonly used members of the 20 pin PAL family, the 16L8 and the 16R8. Notice that when configured in these modes, the EP320 is both a functional as well as a pin to pin replacement for the 16L8 and 16R8.

The tables in Figure 5 give additional information concerning the EP320 as a replacement for the 20 pin PAL family of devices.

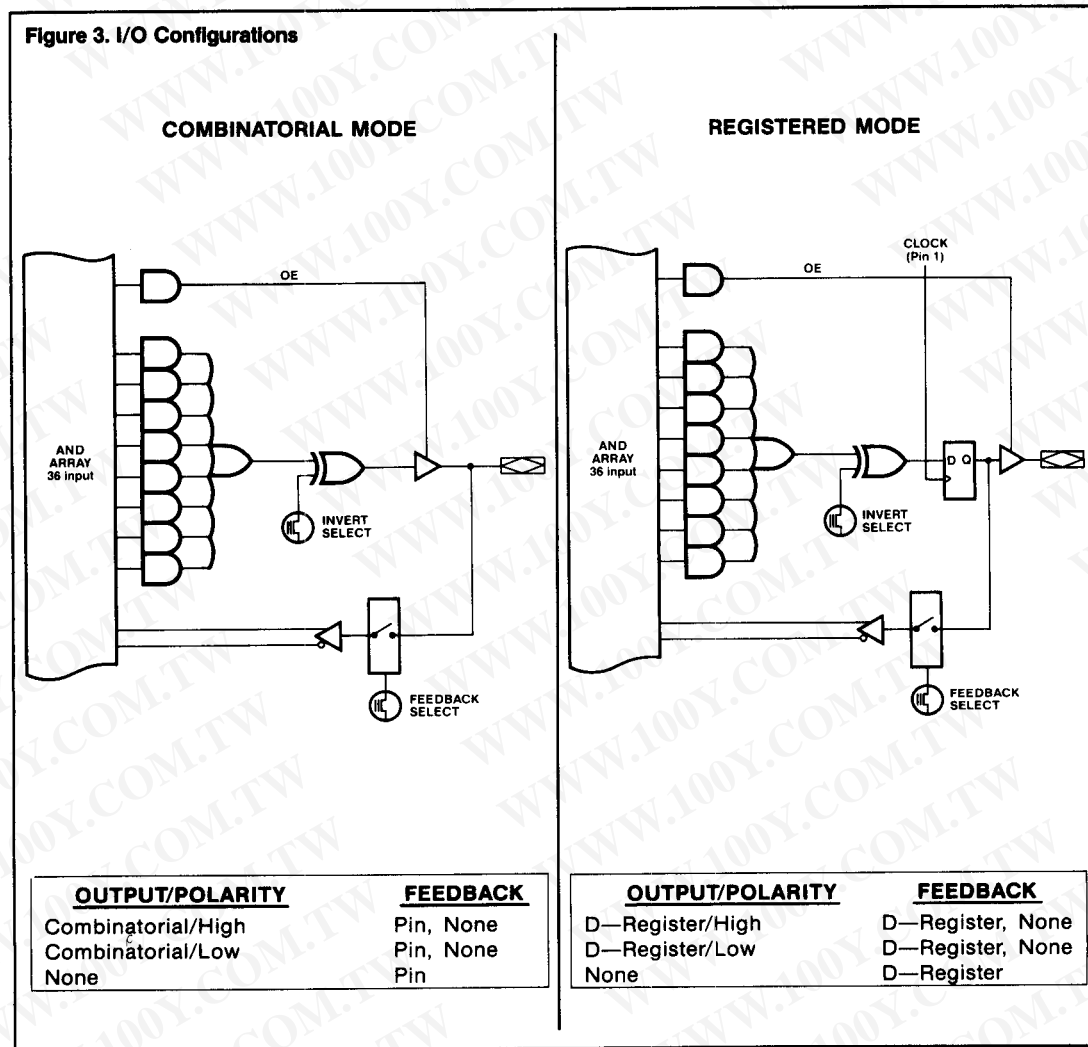
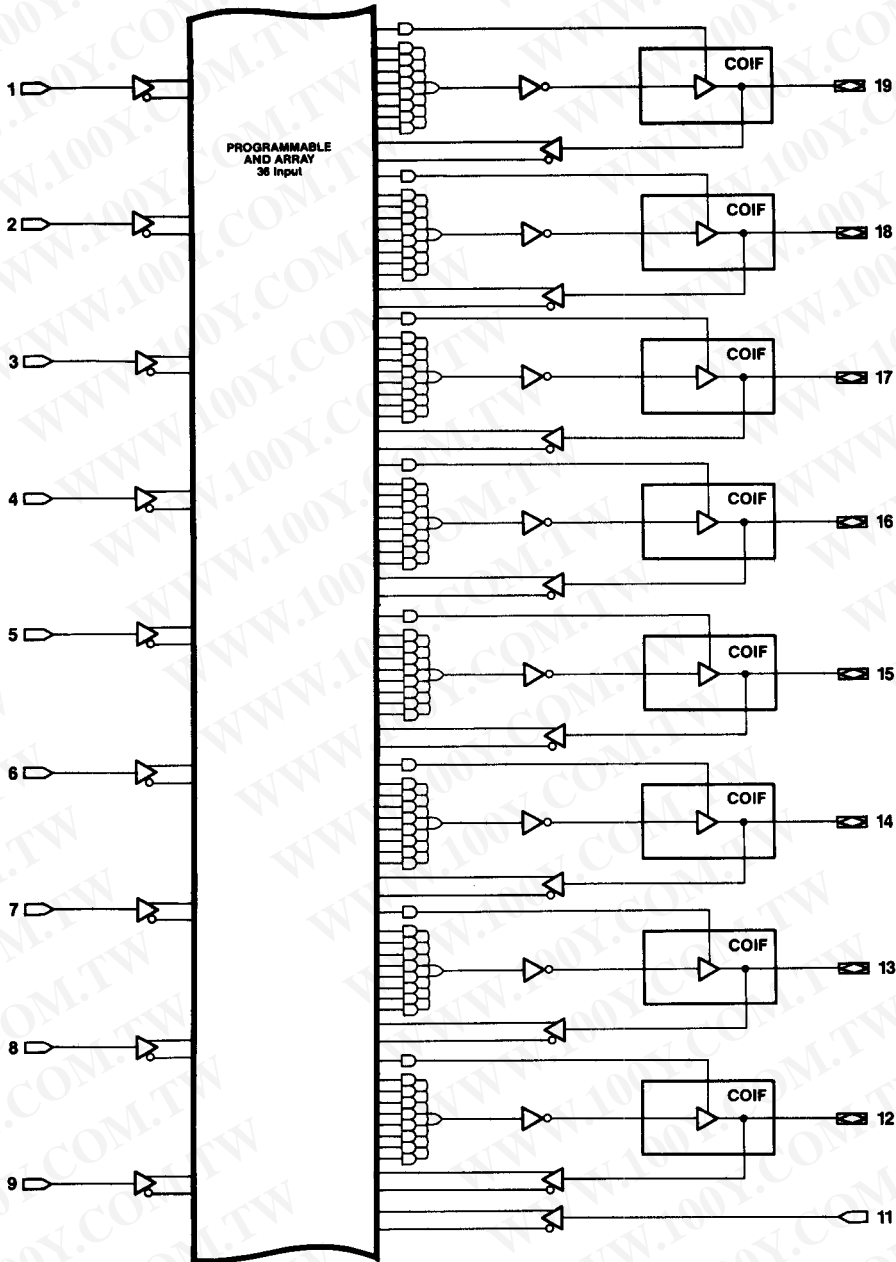
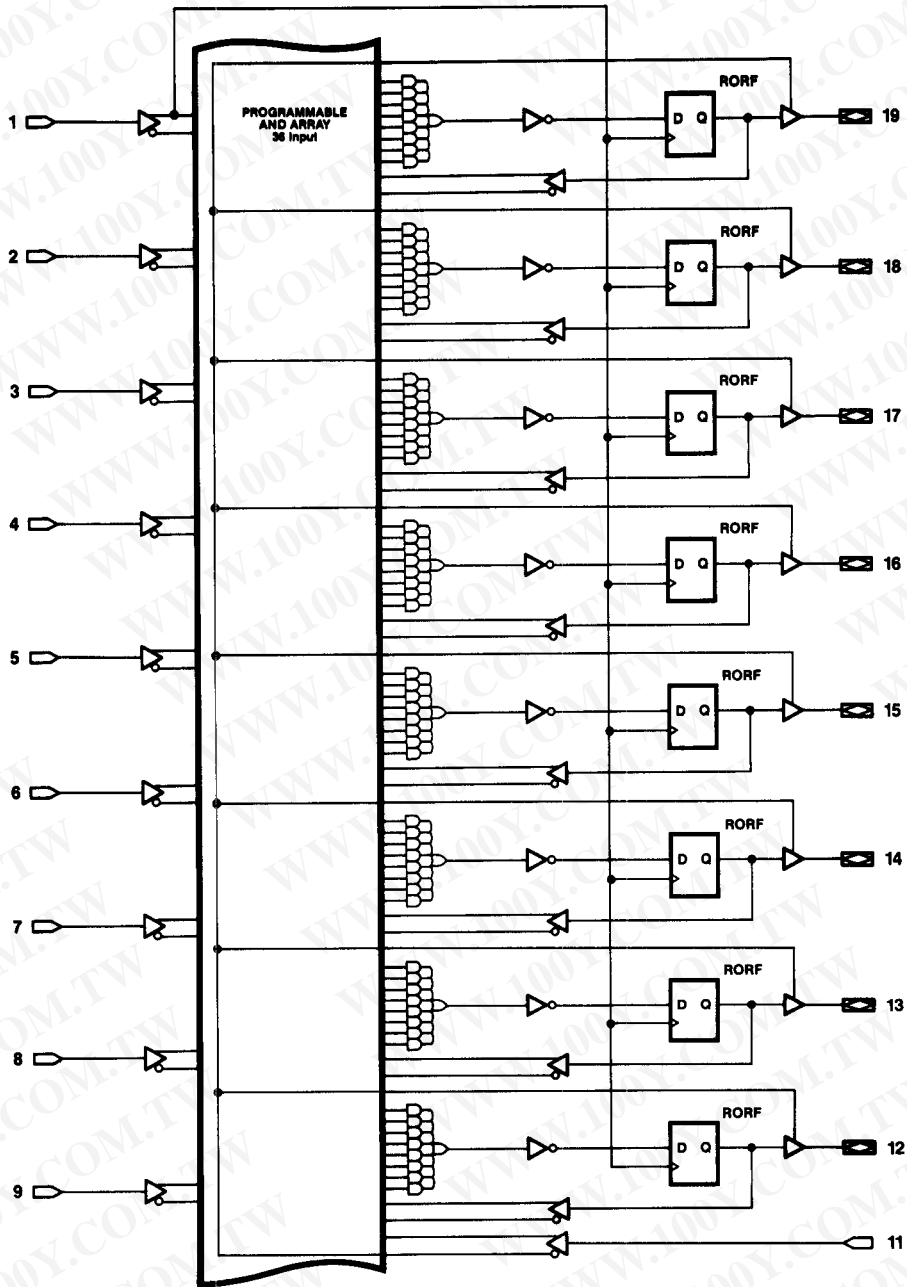


Figure 4A. EP320 Used To Replace PAL 16L8



- "Invert Select" EPROM cell is in the erased state providing active low outputs.
- "Combinatorial Mode" is chosen providing Combinatorial Output with Input (Pin) Feedback (COIF).
- 8 product term OR gate compared to 7 product term OR gate on PAL16L8.
- Pin feedback to the array at pins 12, 19 is not available in PAL16L8.

Figure 4B. EP320 Used To Replace PAL16R8



- "Invert Select" EPROM cell is in the erased state providing active low outputs.
- "Registered Mode" is chosen providing Registered Output with Registered Feedback (RORF).
- Complement of pin 11 is used as common OE term for all 8 output pins.

Figure 5. EP320—PAL Cross Reference

Table 1. EP320 Configurations for 20 Pin PAL Replacement

Pal Part Number	EP320 Pin Number	EP320 Macrocell Number	I/O Configuration Mode	Output/ Polarity	Feedback
10H8	12-19	1-8	Combinatorial	Comb/High	None
10L8	12-19	1-8	Combinatorial	Comb/Low	None
12H6	12	8	Combinatorial	None	Pin
	13-18	2-7	Combinatorial	Comb/High	None
	19	1	Combinatorial	None	Pin
12L6	12	8	Combinatorial	None	Pin
	13-18	2-7	Combinatorial	Comb/Low	None
	19	1	Combinatorial	None	Pin
14H4	12-13	7-8	Combinatorial	None	Pin
	14-17	3-6	Combinatorial	Comb/High	None
	18-19	1-2	Combinatorial	None	Pin
14L4	12-13	7-8	Combinatorial	None	Pin
	14-17	3-6	Combinatorial	Comb/Low	None
	18-19	1-2	Combinatorial	None	Pin
16C1	12-14	6-8	Combinatorial	None	Pin
	15	5	Combinatorial	Comb/Low	None
	16	4	Combinatorial	Comb/High	None
	17-19	1-3	Combinatorial	None	Pin
16H2	12-14	6-8	Combinatorial	None	Pin
	15-16	4-5	Combinatorial	Comb/High	None
	17-19	1-3	Combinatorial	None	Pin
16L2	12-14	6-8	Combinatorial	None	Pin
	15-16	4-5	Combinatorial	Comb/Low	None
	17-19	1-3	Combinatorial	None	Pin
16H8 & 16HD8	12	8	Combinatorial	Comb/High/Z	None
	13-18	2-7	Combinatorial	Comb/High/Z	Comb
	19	1	Combinatorial	Comb/High/Z	None
16L8 & 16LD8	12	8	Combinatorial	Comb/Low/Z	None
	13-18	2-7	Combinatorial	Comb/Low/Z	Comb
	19	1	Combinatorial	Comb/Low/Z	None
16R4	12-13	7-8	Combinatorial	Comb/Low/Z	Comb
	14-17	3-6	Registered	Reg/Low/Z	Reg
	18-19	1-2	Combinatorial	Comb/Low/Z	Comb
16R6	12	8	Combinatorial	Comb/Low/Z	Comb
	13-18	2-7	Registered	Reg/Low/Z	Reg
	19	1	Combinatorial	Comb/Low/Z	Comb
16R8	12-19	1-8	Registered	Reg/Low/Z	Reg
16P8	12	8	Combinatorial	Comb/Option/Z	None
	13-18	2-7	Combinatorial	Comb/Option/Z	Comb
	19	1	Combinatorial	Comb/Option/Z	None
16RP4	12-13	7-8	Combinatorial	Comb/Option/Z	Comb
	14-17	3-6	Registered	Reg/Option/Z	Reg
	18-19	1-2	Combinatorial	Comb/Option/Z	Comb
16RP6	12	8	Combinatorial	Comb/Option/Z	Comb
	13-18	2-7	Registered	Reg/Option/Z	Reg
	19	1	Combinatorial	Comb/Option/Z	Comb
16RP8	12-19	1-8	Registered	Reg/Option/Z	Reg

Table 2. Device Specifications\*

Symbol	Parameter	High Speed EPLD	High Speed, Half-Power PAL (Series 20A-2)	
		EP320-2	PAL 16L8A-2	PAL 16R8A-2
t <sub>pd</sub>	Input to non-registered output	35 ns	35 ns	NA
I <sub>CC1</sub>	Supply current standby	150µA	90 mA	90 mA
I <sub>CC2</sub>	Supply Current Active f=1MHz	5mA	90 mA	90 mA
t <sub>CO1</sub>	Clock to output delay	20 ns	NA	25 ns
t <sub>su</sub>	Input setup time	25 ns	NA	35 ns
f <sub>max</sub>	Max frequency	40 MHz	NA	16 MHz

\* Over commercial temperature range

**ABSOLUTE MAXIMUM RATINGS**COMMERCIAL, INDUSTRIAL, MILITARY  
OPERATING RANGES

Note: See Design Recommendations

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
$V_{CC}$	Supply voltage	With respect to GND note (3)	-2.0	7.0	V
$V_{PP}$	Programming supply voltage		-2.0	13.5	V
$V_I$	DC INPUT voltage		-2.0	7.0	V
$I_{MAX}$	DC $V_{CC}$ or GND current		-80	+80	mA
$I_{OUT}$	DC OUTPUT current, per pin		-25	+25	mA
$P_D$	Power dissipation			400	mW
$T_{STG}$	Storage temperature	No bias	-65	+150	°C
$T_{AMB}$	Ambient temperature	Under bias	-65	+135	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
$V_{CC}$	Supply Voltage	note (6)	4.75 (4.5)	5.25 (5.5)	V
$V_I$	INPUT voltage		0	$V_{CC}$	V
$V_O$	OUTPUT voltage		0	$V_{CC}$	V
$T_A$	Operating temperature	For Commercial	0	70	°C
$T_A$	Operating temperature	For Industrial	-40	85	°C
$T_C$	Case temperature	For Military	-55	125	°C
$T_R$	INPUT rise time			500	ns
$T_F$	INPUT fall time			500	ns

**DC OPERATING CHARACTERISTICS**

( $V_{CC} = 5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$  for Commercial)  
 ( $V_{CC} = 5V \pm 10\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$  for Industrial)  
 ( $V_{CC} = 5V \pm 10\%$ ,  $T_C = -55^\circ C$  to  $125^\circ C$  for Military)\*  
 Note (1) and (6)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IH}$	HIGH level input voltage		2.0		$V_{CC} + 0.3$	V
$V_{IL}$	LOW level input voltage		-0.3		0.8	V
$V_{OH}$	HIGH level TTL output voltage	$I_{OH} = -8mA$ DC	2.4			V
$V_{OH}$	HIGH level CMOS output voltage	$I_{OH} = -4mA$ DC	3.84			V
$V_{OL}$	LOW level output voltage	$I_{OL} = +8mA$ DC			0.45	V
$I_I$	Input leakage current	$V_I = V_{CC}$ or GND	-10		+10	$\mu A$
$I_{OZ}$	3-state output off-state current	$V_O = V_{CC}$ or GND	-10		+10	$\mu A$
$I_{CC1}$	$V_{CC}$ supply current (standby)	$V_I = V_{CC}$ or GND No load note (8)		10	150	$\mu A$
$I_{CC2}$	$V_{CC}$ supply current (non-turbo)	$V_I = V_{CC}$ or GND No load, $f = 1.0$ MHz note (7)		3	5 (15)	mA
$I_{CC3}$	$V_{CC}$ supply current (turbo)	$V_I = V_{CC}$ or GND No load, $f = 1.0$ MHz note (7)		18	30 (40)	mA

**CAPACITANCE**

Note (4)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$ $f = 1.0$ MHz		10	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0V$ $f = 1.0$ MHz		10	pF
$C_{CLK}$	Clock Pin Capacitance	$V_{IN} = 0V$ $f = 1.0$ MHz		10	pF



## AC CHARACTERISTICS

EP320, EP320-1, EP320-2

( $V_{CC} = 5V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  for Commercial)  
 ( $V_{CC} = 5V \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  for Industrial)  
 ( $V_{CC} = 5V \pm 10\%$ ,  $T_C = -55^\circ\text{C}$  to  $125^\circ\text{C}$  for Military)\*

SYMBOL	PARAMETER	CONDITIONS	EP320-1		EP320-2		EP320		NON-TURBO ADDER	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	note (5)	
$t_{PD1}$	Input to non-registered output	$C_1 = 50\text{pF}$		29		34		44	15	ns
$t_{PD2}$	I/O input to non-registered output			30		35		45	15	ns
$t_{PZX}$	Input or I/O input to output enable			30		35		45	15	ns
$t_{PXZ}$	Input or I/O input to output disable	$C_1 = 5\text{pF}$ note (2)		30		35		45	15	ns
$t_{IO}$	I/O input buffer delay			1		1		1	0	ns

## SYNCHRONOUS CLOCK MODE

SYMBOL	PARAMETER	CONDITIONS	EP320-1		EP320-2		EP320		NON-TURBO ADDER	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	note (5)	
$f_{MAX}$	Maximum frequency	note (9)	45.5		40		30.3		0	MHz
$t_{SU}$	Input or I/O input setup time		22		25		33		15	ns
$t_{H}$	Input or I/O input hold time		0		0		0		0	ns
$t_{CH}$	Clock high time		10		12		16		0	ns
$t_{CL}$	Clock low time		10		12		16		0	ns
$t_{C01}$	Clock to output delay			17		20		25	0	ns
$t_{CNT}$	Minimum clock period (register output feedback to register input - internal path)	note (7)		35		40		50	0	ns
$f_{CNT}$	Internal maximum frequency ( $1/t_{CNT}$ )	note (7)	28.6		25		20		0	MHz

### Notes:

- Typical values are for  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5V$
- Sample tested only for an output change of 500mV.
- Minimum DC input is  $-0.3V$ . During transitions, the inputs may undershoot to  $-2.0V$  for periods less than 20ns.
- Capacitance measured at  $25^\circ\text{C}$ . Sample tested only. Pin 11, (high voltage pin during programming), has capacitance of 20 pf max.
- See TURBO-BIT™, page 73.
- Figures in ( ) pertain to military and industrial temperature version.
- Measured with device programmed as an 8-Bit Counter.
- EPLD automatically goes into standby mode if logic transitions do not occur when in non-turbo mode (approximately 100 ns after last transition).
- The  $f_{MAX}$  values shown represent the highest frequency for pipelined data.

GRADE	AVAILABILITY	
Commercial ( $0^\circ\text{C}$ to $70^\circ\text{C}$ )	EP320-1	EP320-2 EP320
Industrial ( $-40^\circ\text{C}$ to $85^\circ\text{C}$ )		EP320
Military ( $-55^\circ\text{C}$ to $125^\circ\text{C}$ )		EP320

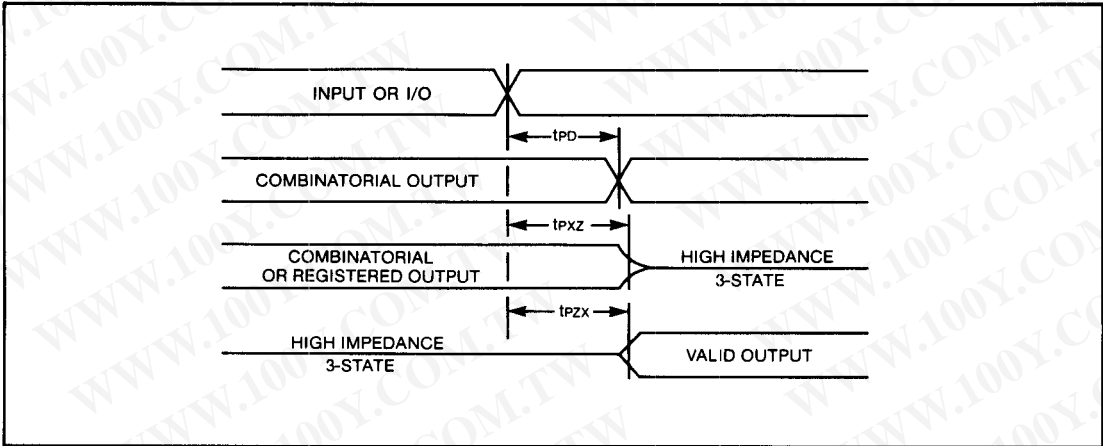
\* The specifications noted above apply to military operating range devices. MIL-STD-883 compliant product specifications are provided in military product drawings available on request from Altera marketing at 408/984-2905, ext. 101. These military product drawings should be used for the preparation of source control drawings.

EP320

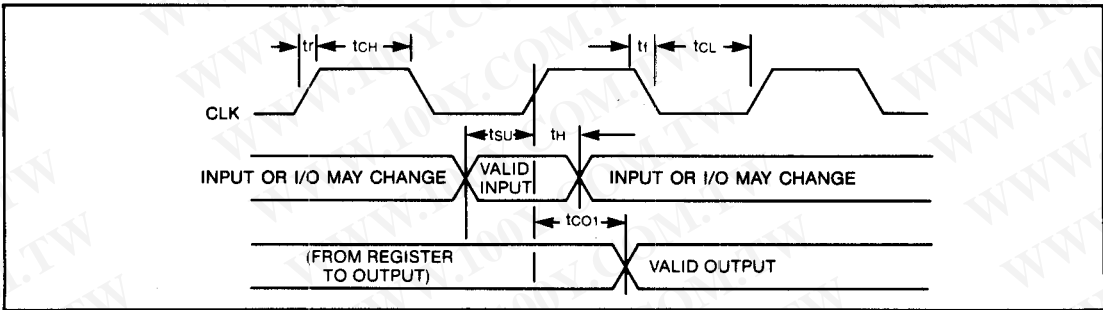
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Figure 6. Switching Waveforms

COMBINATORIAL MODE



SYNCHRONOUS CLOCK MODE



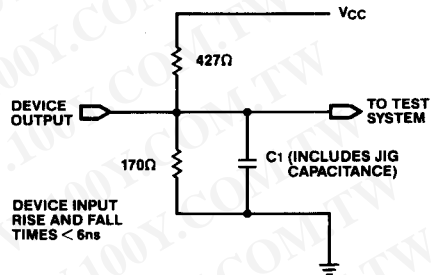
Notes:  $t_r$  &  $t_f < 6ns$   
 $t_{CL}$  &  $t_{CH}$  measured at 0.3V and 2.7V  
 all other timing at 1.5V  
 input voltage levels at 0V and 3V

FUNCTIONAL TESTING

The EP320 is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

As a result, traditional problems associated with fuse-programmed circuits are eliminated. The erasable nature of the EP320 allows test program patterns to be used and then erased. This facility to use application-independent, general purpose tests is called generic testing and is unique among user-defined LSI logic devices.

Figure 7. AC Test Conditions



Power supply transients can affect AC measurements, simultaneous transitions of multiple outputs should be avoided for accurate measurement. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

Figure 8.  $I_{CC}$  vs.  $F_{MAX}$

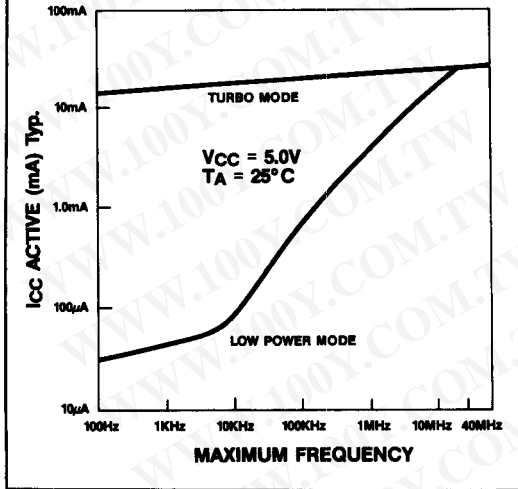
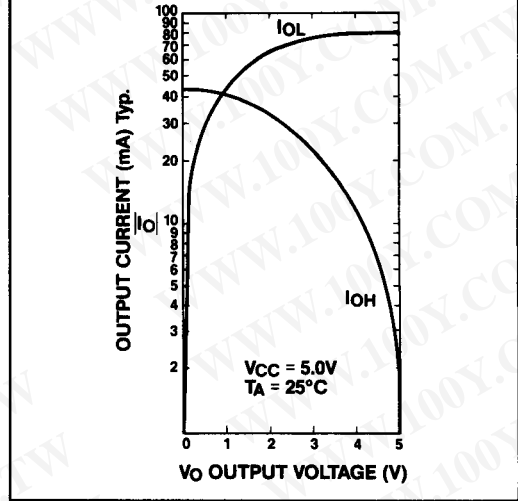


Figure 9. Output Drive Currents



**DESIGN SECURITY**

The EP320 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied nor retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

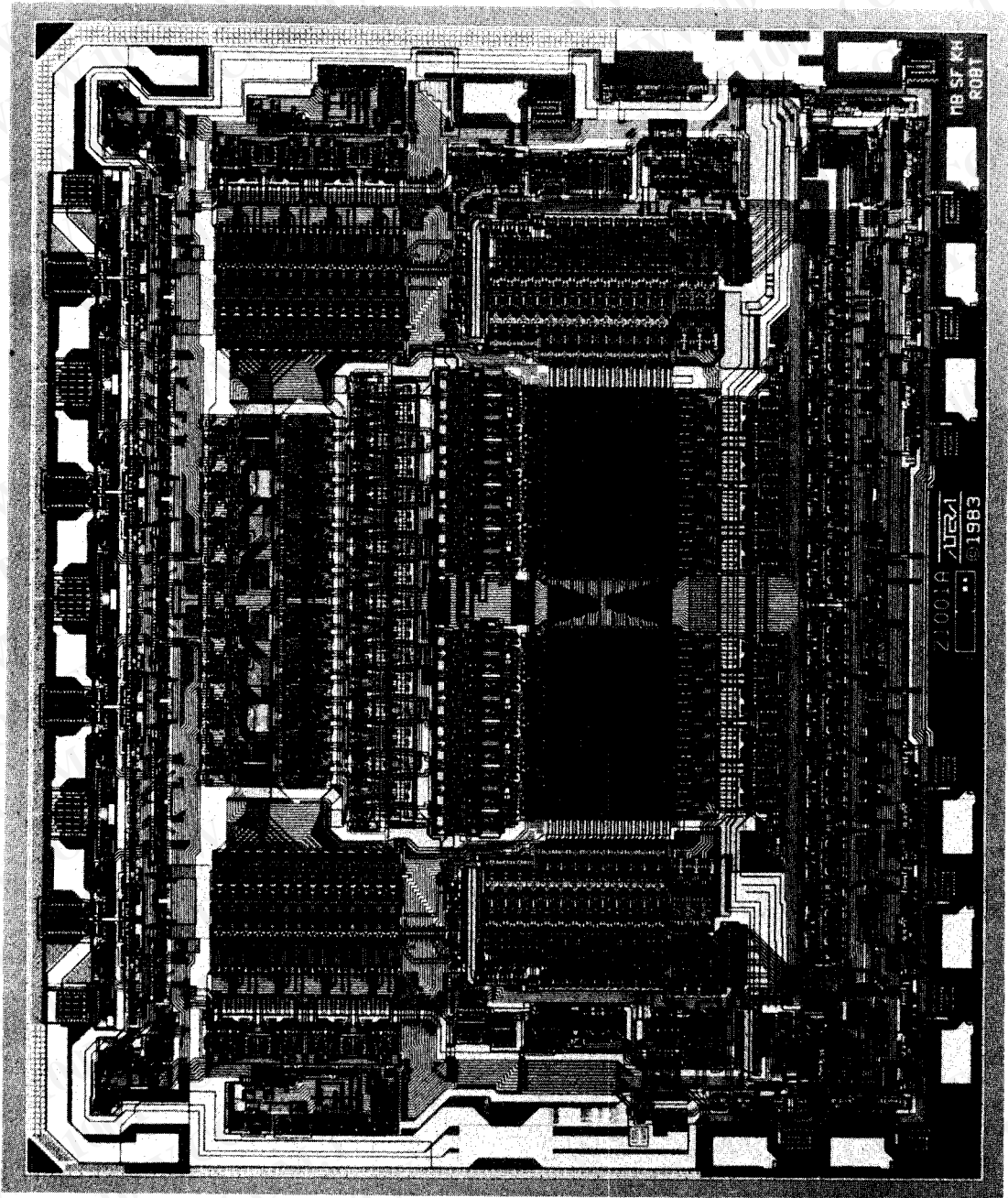
**TURBO-BIT**

Some EPLDs contain a programmable option to control the automatic power down feature that enables the low standby power mode of the device. This option is controlled by a TURBO-BIT which can be set using A+PLUS. When the TURBO-BIT is programmed (Turbo = ON), the low standby power mode ( $I_{CC1}$ ) is disabled. This renders the circuit less sensitive to  $V_{CC}$  noise transients which can be created by the power-up/power-down cycle when operating in the low power mode. The typical  $I_{CC}$  vs frequency data for both Turbo and Non-Turbo (low power) mode is shown in each EPLD data sheet. All AC values are tested with the TURBO-BIT programmed.

If the design requires low power operation then the TURBO-BIT should be disabled (Turbo = OFF). When operating in this mode, some AC parameters are subject to increase. Values given in the AC specifications section under "Non-Turbo Adder" must be added to the respective AC parameter to determine worst-case timing.

**LATCH-UP**

The EP320 input, I/O, and clock pins have been carefully designed to resist latch-up which is inherent in CMOS structures. Each of the EP320 pins will not latch-up for input voltages between  $-1V$  to  $V_{CC} + 1V$  with currents up to 100 mA. During transitions, the inputs may undershoot to  $-2.0V$  for periods less than 20 ns. Additionally, the programming pin is designed to resist latch-up to the 13.5 volt maximum device limit.



*"The World's first EPLD"*

**ALTERA**