

HD14043B, HD14044B

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[Http://www.100y.com.tw](http://www.100y.com.tw)

Quadruple R-S Latch

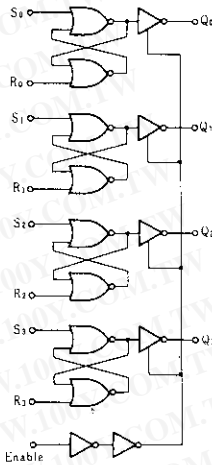
The HD14043B and HD14044B quad R-S latches have an independent Q output and set and reset inputs. The Q outputs are gated through three-state buffers having a common enable input. The outputs are enabled with a logical "1" or high on the enable input; a logical "0" or low disconnects the latch from the Q outputs, resulting in an open circuit at the Q outputs.

FEATURES

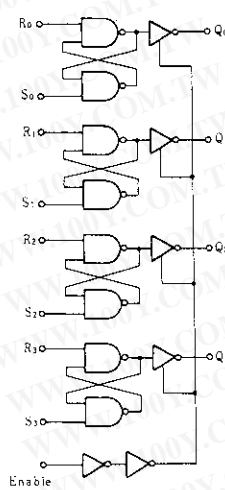
- Quiescent Current = 4 nA/pkg typ. @10V
- Double Diode Input Protection
- Three-State Outputs with Common Enable
- Outputs Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range
- Supply Voltage Range = 3 to 18V

LOGIC DIAGRAM

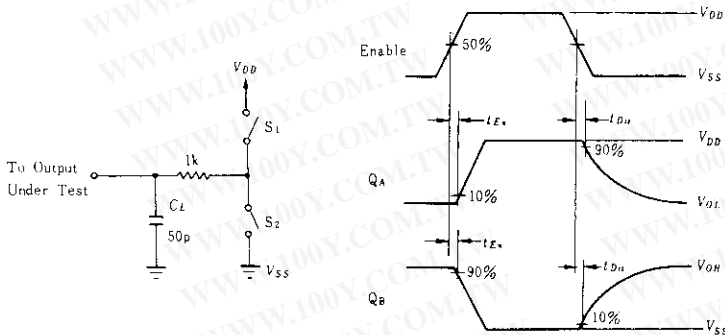
HD14043B



HD14044B



THREE-STATE ENABLE/DISABLE DELAYS

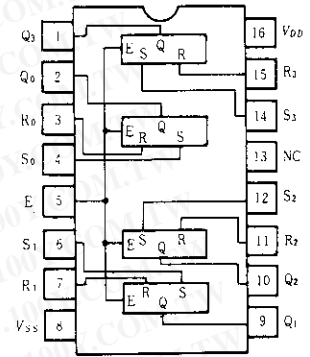


Testing Method

Test	S	R	HD14043B			HD14044B		
			S ₁	S ₂	Q	S ₁	S ₂	Q
t _{Es}	V _{DD}	V _{SS}	Open	Closed	A	Closed	Open	B
t _{Eh}	V _{SS}	V _{DD}	Closed	Open	B	Open	Closed	A
t _{Ds}	V _{DD}	V _{SS}	Open	Closed	A	Closed	Open	B
t _{Dh}	V _{SS}	V _{DD}	Closed	Open	B	Open	Closed	A

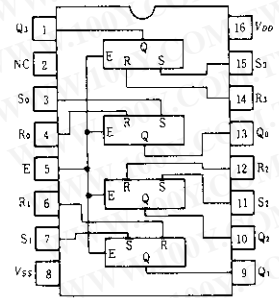
PIN ARRANGEMENT

HD14043B



(Top View)

HD14044B



(Top View)

TRUTH TABLE

HD14043B

S	R	E	Q
X	X	0	High Impedance
0	0	1	No Change
0	1	1	0
1	0	1	1
1	1	1	1

HD14044B

S	R	E	Q
X	X	0	High Impedance
0	0	1	0
0	1	1	1
1	0	1	0
1	1	1	No Change

x=Don't Care

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	-40°C		25°C			85°C		Unit	
			min	max	min	typ	max	min	max		
Output Voltage	V_{OL}	$V_{in} = V_{DD}$ or 0	5.0	-	0.05	-	0	0.05	-	0.05	V
			10	-	0.05	-	0	0.05	-	0.05	
			15	-	0.05	-	0	0.05	-	0.05	
	V_{OH}	$V_{in} = 0$ or V_{DD}	5.0	4.95	-	4.95	5.0	-	4.95	-	V
			10	9.95	-	9.95	10	-	9.95	-	
			15	14.95	-	14.95	15	-	14.95	-	
Input Voltage	V_{IL}	5.0	$V_{out} = 4.5$ or $0.5V$	-	1.5	-	2.25	1.5	-	1.5	V
		10	$V_{out} = 9.0$ or $1.0V$	-	3.0	-	4.50	3.0	-	3.0	
		15	$V_{out} = 13.5$ or $1.5V$	-	4.0	-	6.75	4.0	-	4.0	
	V_{IH}	5.0	$V_{out} = 0.5$ or $4.5V$	3.5	-	3.5	2.75	-	3.5	-	V
		10	$V_{out} = 1.0$ or $9.0V$	7.0	-	7.0	5.50	-	7.0	-	
		15	$V_{out} = 1.5$ or $13.5V$	11.0	-	11.0	8.25	-	11.0	-	
Output Drive Current	I_{OH}	5.0	$V_{OH} = 2.5V$	-2.5	-	-2.1	-4.2	-	-1.7	-	mA
		5.0	$V_{OH} = 4.6V$	-0.52	-	-0.44	-0.88	-	-0.36	-	
		10	$V_{OH} = 9.5V$	-1.3	-	-1.1	-2.25	-	-0.9	-	
		15	$V_{OH} = 13.5V$	-3.6	-	-3.0	-8.8	-	-2.4	-	
	I_{OL}	5.0	$V_{OL} = 0.4V$	0.52	-	0.44	0.88	-	0.36	-	mA
		10	$V_{OL} = 0.5V$	1.3	-	1.1	2.25	-	0.9	-	
15		$V_{OL} = 1.5V$	3.6	-	3.0	8.8	-	2.4	-		
Input Current	I_{in}	15		-	± 0.3	-	± 0.00001	± 0.3	-	± 1.0	μA
Input Capacitance	C_{in}	-	$V_{in} = 0$	-	-	-	5.0	7.5	-	-	pF
Quiescent Current	I_{DD}	5.0	Zero Signal, per Package	-	4.0	-	0.002	4.0	-	30	μA
		10		-	8.0	-	0.004	8.0	-	60	
		15		-	16	-	0.006	16	-	120	
Total Supply Current*	I_T	5.0	Dynamic + I_{DD} , per Gate	-	-	-	0.58	-	-	-	μA
		10		-	-	-	1.15	-	-	-	
		15		$C_L = 50pF$, $f = 1kHz$	-	-	-	1.73	-	-	
Three-State Output Leakage Current	I_{TL}	15		-	± 1.0	-	± 0.00001	± 1.0	-	± 7.5	μA

* To calculate total supply current at frequency other than 1kHz.

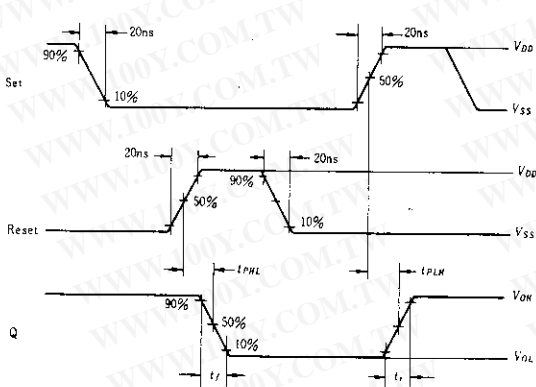
@ $V_{DD} = 5.0V$ $I_T = (0.58 \mu A/kHz) f + I_{DD}$, @ $V_{DD} = 10V$ $I_T = (1.15 \mu A/kHz) f + I_{DD}$, @ $V_{DD} = 15V$ $I_T = (1.73 \mu A/kHz) f + I_{DD}$

SWITCHING CHARACTERISTICS ($C_L=50\text{pF}$, $T_a=25^\circ\text{C}$)

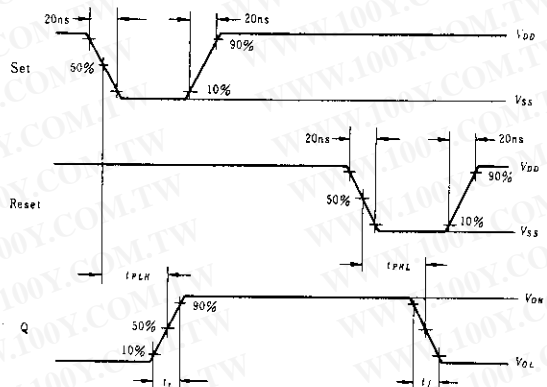
Characteristic	Symbol	V_{DD} (V)	min	typ	max	Unit
Output Rise Time	t_r	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Output Fall Time	t_f	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time	t_{PLH}	5.0	—	175	350	ns
		10	—	75	175	
		15	—	60	120	
	t_{PHL}	5.0	—	175	350	ns
		10	—	75	175	
		15	—	60	120	
Set Pulse Width	PW_S	5.0	200	80	—	ns
		10	100	40	—	
		15	70	30	—	
Reset Pulse Width	PW_R	5.0	200	80	—	ns
		10	100	40	—	
		15	70	30	—	
Three-state Enable/Disable Delay	t_{EN}	5.0	—	150	300	ns
	t_{DIS}	10	—	80	160	
		15	—	55	110	

DYNAMIC SIGNAL WAVEFORMS

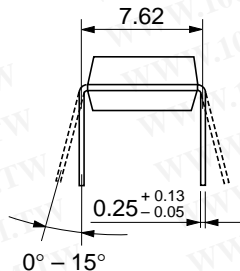
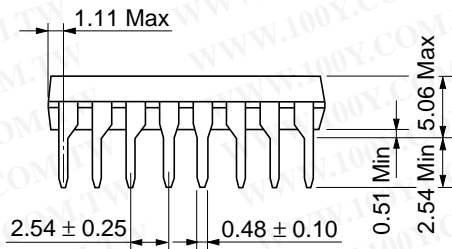
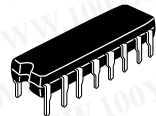
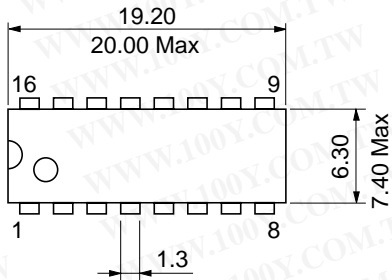
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Unit: mm



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Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g