MOTOROLA

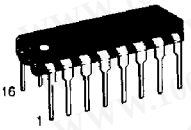
MC14194B

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

The MC14194B is a 4-bit static shift register capable of operating in the parallel load, serial shift left, serial shift right, or hold mode. The asynchronous $\overline{\text{Reset}}$ input, when at a low level, overrides all other inputs, resets all stages, and forces all outputs low. When $\overline{\text{Reset}}$ is at a logic 1 level, the two mode control inputs, S0 and S1, control the operating mode as shown in the truth table. Both serial and parallel operation are triggered on the positive-going transition of the Clock input. The Parallel Data, Data Shift, and mode control inputs must be stable for the specified setup and hold times before and after the positive-going Clock transition.

- Synchronous Right/Left Serial Operation
- Synchronous Parallel Load
- Asynchronous Hold (Do Nothing) Mode
- Functional Pin for Pin Equivalent of LS194

L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648

D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

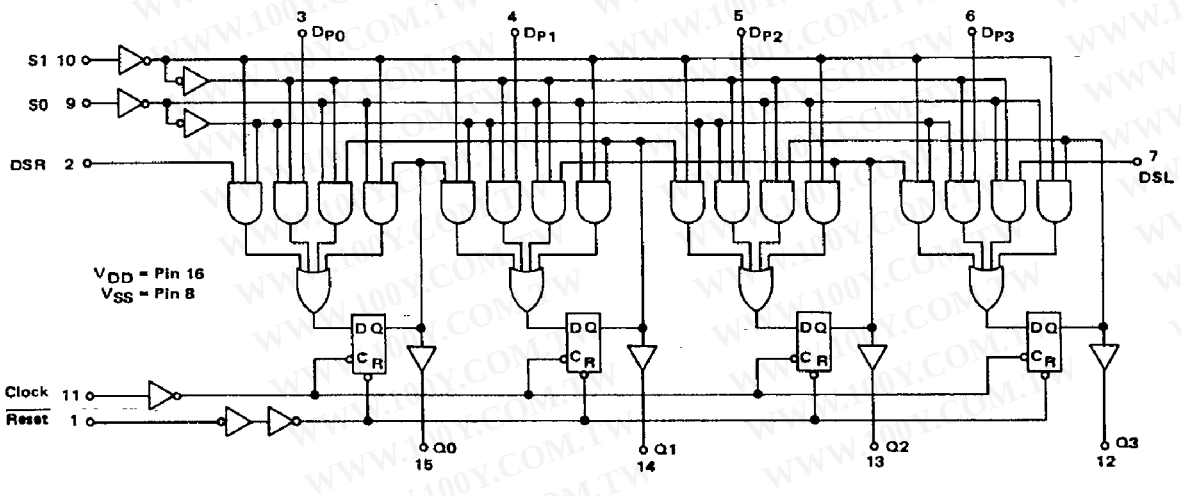
T_A = −55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: −7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: −12 mW/°C From 100°C To 125°C

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
			10	—	0.05	—	0	0.05	—	0.05	
			15	—	0.05	—	0	0.05	—	0.05	
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
			10	9.95	—	9.95	10	—	9.95	—	
			15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
			10	—	3.0	—	4.50	3.0	—	3.0	
			15	—	4.0	—	6.75	4.0	—	4.0	
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Output Drive Current (V_{OH} = 2.5 Vdc)	Source	I_{OH}	5.0	−3.0	—	−2.4	−4.2	—	−1.7	—	mAdc
(V_{OH} = 4.6 Vdc)			5.0	−0.64	—	−0.51	−0.88	—	−0.36	—	
(V_{OH} = 9.5 Vdc)			10	−1.6	—	−1.3	−2.25	—	−0.9	—	
(V_{OH} = 13.5 Vdc)			15	−4.2	—	−3.4	−8.8	—	−2.4	—	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)			10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current		I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
			10	—	10	—	0.010	10	—	300	
			15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0	I_T = (0.95 μA/kHz) f + I_{DD}							μAdc
			10	I_T = (1.90 μA/kHz) f + I_{DD}							
			15	I_T = (2.90 μA/kHz) f + I_{DD}							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

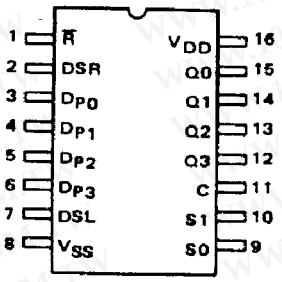
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\,Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

PIN ASSIGNMENT



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

TRUTH TABLE

OPERATING MODE	INPUTS ($\overline{Reset}$ = 1)					OUTPUTS (@ $t_n + 1$)			
	S1	S0	DSR	DSL	D_{P0-3}	Q0	Q1	Q2	Q3
Hold	0	0	X	X	X	Q0	Q1	Q2	Q3
Shift Left	1	0	X	0	X	Q1	Q2	Q3	0
	1	0	X	1	X	Q1	Q2	Q3	1
Shift Right	0	1	0	X	X	0	Q0	Q1	Q2
	0	1	1	X	X	1	Q0	Q1	Q2
Parallel	1	1	X	X	0	0	0	0	0
	1	1	X	X	1	1	1	1	1

X = Don't Care

t_{n+1} = State after the next positive-going transition of the clock.

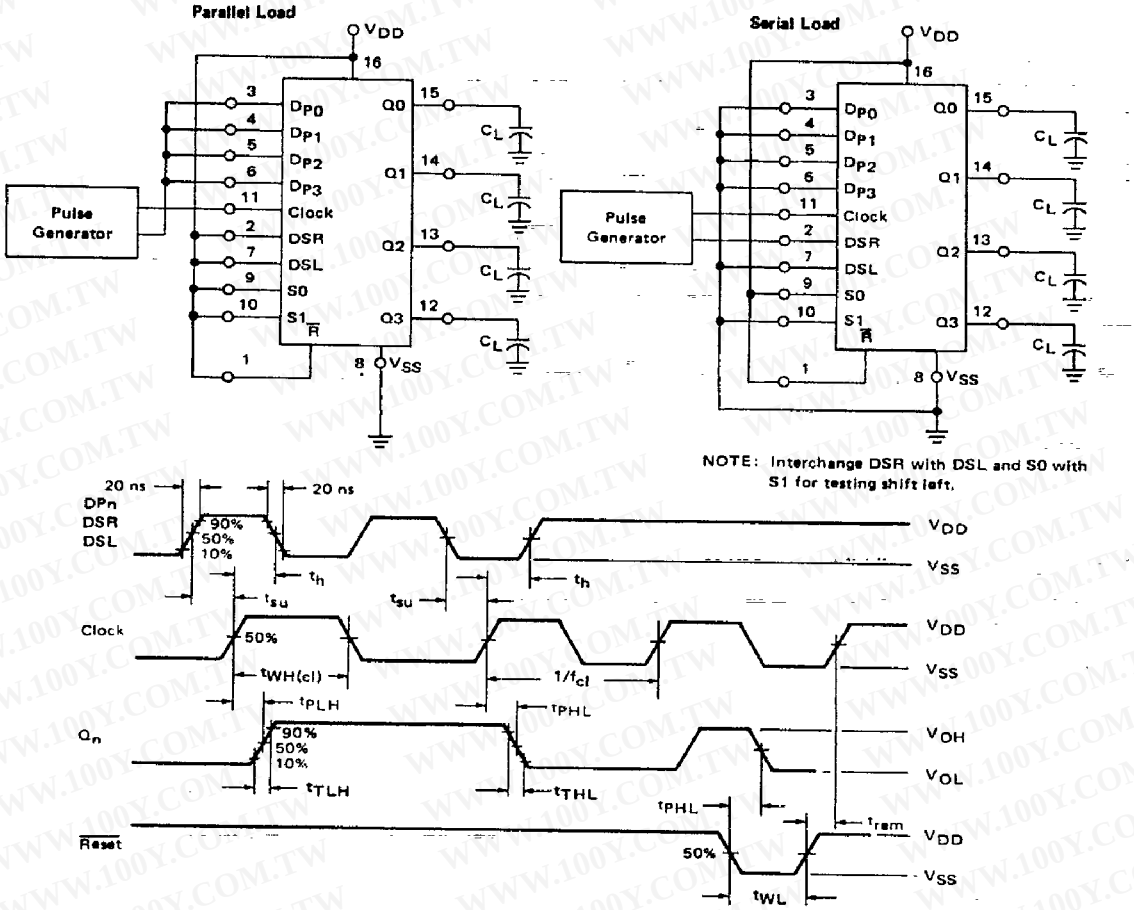
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},t_{PHL}					ns
Clock to Q						
t_{PLH},t_{PHL} = (0.9 ns/pF) C_L + 230 ns		5.0	–	275	550	
t_{PLH},t_{PHL} = (0.36 ns/pF) C_L + 92 ns		10	–	110	220	
t_{PLH},t_{PHL} = (0.26 ns/pF) C_L + 72 ns		15	–	85	170	
$\overline{Reset}$ to Q	t_{PHL}					ns
t_{PHL} = (0.9 ns/pF) C_L + 305 ns		5.0	–	350	700	
t_{PHL} = (0.36 ns/pF) C_L + 122 ns		10	–	140	280	
t_{PHL} = (0.26 ns/pF) C_L + 97 ns		15	–	110	220	
Clock Pulse Width	t_{WH}	5.0	280	140	–	ns
		10	110	55	–	
		15	85	40	–	
$\overline{Reset}$ Pulse Width	t_{WH}	5.0	180	90	–	ns
		10	70	35	–	
		15	50	26	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.6	1.8	MHz
(Shift Right or Left Mode)		10	–	9.0	4.5	
		15	–	12	6.0	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	µs
		10	–	–	5	
		15	–	–	4	
Setup Time	t_{su}					ns
Data to Clock		5.0	10	-8.0	–	
		10	20	0	–	
		15	40	9.0	–	
Mode Control (S) to Clock		5.0	200	100	–	ns
		10	75	36	–	
		15	55	27	–	
Hold Time	t_h					ns
Data to Clock		5.0	180	90	–	
		10	50	25	–	
		15	35	10	–	
Mode Control (S) to Clock		5.0	0	-40	–	ns
		10	0	-27	–	
		15	0	-20	–	
$\overline{Reset}$ Removal Time	t_{rem}	5.0	300	150	–	ns
		10	110	55	–	
		15	80	40	–	

**The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



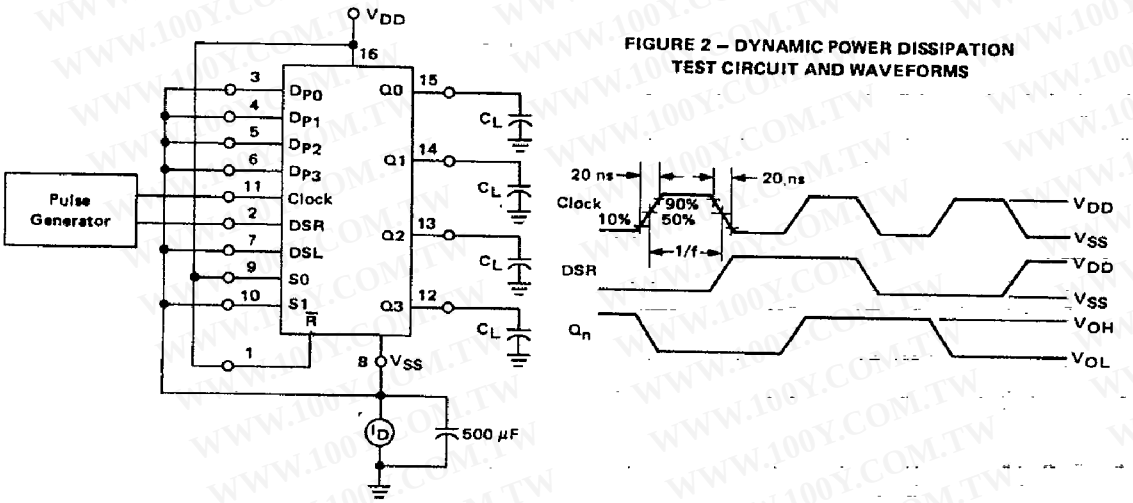


FIGURE 2 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS