

# DATA SHEET

勝特力材料 886-3-5753170  
勝特力电子(上海) 86-21-34970699  
勝特力电子(深圳) 86-755-83298787  
[Http://www.100y.com.tw](http://www.100y.com.tw)

## **74HC2G08; 74HCT2G08** Dual 2-input AND gate

Product specification  
Supersedes data of 2003 Feb 03

2003 Oct 22

## Dual 2-input AND gate

## 74HC2G08; 74HCT2G08

## FEATURES

- Wide supply voltage range from 2.0 to 6.0 V
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- Very small 8 pins package
- Output capability is standard
- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from  $-40$  to  $+85$  °C and  $-40$  to  $+125$  °C.

## DESCRIPTION

The 74HC2G/HCT2G08 is a high-speed Si-gate CMOS device.

The 74HC2G/HCT2G08 provides the 2-input AND function.

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## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 6.0$  ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC2G08	HCT2G08	
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY	$C_L = 15$ pF; $V_{CC} = 5$ V	9	14	ns
$C_I$	input capacitance		1.5	1.5	pF
$C_{PD}$	power dissipation capacitance per gate	notes 1 and 2	10	10	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $C_L$  = output load capacitance in pF;  
 $V_{CC}$  = supply voltage in Volts;  
 $N$  = total load switching outputs;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.
2. For 74HC2G08 the condition is  $V_I = \text{GND to } V_{CC}$ .  
 For 74HCT2G08 the condition is  $V_I = \text{GND to } V_{CC} - 1.5$  V.

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## 74HC2G08; 74HCT2G08

## FUNCTION TABLE

See note 1.

INPUT		OUTPUT
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

## Note

1. H = HIGH voltage level;  
L = LOW voltage level.

## ORDERING INFORMATION

TYPE NUMBER	TEMPERATURE RANGE	PACKAGE				
		PINS	PACKAGE	MATERIAL	CODE	MARKING
74HC2G08DP	-40 to +125 °C	8	TSSOP8	plastic	SOT505-2	H08
74HCT2G08DP	-40 to +125 °C	8	TSSOP8	plastic	SOT505-2	T08
74HC2G08DC	-40 to +125 °C	8	VSSOP8	plastic	SOT765-1	H08
74HCT2G08DC	-40 to +125 °C	8	VSSOP8	plastic	SOT765-1	T08

## PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1B	data input
3	2Y	data output
4	GND	ground (0 V)
5	2A	data input
6	2B	data input
7	1Y	data output
8	V <sub>CC</sub>	supply voltage

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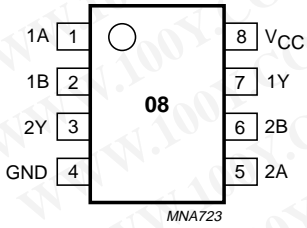


Fig.1 Pin configuration.

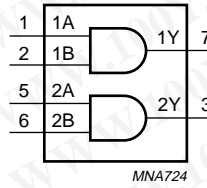


Fig.2 Logic symbol.

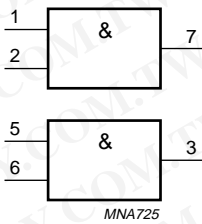


Fig.3 IEC logic symbol.

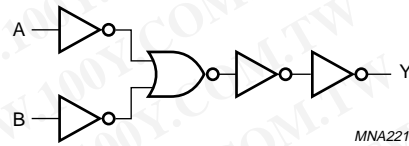


Fig.4 Logic diagram (one driver).



## Dual 2-input AND gate

## 74HC2G08; 74HCT2G08

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC2G08			74HCT2G08			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	–	$V_{CC}$	0	–	$V_{CC}$	V
$V_O$	output voltage		0	–	$V_{CC}$	0	–	$V_{CC}$	V
$T_{amb}$	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
$t_r, t_f$	input rise and fall times	$V_{CC} = 2.0\text{ V}$	–	–	1000	–	–	–	ns
		$V_{CC} = 4.5\text{ V}$	–	6.0	500	–	6.0	500	ns
		$V_{CC} = 6.0\text{ V}$	–	–	400	–	–	–	ns

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		–0.5	+7.0	V
$I_{IK}$	input diode current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ ; note 1	–	±20	mA
$I_{OK}$	output diode current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ ; note 1	–	±20	mA
$I_O$	output source or sink current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$ ; note 1	–	25	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current	note 1	–	50	mA
$T_{stg}$	storage temperature		–65	+150	°C
$P_D$	power dissipation	$T_{amb} = -40\text{ to }+125\text{ °C}$ ; note 2	–	300	mW

## Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 110 °C the value of  $P_D$  derates linearly with 8 mW/K.

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## Dual 2-input AND gate

## 74HC2G08; 74HCT2G08

## DC CHARACTERISTICS

## Type 74HC2G08

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	1.2	–	V
			4.5	3.15	2.4	–	V
			6.0	4.2	3.2	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	0.8	0.5	V
			4.5	–	2.1	1.35	V
			6.0	–	2.8	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = -20 μA	2.0	1.9	2.0	–	V
		I <sub>O</sub> = -20 μA	4.5	4.4	4.5	–	V
		I <sub>O</sub> = -20 μA	6.0	5.9	6.0	–	V
		I <sub>O</sub> = -4.0 mA	4.5	4.13	4.32	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = 20 μA	2.0	–	0	0.1	V
		I <sub>O</sub> = 20 μA	4.5	–	0	0.1	V
		I <sub>O</sub> = 20 μA	6.0	–	0	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	–	0.15	0.33	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	6.0	–	–	±1.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	6.0	–	–	10	μA

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## Dual 2-input AND gate

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -20 μA	2.0	1.9	–	–	V
		I <sub>O</sub> = -20 μA	4.5	4.4	–	–	V
		I <sub>O</sub> = -20 μA	6.0	5.9	–	–	V
		I <sub>O</sub> = -4.0 mA	4.5	3.7	–	–	V
		I <sub>O</sub> = -5.2 mA	6.0	5.2	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 μA	2.0	–	–	0.1	V
		I <sub>O</sub> = 20 μA	4.5	–	–	0.1	V
		I <sub>O</sub> = 20 μA	6.0	–	–	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	–	–	0.4	V
		I <sub>O</sub> = 5.2 mA	6.0	–	–	0.4	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	6.0	–	–	±1.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	6.0	–	–	20	μA

**Note**

1. All typical values are measured at T<sub>amb</sub> = 25 °C.

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## Dual 2-input AND gate

## 74HC2G08; 74HCT2G08

## Type 74HCT2G08

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -20 µA	4.5	4.4	4.5	–	V
		I <sub>O</sub> = -4.0 mA	4.5	4.13	4.32	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 µA	4.5	–	0	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	–	0.15	0.33	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	±1.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	10	µA
ΔI <sub>CC</sub>	additional supply current per input	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; I <sub>O</sub> = 0	4.5 to 5.5	–	–	375	µA
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -20 µA	4.5	4.4	–	–	V
		I <sub>O</sub> = -4.0 mA	4.5	3.7	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 µA	4.5	–	–	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	–	–	0.4	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	±1.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	20	µA
ΔI <sub>CC</sub>	additional supply current per input	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; I <sub>O</sub> = 0	4.5 to 5.5	–	–	410	µA

## Note

1. All typical values are measured at T<sub>amb</sub> = 25 °C.

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## Dual 2-input AND gate

## 74HC2G08; 74HCT2G08

## AC CHARACTERISTICS

## Type 74HC2G08

GND = 0 V;  $t_r = t_f \leq 6.0$  ns;  $C_L = 50$  pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA, nB to nY	see Figs 5 and 6	2.0	–	26	95	ns
			4.5	–	9	19	ns
			6.0	–	8	16	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time	see Figs 5 and 6	2.0	–	20	95	ns
			4.5	–	7	19	ns
			6.0	–	6	16	ns
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA, nB to nY	see Figs 5 and 6	2.0	–	–	110	ns
			4.5	–	–	22	ns
			6.0	–	–	20	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time	see Figs 5 and 6	2.0	–	–	125	ns
			4.5	–	–	25	ns
			6.0	–	–	20	ns

## Note

1. All typical values are measured at T<sub>amb</sub> = 25 °C.

## Type 74HCT2G08

GND = 0 V;  $t_r = t_f \leq 6.0$  ns;  $C_L = 50$  pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA, nB to nY	see Figs 5 and 6	4.5	–	14	30	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time	see Figs 5 and 6	4.5	–	7	19	ns
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA, nB to nY	see Figs 5 and 6	4.5	–	–	36	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time	see Figs 5 and 6	4.5	–	–	22	ns

## Note

1. All typical values are measured at T<sub>amb</sub> = 25 °C.

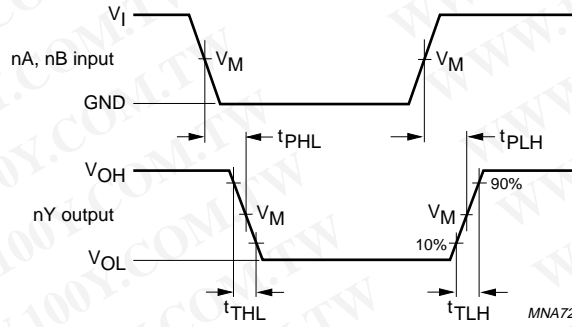
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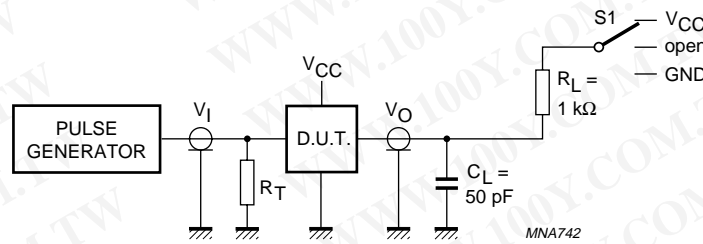
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AC WAVEFORMS



For 74HC2G08:  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 For 74HCT2G08:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3.0 \text{ V}$ .

Fig.5 The input (nA, nB) to output (nY) propagation delays and transition times.



TEST	S1
$t_{PLH}/t_{PHL}$	open
$t_{PLZ}/t_{PZL}$	$V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

Definitions for test circuit:  
 $C_L$  = load capacitance including jig and probe capacitance.  
 $R_T$  = termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

Fig.6 Load circuitry for switching times.

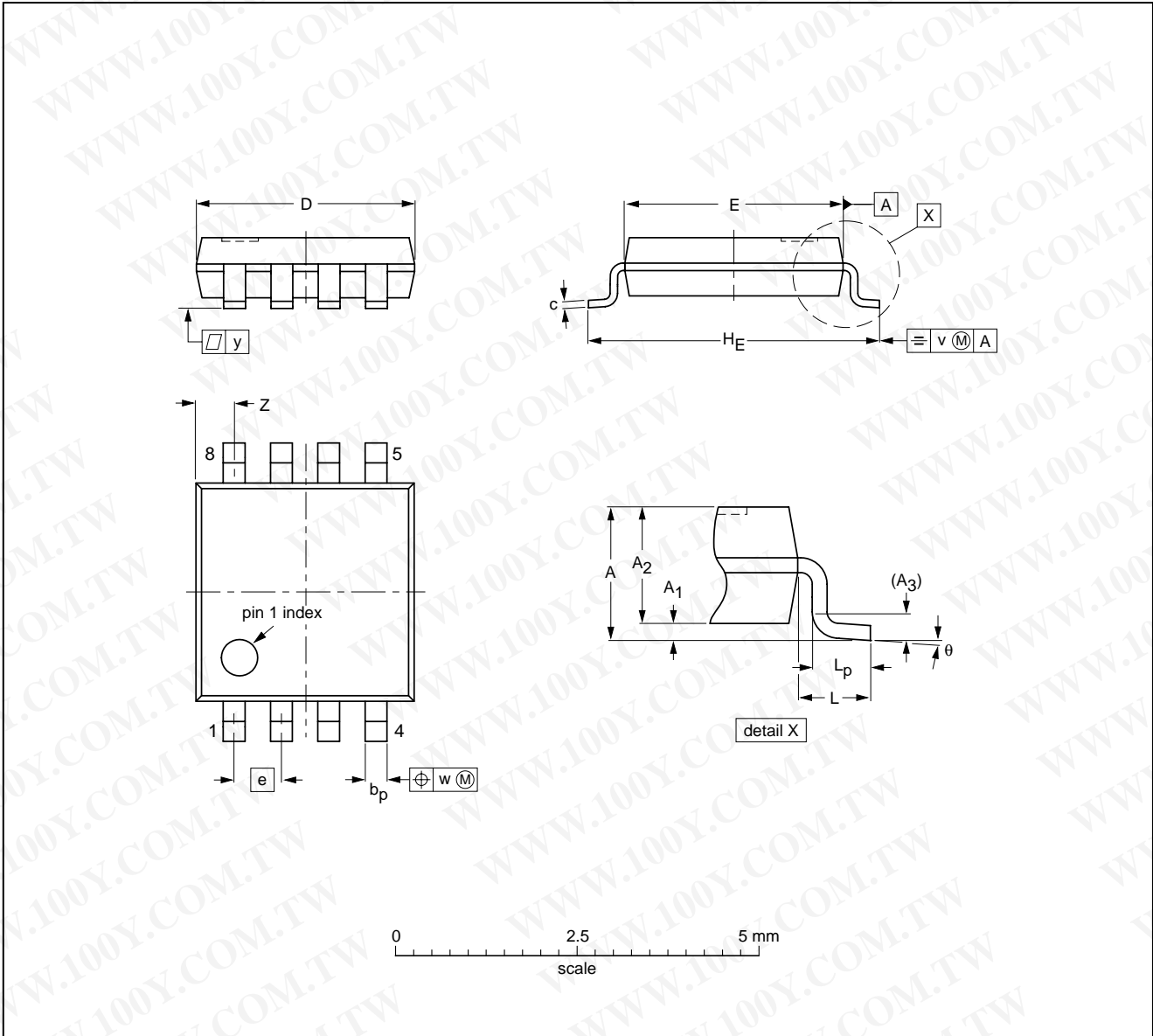
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Dual 2-input AND gate

74HC2G08; 74HCT2G08

PACKAGE OUTLINES

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

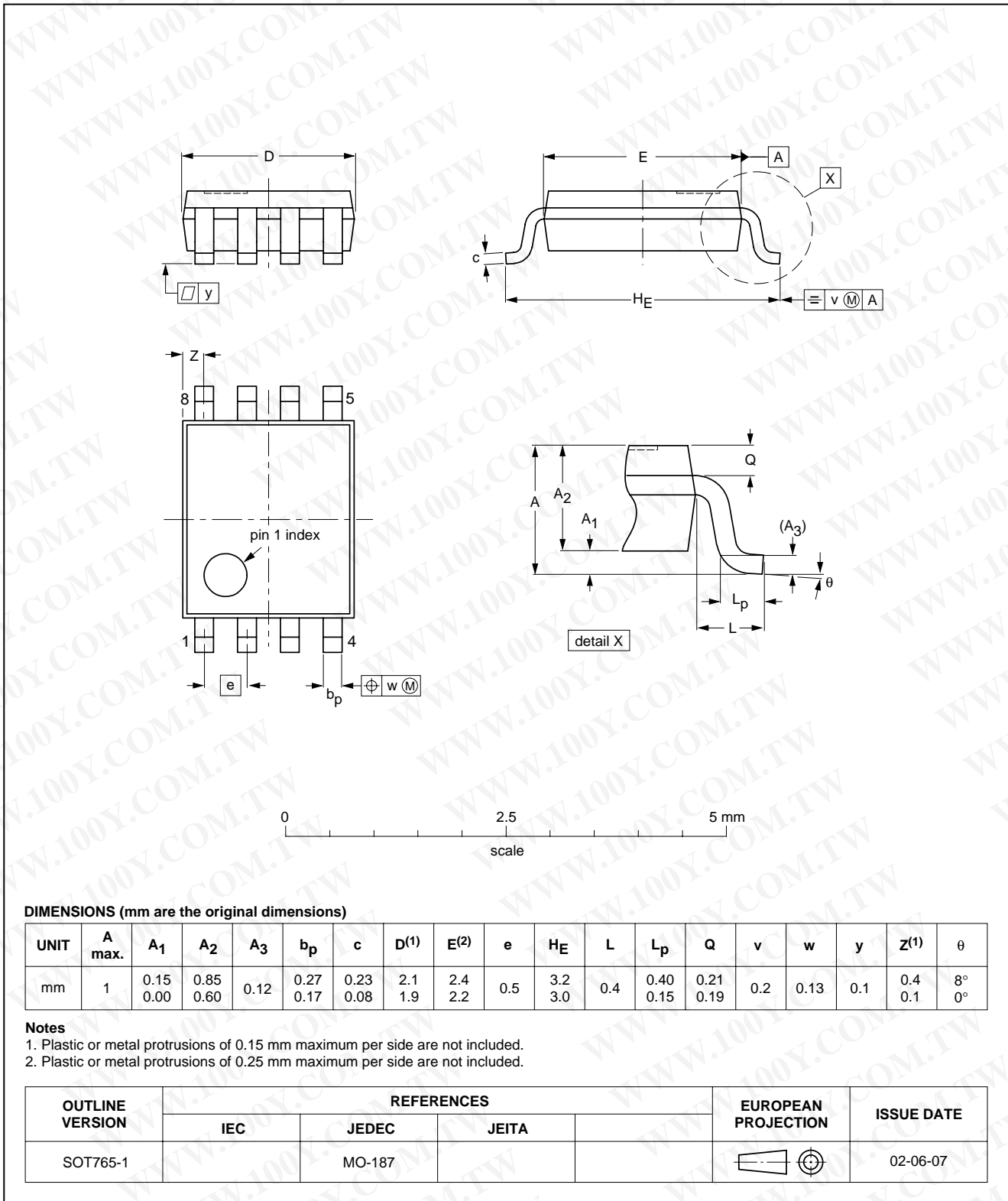
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT505-2		---			02-01-16

Dual 2-input AND gate

74HC2G08; 74HCT2G08

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1





## Dual 2-input AND gate

## 74HC2G08; 74HCT2G08

### SOLDERING

#### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

#### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA and SSOP-T packages
  - for packages with a thickness  $\geq 2.5$  mm
  - for packages with a thickness  $< 2.5$  mm and a volume  $\geq 350$  mm<sup>3</sup> so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness  $< 2.5$  mm and a volume  $< 350$  mm<sup>3</sup> so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

#### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## Dual 2-input AND gate

## 74HC2G08; 74HCT2G08

## Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE <sup>(1)</sup>	SOLDERING METHOD	
	WAVE	REFLOW <sup>(2)</sup>
BGA, LBGA, LFBGA, SQFP, SSOP-T <sup>(3)</sup> , TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable <sup>(4)</sup>	suitable
PLCC <sup>(5)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(5)(6)</sup>	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended <sup>(7)</sup>	suitable

## Notes

- For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.
- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
- These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding  $217\text{ °C} \pm 10\text{ °C}$  measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
- These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- If wave soldering is considered, then the package must be placed at a  $45^\circ$  angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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### DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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